Integrated Modulation of Dual-Parallel Three-Level Inverters With Reduced Common Mode Voltage and Circulating Current

Weiwei Li, *Student Member, IEEE*, Xueguang Zhang, *Member, IEEE*, Feiyu Zhang, Siyuan Zhang, Zhichao Fu, Gaolin Wang, *Senior Member, IEEE*, and Dianguo Xu, *Fellow, IEEE*

***Abstract*—Many reduced common mode voltage (CMV) modulation methods have been proposed for three-level inverters. However, most of them suffer from large current distortion because only part of the available base vectors is utilized. The interleaved paralleling can reduce both CMV and the output current distortion, though the CMV reduction is limited and large zero-sequence circulating current (ZSCC) is inevitably caused by the phase-shifted carriers. To further reduce the CMV while maintaining smaller current distortion and ZSCC, a five-level reduced CMV (RCMV) modulation method is proposed in this article, which treats the parallel inverters as a whole. Theoretical analysis reveals that the integrated modulation provides additional base vectors that contribute to smaller total harmonic distortion (THD) of the current, and the selected vectors ensure the nearest-three-vector synthesis and half-reduced CMV. The switching sequences design and neutral point balancing strategy are also developed for dual-parallel three-level inverters, ensuring that the average circulating current is zero and the neutral point voltage is balanced, which are both critical to the proper operation of parallel inverters. Superior performance in terms of CMV, THD, and ZSCC provided by the proposed method in comparison with conventional modulation is verified by comprehensive simulation and experimental results.**

***Index Terms*—Common mode voltage (CMV), dual-parallel three-level inverters, interleaved modulation, space vector modulation, zero-sequence circulating current (ZSCC).**

I. Introduction

In RECENT years, three-level power converters have been extensively used in many applications, including wind power [1], solar power [2], and medium voltage motor drive [3] systems. In addition, parallel operation of three-level inverters has been adopted by diverse applications to increase the power rating and enhance system performance [4]–[6].

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Weiwei Li, Xueguang Zhang, Feiyu Zhang, Siyuan Zhang, Gaolin Wang, and Dianguo Xu are with the Department of Electrical Engineering, Harbin Institute of Technology, Harbin 150001, China (e-mail: wolf_wei2003@163.com; zxghit@126.com; 15504667916@163.com; 1624515970@qq.com; wgl818@hit.edu.cn; xudiang@hit.edu.cn).

Zhichao Fu is with the Guangzhou Power Supply Bureau of Guangdong Power Grid Corporation, Guangzhou 511400, China (e-mail: fzcsd92@163.com).

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Common mode voltage (CMV) presented between the neutral points at the load and source side is an intrinsic issue of pulsewidth modulated converter that may cause various problems. In variable speed electrical drive applications, CMV may bring forth many problems like winding insulation failure, electromagnetic interference (EMI), leakage current, etc. [7]. Further, in power converter applications, CMV also results in several problems such as current distortion, EMI, and safety issues [8].

For the transformer-less PV and motor drive applications that are sensitive to the CMV induced leakage current rather than the CMV amplitude, the parasitic capacitance in the leakage current loop is a critical factor. For PV applications, different parasitic parameters ranging from 0.01 to 0.2 μF have been used in the literature [9]–[11]. However, a corporate report suggests the practical value should be 0.06–0.1 μF/kW for crystalline silicon cells and 0.1–0.16 μF/kW for thin-film cells [12]. For motor drive systems, the situation is more complicated, because the coupling capacitances from the motor windings to the stator and rotor irons, and the parasitic capacitance between the dc bus and earth should be considered [13]. To sum up, a typical value of 0.03–0.04 μF/kW appears to be acceptable for various motor types [14], [15].

Approaches to suppress CMV fall into hardware enhancement and software improvement these two categories. Many hardware solutions—including passive elements and topology modification—have been proposed.

Passive methods adopt magnetic components including common-mode (CM) inductors, coupled inductors (CI), or other CM filters [16], [17]. However, additional magnetic elements have size and cost penalties. Further, the passive elements involve complicated design and production processes. An improved LCL filter is presented in [18] to attenuate the CMV high-frequency component, however, the resonant circulating current will be generated and need to be controlled, which in turn increases the system complexity and losses.

To overcome the drawbacks of passive methods, many solutions with modified topology are proposed. A fourth arm is added to a three-leg inverter system to suppress CMV in [19], and another solution proposed in [20] even eliminates CMV. However, additional components may lead to increased volume, weight, and cost. Hota *et al.* [21] propose a three-level inverter with an optimized T-type structure, however, separated dc-link increases

system complexity and cost. One novel flying-capacitor topology is proposed to eliminate the CMV [22], though the use of capacitors causes higher cost.

On the other side, the software approaches may be preferable because no additional hardware is needed. Most recent studies of CMV reduction methods focus on modulation strategies known collectively as reduced CMV (RCMV) modulation. The general idea is selecting the base vectors with small CMV to synthesize the voltage reference vector. These methods include the modulation scheme using only part of the available vectors (e.g., LMSVM or LMZVM) [10], virtual space vector modulation [8], discontinuous PWM [23], and improved space vector modulation [24]. However, all these methods sacrifice the utilization of all base vectors, leading to an increased current distortion. Although the switching sequences could be modified to improve the current quality [25], [26], there is always a tradeoff between the CMV and the current total harmonic distortion (THD).

Paralleling offers more control freedoms, which means that the tasks of CMV reduction and THD improvement could be achieved simultaneously, leveraging the interactions between parallel operated inverters. Parallel inverters with interleaved modulation have drawn much attention in the last several years. The phase-shift between the carriers provides a freedom of control that is useful to cancel out the current ripples of parallel inverters, achieving the THD reduction at the parallel output. In addition, the CMV amplitude for the parallel inverter system with interleaving can be reduced to *Vdc*/6 [27]. However, intentionally phase-shifted carriers inevitably cause high-frequency zero-sequence circulating current (ZSCC), which is the main drawback of the interleaved modulation. In [28], an LMSZVM method is proposed to simultaneously reduce the CMV and the circulating current, however, the algorithm is complicated and CMV is only reduced to *Vdc*/6. A different carrier pattern is used to reduce the circulating current in [29], but the output current quality is impaired. A novel 2DoF-Interleaving method has recently been proposed to reduce the circulating current, but the current THD is higher and the maximum CMV amplitude is as much as *Vdc*/6 [30].

All the techniques for parallel inverters described above treat the parallel inverters separately, yet a new freedom of control may be provided by integrated control, which considers the parallel inverters as a whole. In [31], it is revealed that parallel inverters have multilevel voltage output capability, therefore the modulation methods for multilevel inverter can be directly adopted. Based on this idea, several modified three-level modulation methods have been proposed for dual-parallel two-level inverters to alleviate current ripple, ZSCC, or CMV [32]–[34]. Recently, a basic framework of integrated five-level modulation for parallel three-level inverters is proposed in [35] to reduce the output current distortion, but the CMV is not optimized. In [36], an integrated discontinuous modulation scheme is proposed to lower down the switching loss and CMV, but small CMV cannot be maintained in the entire modulation range, and the circulating current is not evaluated. Therefore, in this article, an integrated RCMV technique is presented to achieve smaller CMV, ZSCC, and THD for dual-parallel three-level inverters than the interleaved modulation.

TABLE I
FIVE-LEVEL OUTPUT STATES FORMED BY THREE-LEVEL STATES OF PARALLEL INVERTERS

State of Inverter 1	State of Inverter 2	State of Parallel Output
0	0	0
0	1	1
1	0	
1	1	2
1	2	3
2	1	
2	2	4

The rest of this article is structured in the following way. Section II describes the general idea of integrated modulation and analyzes the effect of modulation methods on CMV and current distortion for parallel three-level inverters. In Section III, the integrated RCMV method is proposed, and a strategy for neutral point voltage balance is also provided. Then, the simulation and experimental results are given in Section IV for various modulation methods. Finally, the conclusions is drawn in Section V.

II. EFFECT OF MODULATION ON CMV AND CURRENT RIPPLE IN PARALLEL THREE-LEVEL INVERTERS

A. Basic Concept of Integrated Modulation

The system structure and integrated control diagram of dual-parallel three-level inverters with a shared dc bus and common neutral point is shown in Fig. 1. In this system, the inverter output of each phase is first connected to the point of connection pccthrough an inductor, and then further connected to the ac side (grid or load).

For the dual-parallel inverters, the output voltage can be represented by

$$V_{xpccN} = \frac{V_{x1N} + V_{x2N}}{2} \quad x = A, B, C \tag{1}$$

where V_{x1N} and V_{x2N} are the x phase output voltages of three-level inverter 1 and 2, respectively.

Since V_{x1N} and V_{x2N} can only have one of three values, there are five possible results from (1), meaning that the equivalent pole voltage V_{xpccN} has five voltage levels. For any phase in the parallel inverter system, the parallel output states formed by three-level inverter states are listed in Table I. Therefore, we can modulate and control the dual-parallel three-level inverters as an integrated five-level system, and only one current control loop (one set of three-phase current measurements as shown in Fig. 1) is needed for the two inverters, which is beneficial to the system cost.

Based on the integrated five-level vector space, various modulation strategies for the system composed of parallel inverters could be evaluated, including the classical space vector modulation (CSV), interleaved modulation, and integrated modulation.

Assume that the voltage reference vectors of three-level inverter 1 and inverter 2 are at the locations shown in Fig. 2, and typically both V_{ref1} and V_{ref2} have identical magnitude and angle θ. The switching sequences for both inverters and

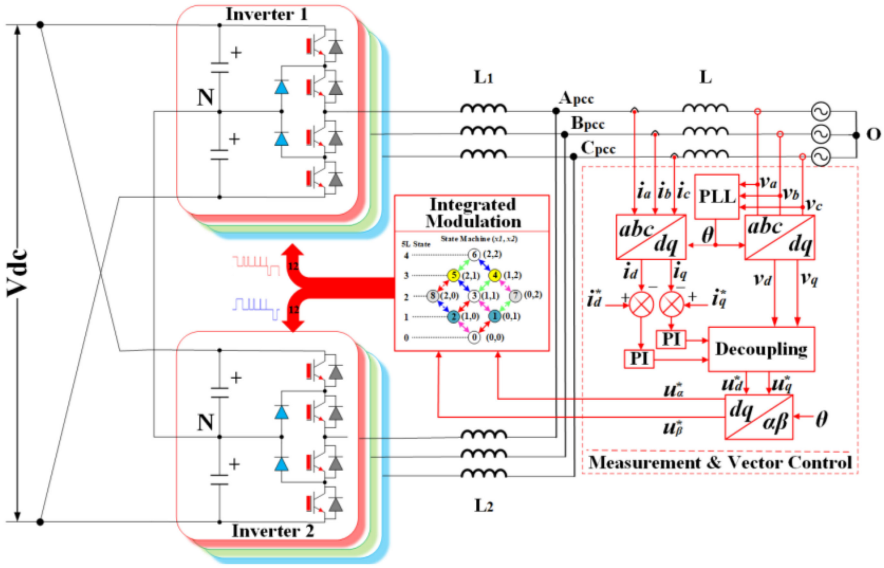

Fig. 1. Dual-parallel three-level inverters with shared dc bus and common neutral point.

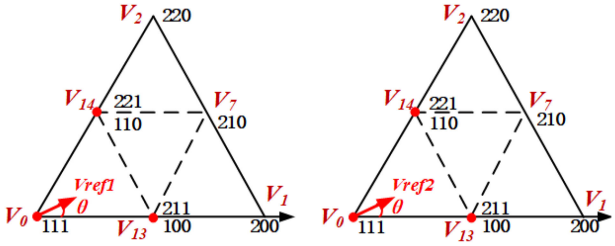

Fig. 2. Vector space for the same voltage reference vectors of three-level inverter 1 and 2.

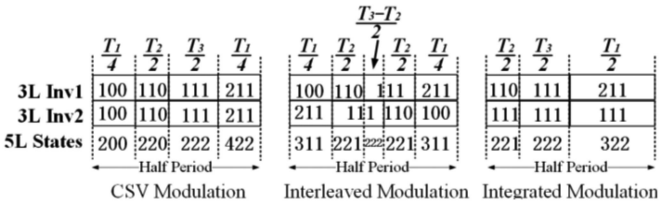

Fig. 3. Switching sequences during a half switching period.

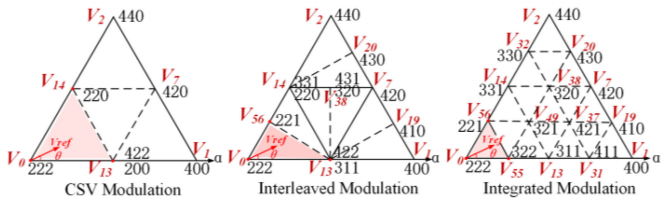

Fig. 4. Combined voltage vector diagram for various modulation methods.

the combined five-level switching states under CSV, interleaved, and integrated modulation are shown in Fig. 3. It should be noted that only half switching period is analyzed here for simplicity.

Corresponding to the switching sequences shown in Fig. 3, the combined voltage reference vector of the parallel system with various modulation schemes will be at the locations shown in Fig. 4.

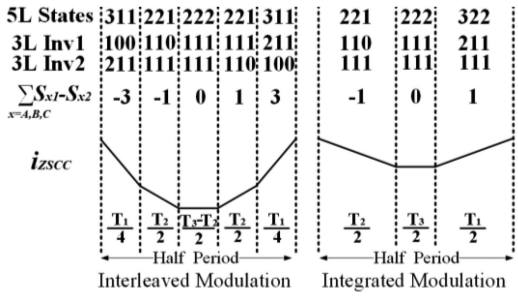

Fig. 5. ZSCC analysis for the interleaved and integrated modulation.

From Fig. 4, it is obvious that the interleaved modulation generates additional vector (221 in this example) that is not a three-level vector. The additional vectors help to finely partition the vector space, resulting in smaller regions than the CSV modulation. However, the interleaving only utilizes part of the five-level base vectors. In comparison, for the integrated modulation, the generated vectors are much more than that for interleaved modulation, contributing to much smaller vector space regions formed by all five-level vectors.

In addition, based on the switching sequences shown in Fig. 3, the corresponding ZSCC pattern of the integrated and interleaved modulation can be directly analyzed as shown in Fig. 5, which implies that the circulating current will also be reduced by the integrated modulation [37].

B. CMV of Dual-Parallel Inverters

The CMV in the parallel three-level inverters refers to the voltage difference between the ac side and dc bus neutral points, which can be expressed as

$$V_{ON} = \left(\sum_{x=A,B,C} V_{xpccN} \right) \Big/ 3. \tag{2}$$

Substituting (1) into (2) and considering the switching state representation of phase leg output, CMV is represented by

$$V_{ON}=\left(\frac{\sum\limits_{x=A,B,C}(S_{x1}-1)\frac{V_{dc}}{2}}{3}+\frac{\sum\limits_{x=A,B,C}(S_{x2}-1)\frac{V_{dc}}{2}}{3}\right)\Big/2$$
$$=\frac{V_{dc}}{12}\left[\sum_{x=A,B,C}(S_{x1}+S_{x2})-6\right] \quad (3)$$

where S_{x1} and S_{x2} refer to the x phase state of three-level inverter 1 and 2, respectively.

As the whole system can be treated as a five-level inverter, (3) can be simplified to

$$V_{ON}=\frac{V_{dc}}{12}\left[\sum_{x=A,B,C}S_x-6\right] \quad (4)$$

where S_x is the x phase state in the integrated five-level system.

For any base vector, its corresponding CMV value can be calculated according to (4). Under CSV modulation, the CMV magnitude of the parallel system is *Vdc*/3, which is contributed by vectors 200 and 442 shown in the left diagram of Fig. 4, according to (4). For the interleaved modulation, the system CMV can be maintained to be *Vdc*/12 when the modulation index (MI) is small (within 0.25), and increases to *Vdc*/6 contributed by vectors 220 and 422 when the MI is larger than 0.25, as shown in the middle diagram of Fig. 4. For the integrated modulation, the system CMV is ensured to be within *Vdc*/12 since the CMV values corresponding to the applied vectors are *Vdc*/12 in accordance with (4).

C. Current Ripple Evaluation

In the space vector modulation process, the nearest three base vectors are utilized to synthesize the voltage reference based on the volt-second-balance principle. However, at any instant within a switching period, there will always be an instantaneous error between the utilized base vector and the reference voltage, which leads to the ripple in the output currents.

Therefore, the magnitude of the voltage error vector can be used to evaluate the current ripple [6]–[9]. Based on the combined five-level space vector diagram presented in Fig. 4, the current ripple values for the three modulation methods with various MI and angle θ can be determined.

Corresponding to the vector spaces shown in Fig. 4 for the three modulation methods, the distribution diagrams of the normalized current ripples are shown in Fig. 6. When V_{ref} lies in different regions, the current ripple varies for different MI and angles. Obviously, the interleaved modulation is capable of reducing the current ripple compared with the CSV modulation, and the integrated modulation further reduces the current distortion.

In fact, the same conclusion can be drawn from the space vector diagram shown in Fig. 4 intuitively. Compared with the CSV modulation, the interleaved modulation generates additional base vectors, and these vectors contribute to smaller regions.

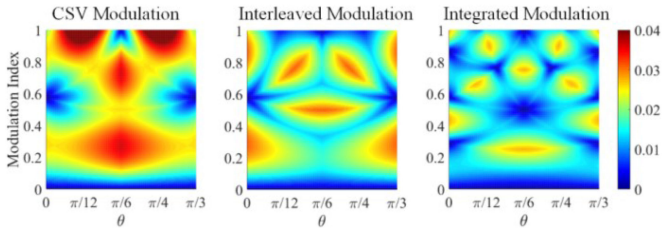

Fig. 6. Distribution of the normalized current ripple for various modulation methods.

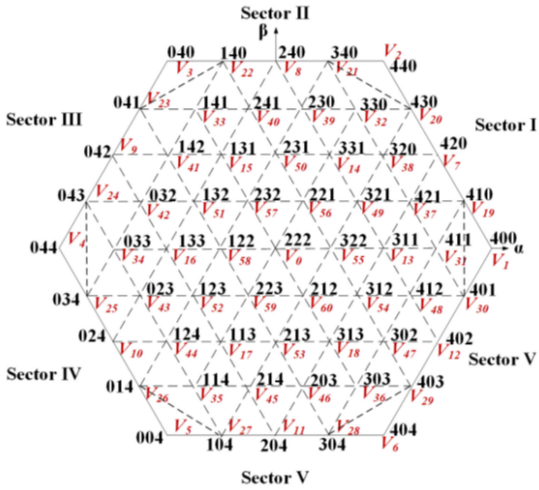

Fig. 7. Complete vector space for the proposed modulation.

Furthermore, the integrated modulation generates much more base vectors, which divide the vector spaces more precisely. The smaller the regions are, the smaller the synthesizing error during the switching period will be, which subsequently contributes to less current ripple.

III. Proposed Integrated RCMV Modulation

A. Modulation Process

The complete vector space of the proposed modulation method is presented in Fig. 7, which is divided into six parts denoted as sector I to sector VI. The vector space is composed of 61 base vectors (V_0 to V_{60}). Although some base vectors have many redundant states, only one state corresponding to the smallest CMV according to (4) is left for use.

The process of space vector modulation is typically composed of three procedures—determining which region the reference vector lies in, calculating the duty ratio of the nearest adjacent three vectors, and then generating appropriate switching sequences. Since sector II to VI could be rotated to sector I to simplify the computation during the modulation process, only the sector I will be analyzed here as an example.

Fig. 8 shows the detailed regions and base vectors of sector I. In fact, as long as the reference voltage vector lies in region 1 to 16, the CMV magnitude of *Vdc*/12 could always be ensured by the selected vector states according to (4).

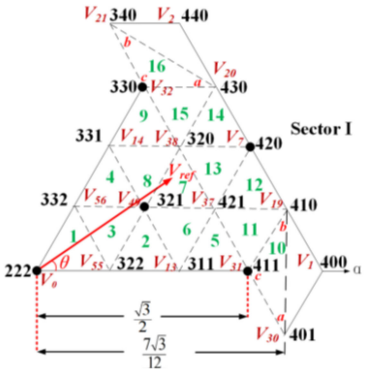

Fig. 8. Space vector diagram of sector I in detail.

TABLE II
SYSTEM PARAMETERS OF SIMULATION AND EXPERIMENT

Parameter	Value	Parameter	Value
V_{dc}	200 V	R	10 Ω
L_1 / L_2	4 mH	f_c	3600 Hz
L	1 mH	T_s	2 μs

Step 1	*Step 2*	*Step 3*	*Step 4*	*Step 5*	*Step 6*
Calculate *Vα* and *Vβ* using formula (A-1)	Determine the region of *Vref* based on Table A-I	Calculate dwell time of vectors based on Table A-II	Determine switching sequences based on Table A-III	Distribute to 3L states according to criteria A.1 -A.3	Generate pulses as traditional 3L modulation

Fig. 9. Overall implementation process of the proposed modulation scheme.

However, there are two exceptions—the regions 10 and 16. The shape of these special regions is different from that of other regions, aiming to avoid the use of vector states 400 and 440 because they may increase the CMV from *Vdc*/12 to *Vdc*/6. To maintain the CMV amplitude to *Vdc*/12 within the entire linear modulation range, the division of regions 10 and 16 must be modified as shown in Fig. 8. However, since the nearest three vectors are changed, the dwell time calculation must be modified accordingly, as listed in Table IV.

Furthermore, the overall implementation steps of the proposed modulation scheme are presented in Fig. 9 below, and the detailed modulation process (including the formulas, switching sequences, and the state distribution criteria, etc.) will be explained in the appendix at the end of this article.

B. Switching Sequences Design

For the integrated modulation of parallel inverters (including two-level and three-level inverters), the higher level switching state must be alternatively distributed within two consecutive switching periods to maintain zero averaged circulating current, which is critical to normal operation of parallel inverters [24]–[29].

TABLE III
REGION DETERMINATION CONDITIONS

Region	Conditions
1	$V_\beta + \sqrt{3}V_\alpha < \sqrt{3}/6$
2	$V_\beta + \sqrt{3}V_\alpha < \sqrt{3}/3$ and $V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/6$
3	$V_\beta + \sqrt{3}V_\alpha > \sqrt{3}/6$, $V_\beta - \sqrt{3}V_\alpha > -\sqrt{3}/6$, $V_\beta < \sqrt{3}/12$
4	$V_\beta + \sqrt{3}V_\alpha < \sqrt{3}/3$ and $V_\beta > \sqrt{3}/12$
5	$V_\beta + \sqrt{3}V_\alpha < \sqrt{3}/2$ and $V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/3$
6	$V_\beta + \sqrt{3}V_\alpha > \sqrt{3}$, $V_\beta - \sqrt{3}V_\alpha > -\sqrt{3}/3$, $V_\beta < \sqrt{3}/12$
7	$V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/6$, $V_\beta + \sqrt{3}V_\alpha < 1.5\sqrt{3}$, $V_\beta > \sqrt{3}/12$
8	$V_\beta + \sqrt{3}V_\alpha > \sqrt{3}$, $V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/6$, $V_\beta < \sqrt{3}/6$
9	$V_\beta + \sqrt{3}V_\alpha < 1.5\sqrt{3}$ and $V_\beta > \sqrt{3}/6$
10	$V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/6$
11	$V_\beta + \sqrt{3}V_\alpha > 1.5\sqrt{3}$, $V_\beta - \sqrt{3}V_\alpha > -\sqrt{3}/2$, $V_\beta < \sqrt{3}/12$
12	$V_\beta - \sqrt{3}V_\alpha > -\sqrt{3}/3$ and $V_\beta > \sqrt{3}/12$
13	$V_\beta + \sqrt{3}V_\alpha > 1.5\sqrt{3}$, $V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/3$, $V_\beta < \sqrt{3}/6$
14	$V_\beta - \sqrt{3}V_\alpha < -\sqrt{3}/6$ and $V_\beta > \sqrt{3}/6$
15	$V_\beta + \sqrt{3}V_\alpha > 1.5\sqrt{3}$, $V_\beta - \sqrt{3}V_\alpha > -\sqrt{3}/6$, $V_\beta < \sqrt{3}/4$
16	$V_\beta > \sqrt{3}/4$

In Fig. 8, the reference voltage vector falls in region 7. Considering only phase A, the switching sequence design and how it influences the circulating current are explained as follows. Within the first half switching period, the five-level switching state "3" is divided into three-level states "2" and "1," and the state difference 1 ($S_{A1} - S_{A2} = 2 - 1 = 1$) causes the differential circulating current i_{diffA} to increase, as shown in Fig. 10. In addition, the five-level state "4" and "0" are equally divided into three-level states, and their state differences are 0 ($S_{A1} - S_{A2} = 2 - 2 = 0$, and $S_{A1} - S_{A2} = 0 - 0 = 0$), which have no impact on the differential current. In the second half switching period, the three-level states are alternated to change the differential circulating current i_{diffA} in the opposite direction. For example, the five-level switching state "3" is divided into three-level states "1" and "2," and the resultant state difference is –1 ($S_{A1} - S_{A2} = 1 - 2 = -1$). Therefore, the differential circulating current can return to the origin value of this switching period.

However, the differential current over the first switching period cannot be kept to be zero. The sequences in the first switching period must be reversed for the second period, ensuring that the average value of differential current over these two consecutive periods is zero, as shown in Fig. 10. Similarly, the switching sequences and circulating current for other phases can also be analyzed.

TABLE IV
DWELL TIME CALCULATION FORMULA FOR NTVS

Region	Dwell time calculation formula
1	$T_{55}=4mT_s\sin(\pi/3-\theta)$, $T_0=4mT_s\sin(\theta)$
2	$T_{49}=T_s(4m\sin(\pi/3-\theta)-1)$, $T_{13}=4mT_s\sin(\theta)$
3	$T_{55}=T_s(1-4m\sin\theta)$, $T_{56}=T_s(4m\sin(\pi/3+\theta)-1)$
4	$T_{56}=T_s(4m\sin(\theta)-1)$, $T_{49}=4mT_s\sin(\pi/3-\theta)$
5	$T_{31}=4mT_s\sin(\theta)$, $T_{37}=T_s(4m\sin(\pi/3-\theta)-2)$
6	$T_{49}=T_s(1-4m\sin(\theta))$, $T_{37}=T_s(4m\sin(\pi/3+\theta)-2)$
7	$T_{49}=T_s(4m\sin(\theta)-1)$, $T_{37}=T_s(4m\sin(\pi/3-\theta)-1)$
8	$T_{14}=T_s(4m\sin(\pi/3+\theta)-2)$, $T_{49}=T_s(2-4m\sin(\theta))$
9	$T_{14}=4mT_s\sin(\pi/3-\theta)$, $T_{32}=T_s(4m\sin(\theta)-2)$
10	$T_{30}=4mT_s\sin(\pi/3\text{-}\theta)\text{-}3$, $T_{31}=T_s(4m\sin(\pi/3+\theta)-3)$
11	$T_{19}=T_s(4m\sin(\pi/3+\theta)-3)$, $T_{37}=T_s(1-4m\sin(\theta))$
12	$T_7=T_s(4m\sin(\pi/3-\theta)-2)$, $T_{19}=T_s(4m\sin(\theta)-1)$
13	$T_7=T_s(4m\sin(\pi/3-\theta)-2)$, $T_{38}=T_s(4m\sin(\theta)-1)$
14	$T_{38}=T_s(4m\sin(\theta)-2)$, $T_7=T_s(4m\sin(\pi/3-\theta)-1)$
15	$T_{20}=T_s(3-4m\sin(\theta))$, $T_{32}=T_s(1+4m\sin(\theta-\pi/3))$
16	$T_{20}=T_s(4m\sin(\pi/3+\theta)-3)$, $T_{32}=4mT_s\sin(\theta)\text{-}3$

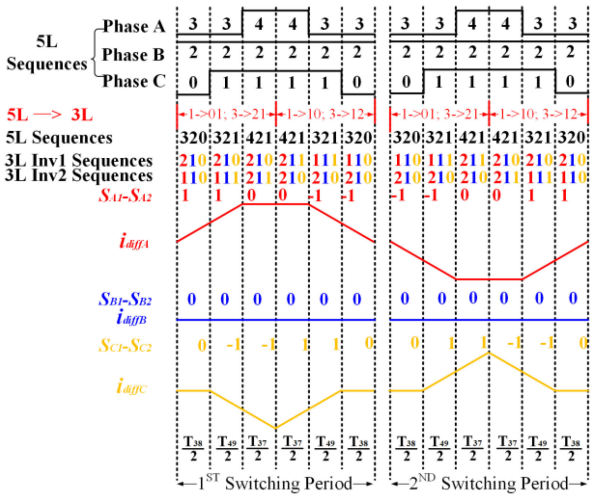

Fig. 10. Analysis of differential circulating current pattern for region 7.

Since ZSCC is defined as the sum of three-phase differential circulating currents, zero averaged ZSCC could be maintained as long as the average differential circulating currents are zero. In fact, with the switching sequences shown in Fig. 10, the impact on ZSCC can also be evaluated, and the analysis process is presented in Fig. 11.

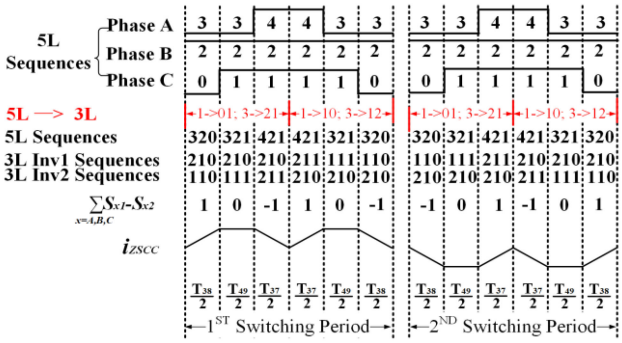

Fig. 11. Analysis of ZSCC pattern for region 7.

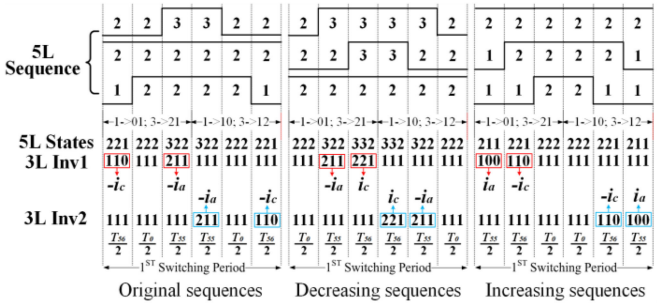

Fig. 12. Analysis of neutral point current for various switching sequences.

C. Neutral Point Balance

The neutral point voltage balance is crucial to neutral-point-clamped (NPC) inverters, and the basic approach is to maintain equal charge to the capacitors by adjusting the neutral point current.

For the space vector diagram presented in Fig. 7, there are not any redundant states, meaning that the classical neutral point balancing method through redistributing the dwell time of redundant states cannot be implemented. Therefore, special neutral point voltage balancing strategy must be developed.

When the reference voltage vector lies in region 1, the left diagram of Fig. 12 shows the switching sequences described in Section III (called the original switching sequences) with the corresponding neutral point currents. Only the first switching period is considered for simplicity. The local averaged neutral point current within a switching period is represented by

$$\begin{aligned} i_{NP\_Original} &= -T_{56}i_c - T_{55}i_a \\ &= -4mIT_s\left[-sin\theta cos\theta + \frac{\sqrt{3}}{2}(cos^2\theta - sin^2\theta)\right] \end{aligned} \tag{5}$$

where T_s is the switching period; T_{55} and T_{56} are the duty ratio of the nearest three vectors; I is the current amplitude; m refers to the MI; and θ is the angle of the reference voltage vector.

In region 1, the angle θ ranges from 0° to 60°. Therefore, the total charge to the neutral point over the entire region is

$$\int_0^{\frac{\pi}{3}} i_{NP\_Original} = -4mIT_s \times \frac{1}{2}\sin\left(\frac{\pi}{6}+2\theta\right)\Big|_0^{\pi/3} = 0. \tag{6}$$

On the one hand, zero average neutral point current means that the original switching sequence does not cause neutral point voltage imbalance during normal operation. However, in case neutral point imbalance occurs, it cannot restore the balance either. Therefore, new switching sequences with balancing capability must be constructed.

To obtain neutral point current with opposite directions, the redundant states other than that shown in Fig. 7 must be used. For example, if the starting vector state 221 is removed and its redundant state 332 is added to the end of the switching sequence (which is called the decreasing switching sequence) shown as the middle diagram in Fig. 12, the averaged neutral point current in a switching period is

$$i_{NP\_Decreasing} = T_{56}i_c - T_{55}i_a = -2\sqrt{3}mIT_s. \quad (7)$$

Negative constant value of neutral point current means that the modulation process will always charge to the neutral point, which subsequently decreases the voltage difference of the dc bus capacitors.

Similarly, if the ending vector state 322 is removed and its redundant state 211 is added to the start of the switching sequence (which is called the increasing switching sequence) shown as the right diagram in Fig. 12, the averaged neutral point current in a switching period is

$$i_{NP\_Increasing} = -T_{56}i_c + T_{55}i_a = 2\sqrt{3}mIT_s. \quad (8)$$

The neutral point current in (8) is always positive, meaning that the sequences will increase the voltage difference.

Therefore, to maintain a balanced neutral point voltage, the following strategy will be adopted. Under normal conditions, the original switching sequence is used, maintaining balanced neutral point voltage. If neutral point imbalance appears during dynamic process, the original sequence will be replaced with decreasing or increasing sequence to decrease or increase the capacitor voltage difference, therefore restoring the neutral point voltage balance.

IV. Simulation and Experimental Results

The system composed of dual-parallel three-level NPC inverters is modeled and simulated to verify the performance of the proposed method, and Table II lists the relevant parameters.

The performance of various modulation methods is also examined on an experimental prototype, and the platform with a controller of TMS320F28377D from Texas Instruments is shown in Fig. 13.

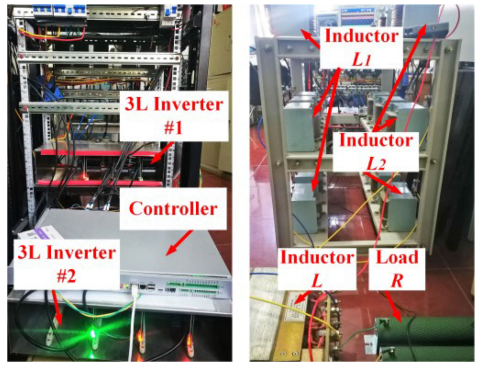

Fig. 13. Photo of the laboratory prototype.

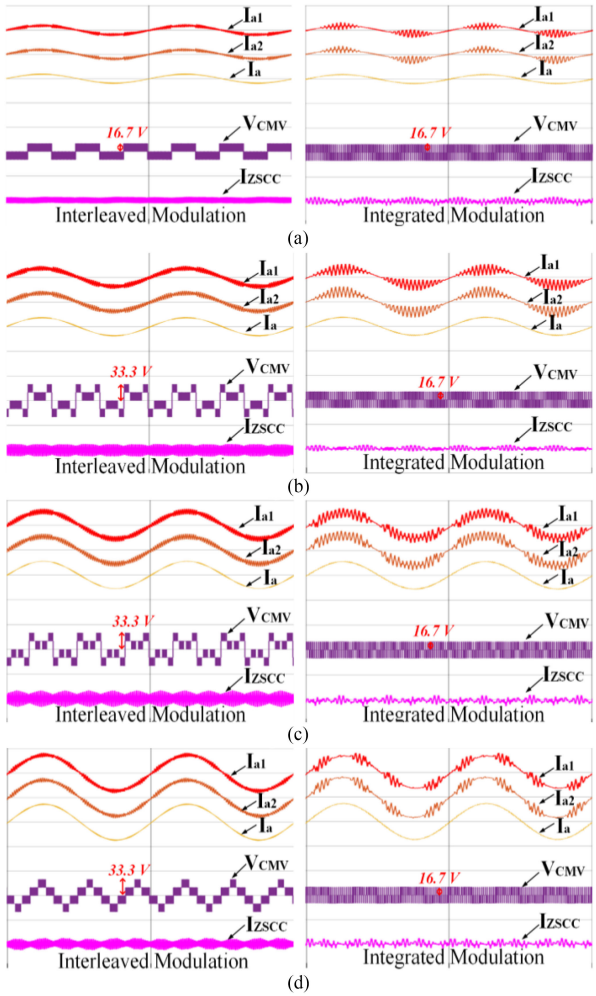

Fig. 14. Simulation waveform of the inverter currents (10 A/div), output current (20 A/div), CMV (20 V/div) and ZSCC (5 A/div) (Time:20 ms/div). (a) MI = 0.2. (b) MI = 0.4. (c) MI = 0.6. (d) MI = 0.8.

A. Steady-State Operation With R-L Load

Under MIs of 0.2, 0.4, 0.6, and 0.8, the simulation waveforms of the phase currents, CMV and ZSCC are presented in Fig. 14(a)–(d), respectively. It is obvious that both the CMV and ZSCC amplitudes are effectively reduced by the proposed modulation method compared with the interleaved modulation.

The experimental waveforms for the interleaved and the integrated modulation are shown in Fig. 15 for different MIs.

First, in terms of CMV, both the simulation and experimental results show that the interleaved modulation can reduce the CMV to *Vdc*/12 (16.7 V, when the MI is 0.2) or *Vdc*/6 (33.3 V, when the MI is larger than 0.2). Furthermore, the proposed integrated modulation can reduce the CMV amplitude to *Vdc*/12 for any MI.

Second, in terms of output current distortion, the THD values for various modulation methods are graphically represented in Fig. 16(a). It is obvious that the proposed modulation method provides better current quality than CSV and the interleaved

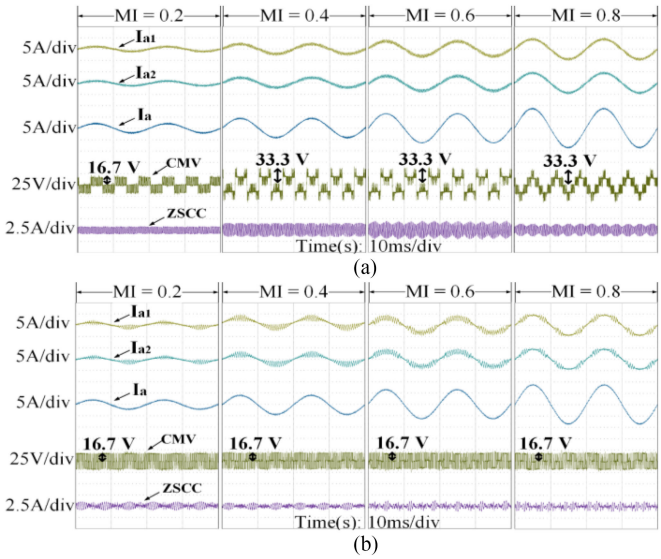

Fig. 15. Experimental waveform of the phase currents, CMV and ZSCC for different MIs.

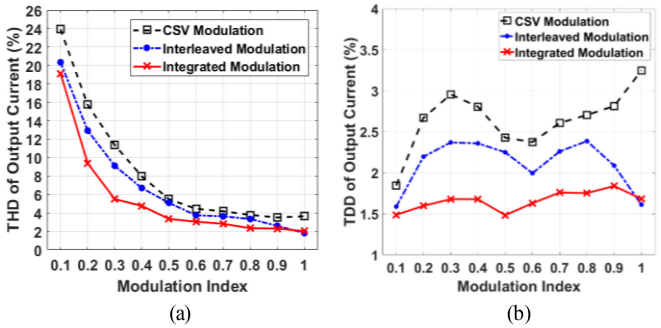

Fig. 16. Current THD and TDD comparison for various modulation methods. (a) THD comparison. (b) TDD comparison.

modulation. It should be noted that the data of CSV modulation are only used here as a reference.

In addition, although the THD is widely used, the total demand distortion (TDD) is a better measure of harmonic distortion. Since the practical impact of current harmonics is largely independent of the actual current, the corresponding TDD values with respect to the MIs are shown in Fig. 16(b), from which the harmonic performance of various modulation methods can be objectively compared. Apparently, the proposed method provides a smaller current distortion.

Third, in terms of ZSCC, as presented in Fig. 17, the integrated modulation also generates smaller ZSCC than the interleaved modulation at any MI, which is consistent with the analysis in Section II and beneficial to reduced volume and cost of the filter inductor.

B. CMV Spectra and Leakage Current

Taking the operation when the MI is 0.6 as an example, the CMV spectra for the interleaved and integrated modulation methods are analyzed and compared, and the spectra analysis results are shown in Fig. 18 below. To clearly show the low

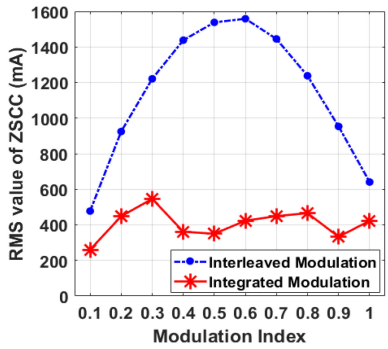

Fig. 17. ZSCC comparison for interleaved and integrated modulation.

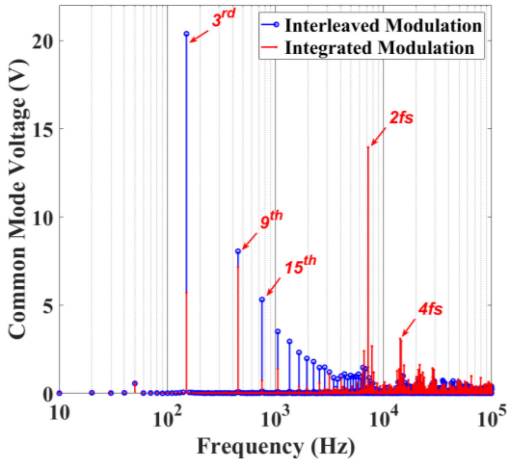

Fig. 18. CMV spectra comparison for the interleaved and integrated modulation.

order harmonics, the frequencies on the x-axis are displayed logarithmically. The spectra results for other MIs are similar and will not be presented here.

Generally speaking, in case of CMV, the interleaved modulation has significant low-frequency components, and the integrated modulation has larger high-frequency components.

On the one hand, high-frequency components are more harmful because a large leakage current may be generated through the parasitic capacitors within the system (e.g., in PV or motor drive applications). On the other hand, high-frequency components are much easier to be filtered out by the common mode filters, which are commonly used in practical applications, especially considering that the harmonic spectra concentrate at frequencies higher than 2 times the switching frequency. For the interleaved modulation, the CMV components which concentrate at low frequencies that are lower than the switching frequency will be difficult to filter out. Furthermore, it should be noted that the interleaved modulation has larger components in terms of side-band harmonics in the high-frequency range.

When the parasitic capacitance is 0.2 μF—a typical value corresponding to a transformer-less PV system of 2 kW or a motor of 5 kW—the simulation waveforms of leakage current under various MIs for the interleaved and integrated modulation methods are shown in Fig. 19. Obviously, the integrated modulation generates similar even larger leakage current than the interleaved method. Therefore, although the CMV amplitude

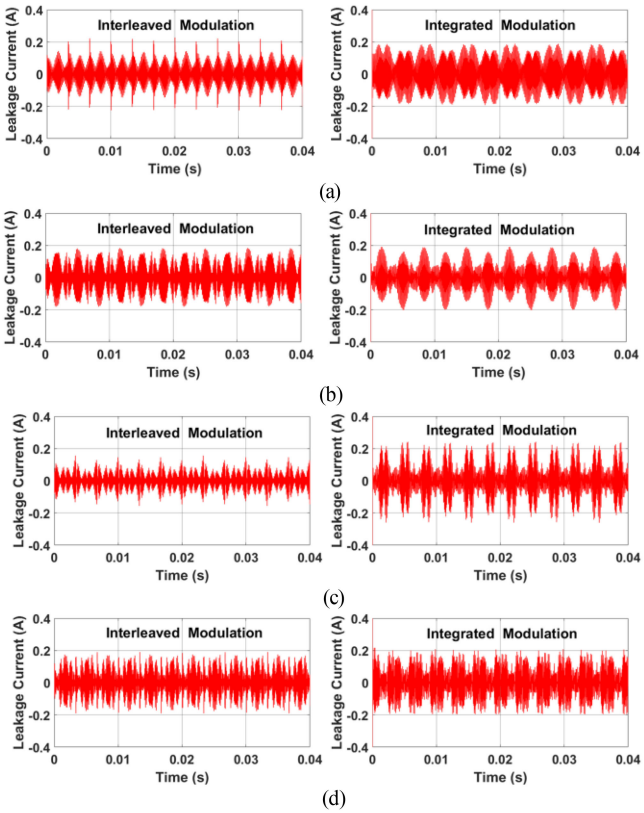

Fig. 19. Simulation waveforms of leakage current for the interleaved and integrated modulation methods.

for the proposed method is only *Vdc*/12 (i.e., half of that for the interleaved modulation), the high-frequency components cause large leakage current, which needs to be concerned in practical applications.

C. Dynamic Operation With Grid-Connection

The experimental waveforms for the interleaved and the integrated modulation methods when the *d*-axis current (corresponding to the active power injected into the grid) command changes from 6 to 12 A are shown as Fig. 20(a). During the grid-connected operation, the dc bus voltage is set to 400 V, and the ac side voltage is 190 Vrms.

Similarly, the experimental waveforms when the *q*-axis current (corresponding to the reactive power injected into the grid) command changes from 6 to 12 A are shown as Fig. 20(b).

Furthermore, when the injected power changes from pure active (*d*-axis current is 12 A, and *q*-axis current is 0 A) to pure reactive (*d*-axis current is 0 A, and *q*-axis current is 12 A), the waveforms for the two methods are shown in Fig. 20(c).

In addition, when the injected power changes from pure reactive (*d*-axis current is 0 A, and *q*-axis current is 12 A) to pure active (*d*-axis current is 12 A, and *q*-axis current is 0 A), the experimental waveforms are shown in Fig. 20(d).

Obviously, no matter active or reactive power is injected into the grid, the dynamic response is very fast for both

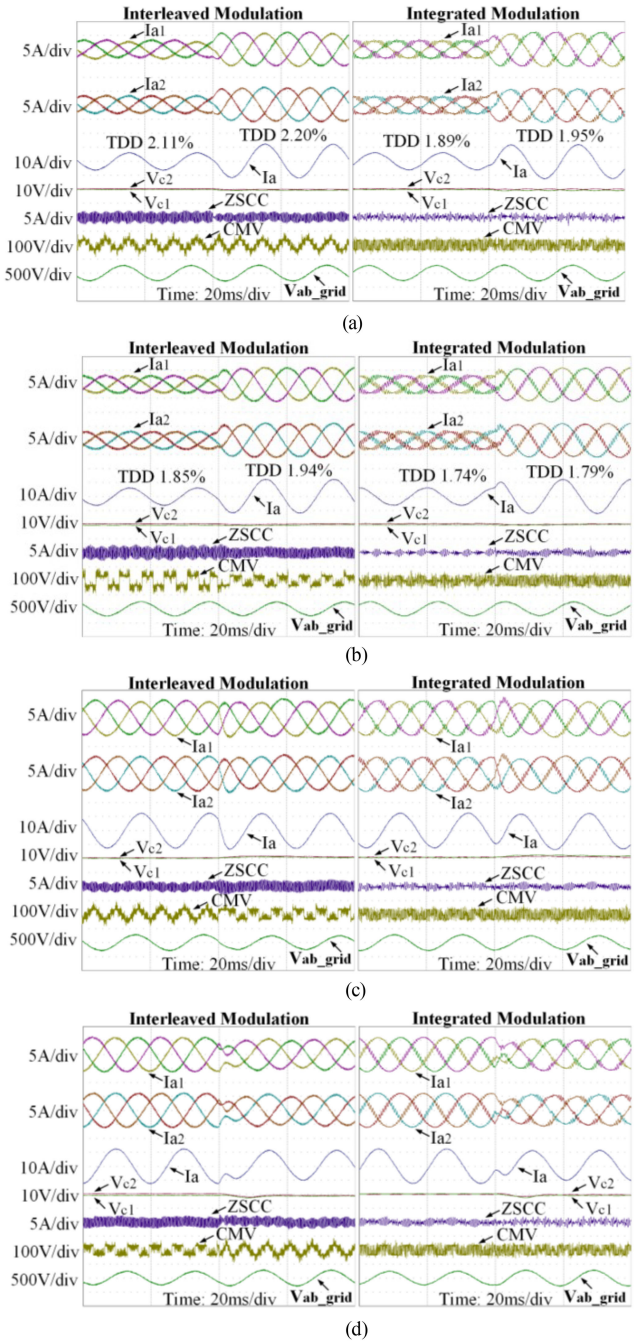

Fig. 20. Experimental waveforms of dynamic processes under grid-connected operation for various modulation methods.

modulation methods. In addition, for the integrated modulation, all the CMV amplitude, output current distortion, and the ZSCC magnitude are smaller than that for the interleaved modulation.

In fact, generally speaking, the dynamic response is mainly affected by the controller structure, controller parameters, and system characteristics, etc., instead of the modulation process. Therefore, for the same controller and system conditions, it is reasonable to find out that both modulation methods have comparable dynamic responses.

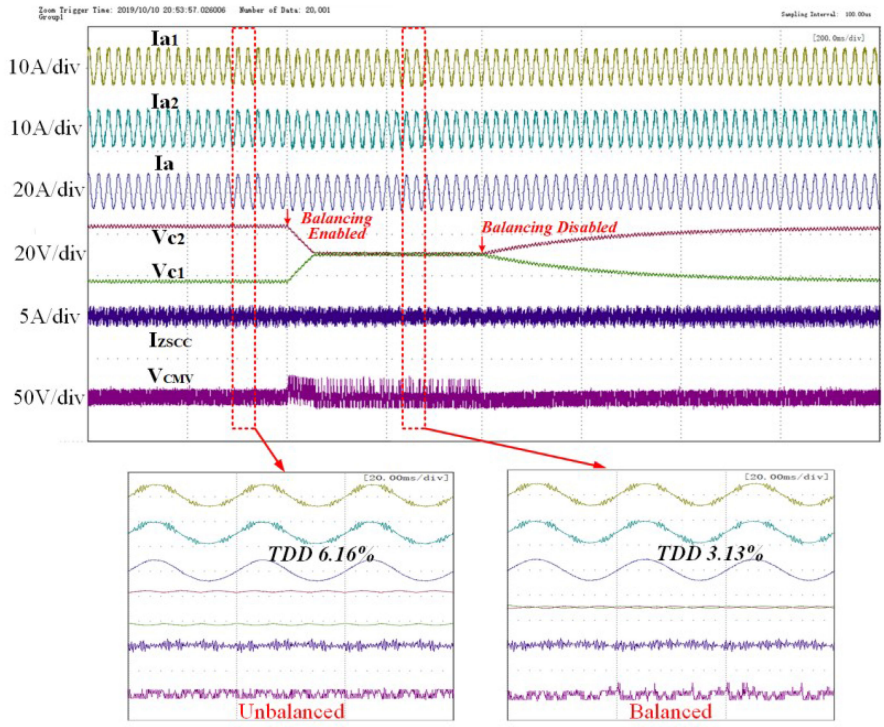

Fig. 21. Experimental results of the phase currents, capacitor voltages, ZSCC, and CMV during neutral point balancing process.

D. Neutral Point Balancing Process

The neutral point voltage is intentionally unbalanced through connecting a power resistor across the lower capacitor to test the balancing algorithm on the experiment platform, and the experimental waveforms are presented in Fig. 21.

The overall waveform is at the top of Fig. 21, which shows that the balancing algorithm is capable of eliminating the neutral point imbalance. In addition, the zoom-in views on the bottom show the detailed waveforms when neutral point imbalance exists and disappears. When the neutral point imbalance exists, the output current has a significant distortion. However, the balancing strategy is effective to restore the balance and reduce the output current distortion.

However, during the balancing process, the vectors used by the decreasing and increasing sequence cause the CMV peak value increases to *Vdc*/6. Fortunately, the balancing strategy is needed only under abnormal conditions. As soon as the original switching sequences are used after the neutral point voltage is balanced, CMV peak value will decrease to *Vdc*/12 again.

V. Conclusion

A novel integrated RCMV modulation scheme is proposed for dual-parallel three-level NPC inverters with simultaneously reduced CMV, current distortion, and ZSCC of the whole system. Compared with the interleaved modulation, the proposed method can maintain the CMV to be within *Vdc*/12 at any MI, and keeping reduced current THD and smaller ZSCC at the same time.

The selected voltage vectors corresponding to the smallest CMV value form an integrated five-level vector space, and the modulation process can be implemented in the same way as five-level CSV modulation. The complete vector space of parallel inverters is divided into smaller regions by the additional vectors generated by the proposed integrated modulation, contributing to a smaller current distortion in comparison with conventional modulation methods. The average differential circulating current and ZSCC are maintained to be zero by appropriately designed switching sequences, ensuring the normal operation of parallel inverters.

Since there are not any redundant states that can be used, the conventional neutral point balance method is impossible to use. Therefore, two special switching sequences are constructed to eliminate the capacitor voltage difference and keep balanced neutral point voltage.

However, there are still several issues need to be studied.

First, to objectively compare the current harmonic performance for the proposed and the conventional modulation methods, only normal inductors have been used at the ac side output. The inductors seem to be oversized because they also act as the circulating current suppressor within the zero-sequence current path. Since the integrated modulation is actually a novel interleaving method, the CI may be a better solution, which will be left for future research.

Second, the implementation in this article uses a primitive algorithm for the integrated modulation, making the calculation process complicated. Generally speaking, carrier-based implementation is much simpler than the space vector approach. Therefore, it is necessary to develop an equivalent carrier-based method as a better option for practical applications.

Third, although the integrated modulation simultaneously reduces the output harmonics, ZSCC, and CMV amplitude

compared with interleaved modulation, it may not be a good option for applications sensitive to the leakage current (e.g., transformer-less PV system) because it generates a larger leakage current. However, additional measures could be adopted to suppress the leakage current, while still maintaining the advantages of the integrated modulation in terms of less output harmonics and smaller ZSCC. No matter whether leakage current exists or not, a reduced CMV amplitude is beneficial to less voltage stress and EMIs.

Furthermore, the state distribution pattern during the switching sequence design provides an additional degree of freedom, which can be exploited to further reduce the ZSCC and provide superior performance for the proposed method. However, this will be left for future research.

APPENDIX

For the completeness of this article and the convenience in understanding the proposed modulation process, the detailed implementation steps are affixed in this section.

The proposed integrated modulation method consists of six steps as shown in Fig. 9, and the detailed processes will be explained as follows, taking the sector I as an example. Other sectors can be rotated to the first sector to be analyzed in a similar way.

Step 1: The region within which the reference voltage vector locates should be determined. The coordinate value of the reference voltage vector can be expressed by

$$\begin{cases} V_\alpha = |V_{ref}| \cos\theta \\ V_\beta = |V_{ref}| \sin\theta. \end{cases} \tag{A1}$$

Step 2: Based on the boundary conditions of various regions listed in Table III, it is easy to determine the reference vector V_{ref} falls in which region.

Step 3: Depending on the position of the reference vector and the triangle in which the tip of the vector is located within, the on-duration time intervals of appropriate switching vectors are calculated based on the voltage-second balance principle, and the formulas of dwell time calculation can be referred to Table IV.

For all the formulas in Table IV, *m* refers to the MI, and θ is the angle of the reference vector. Only the formulas for two vectors out of the nearest three vectors are provided in this table, and the duty ratio of the remaining one vector can be obtained by subtracting the calculated values from the switching period.

Step 4: The five-segment switching sequences with three states of the NTVs will be adopted for the output. Taking the reference voltage vector shown in Fig. 7 as an example, the switching sequences are shown in Fig. 22. All switching sequences in one switching cycle for regions 1–16 in sector I are listed in Table V.

Step 5: The criteria for distributing five-level switching sequences to three-level states for the two parallel inverters can be summed up as follows.

A.1) All the five-level states with even number—including states "0", "2" and "4"—should be equally divided.

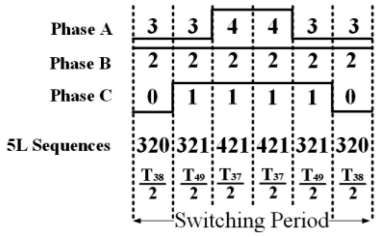

Fig. 22. Switching sequences for region 7 in sector I.

TABLE V
SWITCHING SEQUENCES FOR SECTOR I

Region	Switching Sequences
1	221-222-322-222-221
2	311-321-322-321-311
3	221-321-322-321-221
4	221-321-331-321-221
5	311-411-421-411-311
6	311-321-421-321-311
7	320-321-421-321-320
8	320-321-331-321-320
9	320-330-331-330-320
10	401-410-411-410-401
11	410-411-421-411-410
12	410-420-421-420-410
13	320-420-430-420-320
14	320-420-430-420-320
15	320-330-430-330-320
16	430-340-330-340-430

A.2) For the five-level states with odd number—including states "1" and "3," different three-level state combinations should be used in each half of the switching period. For example, if the first half uses "01" combination, then the second half must adopt "10" combination, and vice versa. Similarly, if "12" combination is used in the first half, then "21" combination must be used in the second half, and vice versa.

A.3) In the first half of the switching period, "01" combination for five-level state "1" should be used in conjunction with "21" combination for five-level state "3"; while in the second half period, "10" combination for five-level state "1" should be used in conjunction with "12" combination for five-level state "3"; afterward, the switching sequence order is reversed in the next

switching period, ensure that the average circulating current is kept to zero.

For various reference vectors which may fall into any region of the five-level vector space, the corresponding switching sequences for the parallel inverters can be derived based on these criteria, which will not be discussed in detail here.

Step 6: The final switching pulses for the parallel inverters can be generated as that of the traditional three-level modulation process.

REFERENCES

[1] J. Lee and K. Lee, "Open-switch fault tolerance control for a three-level NPC/T-type rectifier in wind turbine systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1012–1021, Feb. 2015.

[2] U. Choi, F. Blaabjerg, and K. Lee, "Control strategy of two capacitor voltages for separate MPPTs in photovoltaic systems using neutral-point clamped inverters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3295–3303, Aug. 2015.

[3] C. Xia, G. Zhang, Y. Yan, X. Gu, T. Shi, and X. He, "Discontinuous space vector PWM strategy of neutral-point-clamped three-level inverters for output current ripple reduction," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5109–5121, Jul. 2017.

[4] J. Chivite-Zabalza, M. R. Vidal, P. Izurza-Moreno, G. Calvo, and D. Madariaga, "A large-power voltage source converter for FACTS applications combining three-level neutral-point-clamped power electronic building blocks," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4759–4772, Nov. 2013.

[5] A. Laka, J. Barrena, J. Chivite-Zabalza, M. Á. Rodríguez Vidal, and P. Izurza-Moreno, "New hexagonal three-phase voltage-source converter topology for high-power applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 30–39, Jan. 2015.

[6] S. Bhattacharya, D. Mascarella, G. Joós, J. Cyr, and J. Xu, "A dual Three-level T-npc inverter for high-power traction applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, pp. 668–678, Jun. 2016.

[7] Z. Liu, Z. Zheng, S. D. Sudhoff, C. Gu, and Y. Li, "Reduction of common-mode voltage in multiphase two-level inverters using SPWM with phase shifted carriers," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6631–6645, Sep. 2016.

[8] C. Hu *et al.*, "An improved virtual space vector modulation scheme for three-level active neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7419–7434, Oct. 2017.

[9] M. Cavalcanti, A. Farias, K. Oliveira, F. Neves, and J. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 435–443, Jan. 2012.

[10] J. Lee and K. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformer-less photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014.

[11] X. Wang *et al.*, "Model predictive control methods of leakage current elimination for a three-level T-type transformer-less PV inverter," *IET Power Electron*, vol. 11, no. 8, pp. 1492–1498, Jul. 2018.

[12] SMA Solar Technology, "Capacitive leakage currents," [Online]. Available: https://files.sma.de/dl/Ableitstrom-TI-en-25.pdf

[13] S. Chen, T. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1365–1370, Nov./Dec. 1996.

[14] H. Akagi, and S. Tamura, "A passive EMI filter for eliminating both bearing current and ground leakage current from an inverter driven motor," *IEEE Trans. Power Electron.*, vol. 21, pp. 1459–1469, Sep. 2006.

[15] H. Akagi and T. Oe, "A specific filter for eliminating high-frequency leakage current from the grounded heat sink in a motor drive with an active front end," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 763–770, Mar. 2008.

[16] N. Perera, A. Haque, and J. Salmon, "A preprocessed PWM scheme for three-limb core coupled inductor inverters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4208–4217, Sep. 2016.

[17] D. Boillat, F. Krismer, and J. Kolar, "EMI filter volume minimization of a three-phase three-level T-type PWM converter system," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2473–2480, Apr. 2017.

[18] X. Li, X. Xing, C. Zhang, A. Chen, C. Qin, and G. Zhang, "Simultaneous common-mode resonance circulating current and leakage current suppression for Transformer-less three-level T-Type PV inverter system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4457–4467, Jun. 2019.

[19] S. Chee, S. Ko, H. Kim, and S. Sul, "Common-mode voltage reduction of three-level four leg PWM converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4006–4016, Sep. 2015.

[20] K. Dagan, A. Zuckerberger, and R. Rabinovici, "Fourth-arm common-mode voltage mitigation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1401–1407, Feb. 2016.

[21] A. Hota, S. Jain, and V. Agarwal, "A modified T-structured three-level inverter configuration optimized with respect to PWM strategy used for common-mode voltage elimination," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4779–4787, Sep./Oct. 2017.

[22] P. Kumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A three-level common-mode voltage eliminated inverter with single DC supply using flying capacitor inverter and cascaded h bridge," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1402–1409, Mar. 2014.

[23] J. Wang *et al.*, "A novel discontinuous modulation strategy with reduced common-mode voltage and removed DC offset on neutral point voltage for neutral point clamped Three-level converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7637–7649, Aug. 2019.

[24] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "A space vector modulation scheme of the quasi-Z-source three-level T-type inverter for common-mode voltage reduction," *IEEE Trans. Ind. Electron.,* vol. 65, no. 10, pp. 8340–8350, Oct. 2018.

[25] T.-K. T. Nguyen, N.-V. Nguyen, and N. R. Prasad, "Novel eliminated common-mode voltage PWM sequences and an online algorithm to reduce current ripple for a three-level inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7482–7493, Oct. 2017.

[26] T.-K. T. Nguyen and N.-V. Nguyen, "An efficient four-state zero common-mode voltage PWM scheme with reduced current distortion for a three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1021–1030, Feb. 2018.

[27] Z. Quan and Y. Li, "Impact of PWM schemes on the common-mode voltage of interleaved three-phase two-level voltage source converters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 852–864, Feb. 2019.

[28] Q. Zhang, X. Xing, and K. Sun, "Space vector modulation method for simultaneous Common-mode voltage and circulating current reduction in parallel three-level inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3053–3066, Apr. 2019.

[29] G. Konstantinou, J. Pou, G. J. Capella, K. Song, S. Ceballos, and V. G. Agelidis," Interleaved operation of three-level neutral point clamped converter legs and reduction of circulating currents under SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3323–3332, Jun. 2016.

[30] Z. Quan and Y. Li, "Phase-disposition PWM based 2DoF-interleaving scheme for minimizing high frequency ZSCC in modular parallel three-level converters," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10590 - pp. 10599, Nov. 2019.

[31] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, Feb. 2012.

[32] K. Shukla, M. Varun, and R. Maheshwari, "A novel carrier-based hybrid PWM technique for minimization of line current ripple in two parallel interleaved two-level VSIs," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 1908–1918, Mar. 2018.

[33] Z. Quan and Y. Li, "A three-level space vector modulation scheme for paralleled converters to reduce circulating current and common-mode voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 703–714, Jan. 2017.

[34] D. Jiang, Z. Shen, and F. Wang, "Common-mode voltage reduction for paralleled inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3961–3974, May 2018.

[35] W. Li, X. Zhang, Y. Zhuang, G. Zhang, G. Wang, and D. Xu, "A five level space vector modulation scheme for parallel operated three level inverters with reduced line current distortion," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11235–11249, Jun. 2020.

[36] W. Li, X. Zhang, Z. Zhao, G. Zhang, G. Wang, and D. Xu, "Implementation of five-level DPWM on parallel three-level inverters to reduce common mode voltage and AC current ripples," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4017–4027, Jul. 2020.

[37] A. Zorig, S. Barkat, M. Belkheiri, A. Rabhi, and F. Blaabjerg, "Novel differential current control strategy based on a modified three-level SVPWM for two parallel-connected inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1807–1818, Dec. 2017.

Weiwei Li (Student Member, IEEE) was born in Henan Province, China, in 1982. He received the B.S. and M.S. degrees in electrical engineering, in 2006 and 2008, respectively, from Harbin Institute of Technology, Harbin, China, where he is currently working toward the Ph.D. degree with the Department of Electrical Engineering.

His current research interests include modulation and control of multilevel converters, and renewable energy conversion systems.

Xueguang Zhang (Member, IEEE) was born in Heilongjiang Province, China, in 1981. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2003, 2005, and 2010, respectively.

Since 2015, he has been an Associate Professor with the Department of Electrical and Engineering, Harbin Institute of Technology. His current research interests include distributed power generation and renewable energy conversion systems.

Feiyu Zhang was born in Henan Province, China, in 1997. He received the B.S. degree in electric engineering, in 2019, from Harbin Institute of Technology, Harbin, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include the zero-sequence circulating current suppression strategy of parallel three-level converters.

Siyuan Zhang was born in Heilongjiang Province, China, in 1997. He received the B.S. degree in electrical engineering, in 2019, with Harbin Institute of Technology, Harbin, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include voltage source type VSG converter control, and the modeling and stability analysis of grid-connected converter.

Zhichao Fu was born in Shandong Province, China. He received the M.S. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2018.

He is currently an Engineer of the Guangzhou Power Supply Bureau of Guangdong Power Grid Corporation. His research interests include grid-connected converter stability analysis and back-to-back VSC-HVdc transmission.

Gaolin Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2002, 2004, and 2008, respectively.

He has been a Full Professor of Electrical Engineering with Harbin Institute of Technology since 2014. His current research interests include permanent magnet synchronous motor drives, high performance direct-drive for traction system, position sensorless control of ac motors, efficiency optimization control of PMSM, and digital control of power converters.

Dr. Wang serves as a Guest Associate Editor of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, an Associate Editor of IEEE ACCESS, IET ELECTRIC POWER APPLICATIONS, and *Journal of Power Electronics*.

Dianguo Xu (Fellow, IEEE) was born in Heilongjiang Province, China, in 1960. He received the B.S. degree in control engineering from Harbin Shipbuilding Engineering Institute, Harbin, China, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 1984 and 1990, respectively.

Since 1994, he has been a Professor with the Department of Electrical Engineering, Harbin Institute of Technology. His current research interests include robotics, lighting electronics, power quality mitigation, consumer electronics, power electronics, and motor drives.

Dr. Xu is a member of the China Electrotechnical Society and China Power Supply Society.