Letters

Impact of Drain Leakage Current on Short Circuit Behavior of GaN/SiC Cascode Devices

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***Abstract*—The short circuit (SC) behavior of a newly developed GaN-HEMT/SiC-JFET cascode device is investigated in this work. The reverse leakage current through the drain-side PN junction (I_R) of the SiC JFET under SC conditions is measured simultaneously during the SC event. I_R of the SiC JFET increases to 6.4 A at the end of a 5-μs nondestructive SC pulse. The increase of I_R during the SC pulse induces a turning point in the SC current waveform and a dramatic negative threshold voltage shift (>30 V) in the SiC JEFT, resulting in high transient drain-to-source voltage in the GaN HEMT. The underlying mechanism is associated with the increase of local potential in the P-type layer of the SiC JFET with inevitable spread resistance ($R_{\rm SPD}$). It is suggested that reducing $R_{\rm SPD}$ can improve SC capability and high I_R should be considered in SC failure mechanism analysis and the design of external gate resistance of the SiC JFET.**

***Index Terms*—Cascode device, gallium nitride (GaN) high-electron-mobility transistors (HEMT), short circuit (SC) current, silicon carbide (SiC) junction field-effect transistor (JFET), threshold voltage.**

I. Introduction

WIDE-BANDGAP semiconductors enable more favorable tradeoff between specific ON-resistance and breakdown voltage ($R_{SP,\rm ON}$ vs. V_{BK}), faster switching speed and higher operating temperatures in power transistors, compared with conventional silicon-based power devices [1]–[3]. Power devices based on gallium nitride (GaN) and silicon carbide (SiC) are being commercialized and have been deployed to realize high-efficiency power converters with greatly reduced size [4], [5]. For example, planar GaN-on-Si power high-electron-mobility transistors (HEMTs) can be used in low- and medium-voltage (15 ∼ 650 V) and high frequency (100 kHz ∼ 10 MHz range) applications such as LiDAR (light detection and ranging), compact fast chargers for mobile devices, and UPS (uninterrupted power supplies). 650-V ∼ 1700-V SiC power devices are being adopted in industrial power supplies, photovoltaic inverters, on-board chargers, motor drives for electric vehicles, etc.

Manuscript received March 11, 2021; revised April 7, 2021; accepted April 21, 2021. Date of publication April 27, 2021; date of current version July 30, 2021. This work was supported in part by Shenzhen Science and Technology Innovation Committee under Grant JCYJ20170818113423666 and in part by Hong Kong Research Grants Council's Research Impact Fund under Grant R6008-18. *(Corresponding author: Kevin J. Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3076002.

Digital Object Identifier 10.1109/TPEL.2021.3076002

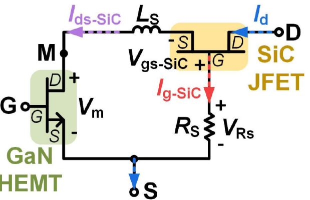

Fig. 1. Schematic of a GaN/SiC cascode device. $R_{\rm S}$ is a current sensing resistor for gate current of the SiC JFET ($I_{\text{g-SiC}}$). $L_{\rm S}$ is the internal stray inductance.

A recently reported GaN/SiC cascode device combines the benefits of the GaN HEMT and SiC junction field-effect transistor (JFET) (Fig. 1) [6]–[8]. The low voltage (LV) GaN HEMT is used for normally-OFF gate control and the normally-ON SiC JFET provides high voltage (HV) blocking capability. The GaN/SiC cascode device makes up for the shortcomings of GaN HEMTs by exhibiting avalanche capability, negligible dynamic ON-resistance ($R_{\rm ON}$) degradation, and dynamic threshold voltage (V_{TH}) shift under high drain bias stress [6]. Compared with SiC MOSFETs and Si/SiC cascode devices, GaN/SiC cascode devices show faster switching speed, lower switching loss, greatly improved thermal stability in V_{TH} and negligible reverse recovery [6], [7].

For power semiconductor devices used in industrial and automotive applications, reliability and robustness are important, especially under harsh operating conditions such as high temperature, short circuit (SC), and unclamped inductive switching. Among them, SC events could occur as a result of unintended situations such as SC across the load and faulty gate control signals in the half-bridge configuration. In a SC event, the device operates in the saturation region with simultaneous presence of ON-state gate voltage, high drain-to-source voltage (V_{ds}), and high drain current (I_d). In general, SC events impose extreme local thermal stress to the device and their impact to device characteristics needs to be comprehensively investigated.

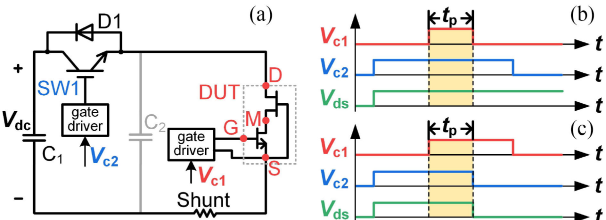

Fig. 2. (a) Schematic diagram of the SC test circuit. (b) First and (c) second control sequence and schematic of V_{ds}. C_2 is only used for the first control sequence to reduce the V_{ds} spike during the turn-OFF transient [10]. The case temperature (T_C) of the DUT is 25 °C.

Although SC robustness of commercial SiC and GaN power devices has been extensively studied [9], [10], the SC behavior of GaN/SiC cascode devices has not been investigated yet. In the SC condition, most power loss and heat are generated in the HV SiC JFET. The SC withstand time (SCWT) of SiC JFETs and Si/SiC cascode devices have been reported to vary from several microseconds to several milliseconds depending on the SC current density and V_{ds} [11]–[13]. Meanwhile, the latest commercial SiC JFET has not been evaluated in terms of SC performances [14], [15].

In this work, SC behaviors of 650-V GaN/SiC cascode devices are characterized and analyzed. It is found that the I_d waveform shows a turning point in the ON-state and tail current in the OFF-state. Threshold voltage of the SiC JFET ($V_{TH\text{-SiC}}$) experiences a dramatic decrease, leading to high transient V_{ds} of the GaN HEMT (V_m) after the turn-OFF. The underlying mechanism is revealed by analyzing the influence of drain-side leakage current in the JFET.

II SC Current

A. DUT and SC Test Setup

The device under test (DUT) is a GaN/SiC cascode device composed of a 40-V/4-mΩ GaN HEMT and a 650-V/80-mΩ SiC JFET (Fig. 1) [15], [16]. $V_{TH\text{-SiC}}$ is −9.5 V at $V_{ds} = 0.1$ V, $I_d = 1$ mA and a case temperature (T_C) of 25 °C. The SC test circuit is similar to the one reported previously [Fig. 2(a)] [10]. In the SC event, SW1 and the DUT are both in the ON-state. The saturation current of SW1 is much higher than that of the DUT. Thus, the high bus voltage (V_{dc}) provided by the storage capacitor (C_1) is mostly dropped across the DUT that operates in the saturation region. Two control sequences are adopted as shown in Fig. 2(b) and (c). In Fig. 2(b), the SC pulse is ended by gate turn-OFF of the DUT and high V_{ds} is maintained in the OFF-state. In Fig. 2(c), SW1 is turned off first to reduce V_{ds} to zero at the end of a SC pulse.

B. SC Waveforms

Fig. 3 shows SC waveforms of a cascode device tested with the first control sequence [Fig. 2(b)]. The trend of junction temperature in the SiC JFET [$T_{\text{j-SiC}}$, Fig. 3(d)] is simulated in Ansys Workbench using a three-dimensional heat source with

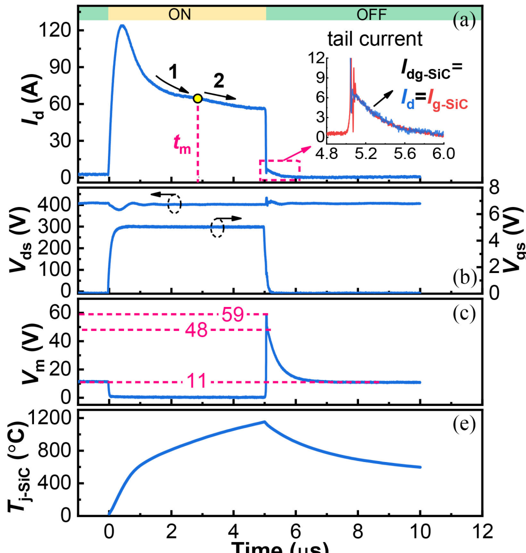

Fig. 3. (a) I_d, (b) V_{ds}, *and* V_{gs}. (c) V_m waveforms of a DUT tested with the first control sequence [Fig. 2(b)]. (d) Simulated $T_{j\text{-SiC}}$. The inset of (a) is I_d and $I_{g\text{-SiC}}$ after the gate turn-OFF. SC test conditions: $V_{\text{dc}} = 400$V, $V_{gs} = 5$ V/0 V, $t_p = 5$ μs, $R_S = 50$ mΩ.

the vertical distribution of heat generation rate similar to that in [17]. $T_{\text{j-SiC}}$ is defined as the average temperature in the top surface of the heat source and is close to the maximum temperature. $T_{\text{j-SiC}}$ rises during the ON-state and decreases during the OFF-state. The ON-state I_d waveform is clearly separated into two phases by a turning point at t_m where the I_d change rate exhibits an obvious discontinuity [Fig. 3(a)]. I_d decreases more slowly as the device operates in each phase. However, the decreasing rate in the beginning of phase 2 is higher than that at the end of phase 1. A similar turning point in the SC I_d waveform of another SiC JFET was reported and explained by forward bias of the gate-to-source junction induced by the increase of voltage across the external gate resistance [11], [18]. For the JFET in our work, the corresponding external gate resistance of 50 mΩ is negligible. Similar turning points have never been observed in the SC waveforms of SiC MOSFETs or GaN HEMTs.

Gate current of the JFET ($I_{g\text{-SiC}}$, Fig. 1) in the ON-state is much lower than that after the turn-OFF [inset of Fig. 3(a)], which is measured with a 50-mΩ current sensing resistance (R_S, Fig. 1). The waveforms in the OFF-state will be discussed in Section III. To explain different $I_{g\text{-SiC}}$ in the ON-state and OFF-state, ON-state $I_{g\text{-SiC}}$ is measured more accurately through R_S with higher values as shown in Fig. 4. To avoid HV across R_S (V_{Rs}), the high OFF-state $I_{g\text{-SiC}}$ is eliminated by reducing V_{ds} to zero at the end of the SC pulse with the second control sequence in Fig. 2(c). With the same R_S, the turning points in I_d, $I_{g\text{-SiC}}$, and V_{Rs} waveforms are located at the same time (t_m), indicating the same mechanism. With a larger R_S, the turning point appears earlier. Despite different R_S, $I_{g\text{-SiC}}$ shows nearly identical characteristics before t_m. After t_m, $I_{g\text{-SiC}}$ increases

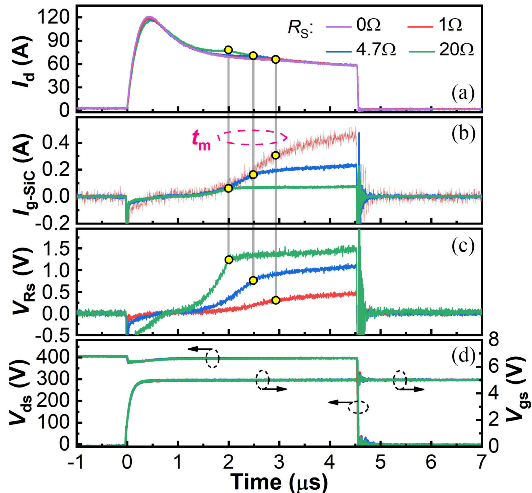

Fig. 4. (a) I_d, (b) $I_{g\text{-SiC}}$, (c) V_{Rs}, and (d) V_{ds} and V_{gs} waveforms of a DUT tested with different R_S and the second control sequence [Fig. 2(c)]. SC test conditions: $V_{\text{dc}} = 400$V, $V_{gs} = 5$ V/0 V, $t_p = 4.5$ μs.

more slowly. These characteristics help understand the mechanism of the turning point as follows.

C. Analysis of Current Waveforms

Considering the negative temperature coefficient of electron mobility, channel current ($I_{ch} \approx I_d$) of the SiC JFET will decrease more and more slowly [19]. In a SC pulse, $T_{\text{j-SiC}}$ increases due to high power. Higher $T_{\text{j-SiC}}$ leads to lower electron mobility and I_{ch}. Lower I_{ch} in return decelerates the $T_{\text{j-SiC}}$ rise, leading to slower decrease of I_{ch} with time.

Before t_m (Figs. 3 and 4), the local potential increase of the lower P layer (LP) in the JFET also contributes to the slower decrease of I_d with time [Fig. 5(c)]. The drain-side reverse leakage current (I_R) flows from drain to gate through the N^+ layer, the N^- layer, LP, and the P^+ layer. In LP [Fig. 5(b)], I_R flows toward and converges in the P^+ region near the gate contact. Due to the existence of spread resistance (R_{SPD}), local LP potential is higher than the gate potential. I_R increases with rising $T_{\text{j-SiC}}$ because the density of minority carriers increases at higher temperature due to thermal generation of electron-hole pairs [Fig. 3(d)]. Thus, the local LP potential keeps rising, and I_{ch} ($\approx I_d$) is being enhanced. In Fig. 5(c), an equivalent circuit with a virtual internal gate node (G_i) is built for the DUT to facilitate the explanation. As the voltage between G_i and the JFET source increases with I_R that flows through R_{SPD}, I_{ch} is enhanced.

With the increase of local LP potential, the source-side LP-N diode (D_1) is turned on after t_m [Fig. 5(d)]. Part of I_R (I_{npn}) flows to the JFET source through D_1, leading to reduced rising rate of $I_{g\text{-SiC}}$ [Fig. 4(b)]. D_1 forward conduction inhibits LP potential increase. In other words, G_i potential is clamped. Thus, I_d decreases more rapidly after t_m [Figs. 3(a) and 4(a)].

With a higher R_S and similar $I_{g\text{-SiC}}$, V_{Rs} and thus $V_{\text{gs-SiC}}$ increase faster [Figs. 1 and 4(c)]. Therefore, I_{ch} ($\approx I_d$) decreases more slowly and even increases before t_m [Fig. 4(a)]. Besides, D_1 is turned on earlier and the turning point appears earlier [Fig. 5(d)]. Since V_{Rs} of different R_S can only induce a negligible change of 0 $\sim$1.5 V in the drain-to-gate voltage of the JFET of $\sim$400 V [Fig. 4(c)], I_R is nearly not influenced by R_S, which equals $I_{g\text{-SiC}}$ before t_m. Thus, positive $I_{g\text{-SiC}}$ waveforms before t_m nearly coincide regardless of R_S [Fig. 4(b)].

R_{SPD} of LP can be lowered by reducing the cell width [W, see Fig. 5(a) and (b)] or increasing the thickness of LP, which inhibits the local LP potential (i.e., G_i potential) increase and accelerates the I_d drop with $T_{\text{j-SiC}}$ during t_p. Thus, $T_{\text{j-SiC}}$ will rise more slowly and SCWT could be prolonged.

III. Dynamic Threshold Voltage of SiC JFET

As shown in the inset of Fig. 3(a), after the GaN HEMT is turned off, a tail current from drain to gate of the SiC JFET ($I_{dg\text{-SiC}}$) decreases from 6.4 A to zero slowly. However, $I_{dg\text{-SiC}}$ is only 76 nA at $T_{j\text{-SiC}} = 25$ °C, $V_{dg\text{-SiC}} = 400$ V and $V_{gs\text{-SiC}} = -20$ V measured by Keysight B1505. In Fig. 3(c), during the turn-OFF transient, V_m rises to 59 V that is lower than the breakdown voltage of the GaN HEMT and drops to 48 V rapidly since the voltage across the internal stray inductance (L_S, Fig. 1) changes with the decrease of JFET source current ($I_{ds\text{-SiC}}$, Fig. 1). Without avalanche capability in the GaN HEMT, V_m is not clamped. Then, V_m falls slowly to 11 V. The high transient V_m (48 V$\sim$11 V) after the turn-OFF transient may be related to $V_{TH\text{-SiC}}$ variation. Therefore, transient transfer *I-V* curves of the SiC JFET immediately after the SC pulse are measured by varying V_m and thus $V_{gs\text{-SiC}}$ after the turn-OFF of the GaN HEMT. Transient V_m is clamped by a Zener diode connected in parallel with the GaN HEMT [Fig. 6(a)]. After the GaN HEMT is turned off, $I_{ds\text{-SiC}}$ flows through the Zener diode.

In Fig. 6(b) and (c), data extraction for transfer *I-V* curves of the SiC JFET is illustrated in $I_{ds\text{-SiC}}$ and V_m waveforms after the GaN HEMT is turned off at 5 μs. $I_{ds\text{-SiC}}$ is mainly composed of I_{ch} instead of I_R and is calculated by $I_{ds\text{-SiC}} = I_d - I_{g\text{-SiC}}$. SC tests are conducted with the first control sequence [Fig. 2(b)]. With lower Zener voltages (V_{Z}), V_m waveforms are clamped at lower values and $I_{ds\text{-SiC}}$ is higher. Assuming $L_S = 10$ nH (overestimated), the voltage across L_S ($L_S{\cdot}\text{d}I_{ds\text{-SiC}}/\text{d}t$) is ~-0.5 V when $I_{ds\text{-SiC}}$ slowly decreases. Thus, $V_{gs\text{-SiC}}$ can be calculated approximately by

$$V_{gs-SiC} \approx V_{Rs} - V_m = I_{g-SiC} \cdot R_S - V_m \tag{1}$$

Considering the switching noise, $I_{ds\text{-SiC}}$ and $V_{gs\text{-SiC}}$ data with a delay time of 180 ns are extracted and plotted in Fig. 6(d).

Data points measured after the GaN HEMT is turned off at $t_{\text{p}} = 4.5$ and 4 μs are also depicted in Fig. 6(d). The transfer *I-V* curves at $T_{\text{j-SiC}}$ near 25 °C are shown for reference. The small number of SC pulses prevents the device degradation that may affect the results in Fig. 6(d). $V_{TH\text{-SiC}}$ decreases by over 30 V with increasing t_p. However, temperature-dependent $|\Delta V_{TH\text{-SiC}}|$ of an ideal SiC JFET would not exceed 3.3 V, which is dominated by changes in built-in potential of the PN junction between gate and source [20]. At $t_p = 5$ μs, $V_{TH\text{-SiC}}$ decreases to ~-43 V at the end of the SC pulse. Therefore, the high transient

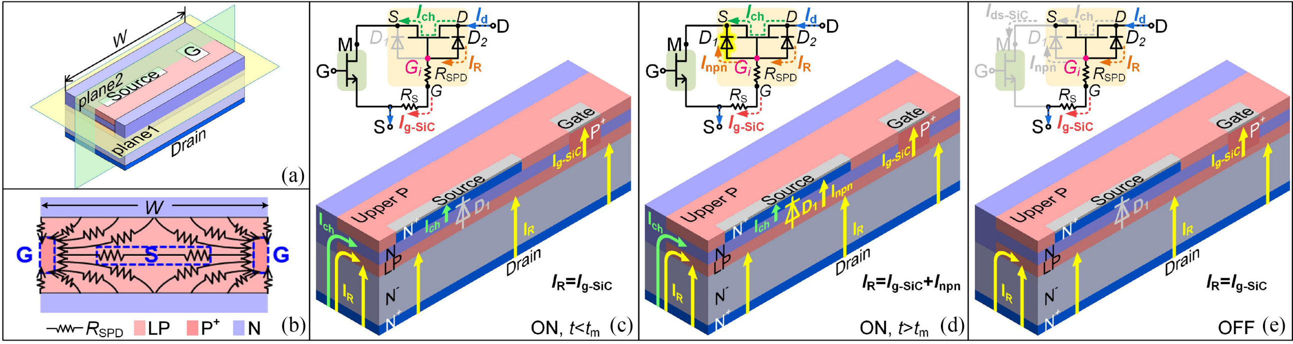

Fig. 5. (a) Schematic of a JFET cell. (b) Schematic I_R path in plane1 of (a). The projections of gate and source contacts are plotted. Schematic paths of I_R and I_{ch} (c) before and (d) after the turning point (t_m) in the ON-state. (e) After the GaN HEMT is turned off are plotted in a half cell divided by plane 2 in (a) and in an equivalent circuit. The arrows do not represent the magnitude of current. LP denotes the lower P layer. $R_{\rm SPD}$ is the spread resistance in LP.

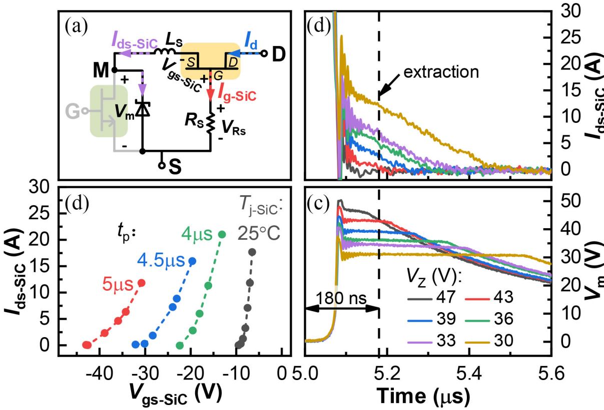

Fig. 6. (a) Schematic of the cascode device with a Zener diode. (b) $I_{ds\text{-SiC}}$ and (c) V_m waveforms after the GaN HEMT is turned off ($V_{\rm dc} = 400$V, $V_{gs} = 5$ V/0 V, $t_p = 5$ μs, $R_S = 50$ mΩ). (d) $I_{ds\text{-SiC}}$-$V_{gs\text{-SiC}}$ curves of the SiC JFET extracted at different t_p, and at $T_{j\text{-SiC}}$ near 25 °C. Data points at $T_{j\text{-SiC}}$ near 25 °C are extracted from ON-state SC waveforms of the individual SiC JFET tested under different ON-state $V_{gs\text{-SiC}}$ and $V_{\rm dc} = 400$ V.

V_m of 48 V after the spike in Fig. 3(c) is mainly induced by the negative $V_{TH\text{-SiC}}$ shift.

The negative $V_{TH\text{-SiC}}$ shift is caused by high I_R, which is not controlled by $V_{gs\text{-SiC}}$ and thus the GaN HEMT. For the DUT without a Zener diode in Fig. 3, all I_R flows toward the JFET gate after the GaN HEMT is turned off while part of I_R flows to the JFET source after t_m in the ON-state [Fig. 5(d) and (e)]. Therefore, $I_{g\text{-SiC}}$ in the OFF-state is higher than that in the ON-state [Fig. 3(a)]. Also, the OFF-state I_R ($=I_{g\text{-SiC}}$) decreases with $T_{j\text{-SiC}}$. After the turn-OFF, high I_R in LP flowing toward the JFET gate leads to high local LP potential compared with the gate potential, i.e., HV between G_i and the JFET gate [Fig. 5(b) and (e)]. Thus, low $V_{gs\text{-SiC}}$ is needed to reduce the voltage between G_i and the JFET source, so that $I_{ds\text{-SiC}}$ ($=I_{ch} + I_{npn}$) can be stopped.

The high I_R should be considered in the SC failure analysis and dv/dt control. The PN junction between drain and gate in the SiC JFET is similar to that between drain and source in the SiC MOSFET. Positive feedback between I_R and $T_{j\text{-SiC}}$ is considered to induce thermal runaway of SiC MOSFETs in SC events while it is difficult to discriminate between I_R and I_{ch} in SiC MOSFETs [9]. The high I_R measured in the JFET may help confirm the SC failure mechanism in the MOSFET and will be considered in the future SC failure analysis of GaN/SiC cascode devices.

The significant OFF-state I_R (tail current) flowing through the JFET gate and the breakdown voltage of the GaN HEMT should be considered together in the selection of external gate resistance of the JFET (R_J) for dv/dt control [Fig. 3(a)] [21]. High I_R through R_J can induce HV across R_J and large V_m after the turn-OFF. The GaN HEMT may be destroyed by drain-to-source overvoltage. To avoid the limitation of SC events on the R_J design, the GaN HEMT should be turned off in a short time (e.g., 3 μs) so that no significant tail current occurs.

IV. Conclusion

The dynamic SC behavior of a 650-V GaN/SiC cascode device is dominated by the SiC JFET. The drain leakage current I_R increases with $T_{j\text{-SiC}}$ in the SC pulse. Since I_R induces higher local potential in LP with $R_{\rm SPD}$ of the JFET, $V_{TH\text{-SiC}}$ decreases dramatically, leading to high transient V_m across the GaN HEMT. With the increase of local LP potential, the source-side PN diode (D_1) is turned on, resulting in a turning point at the same time in I_d and $I_{g\text{-SiC}}$ waveforms, respectively. The reduction of $R_{\rm SPD}$ of LP may improve SC robustness. High $I_{\rm R}$ is an important factor in the future SC failure analysis and R_J selection for dv/dt control.

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