High Gain and High-Efficiency Bidirectional DC–DC Converter With Current Sharing Characteristics Using Coupled Inductor

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***Abstract*—Application of coupled inductor in designing nonisolated bidirectional dc–dc converter provides flexibility to attain high voltage conversion ratio both in buck and boost mode of operation. In this article, a new coupled inductor bidirectional converter is designed with low winding turns ratio ($n = 1$). The proposed topology uses two current path inductor structure which improves voltage conversion ratio and shares current in all operating modes. All the active switches in the proposed topology are soft switched utilizing synchronous rectification concept. Higher efficiency operation is possible as no extra circuit elements are required to achieve soft switching. Leakage energy of coupled inductor is successfully stored in a clamped capacitor which is utilized in the circuit topology. The voltage stress and current stress level of main active switches are low. The proposed circuit is simulated and performance parameters are verified through hardware results. Both simulation and experimental results performed on a 250 W prototype confirm to attain a high efficiency of the proposed converter with simple hardware requirement for practical implementation.**

***Index Terms*—Bidirectional dc–dc converter, coupled inductor.**

I. Introduction

NOW-A-DAYS bidirectional dc–dc converters (BDC) are indispensable as buffer stage which is widely used in the applications like storage interface [1] and electric vehicle (EV) [2]. Traditional two switch nonisolated BDC [3], [4] is not suitable for these applications as it requires extreme duty ratios to attain voltage gain ($\geq$10) in boost mode and ($\leq$1/10) in buck mode to interface low voltage battery, i.e., 12–48 V source to high voltage side i.e., 150—400 V bus [1], [2]. The efficiency and the voltage stress performance are also poor of the conventional BDC. To solve the difficulty in attaining required conversion ratio in both buck and boost mode of operation BDCs are classified into two broad categories, i.e., isolated BDC and nonisolated BDC. Isolated BDC uses transformer as an isolating element which offers flexibility in varying turns ratio and helps in attaining high conversion ratios. However, the number of active switches is generally greater than eight or more in full bridge isolated BDC [5]–[7]. Camped capacitor circuits [8] are used in these topologies to overcome voltage stress due to leakage inductance, which further increase control complexity of these isolated BDC. Half bridge topologies [9] are alternative choice in these categories to reduce the number of active switches. However, achieving soft switching (ZVS) [10] and control complexity is a major problem of these converters. Nonisolated BDCs uses different circuit concepts like SEPIC, voltage multiplier cell, switched capacitor, coupled inductor to achieve high conversion ratio. The efficiency of SEPIC derived BDCs [11] is low because of its cascaded structure. Voltage multiplier cell can be used in designing BDCs but it creates large voltage stress across switches. Switched capacitor based BDCs [12]–[14] are inherently perform better because of its simple structure and less control complexity. However, the switching loss and large switch current stress in these types of converter continues to be the major problem. Hybrid structures, like SEPIC with switched capacitor and quasi-Z source with switched capacitor [15] are capable of achieving high conversion factor. But large component count and inability to achieve soft switching limits conversion efficiency. In contrary coupled inductor based BDCs are well suited for achieving wide range voltage gain with low stress voltage [16]. The efficiency of these converters is also comparable to the isolated BDCs. By proper circuit arrangement, switch current [17] and voltage stress can also be minimized. The leakage inductance energy can be stored in clamped capacitor which can be utilized in power flow. Soft switching, i.e., ZVS of active switches in these converters can be attained using auxiliary circuit [18]–[20] but has limited gain and control complexity. However, soft switching of these converters can be achieved using synchronous rectification concept which do not require extra circuit elements.

In the last decade, there are many coupled based bidirectional dc–dc converter topology is proposed in this direction. The fundamental topology with interleaved structure is proposed by Yang *et al.* [21] as shown in Fig. 1(a). Intermediate capacitor-based topology is proposed [22] in modification of

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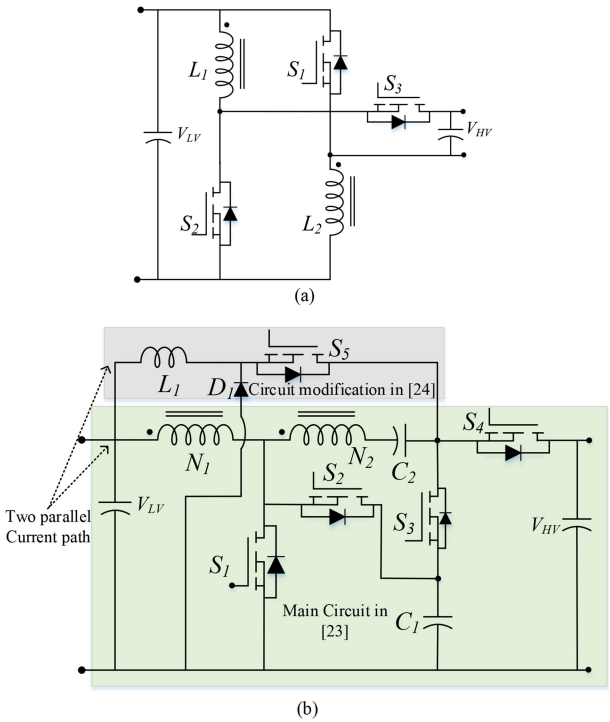


Fig. 1. BDC configurations using coupled inductor. (a) Interleaved structure by Yang *et al.* [21]. (b) Clamped capacitor-based high gain circuit [23] and modified circuit [24].

initial topology to increase the voltage gain but lost parallel inductor structure which is helpful in current sharing during buck mode. The main topology which recovers the leakage energy in a clamped capacitor and use it in circuit operation is originally proposed by Duan *et al*. [23] as shown in Fig. 1(b). This topology has inherently higher conversion ratios, i.e., $(n+2)/(1–d)$ and $(d/n+2)$ in boost and buck mode, respectively. This topology also has the capability to achieve soft switching.

The current sharing in buck mode is not achieved in this topology which was rectified by Wai *et al*. in [24], where extra inductor is used in parallel to the coupled inductor as shown in Fig. 1(b). This extra inductor is used in buck operation and remained unused in boost operation which left a research gap. Topology proposed by Das *et al*. [25] can achieve soft switching like [23] but conversion ratio is inferior. Exactly same circuit like in [23] with one extra capacitor is proposed in [26] which provides same performance like original circuit. Circuit proposed by Hassan *et al*. [27] utilized the same structure [23] with a small modification by branching coupled inductor but reached to the same conversion factor as in the original circuit. Amir *et al*. [28] proposed same coupled inductor based BDC as previously proposed in [24]. Quasi resonant operation of same [23] BDC structure where coupled inductor is replaced by simple inductor is proposed [29] which is further generalized to make the topology suitable for high power application. But the basic circuit structure remains the same. Liu *et al*. [30] utilized the same structure but branching coupled inductor path leads to reduced voltage gain compared to the original circuit [23]. Interleaved structure using two extra inductors is utilized by the proposal [31] to achieve current sharing, whereas coupled inductor increases the voltage conversion factor. Interleaved structure with switched capacitor network [32], [33] is also promising solution in nonisolated BDC circuit design. Though topology [31] performs better in terms of gain, stress level, and efficiency compared to [25], [27] but circuit operation is complex with additional parallel inductors. However, the limitation of [31] can be eliminated by effectively utilizing the coupled inductor.

In this article, a coupled inductor based bidirectional dc–dc (CIBDC) is proposed which is capable of achieving the following.

1) Higher conversion ratio both in buck and boost mode compared to proposals [23], [25], [27] and [31] for less winding turns ratio ($n = 1$).
2) Sharing current in either mode of operation due to parallel path structure utilizing coupled inductor and it do not need extra inductors [31]. This proposal has major advantage compared to the initial work [24] that coupled inductor winding is used to create parallel path which shares current in both operating modes and helps in increasing conversion ratio, reducing coil size unlike an extra inductor path [24] which is unused during boosting operation.
3) Clamped capacitor helps to recover leakage energy which helps in increasing the efficiency.
4) All switches are soft switched (ZVS) utilizing synchronous rectification concept which further improves the efficiency.
5) Low main switch current and voltage stress.

The topology derivation of this proposal is discussed in the next section.

II. Circuit Topology Derivation of the Proposed Converter

Circuit design of BDC using the coupled inductor has the flexibility to improve voltage conversion factor without increasing the complexity of the circuit. Reduction in input current ripple and current sharing is possible by using parallel structure as shown in Fig. 1(a). Voltage gain can be improved using cascading structure [35] as shown in Fig. 2(a). However, the hard-switched cascading structure has less efficiency and do not have current sharing benefit. To achieve high conversion factor and soft switching using synchronous rectifier concept secondary coupled inductor branch is used primarily in [23] as shown in Fig. 1(b). Later modification of the secondary coupled inductor branch position is adopted in [25] as shown in Fig. 2(b) to achieve current sharing and higher gain but fails to achieve it. Similarly, modification in coupled inductor branch position is mentioned in [27] as shown in Fig. 2(c) to achieve same objectives but the performance parameter remains same as [23].

In the proposed CIBDC, two secondary coupled inductor branches are used to achieve higher voltage conversion factor, current sharing characteristics along with soft switching, i.e., ZVS of all active switches using synchronous rectification concept as shown in Fig. 3.

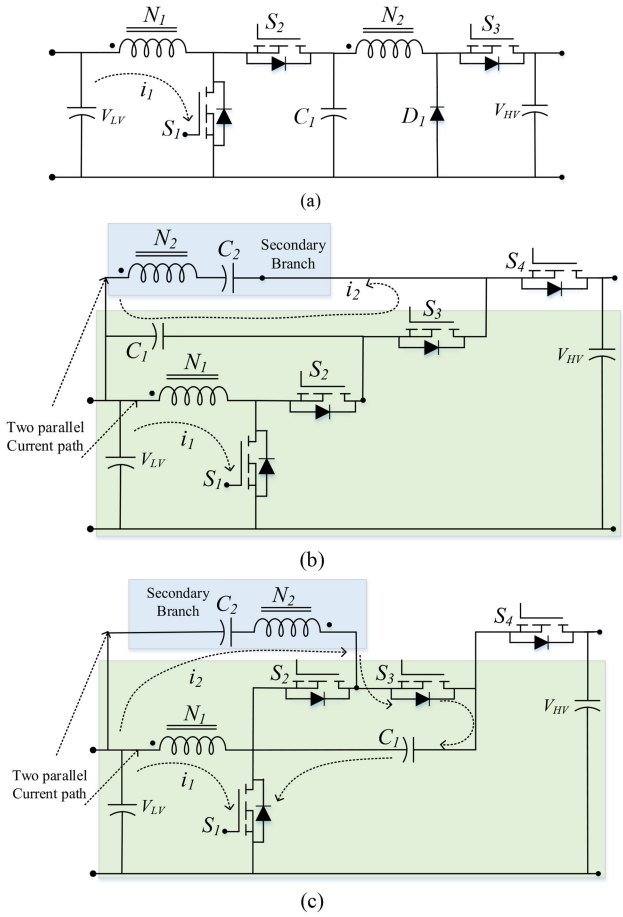


Fig. 2. BDC configurations using the coupled inductor. (a) Cascade structure by Liang *et al.* [35]. (b) Position changing secondary branch [25] of coupled inductor. (c) Rearrangement of secondary branch [27] of the coupled inductor.

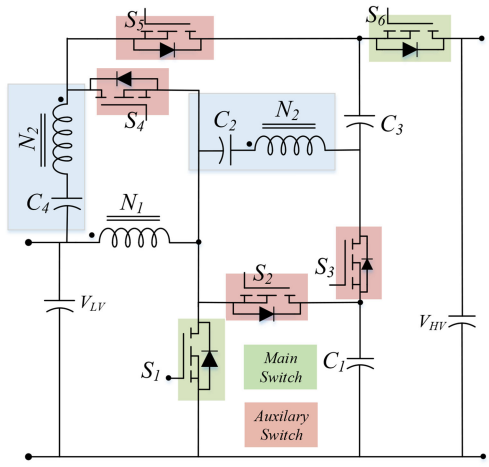


Fig. 3. Proposed coupled-inductor based bidirectional converter (CIBDC) using two secondary branches.

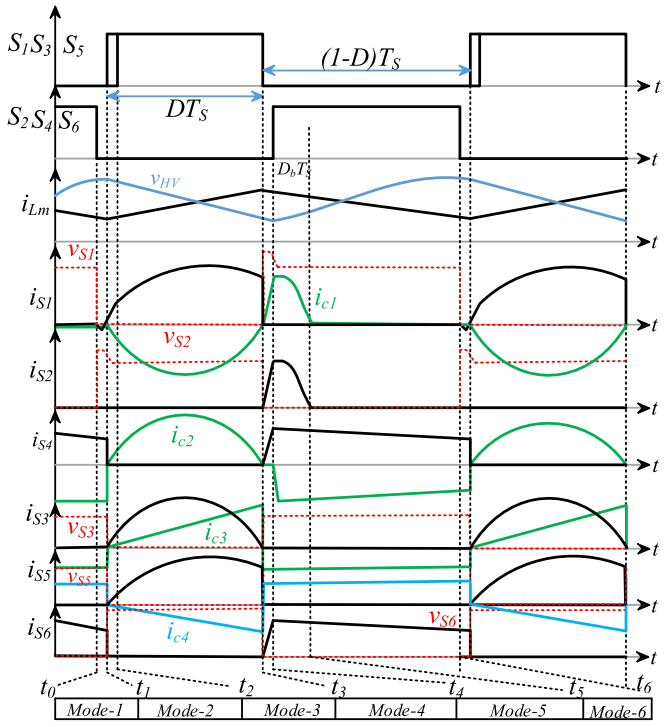


Fig. 4. Key waveforms of the proposed CIBDC in boost mode.

III. Steady State Operation of the Proposed Converter

Two secondary coupled inductor winding branches are used in the proposed BDC as shown in Fig. 3. The current topology uses six active MOSFET switches, four capacitors and coupled inductor to design CIBDC. To simplify the analysis, coupled inductor is modelled as an ideal transformer with two secondary winding and magnetizing inductance L_m. Leakage inductance $L_{\rm lk}$ is also considered in the model. Circuit parameter like ripple voltage across capacitors is taken very small and ignored for simplifying analysis. The active MOSFET switches are considered as ideal switches. The ratio of magnetizing inductance ($L_{\rm m}$) to ($L_{\rm m}$+$L_{\rm lk}$) i.e., $\frac{L_{\rm m}}{L_{\rm m}+L_{\rm lk}}$ is considered as coupling coefficient (k), whereas $n=\frac{N_2}{N_1}$ is winding turns ratio. The steady-state operating principle of the proposed CIBDC is discussed using two operating modes, i.e., boost and buck mode in continuous conduction (CCM).

A. Boost Mode of Operation

In the boost mode of operation, power flows from low voltage source ($V_{\rm LV}$) to the high voltage bus ($V_{\rm HV}$). This mode of proposed CIBDC is divided into six subintervals based on switching states as shown in Fig. 4. The circuit operation of six subintervals are shown in Fig. 5 indicates each mode of operation. The high voltage side ($V_{\rm HV}$) circuit model is considered to be a combination of output capacitor and resistance for verifying the boosting operation.

1) Mode 1 [t_0–t_1]: This mode starts from t_0 when S_4 and S_6 are turned OFF under ZVS condition as shown in Fig. 4. The current is diverted through antiparallel body diode of switch S_4 and S_6. Switch S_1 current flows through its body diode which makes S_1 voltage to be zero. The equivalent circuit of the mode is shown in Fig. 5(a). At t_1 this mode ends when switch S_1 is turned ON.

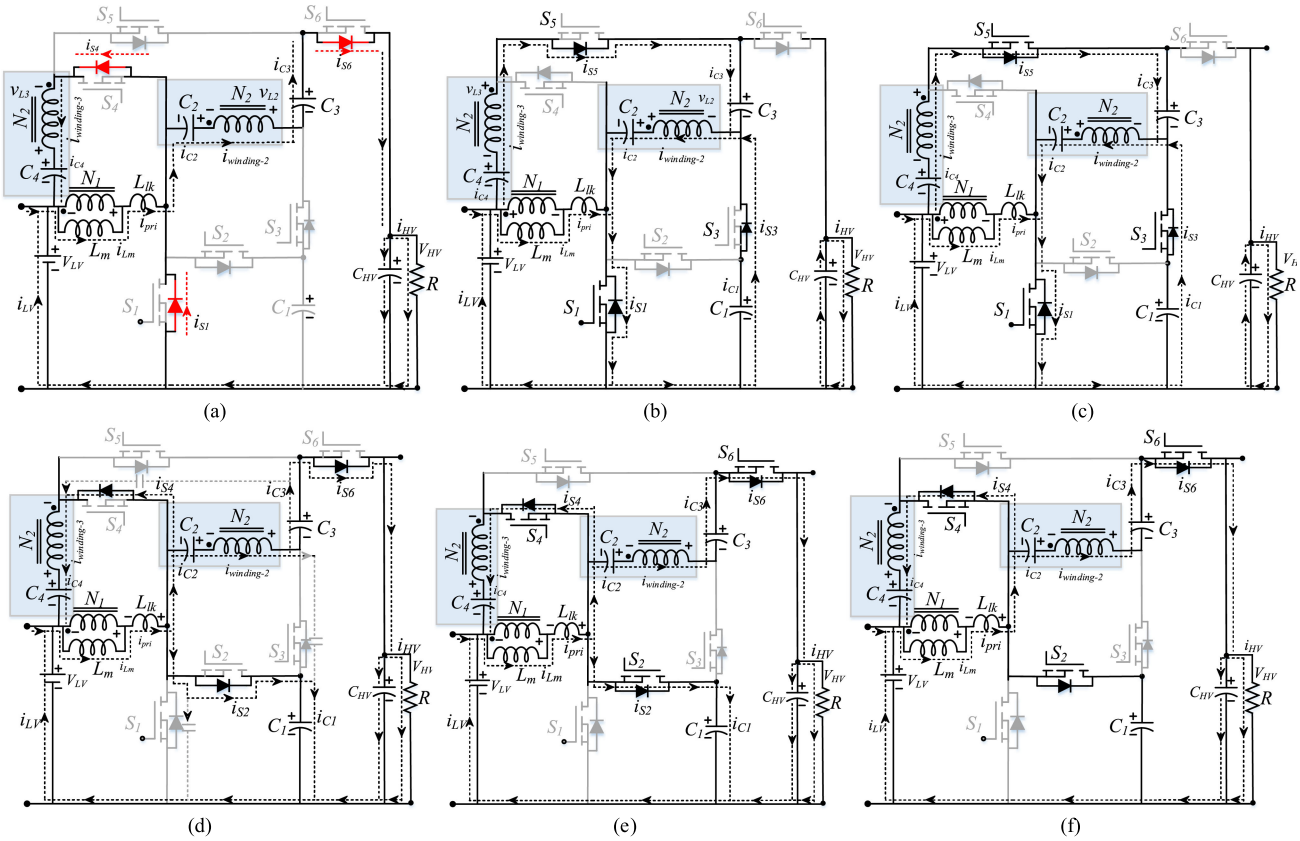


Fig. 5. Operation of the proposed converter in boost mode. (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6].

2) Mode 2 [t_1–t_2]: Body diode of S_1 is conducting before starting of the mode and switch voltage is zero. Therefore, ZVS switch on operation is achieved when switch S_1 is turned ON at the beginning of this mode. The coupled inductor magnetizing current (i_{Lm}) starts rising. The polarity of the coupled inductor secondary and tertiary winding makes the antiparallel body diode of switch S_3 and S_5 forward biased as shown in Fig. 5(b). The capacitor C_1 and C_4 along with coupled inductor secondary, tertiary winding release its energy to capacitor C_2 and C_3. The load current is supplied by the output high voltage side capacitor (C_{HV}). In this mode soft switching operation of S_1, is achieved during turn on similarly like synchronous rectifier. The magnetizing and switch current equation in this mode are as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lm}}}{\mathrm{d}t} = \frac{\mathrm{d}i_{\mathrm{S1}}}{\mathrm{d}t} = \frac{v_{\mathrm{LV}}}{L_{\mathrm{m}}},\ \frac{\mathrm{d}i_{\mathrm{S3}}}{\mathrm{d}t} = \frac{v_{\mathrm{C2}} - v_{\mathrm{C1}}}{n^2 L_1},\ \frac{\mathrm{d}i_{\mathrm{S5}}}{\mathrm{d}t} = \frac{v_{\mathrm{C3}} + v_{\mathrm{C1}} - v_{\mathrm{C4}} - v_{\mathrm{LV}}}{n^2 L_1}. \quad (1)$$

3) Mode 3 [t_2–t_3]: Switch S_3 and S_5 is turned ON at ZVS condition similar to S_1 in this mode. The magnetizing current (i_{Lm}) continues rising. The capacitor C_1 and C_4 along with the coupled inductor secondary, tertiary winding continue to release its energy to capacitor C_2 and C_3 in this mode as shown in Fig. 5(c). The load current is supplied by high voltage side capacitor similar to mode 2. By selecting the proper capacitance values of C_1 and C_2 along with coupled inductor secondary winding inductance (L_{sec}) half cycle quasi resonant current (t_r) operation is possible during DT_s interval ($DT_s = t_r$) which makes switch S_1 current stress lower [17]. Similarly, like synchronous rectifier, soft switching operation of S_3 and S_5 is achieved in this mode.

4) Mode 4 [t_3–t_4]: Switch S_1, S_3, and S_5 are turned OFF at the starting of this mode. The polarity of the coupled inductor primary winding as well as leakage inductance is reversed which naturally turn ON the body diode of switch S_2, S_4 and high voltage side switch S_6 as shown in Fig. 5(d). This makes these switch voltages zero during this mode. The magnetizing energy stored in leakage inductance is transferred through the body diode of switch S_2 to the capacitor C_1. During this mode, capacitor C_4 is in charging mode which stores energy from tertiary winding of the coupled inductor. The stored energy of the capacitor C_2, C_3 and coupled inductor secondary winding is discharged to the high voltage side capacitor and to the load. The magnetizing current starts falling during this mode.

5) Mode 5 [t_4–t_5]: This mode starts with S_2, S_4 and S_6 are turned on at ZVS condition. The magnetizing current (i_{Lm}) continue to fall at this mode. The stored energy of capacitor C_2, C_3 and coupled inductor secondary winding is discharged

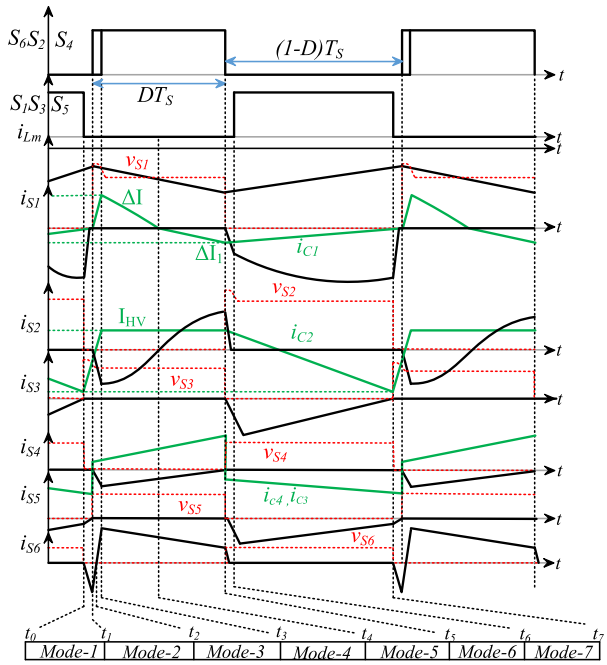


Fig. 6. Key waveforms of the proposed CIBDC in buck mode.

to the high voltage side capacitor and load as shown in Fig. 5(e). This mode ends when S_2 stops conduction as stored leakage energy is transferred to C_1

$$\frac{\mathrm{d}i_{\mathrm{Lm}}}{\mathrm{d}t}=\frac{\mathrm{d}i_{\mathrm{S2}}}{\mathrm{d}t}=\frac{v_{\mathrm{C1}}-v_{\mathrm{LV}}}{L_m},\ \frac{\mathrm{d}i_{\mathrm{S4}}}{\mathrm{d}t}=\frac{v_{\mathrm{LV}}+v_{\mathrm{C4}}-v_{\mathrm{C1}}}{n^2L_1}\ \frac{\mathrm{d}i_{\mathrm{S6}}}{\mathrm{d}t}=\frac{v_{\mathrm{HV}}-v_{\mathrm{C3}}-v_{\mathrm{C1}}}{n^2L_1}. \tag{2}$$

6) Mode 6 [t_5–t_6]: This mode is same as mode 5 only switch S_2 will not carry any charging current to capacitor C_1 as shown in Fig. 5(f).

B. Buck Mode of Operation

In the buck mode operation power flows from high voltage (V_{HV}) source to low voltage (V_{LV}). The buck mode operation of proposed CIBDC is divided into seven subintervals based on switching states as shown in Fig. 6. The circuit operation of seven subintervals are shown in Fig. 7 which indicates each mode of operation. The low voltage side (V_{LV}) circuit model is considered to be a combination of output capacitor and resistance for verifying the buck operation. There are seven operating modes of buck operation within an operating cycle (T_s).

1) Mode 1 [t_0–t_1]: This mode starts from t_0 when S_1, S_3, and S_5 are turned OFF as shown in Fig. 7(a). Due to the polarity of coupled inductor windings, the body diode of switch S_1, S_5, and S_6 become forward biased. In this mode, coupled inductor secondary and tertiary winding current goes to high voltage side using the body diode of switch S_6. This makes possible to turn ON S_6 under ZVS condition which is at the end of the mode at t_1. Switch S_1 and S_5 current decreases to zero value at the end of this mode. S_1 and S_5 is turned OFF at ZVS condition due to conduction of body diodes.

2) Mode 2 [t_1–t_2]: Mode 2 starts from t_1 when S_6 is turned ON at ZVS condition as shown in Fig. 7(b). During this mode, the reverse current which is flowing into high voltage side decreased to zero value as shown in Fig. 6. At the end of this mode, freewheeling stage of buck operation stops.

3) Mode 3 [t_2–t_3]: As S_1 is already on before the starting of this mode, it makes easier to flow power from high voltage side to low voltage side through coupled inductor and capacitor C_3, C_2. This mode is the active mode in buck operation. The body diode of switch S_2 and S_4 are turned ON based on coupled inductor polarity as shown in Fig. 7(a). The magnetizing current (i_{m}) is rising in opposite direction if compared with boost mode of operation as shown in Fig. 6. Capacitor C_1 and C_4 charges in this mode through body diode of switch S_2 and S_4, respectively. The operation of this mode is mentioned in Fig. 7(c). As body diode of S_2 and S_4 are conduction therefore it is possible to turn ON these switches under ZVS condition. This mode ends at t_3 when S_2 and S_4 are turned ON. During this mode low voltage side capacitor and load current is supplied directly by high voltage side.

The magnetizing and switch current equation are as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lm}}}{\mathrm{d}t}=\frac{\mathrm{d}i_{\mathrm{S2}}}{\mathrm{d}t}=\frac{v_{\mathrm{C1}}-v_{\mathrm{LV}}}{L_m},\frac{\mathrm{d}i_{\mathrm{S6}}}{\mathrm{d}t}=\frac{v_{\mathrm{HV}}-v_{\mathrm{C2}}-v_{\mathrm{C3}}-v_{\mathrm{C1}}}{n^2L_1}$$
$$\frac{\mathrm{d}i_{\mathrm{S4}}}{\mathrm{d}t}=\frac{v_{\mathrm{C4}}+v_{\mathrm{LV}}-v_{\mathrm{C1}}}{n^2L_1} \tag{3}$$

4) Mode 4 [t_3–t_4]: In this mode switch S_2 and S_4 are turned ON at ZVS condition. The charging current path is same as mode 3. This mode ends when current through S_2 becomes zero and capacitor C1 is fully charged. The circuit operation of this mode is shown in Fig. 7(d).

5) Mode 5 [t_4–t_5]: As switch S_2 is ON and capacitor C_1 starts discharging in this mode as shown in Fig. 7(e). The other branch current path remains same as mode 4. From mode 3 to mode 5 is the active stage of buck operation. This mode ends when witch S_6 is turned OFF at t_5.

6) Mode 6 [t_5–t_6]: At the starting of this mode S_6 switch is turned OFF. The polarity of coupled inductor changes to maintain continuity of inductor current which makes body diode of switches S_1, S_3, and S_5 forward biased and starts conduction from the beginning of this mode. This state is similar to freewheeling state of conventional buck converter. In this mode, capacitor C_1 discharges and capacitor C_2 and C_3 charges as shown in Fig. 7(f). The magnetizing current starts decreasing in this mode as mentioned in Fig. 6. The switch voltages of S_1, S_3, and S_5 are zero as body diodes are in conduction. This makes possible to achieve ZVS turn ON of corresponding switches in the next mode. The magnetizing and switch current equation in this mode is as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lm}}}{\mathrm{d}t}=\frac{v_{\mathrm{LV}}}{L_{\mathrm{m}}}\ \frac{\mathrm{d}i_{\mathrm{S3}}}{\mathrm{d}t}=\frac{v_{\mathrm{C2}}-v_{\mathrm{C1}}}{n^2L_1}\ \frac{\mathrm{d}i_{\mathrm{S5}}}{\mathrm{d}t}=\frac{v_{\mathrm{C3}}+v_{\mathrm{C1}}-v_{\mathrm{C4}}-v_{\mathrm{LV}}}{n^2\mathrm{L}_1}. \tag{4}$$

7) Mode 7 [t_6–t_7]: This mode starts with turning ON of switches S_1, S_3, and S_5 under ZVS condition. The same operation like mode 6 continues in this mode. This is also like

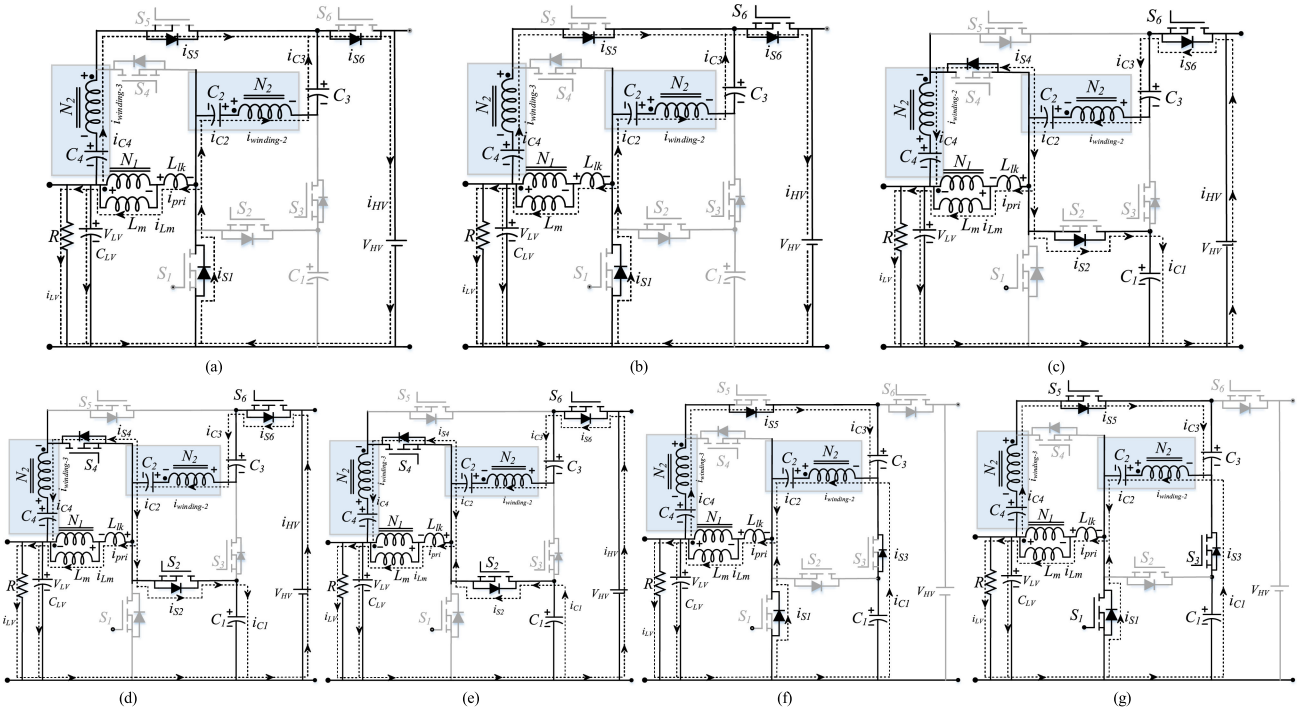


Fig. 7. Operation of the proposed converter in buck mode. (a) Mode 1 [t_0–t_1] (b) Mode 2 [t_1–t_2] (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6]. (g) Mode 7 [t_6–t_7].

a freewheeling mode of the conventional buck converter. This mode ends when switches S_3, S_5, and S_1 are turned OFF and mode-1 repeats the cycle by turning ON body diode of switches S_5 and S_6. The circuit of this mode is shown in Fig. 7(g).

IV. Analysis of the Proposed CIBDC in Steady-State CCM

A. Voltage Gain of Boost Stage

The boost mode operation of the proposed CIBDC is shown in Fig. 5. From Fig. 5(b) which is same as switch on operation of the conventional boost converter, the voltage equations are derived where V_{Lm}, V_{L2}, V_{L3}, V_{Lk}, are main winding voltage, secondary winding voltage, tertiary winding voltage, and leakage inductance voltage, respectively

$$v_{\mathrm{Lm}} = v_{\mathrm{L1}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{LV}} = k v_{\mathrm{LV}} \tag{5}$$

$$v_{\mathrm{Lk}} = \frac{L_{\mathrm{lk}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{LV}} = (1-k) v_{\mathrm{LV}} \tag{6}$$

$$v_{\mathrm{L2}} = v_{\mathrm{L3}} = nk v_{\mathrm{LV}}. \tag{7}$$

Switch ON and OFF time voltage equations of secondary loop as well as third loop are required to apply volt-second balance in coupled inductor primary winding from which C_1 and C_4 voltages can be derived

$$v_{\mathrm{C_1}} = \frac{2D(k-1)+(2-k)}{1-D} v_{\mathrm{LV}} \tag{8}$$

$$v_{\mathrm{C_4}} = \frac{kD(n+1)}{1-D} v_{\mathrm{LV}}. \tag{9}$$

Similarly, from coupled inductor secondary, tertiary winding volt-sec balance, capacitor C_2, C_3 and high voltage side capacitor voltage can be derived

$$v_{\mathrm{C_2}} = \left(nk + \frac{2D(k-1)+(2-k)}{1-D} \right) v_{\mathrm{LV}} \tag{10}$$

$$v_{\mathrm{C_3}} = \left(\frac{Dk(n-2)+k(D+1)+(D-1)}{D(1-D)} \right) v_{\mathrm{LV}}. \tag{11}$$

For ideal coupling coefficient $k = 1$, the boosting voltage gain of CIBDC can be derived from (13)

$$v_{\mathrm{HV}} = v_0 = \frac{2nk+4D\,(k-1)+2\,(2-k)}{1-D} v_{\mathrm{LV}} \tag{12}$$

$$M_{\mathrm{CCM}} = \frac{v_{\mathrm{HV}}}{v_{\mathrm{LV}}} = \frac{2n+2}{1-D} \tag{13}$$

$$v_{\mathrm{C_1}} = \frac{v_{\mathrm{LV}}}{1-D},\ v_{\mathrm{C_2}} = \left(n + \frac{1}{1-D} \right) v_{\mathrm{LV}},\ v_{\mathrm{C_4}} = \left(\frac{D(n+1)}{1-D} \right) v_{\mathrm{LV}}. \tag{14}$$

For different coupling coefficient k value, the boosting voltage gain of the proposed CIBDC is shown in Fig. 8(a). The boosting gain (M_{CCM}) of the proposed CIBDC is compared to other topologies for $n = 1$ as shown in Fig. 8(b). The voltage gain (M_{CCM}) is derived (15) in terms of normalized time constant

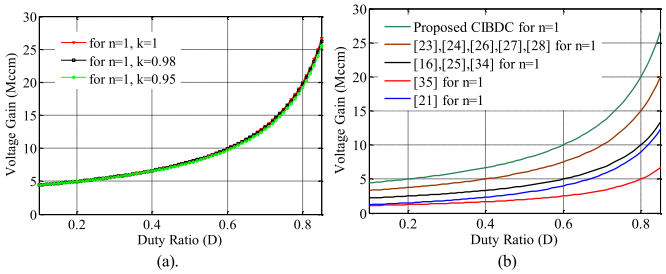


Fig. 8. M_{CCM} (a) for different coupling coefficient (k). (b) Comparison of M_{CCM} of CIBDC and existing topologies @$k = 1$ and $n = 1$.

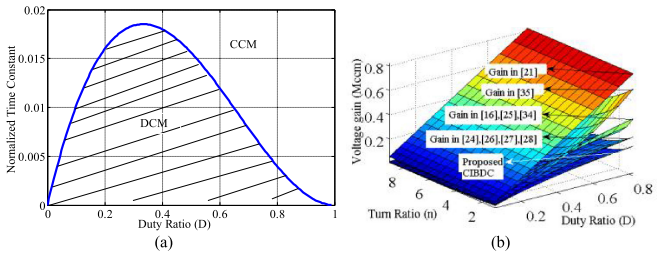


Fig. 9. (a) Normalized time constant at boundary condition in boost mode when $k = 1$. (b)Voltage gain comparison of CIBDC in buck mode.

TABLE I
COMPARISON OF VOLTAGE STRESS

	Proposed	[25], [16], [34]	[24], [26], [27], [28]	[35]	[21]
High Voltage Side (S_6) Switch Stress	$\frac{v_{HV}}{2n+2}$	$\frac{n}{n+1}v_{HV}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{n}$	$\frac{v_{HV}}{1+D}$
Low Voltage Side (S_1) Switch Stress	$\frac{v_{HV}}{2n+2}$	$\frac{v_{HV}}{n+1}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{n}$	v_{HV}

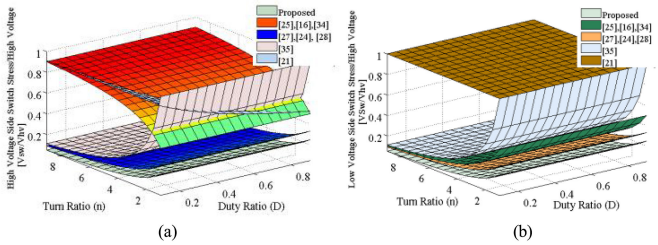


Fig. 10. Switch voltage stress comparison of (a) high voltage side (S_6) and (b) low voltage side (S_1) of CIBDC in CCM.

from CCM and DCM voltage gain and output capacitor charge balance equation.

$$M = (n+1) \pm \sqrt{(n+1)^2 + \frac{D^2}{2\tau_{\mathrm{Lm}}}}. \tag{15}$$

From the boundary condition of CCM and DCM mode the normalized time constant at boundary (τ_{Lmb}) is derived

$$\tau_{\mathrm{Lmb}} = \frac{(1-D)^2 D}{2(n+1)^2}. \tag{16}$$

Thus, correct selection of normalized time constant $\frac{L_{\mathrm{m}}}{RT_s} = \tau_{Lm} > \tau_{Lmb}$., which depends on magnetizing inductance (L_{m}), switching frequency (f_{sw}), and load resistance (R) is essential for ensuring CCM operation of CIBDC as shown in Fig. 9(a).

B. Voltage Gain of Buck Stage

The buck mode operation of the proposed CIBDC is shown in Fig. 7. Form Fig. 7(b) which is the same as switch on operation of conventional buck converter, the voltage equations are derived from volt-sec balance of primary, secondary winding like in boost mode. Loop voltage equations are essential both for switch ON time and OFF time. The capacitor voltage equations are as follows:

$$v_{\mathrm{C_4}} = \frac{k(1-D)(n+1)}{D} v_{\mathrm{LV}} \tag{17}$$

$$v_{\mathrm{C_1}} = \frac{k + 2D(1-k)}{D} v_{\mathrm{LV}} \tag{18}$$

$$v_{\mathrm{LV}} = v_0 = \frac{D}{2nk + 4D(k-1) + 2(2-k)} v_{\mathrm{HV}}. \tag{19}$$

Taking coupling coefficient $k = 1$, the voltage gain in buck mode is derived from (19) and gain is compared with other topologies as shown in Fig. 9(b)

$$\mathrm{M_{CCM}} = \frac{v_{\mathrm{LV}}}{v_{\mathrm{HV}}} = \frac{D}{2n+2} \tag{20}$$

$$v_{\mathrm{C_1}} = \frac{v_{\mathrm{LV}}}{D},\ v_{\mathrm{C_4}} = \left(\frac{(n+1)(1-D)}{D}\right) v_{\mathrm{LV}}. \tag{21}$$

C. Voltage Stress Analysis

There are six switches in the proposed CIBDC. Switch voltage stress (V_{sw}) of S_1 the converter is as follows:

$$v_{\mathrm{S1}} = \frac{v_{\mathrm{LV}}}{1-D} = \frac{v_{\mathrm{HV}}}{2n+2}. \tag{22}$$

Similarly, switch voltage stress for S_2, S_3, S_4, S_5, and S_6 are respectively

$$v_{\mathrm{S2}} = v_{\mathrm{S6}} = \frac{v_{\mathrm{HV}}}{2n+2},\ v_{\mathrm{S3}} = v_{\mathrm{S4}} = \frac{v_{\mathrm{HV}}}{2},\ v_{\mathrm{S5}} = \frac{2n+1}{2n+2} v_{\mathrm{HV}}. \tag{23}$$

The switch voltage stress comparison is mentioned in Table I.

The normalized switch voltage stress for high voltage and low voltage switch is compared and shown in Fig. 10. It is clear that voltage stress is less in the proposed CIBDC. Therefore, the conduction loss can be minimized by selecting low voltage rating switches which has low ON state resistance.

D. Current Stress in CCM

1) Boost Mode: The magnetizing current (i_{Lm}) value can be calculated from of high voltage side capacitor ($\mathrm{C_{HV}}$) change

balance in CCM. The magnetizing current value is as follows:

$$i_{\mathrm{Lm}} = \frac{v_{\mathrm{HV}}(n+1)}{(1-D)R} = \frac{2v_{\mathrm{LV}}(n+1)^2}{(1-D)^2R}. \quad (24)$$

The maximum of magnetizing current (i_{Lm}) value is as follows:

$$i_{\mathrm{Lm\_Peak}} = i_{\mathrm{Lm}} + \frac{\Delta i_{\mathrm{Lm}}}{2} = \frac{2v_{\mathrm{LV}}(n+1)^2}{(1-D)^2R} + \frac{v_{\mathrm{LV}}DT_s}{2L_{\mathrm{m}}}. \quad (25)$$

Coupled inductor winding-2 current is necessary to find peak switch current (i_{S1}) during ON time

$$i_{S1\_\mathrm{Peak}} = i_{Lm\_\mathrm{Peak}} + (n+1)i_{\mathrm{winding2\_Peak}}. \quad (26)$$

The proposed CIBDC is capable of achieving low switch current stress like proposed in [17] by properly selecting C_1, C_2 values and half cycle resonating time. RMS current of switch S_1 can also be minimized.

Thus, the peak current of low voltage switch S_1 is as follows:

$$i_{\mathrm{S1\_Peak}} \cong \frac{2v_{\mathrm{LV}}(n+1)^2}{(1-D)^2R} + \frac{v_{\mathrm{LV}}}{1-D}\sqrt{\frac{C_{\mathrm{eq}}}{\mathrm{L}_2}} + \frac{2v_{\mathrm{LV}}(1+n)}{DR}. \quad (27)$$

Similarly, the peak current for high voltage side switch S_6 is as follows:

$$i_{\mathrm{S6\_Peak}} = \frac{2v_{\mathrm{LV}}(n+1)^2}{n(1-D)^2\mathrm{R}} + \frac{v_{\mathrm{LV}}DT_s}{2n\mathrm{L_m}}. \quad (28)$$

The peak switch currents of S_3, S_2, and S_4 are, respectively

$$i_{\mathrm{S2\_Peak}} = i_{\mathrm{S4\_Peak}} = i_{\mathrm{Lm\_Peak}} \mathrm{and} i_{\mathrm{S3\_Peak}} \cong \frac{v_{\mathrm{LV}}}{1-D}\sqrt{\frac{C_{\mathrm{eq}}}{L_2}}. \quad (29)$$

The RMS values of switch currents during boost mode are derived from current waveform as shown in Fig. 4

$$i_{\mathrm{S1-RMS}} \cong \frac{1+n}{1-D} i_{\mathrm{Lm}}\sqrt{D}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{Lm}}{i_{\mathrm{HV}}}\right)^2\left(\frac{1-D}{n+3}\right)^2} \quad (30)$$

$$i_{\mathrm{S3-RMS}} = \sqrt{\frac{1}{T_s}\int_0^{\mathrm{DT}_s}\left(v_{\mathrm{ceq}}\sqrt{\frac{C_{\mathrm{eq}}}{L_2}}\sin\frac{2\pi}{T_s}t\right)^2 dt} \quad (31)$$

$$i_{\mathrm{S2-RMS}} = \frac{2+2n}{1-D}\sqrt{D_b} i_{\mathrm{HV}} \mathrm{and} i_{\mathrm{S4-RMS}} = \frac{i_{\mathrm{Lm}}}{n}\sqrt{1-D} \quad (32)$$

$$i_{\mathrm{S5-RMS}} = \sqrt{\frac{1}{T_s}\int_0^{\mathrm{DT}_s}\left(v_{\mathrm{ceq}}\sqrt{\frac{C_{\mathrm{eq1}}}{L_{\mathrm{eq}}}}\sin\frac{2\pi}{T_s}t\right)^2 dt} \quad (33)$$

$$i_{S6-\mathrm{RMS}} = i_{Lm-\min}\sqrt{(1-D)\left[1+\frac{1}{3}\left(\frac{\Delta i_{Lm}}{i_{Lm-\min}}\right)^2\right]}. \quad (34)$$

2) Buck Mode: In the buck mode operation of the proposed CIBDC, the switch current stress of S_1 is same as peak magnetizing current as it only conducts during freewheeling time like conventional buck converter

$$i_{\mathrm{S1\_Peak}} = i_{\mathrm{S2\_Peak}} = i_{\mathrm{Lm\_Peak}}. \quad (35)$$

Similarly, the peak current of high voltage side switch S_6 is as follows:

$$i_{\mathrm{S6\_Peak}} \cong \frac{Dnv_{\mathrm{LV}}}{(1-D)L_2}(t_3 - t_2) \quad (36)$$

where t_3–$t_2 = D_cT_s$.

The average magnetizing current during the buck mode of operation is as follows:

$$i_{\mathrm{Lm}} = \frac{n+1-nD}{n+1} i_{\mathrm{LV}} \mathrm{and} \Delta i_{Lm} = \frac{v_{\mathrm{LV}}(1-D)T_s}{L_m}. \quad (37)$$

The RMS values of switch currents during buck mode are derived from current waveform as shown in Fig. 6

$$i_{S1-\mathrm{RMS}} = i_{\mathrm{Lm-min}}\sqrt{1-D+\frac{2}{i_{\mathrm{Lm-min}}}+\left(\frac{\Delta i_{\mathrm{Lm}}}{i_{\mathrm{Lm-min}}}\right)^2} \quad (38)$$

$$i_{\mathrm{S2-RMS}} = \frac{D}{6(n+1)}\sqrt{\frac{5D}{3}} i_{\mathrm{LV}} \mathrm{and} i_{\mathrm{S3-RMS}} = \frac{D\sqrt{1-D}}{6\sqrt{3}(n+1)} i_{\mathrm{LV}} \quad (39)$$

$$i_{\mathrm{S4-RMS}} = \frac{n\mathrm{D}\sqrt{D}}{2\sqrt{3}(n+1)} i_{\mathrm{LV}} \mathrm{and} i_{\mathrm{S5-RMS}} = \frac{n\mathrm{D}\sqrt{1-D}}{2\sqrt{3}(n+1)} i_{\mathrm{LV}} \quad (40)$$

$$i_{\mathrm{S6-RMS}} = \frac{i_{\mathrm{Lm-min}}}{n}\sqrt{D+\frac{D}{3}\left(\frac{\Delta i_{Lm}}{i_{Lm-\min}}\right)}. \quad (41)$$

E. Winding and Capacitor Current

The RMS currents of capacitor C_1, C_2, C_3, and C_4 are calculated from ideal capacitor current waveforms in both buck and boost mode. Similarly, winding RMS currents are also derived in both the operating modes.

The capacitors RMS current in boost mode are given by

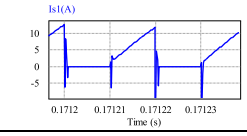
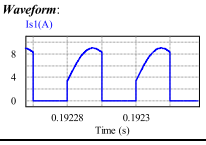
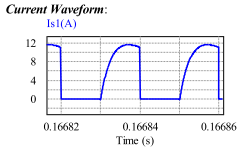
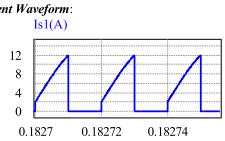
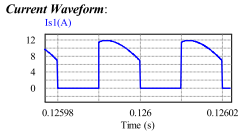
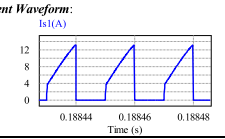
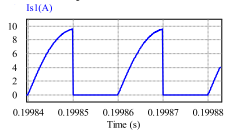
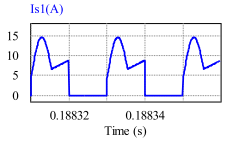
$$i_{\mathrm{c_1(RMS)}} = \sqrt{i^2_{\mathrm{pri\_min}} \times (D_b) + \frac{v^2_{\mathrm{c1}}}{2\pi^2}\frac{c_{\mathrm{eq}}}{L_2}D - \frac{\sin 4\pi \mathrm{D}}{4\pi}} \quad (42)$$

$$i_{\mathrm{c_2(RMS)}} = i_{\mathrm{winding-2(RMS)}} = \sqrt{i^2_{\mathrm{HV}} \times (1-D-D_b) + \frac{v^2_{\mathrm{c1}}}{2\pi^2}\frac{\mathrm{c_{eq}}}{L_2}D - \frac{\sin 4\pi D}{4\pi}} \quad (43)$$

$$i_{\mathrm{c_3(RMS)}} = i_{\mathrm{c_4(RMS)}} = i_{\mathrm{winding-3(RMS)}} = \sqrt{i^2_{\mathrm{HV}}\frac{1-D}{3D}(4-D)} \quad (44)$$

where $D_b = \frac{v_{\mathrm{c1}}D}{4\pi i_{\mathrm{HV}}}\sqrt{\frac{c_{\mathrm{eq}}}{L_2}}(1-\cos(2\pi\mathrm{D}))\times(\frac{1-D}{n+1})$.

TABLE II
COMPARISON OF SWITCH CURRENT STRESS, GAIN, SWITCHES, AND EFFICIENCY @ 200 W

Topology	Main Switch Peak Current at LV side		Main Switch RMS Current at LV side, no of components, Gain and Efficiency		Switch Selection @ 200W Converter Specification	Stress
	Buck	Boost	Buck	Boost		
Proposed	$\frac{n+1-nD}{n+1} i_{LV} + \frac{v_{LV}(1-D)T_s}{2L_m}$ ***Current Waveform***: 	$\frac{2v_{LV}(n+1)^2}{(1-D)^2R} + \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}} + \frac{2v_{LV}(1+n)}{DR}$ ***Current Waveform***: 	$i_{Lm\text{-}min}\sqrt{1-D+\frac{2}{i_{Lm\text{-}min}}+\left(\frac{\Delta i_{Lm}}{i_{Lm\text{-}min}}\right)^2}$ ***Capacitor***:4 ***Switches***:6, ***Efficiency***: 95.6% ***Buck gain***: $=\frac{D}{(2+2n)}$	$\frac{1+n}{1-D}\sqrt{D}i_{Lm}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{Lm}}{i_{HV}}\right)^2\left(\frac{1-D}{n+3}\right)^2}$ or $\approx \frac{2+n+D}{(2+2n)\sqrt{D}} i_{LV}$ ***Boost gain***: $=\frac{2+2n}{(1-D)}$ ***Efficiency:*** 96.13%	FQP34N20 V_{ds}=200V, R_{ds}=0.075Ω I_d=31A. f_{sw}=50kHz *n=1* V_{in}=48V V_o=384V	Low
[27]	$\frac{v_{LV}(n+1)(2+n)}{(1-D)^2R} + \frac{v_{LV}(1-D)T_s}{2L_m}$ ***Current Waveform***: 	$\cong \frac{v_{LV}(n+1)(2+n)}{(1-D)^2R} + \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}$ ***Current Waveform***: 	$\frac{2+n-D}{(2+n)\sqrt{1-D}} i_{LV}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 95.61% ***Buck gain***: $=\frac{D}{(2+n)}$	$\frac{1+n+D}{(2+n)\sqrt{D}} i_{LV}$ ***Boost gain***: $=\frac{2+n}{(1-D)}$ ***Efficiency:*** 96.38%	IPB027N10N5 V_{ds}=100V, R_{ds}=2.7mΩ I_d=120A *n=4.5* f_{sw}=50kHz V_{in}=30V V_o=380V	High
[25]	$\approx \frac{i_{HV}(n+1)}{D} + \frac{v_{LV}DT_s}{2L_m}$ ***Current Waveform***: 	$\approx \frac{i_{HV}(n+1)}{(1-D)} + \frac{v_{LV}DT_s}{2L_m}$ ***Current Waveform***: 	$\approx \frac{nT_s(1-D)\sqrt{1-D}}{L_m\sqrt{3}} v_{LV}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 90% ***Buck gain***: $=\frac{D}{(1+n)}$	$\frac{nT_sD\sqrt{D}}{L_m\sqrt{3}} v_{LV}$ ***Boost gain***: $=\frac{1+n}{(1-D)}$ ***Efficiency:*** 88%	IPA075N15N3 V_{ds}=150V, R_{ds}=0.0075Ω I_d=172A. *n=4* f_{sw}=50kHz V_{in}=40V V_o=400V	High
[16]	$\frac{2P}{V_{LV}} + \frac{V_{HV}}{nR}$ ***Current Waveform***: 	$\frac{P}{V_{LV}} + \frac{(1-D)V_{LV}}{2f_{sw}}\left(\frac{1}{L_1}+\frac{1}{L_m}\right) + i_{pri\_max}$ ***Current Waveform***: 	$\simeq \frac{1+n-D}{(1+n)\sqrt{1-D}} i_{LV}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 96.4% ***Buck gain***: $=\frac{D}{(1+n)}$	$\cong \frac{1+n}{1-D} i_{Lm}\sqrt{D}$ ***Boost gain***: $=\frac{1+n}{(1-D)}$ ***Efficiency:*** 95%	IRFB4332 V_{ds}=250V, R_{ds}=0.033Ω I_d=60A. *n=3.4* f_{sw}=50kHz V_{in}=48V V_o=380V	High

The RMS current of primary winding of the proposed CIBDC is given by the following:

$$i_{\mathrm{pri(RMS)}} = \sqrt{\left[\begin{array}{l}(x^2+x(x-I_{\mathrm{pri\_min}})(1-D)+\frac{(x-I_{\mathrm{pri\_min}})^2}{3}(1-D)+\\ +\frac{v_{c1}}{\pi}\sqrt{\frac{c_{eq}}{L_2}}(1-\cos(2\pi D))+\frac{v_{c1}^2}{2\pi^2}\frac{c_{eq}}{L_2}D-\frac{\sin 4\pi D}{4\pi})\end{array}\right]} \quad (45)$$

where $x \cong \frac{2n+2}{1-D} i_{\mathrm{HV}}$.

Again, during the buck mode of operation, the capacitors RMS currents are given by

$$i_{c_1(\mathrm{RMS})} = \sqrt{\frac{\Delta i^2 D}{2} + \Delta i_1^2\left(1-\frac{D}{2}\right)} \quad (46)$$

where $\Delta i = \frac{n+1}{2L_2}T_s$ and $\Delta i_1 = \frac{n+1}{4L_2}T_s\frac{D}{1-0.5D}$

$$i_{c_2(\mathrm{RMS})} = i_{\mathrm{winding-2(RMS)}} \cong i_{c_3(\mathrm{RMS})} = i_{\mathrm{HV}}\sqrt{D+\frac{4D^2}{1-D}} \quad (47)$$

$$i_{c_4(\mathrm{RMS})} = i_{\mathrm{winding-3(RMS)}}$$

$$= 2i_{\mathrm{HV}}D\left(\frac{2}{1-D}+n\right)\sqrt{1+\frac{1}{D}}. \quad (48)$$

Switch current stress of different topologies is performed and shown in Table II.

F. Converter Circuit Parameter Design

Coupled inductor number of turn (n) is derived from the voltage gain equation of boost mode of CIBDC which is as follows:

$$n \geq \frac{v_{\mathrm{HV}}(1-D)-2v_{\mathrm{LV}}}{2v_{\mathrm{LV}}}. \quad (49)$$

The magnetizing inductance is derived from the normalized time constant at boundary as mentioned in (16). Therefore, to ensure the CCM operation in proposed CIBDC $\frac{L_m}{R_L T_s} = \tau_{Lm} > \tau_{Lmb}$

$$L_m \geq \frac{RD(1-D)^2}{2f_{\mathrm{sw}}(n+1)^2}. \quad (50)$$

High voltage side capacitance (C_{HV}) is derived from the change in capacitor charge based on the change in capacitor

ripple voltage (ΔV)

$$C_{\rm HV} \geq \frac{i_{\rm HV} D}{f_{\rm sw} \Delta v_{\rm HV}}. \tag{51}$$

Low voltage side capacitance is designed from the buck operation using the capacitor charge and voltage ripple

$$C_{\rm LV} \geq \frac{v_{\rm HV}(1-D)}{16(n+1) L_m f_{\rm sw}^2 \Delta v_{\rm LV}}. \tag{52}$$

Similarly, the values of the intermediate capacitor $\rm C_1$, $\rm C_2$, $\rm C_3$, and $\rm C_4$ are derived based on the ripple voltage and charge

$$\rm C_1 \geq \frac{i_{LV} D}{n f_{sw} \Delta v_{C1}} and C_2 \geq \frac{2 i_{LV} D}{n f_{sw} \Delta v_{C2}} \tag{53}$$

$$C_3 \geq \frac{i_{\rm LV} D}{2(n+1) f_{\rm sw} \Delta v_{\rm C3}} \text{and } \rm C_4 \geq \frac{i_{LV} D}{(n+1) f_{sw} \Delta v_{C4}}. \tag{54}$$

Soft switching condition of auxiliary switches, i.e., $\rm S_2$, $\rm S_3$, $\rm S_4$, and $\rm S_5$ are dependent on the leakage inductance and fall in the stored electrostatic energy due to the switch parasitic capacitance. During switch transition, the capacitor stored energy should be dissipated before gaining magnetizing energy due to leakage inductance to achieve the ZVS condition.

G. Theoretical Loss Calculation of CIBDC

The RMS values of switch currents can be calculated in both the buck and boost mode of CIBDC which is explained in previous section. These RMS current values are essential for calculating theoretical conduction loss of active switches. Thus, total conduction loss in buck/boost mode is

$$P_{\rm Cu-buck/boost} = \sum_{i=1}^{6} i^2_{\rm i_{RMS\_Buck/boost}} R_{\rm i_{DS-ON}} \tag{55}$$

Parasitic resistance value of coupled inductor windings and capacitor create extra ESR conduction loss in both the operating modes.

The ESR loss of the boost/buck mode is as follows:

$$\begin{aligned} P_{\rm ESR-boost/buck} = {} & i^2_{\rm i_{RMS\_pri}} R_{\rm ESR} + i^2_{\rm i_{RMS\_winding2}} R_{\rm ESR} \\ & + i^2_{\rm i_{RMS\_winding3}} R_{\rm ESR} \\ & + \sum_{i=1}^{4} i^2_{C_{\rm i\_RMS}} R_{\rm i_{ESR}}. \end{aligned} \tag{56}$$

Ferrite core is used for designing the coupled inductor and core losses are derived from the data sheet loss density curve with respect to flux density change for a given frequency.

Therefore, considering all losses of CIBDC, the efficiency (57) is derived for both operating modes

$$\eta = \frac{P_0}{P_0 + P_{\rm cu\_buck/boost} + P_{\rm core} + P_{\rm ESR\_buck/boost}}. \tag{57}$$

H. Small-Signal Analysis and Controller Design

Small-signal analysis of the proposed CIBDC is performed to derive the transfer function. There are five energy storing elements in form of a coupled inductor and four capacitors. The voltage across intermediate capacitors $\rm C_1$, $\rm C_2$, $\rm C_3$ are constant and depending on input or output voltages. Therefore, they are not considered [27] as state variable in the small-signal analysis. The state variables are coupled inductor current and output capacitor voltage. Hence, the resultant transfer function model is reduced to the second-order model. In boost mode, the state variables are coupled inductor current (i_L) and output capacitor voltage ($V_{\rm HV}$). Similarly, in buck mode, the state variables are coupled inductor current (i_L) and output capacitor voltage ($\rm V_{LV}$).

1) Boost Mode: In boost mode, $\rm S_1$ is the main switch. At switch ON time ($\rm S_1 = 1$) the circuit equations are as follows:

$$L_1 \frac{{\rm d}i_L(t)}{{\rm d}t} = V_{\rm LV} \tag{58}$$

$$C_{\rm HV} \frac{{\rm d}V_{\rm HV}({\rm t})}{{\rm d}t} = \frac{-V_{\rm HV}}{R_L}. \tag{59}$$

At the switch OFF time ($\rm S_1 = 0$), the circuit equations are as follows:

$$\begin{aligned} (n+1)\, L_1 \frac{{\rm d}i_L({\rm t})}{{\rm d}t} &= V_{\rm LV} + V_{\rm C2} + V_{\rm C3} - V_{\rm HV} \\ &= V_{\rm LV} \left[\frac{2 + 2n - D - nD}{1 - D} \right] - V_{\rm HV}(t) \end{aligned} \tag{60}$$

$$C_{\rm HV} \frac{{\rm d}V_{\rm HV}({\rm t})}{{\rm d}t} = \frac{-V_{\rm HV}({\rm t})}{R_L} + \frac{i_L(t)}{n}. \tag{61}$$

For "on" time the state-space matrix equations are as follows:

$$\frac{\rm d}{{\rm d}t}[X] = [A_1]\, X + [B_1]\, u \tag{62}$$

$$\frac{\rm d}{{\rm d}t} \begin{bmatrix} i_L \\ V_{\rm HV} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C_{\rm HV} R_L} \end{bmatrix} \begin{bmatrix} i_L \\ V_{\rm HV} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} V_{\rm LV}. \tag{63}$$

For "off" time the state-space matrix equations are as follows:

$$\frac{\rm d}{{\rm d}t}[X] = [A_2]\, X + [B_2]\, u \tag{64}$$

$$\begin{aligned} \frac{\rm d}{{\rm d}t} \begin{bmatrix} i_L \\ V_{\rm HV} \end{bmatrix} = {} & \begin{bmatrix} 0 & \frac{-1}{L_1(n+1)} \\ \frac{1}{nC_{\rm HV}} & \frac{-1}{C_{\rm HV} R_L} \end{bmatrix} \begin{bmatrix} i_L \\ V_{\rm HV} \end{bmatrix} \\ & + \begin{bmatrix} \frac{2}{\rm L_1(1-D)} - \frac{D}{L_1} \\ 0 \end{bmatrix} V_{\rm LV}. \end{aligned} \tag{65}$$

State-space averaging technique is applied and after linearizing the small-signal model is developed for boost mode

$$\frac{\rm d}{{\rm d}t} \left[\widetilde{x} \right] = [a]\, \widetilde{x} + [b]\, \widetilde{u} + [[A_1 - A_2]\, X + [B_1 - B_2]\, u]\, \widetilde{d} \tag{66}$$

$$\begin{aligned} \frac{\rm d}{{\rm d}t} \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_{\rm HV}} \end{bmatrix} = {} & \begin{bmatrix} 0 & \frac{-1+D}{L_1(n+1)} \\ \frac{1-D}{nC_{\rm HV}} & \frac{-1}{C_{\rm HV} R_L} \end{bmatrix} \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_{\rm HV}} \end{bmatrix} + \begin{bmatrix} \frac{2+{\rm D}^2}{L_1} \\ 0 \end{bmatrix} \widetilde{v_{\rm LV}} \\ & + \begin{bmatrix} \frac{V_{\rm HV}}{L_1(n+1)} - \frac{1+D^2}{\rm L_1(1-D)} V_{\rm LV} \\ \frac{-I_L}{nC_{\rm HV}} \end{bmatrix} \widetilde{d}. \end{aligned} \tag{67}$$

Small change in input voltage is zero, i.e., $V_{\mathrm{LV}} = 0$. Thus, from (67), the transfer function of output voltage to duty ratio is derived, i.e.

$$\frac{\tilde{v_{\mathrm{HV}}}(s)}{\tilde{d}(s)} = \frac{k(-\beta s+1)}{\mathrm{s}^2+2\xi\omega_n s+\omega_n^2} \tag{68}$$

where

$$k = \frac{V_{\mathrm{HV}}(1-D) - V_{\mathrm{LV}}(n+1)(1+D^2)}{n(n+1)C_{\mathrm{HV}}L_1},$$

$$\beta = \frac{L_1(n+1)I_L}{V_{\mathrm{HV}}(1-D) - [(n+1)(1+D^2)V_{\mathrm{LV}}]},$$

$$2\xi\omega_n = \frac{1}{R_L C_{\mathrm{HV}}} \text{ and } \omega_n = \frac{(1-D)^2}{n\mathrm{C}_{\mathrm{HV}}L_1(n+1)}.$$

2) Buck Mode: In boost mode, S_6 is the main switch. At the switch ON time ($\mathrm{S}_6 = 1$) the circuit equations are as follows:

$$L_1\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \frac{V_{\mathrm{HV}}}{2+2n} - V_{\mathrm{LV}}(t) \tag{69}$$

$$C_{\mathrm{LV}}\frac{\mathrm{d}V_{\mathrm{LV}}(t)}{\mathrm{d}t} = \frac{-V_{\mathrm{LV}}}{R_L} + i_L(t). \tag{70}$$

At the switch OFF time ($\mathrm{S}_1 = 0$), the circuit equations are as follows:

$$L_1\frac{\mathrm{d}i_L(t)}{\mathrm{d}t} = -V_{\mathrm{LV}}(t) \tag{71}$$

$$C_{\mathrm{LV}}\frac{\mathrm{d}V_{\mathrm{LV}}(t)}{\mathrm{d}t} = i_L(t) - \frac{V_{\mathrm{LV}}(t)}{R_L}. \tag{72}$$

For "ON" time, the state-space matrix equations are as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_L \\ V_{\mathrm{LV}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_{\mathrm{LV}}} & \frac{-1}{C_{\mathrm{LV}}R_L} \end{bmatrix}\begin{bmatrix} i_L \\ V_{\mathrm{LV}} \end{bmatrix} + \begin{bmatrix} \frac{1}{2+2n} \\ 0 \end{bmatrix} V_{\mathrm{HV}}. \tag{73}$$

For "OFF" time, the state-space matrix equations are as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_L \\ V_{\mathrm{LV}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_{\mathrm{LV}}} & \frac{-1}{C_{\mathrm{LV}}R_L} \end{bmatrix}\begin{bmatrix} i_L \\ V_{\mathrm{HV}} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{\mathrm{HV}}. \tag{74}$$

State-space averaging technique is applied and after linearizing the small-signal model is developed for boost mode

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \tilde{i_{\mathrm{L}}} \\ \tilde{v_{\mathrm{LV}}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_{\mathrm{LV}}} & \frac{-1}{C_{\mathrm{LV}}R_L} \end{bmatrix}\begin{bmatrix} \tilde{i_L} \\ \tilde{v_{\mathrm{LV}}} \end{bmatrix} + \begin{bmatrix} \frac{V_{\mathrm{HV}}}{(2n+2)} \\ 0 \end{bmatrix}\tilde{d}. \tag{75}$$

Thus, from (77), the transfer function of output voltage to duty ratio is derived, i.e.

$$\frac{\tilde{v_{\mathrm{LV}}}(s)}{\tilde{d}(s)} = \frac{k_1}{\mathrm{s}^2+2\xi\omega_n\mathrm{s}+\omega_n^2} \tag{76}$$

where $k_1 = \frac{V_{\mathrm{HV}}}{(2n+2)C_{\mathrm{LV}}L_1}$, $2\xi\omega_n = \frac{1}{R_L C_{\mathrm{LV}}}$ and $\omega_n = \frac{1}{C_{\mathrm{LV}}L_1}$.

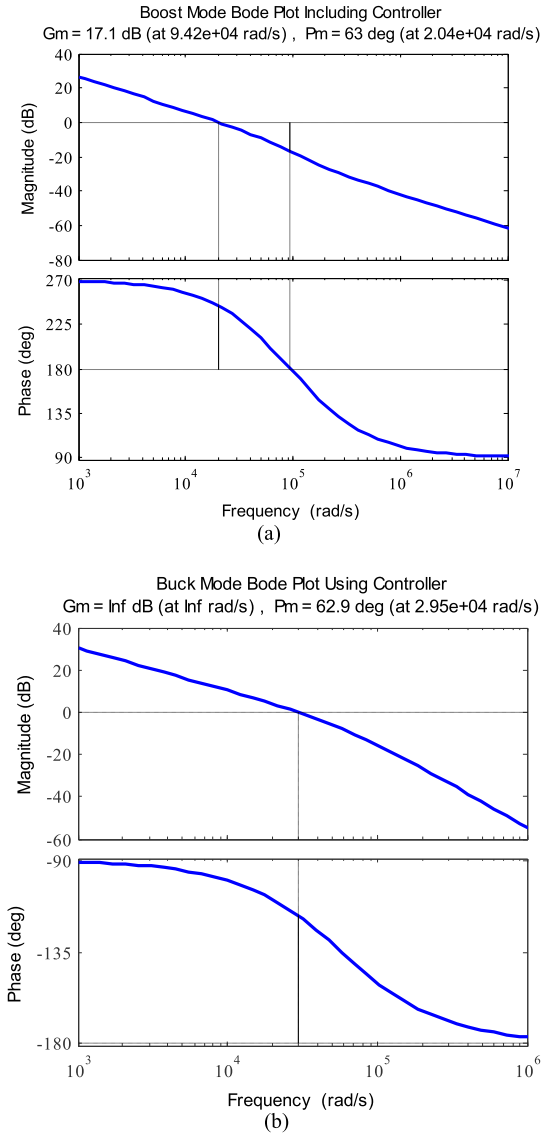


Fig. 11. Frequency response of the proposed CIBDC (a) boost mode and (b) buck mode.

3) Controller Design: The controller $C(s)$ is designed based on desired closed loop performance by specifying the closed loop natural undamped frequency (ω_{cl}) and damping ratio (ζ_{cl}). The controller is in the PID format [27] which can be represented by the following:

$$C(s) = \frac{s^2+2\xi\omega_n s+\omega_n^2}{k_2 s(\alpha_2 s+\alpha_1)} \tag{77}$$

where $\alpha_2 = \frac{1}{\omega_{\mathrm{cl}}^2}$ and $\alpha_1 = \frac{2\xi}{\omega_{\mathrm{cl}}}$.

Using the controller, the bode diagram of the closed-loop system for both modes are shown in Fig. 11 which shows a good phase margin of 63° and 62.9° for boost and buck mode, respectively.

Mode transfer of the proposed CIBDC from buck to boost mode or vice versa can be done easily using the switching function of main switches, i.e., $S_1 = \mathrm{M}v$ and $S_6 = \bar{\mathrm{M}}\,v$,

TABLE III
SIMULATION AND HARDWARE PARAMETERS

CIBDC Specification		
Input Voltage = 48 V	Power Output = 250 W	Output Voltage = 384 V
	Switching Frequency=50 kHz	
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 45 µH, Turns Ratio 25:25 (n = 1), $L_{leakage}$ = 7.15 µH	Ferrite Core PQ 32/30
Switch (S_1, S_2, S_3, S_4)	FQP34N20 (V_{ds} = 200 V, R_{ds} = 0.075 Ω, I_d=31 A.) @ 250W	FQP34N20
Switch (S_6)	FQP17N40 (V_{ds} = 400 V, R_{ds} = 0.27 Ω, I_d=16 A.) @ 250W	FQP17N40
Capacitor C_1, C_2, C_3	Simulated:12 µF hardware: 10µF	
Capacitor C_4	Simulated:15 µF hardware: 10µF	
Capacitor C_{LV}	100 µF	
Capacitor C_{HV}	470 µF	

where v is the switching function and M is for mode selection

$$v = \begin{cases} 1 & 0 < t < DT_s \\ 0 & DT_s < t < T_s \end{cases}, \quad \mathrm{M} = \begin{cases} 1 & \text{Boost} \\ 0 & \text{Buck} \end{cases}. \tag{78}$$

Voltage mode control is implemented in NI-cRIO 9082 using Lab-VIEW programming. NI-9225 is the voltage sensor module is used to sense the output voltage of the converter directly. After the control operation, the digital pulsewidth modulation (PWM) pulses for S_1 to S_6 is generated through NI-9401 digital input/output module. The total control function is developed in scan interface of NI-cRIO9082. The PWM pulses are sent to optocoupler stage (6N137) for isolation from control to the power stage. IR2110 driver is used to drive the six MOSFET switches. The total hardware set-up and controller for testing the proposed CIBDC are shown in Fig. 12(b) and (c), respectively.

V. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed CIBDC circuit in buck and boost mode is tested on a 250 W prototype converter as shown in Fig. 12(a). The low voltage input is 48 V, where 384 V is the output voltage designed at 50 kHz switching frequency. The optimum duty ratio of 0.5 is selected for testing prototype CIBDC. Unity turns ratio ($n = 1$) is selected for coupled inductor which is derived from (49).

The designed parameter for the proposed BDC is mentioned in Table III.

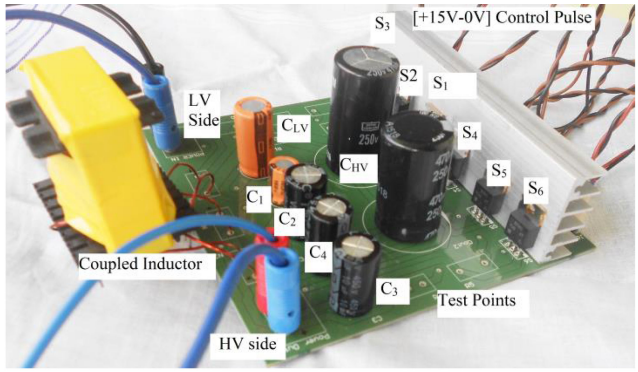
The performance of the proposed BDC is tested and demonstrated which shows a good match with theoretical results.

The recorded waveforms of boost mode of operation are mentioned in Fig. 13. ZVS turn ON is achieved in all the active MOSFET switches as shown in Fig. 13(a)–(f). In S_4, S_6 switches ZVS turn ON and turn OFF is achieved, where in S_2 ZVS turn ON and ZCS turn OFF is recorded as shown in Fig. 13(e), (f), and (d), respectively.

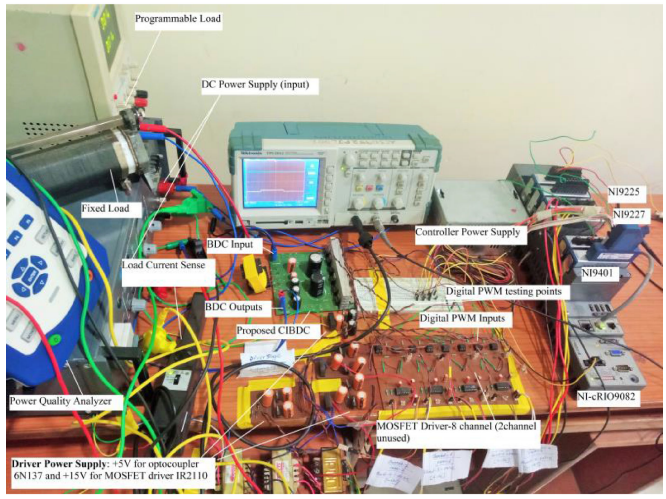
Similarly, the performance of the buck mode is reported in Fig. 14. All switches are inherently soft switched like in the boost mode.

Dynamic performance of CIBDC is tested during step load change both in the duck mode and boost mode as shown in Fig. 15(a) and (b), which shows stable converter operation.

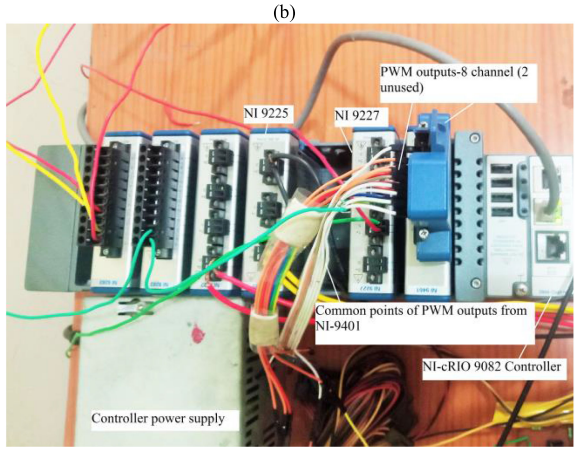
The theoretical and experimental efficiency of the proposed BDC in both buck and boost mode is shown in Fig. 16. The



(a)



(b)



(c)

Fig. 12. Proposed Prototype of CIBDC @ 250 W. (a) Power circuit of CIBDC. (b) Controller circuit including the driver stage. (c) NI-cRIO 9082 controller with NI9225 (voltage sense module) and NI9401 (digital PWM module).

difference of the theoretical and measured efficiency is due to the fact that RMS and average current for switches, capacitors, and inductor coil is calculated using ideal waveforms. However, the efficiency pattern is the same throughout the entire operating range. The maximum measured efficiencies for buck and boost mode of operation are 96.12% and 96.63%, respectively. The loss distribution of CIBDC at 250 W is shown in Fig. 17(a) and (b). The proposed converter is designed with taking less coupled

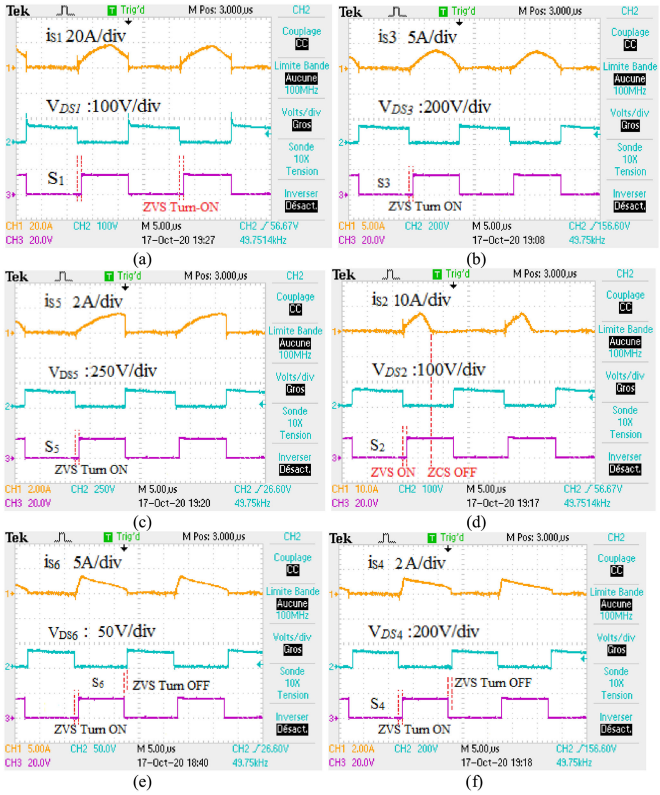


Fig. 13. Experimental results in boost mode.

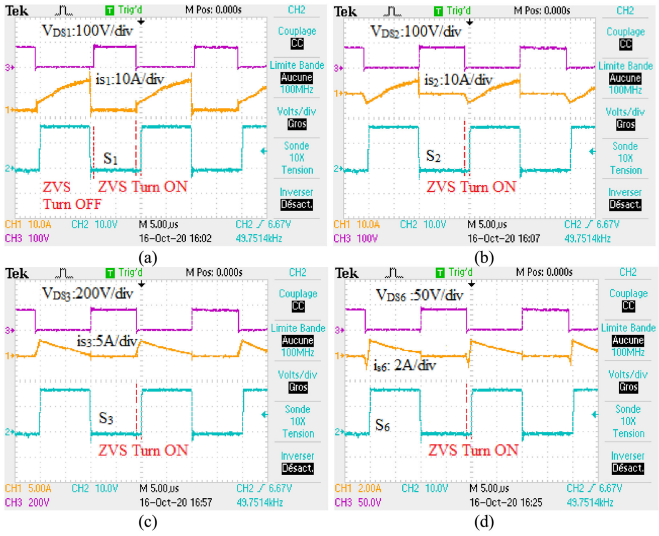


Fig. 14. Experimental results in buck mode.

inductor winding turns ($n = 1$) taking topological advantage to meet same voltage gain, whereas in existing literatures the number of turns [25], [27] is generally greater than four ($n \geq 4$). The proposed CIBDC has lesser switch current stress by 15%–20% and RMS values compared to the topologies like in [16], [25], and [27].

The voltage stress performance of the proposed converter is almost similar to existing topologies. The boosting voltage gain

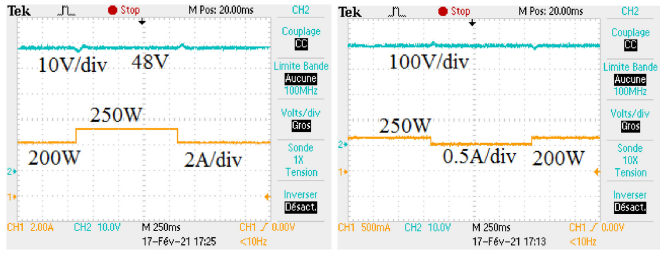


Fig. 15. Voltage response for a load change from (a) 200–250–200 W in buck mode, (b) 250–200–250 W in boost mode.

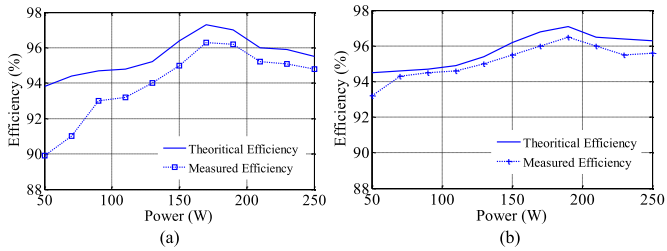


Fig. 16. Efficiency of the proposed CIBDC in (a) buck mode and (b) boost mode.

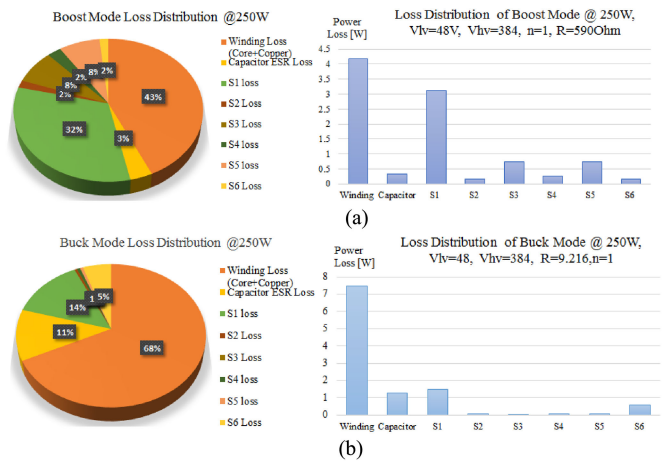


Fig. 17. Loss distribution of CIBDC @250 W. (a) Boost mode. (b) Buck mode.

factor of CIBDC for 0.4 duty ratio at $n = 1$ is 6.66, whereas in [16] and [25] the same factor is 3.33 and in [23], [24], [27], the value is 5. At the same condition the conversion factor is 3.21 in [31].

VI. Conclusion

In this article, a novel coupled inductor based bidirectional dc–dc converter is proposed which is capable of delivering high voltage conversion ratio in both buck and boost mode of operation. In this CIBDC topology, higher conversion factor, i.e., $\geq$10 in boost and $\leq$1/10 in buck mode are obtained with unity turns ratio ($n = 1$). Current and voltage stress is less in main MOSFET switches in both the operating modes which enables to select low voltage, low ON state resistance MOSFET.

This helps to reduce the conduction loss. Again, all the active switches are soft switched, i.e., ZVS. Therefore, switching loss is negligible which further improves the conversion efficiency. The proposed converter utilized two parallel inductor current paths to share input currents during boost as well as in buck mode which reduces the current rating of individual coils and helps in reducing the input current ripple. Due to topological advantage the leakage inductance energy is directly transferred to load. The detailed analysis of topological derivation, current, and voltage stress along with the efficiency calculation in steady state is discussed in details. The maximum measured efficiency is 96.12% in buck mode at 170 W and 96.63% in boost mode at 190 W.

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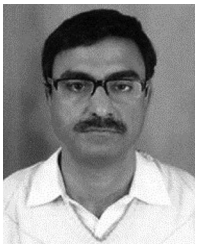

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