Asymmetrical-PWM DAB Converter With Extended ZVS/ZCS Range and Reduced Circulating Current for ESS Applications

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***Abstract*—The dual-active bridge (DAB) topology is commonly preferred in bidirectional applications due to several attractive features, including auto-adjust of power flow, galvanic insulation, wide voltage gain, and zero voltage switching (ZVS) capability over some power ranges. However, the efficiency of the converter drops at light loads because the ZVS range is directly dependent on the circulating current. Assuming that the processed power is variable, the DAB converter's design must find a compromise between extending ZVS ranges and reducing the reactive power processing to ensure higher efficiency. Aiming this compromise, many papers propose hybrid approaches in which the modulation strategy is selected according to the processed power. However, this is not a simple solution because it demands multivariable control and offline optimizations. This paper proposes a modulation strategy to ensure ZVS and reduce the circulating current for the DAB converters. While the usual phase-shift modulation provides ZVS operation in a range of 40% to 100% of rated power, the proposed asymmetrical pulse-width modulation can obtain ZVS operation in a range of 2% to 100% of rated power. Experimental results demonstrated that the proposed strategy improves the converter efficiency for all power ranges, especially at light loads.**

***Index Terms*—Battery chargers, dc–dc power conversion, energy storage, power electronics.**

I. Introduction

THE dual-active bridge (DAB) converter has received significant attention in recent years in industrial applications and renewable power generation due to some advantages, such as bidirectional power processing, wide voltage ratio, and high power capability [1]–[3]. It also has many other benefits, such as galvanic insulation, zero voltage switching (ZVS), and autoadjustment of power flow [1].

The DAB converter is a possible choice to interconnect energy storage systems (ESS) with renewable energy generation units such as solar and wind to reduce their power intermittency [4], [5]. One common requirement for ESS applications is that the converter must operate over a wide voltage range to manage deeply discharged batteries or use technologies with low voltage (LV) and high power capacity, such as fuel cells and supercapacitors [4]–[8]. The DAB converter's typical industrial applications are solid-state transformers, uninterrupted power supplies, and on-board battery chargers for electric vehicles [9]–[12].

The DAB converter operates under wide voltage ratios and wide power ranges in the applications above due to the variable characteristic of the loads and batteries state-of-charge (SoC), supercapacitors, or fuel cells [12], [13]. At the same time, the DAB is commonly controlled with phase-shift modulation (PSM), operating in ZVS for limited voltage and power ranges with the drawback of having a high circulating current at light loads [14], [15].

A possible solution to extended the ZVS-ON range is to increase the leakage inductance of the high frequency (HF) transformer or add a series auxiliary inductor since the DAB-PSM employs this as the power transfer element [14]. With a larger series inductances, the circulating current also increases. Consequently, conduction and magnetic losses reduce the converter efficiency. Therefore, the DAB converter's design requires a compromise between keeping the ZVS-ON range and limiting the circulating current, especially for designs with wide voltage conversion ratios [16]–[18].

Soft-switching methods are applied to some topologies, including resonant cells [12], [19] current-fed configurations [20], and active-clamp circuits [4]–[8], [22] to reduce switching losses. These are hardware solutions that increase the converter complexity due to the extra components, including auxiliary inductors, clamping capacitors, semiconductors, and driver circuits [20].

To avoid these problems, recently, some advances of DAB converters modulation strategies were reported, including the extended PSM (EPSM) [20], dual phase-shift (DPSM) [20]–[24],

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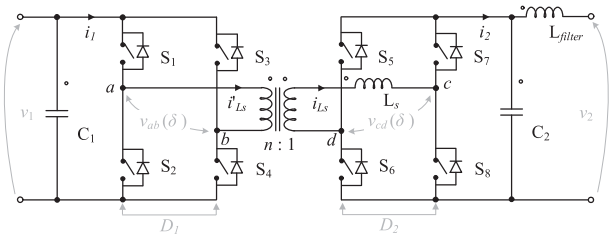


Fig. 1. Power circuit of DAB converter.

triple phase-shift (TPSM) [9], [11], [25]–[26] that is subdivided into triangular (TRM) and trapezoidal (TZM) [9], [11], and frequency modulations [19]. The usual PSM controls only the phase angle δ, which is related to the phase between the transformer voltages (v_{ab},v_{cd}), as shown in Fig. 1. Other modulations use the duty cycles D_1 and D_2 of each active-bridge in addition to δ to control the converter [14]. For instance, DPSM uses δ and D_1, and TPSM uses δ, D_1, and D_2.

Previous papers [8], [20], and [25]–[30] have shown that it is possible to improve the efficiency of the DAB converters using an appropriate modulation strategy. In [20], e.g., an enhanced DPSM hybrid modulation ensures the ZVS-ON from 6% to 100% of the converter rated power and almost flat efficiency around 96%. In this modulation, the DPSM allows ZVS-ON with light loads, and an EPSM reduces the rms current at heavy loads. The main drawback of this modulation strategy is its complexity due to the multivariable control.

The TPSM operates with three degrees of freedom (δ, D_1, and D_2). These parameters depend on the voltage conversion ratio, power processing, and soft-switching requirements [26]. Therefore, there is no unified implementation procedure in the current literature, and many TPSM schemes have been proposed with different optimization objectives [5], [27]. Some papers mention that offline optimization is necessary to select the correct combination of these possible parameters and modulation strategies [27], [31]. Consequently, the control system is no easy to implement.

To avoid these drawbacks, this paper proposes an asymmetrical pulse-width modulation (a-PWM) where the converter control depends only on the high-voltage side duty cycle (D_1) while the LV active-bridge operates with a fixed duty cycle. The main contribution is to achieve ZVS and zero current switching (ZCS) operation for a wide power range using only a single variable to control the converter. The a-PWM also avoids circulating current because the antiparallel diodes are used to block possible reverse currents. It results in asymmetrical losses. However, the transformer current's discontinuous conduction mode allows ZCS for all semiconductors. Experimental results demonstrate that it is possible to ensure the ZCS and ZVS-ON operation from 2% to 100% of the nominal power and an efficiency of up to 96.30%.

II. Circulating Current and ZVS-ON

As shown in Fig. 1, the DAB comprises two full-bridge converters operating at HF as an inverter or controlled rectifier. In this figure, L_s represents the equivalent inductance formed

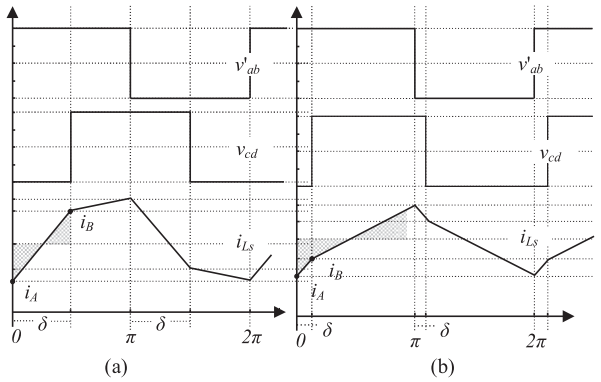


Fig. 2. Circulating current and ZVS conditions on conventional PSM-DAB. (a) ZVS-ON with high power processing. (b) ZVS lost with low power processing.

by the leakage inductance and a possible series inductance used to increase the inductance of the converter. The HF transformer provides galvanic insulation and wide voltage gain. Additionally, L_s acts as a power transfer element. The voltages v_{ab} and v_{cd} are applied over L_s, and the power flow depends on the phase angle (δ) between v_{ab} and v_{cd}. In the traditional PSM, the duty cycle of v_{ab} and v_{cd} has a constant value of 50%.

Fig. 2(a) and (b) shows the ZVS-ON conditions and circulating current of the DAB converter operating with PSM for light and heavy loads. In this figure, v'_{ab} is the voltage v_{ab} referred to the LV side. The circulating current is the rms value of the hatched areas related to converter inductance L_s. According to [14], the circulating current in DAB converters is similar to the reactive power in ac systems because it does not transfer any active energy and increases the conduction and magnetic losses. At higher power loads, the circulating current may be a tiny percentage of the nominal current [see Fig. 2(a)]. However, when the power levels decrease, the circulating current assumes a significant part of the processed power [see Fig. 2(b)]. As a consequence, this reduces the global efficiency of the converter.

On the other hand, the ZVS-ON condition depends on the circulating current. The power switches achieve ZVS only if the transformer current flows through their intrinsic diodes at the switches turn-ON. This condition occurs when the following relations are accomplished [14]: $i_A < 0$; and $i_B > 0$. Hence, a minimum circulating current level is required to ensure this situation. In a practical situation, to enable the ZVS-ON, the design of the DAB converter must also consider the semiconductors' output capacitances and an appropriated dead-band period. A large enough series inductance is necessary to discharge the output capacitances of the semiconductors during the turn-ON. The ZVS-ON range can be evaluated by

$$\frac{1}{2}\cdot \mathrm{L}'_s \cdot (i_{\mathrm{zvs}})^2 \geq \frac{1}{2}\cdot C_o \cdot (v_1)^2 \tag{1}$$

where C_o is the total output capacitance, L'_s is the equivalent inductance L_s reflected to the HV side, and i_{zvs} is the current at turn-ON instant [31].

Since C_o and the output voltage v_1 cannot be easily changed, it is possible to note that there are not many degrees of freedom to extend the ZVS range. However, a high L_s inductance value can

inappropriately increase the circulating current, impacting the converter efficiency. On the other hand, reducing the inductance can lead to loss of the ZVS-ON operation, increasing switching losses. As a result, the determination of L_s is critical to allow the ZVS while maintaining the circulating current limited. Moreover, some conduction losses remain since traditional PSM does not ensure ZVS under a null circulating current.

Based on the aforementioned limitations, the following section describes the proposed a-PWM and the design of L_s to achieve ZVS and ZCS at the same time the circulating current is reduced. This method extends the soft-switching range and mitigates conduction losses caused by circulating current.

III. Proposed Modulation and Design Guidelines

Considering the DAB converter shown in Fig. 1, the v_1 voltage and the active H-bridge (S_1–S_4) are related to the high voltage (HV) side. At the LV side, the H-bridge (S_5–S_8) is associated with a second-order filter (C_2–L_{filter}) [33]. L_{filter} is used to limit the current ripple of the batteries. For ESS applications, the current ripple is defined according to specifications of standards and manufacturers [33], [34]. L_{filter} is not necessarily related to converter operation. However, it is used due to the ESS application.

When the power flows from the HV to the LV side, the DAB is in step-down mode, and the LV bridge acts as a passive rectifier. On the other hand, when the power flows from the LV to the HV side, the DAB is in step-up mode, and the LV bridge operates as an inverter. The operation modes can be detailed in eight stages. The following analysis shows both operation modes separately due to their different voltage gain. However, only one modulation is used for both operation modes. Fig. 3 depicts the main stages of the step-down mode. Fig. 4 shows the associated theoretical waveforms for both operation modes, and Fig. 5 shows the power stages of the step-up mode.

A. Step-Down Mode

In this operation mode, the LV bridge operates only as a passive rectifier to avoid circulating current. In the positive half-cycle, this operation mode has four stages, as presented in Fig. 3. The negative half-cycle also has four similar stages. Concerning the theoretical waveforms, Fig. 4(a) shows the main waveforms of the step-down mode. The transformer current has a TRM waveform, with a zero current level in the last stages (t_3-$T/2$). The gate signals (v_{g1}-v_{g8}) and the blocking voltages (v_{S1}-v_{S8}) are shown for each semiconductor. The currents of the switches are also presented to verify the switching conditions.

1) *Stage 1 [see Fig. 3(a)], t_0–t_1:* The first stage begins when S_1 and S_4 are turned ON. A positive power flow is established to v_2 through the diodes of S_6 and S_7. In this stage, the inductance L_s and the output filter (C_2) store the power transferred from v_1. Initially, $i_{Ls} = 0$. The voltage over the inductance L_s is $v_{Ls} = v_1/n - v_2$. Due to v_{Ls}, i_{Ls} increases from zero to the transformer current peak, as shown in Fig. 4(a).
2) *Stage 2 [see Fig. 3(b)], t_1–t_2:* This stage is related to the dead-band period. When S_1 is turned OFF (t_1), S_1 is turned OFF, and their output capacitor is charged from zero to v_1. Output capacitance of S_2 is discharged to zero so that the current flows through the S_2 antiparallel diode. In this stage, ZVS-ON occurs at S_2 because the v_{S2} blocking voltage is zero when S_2 is turned ON.
3) *Stage 3 [see Fig. 3(c)], t_2–t_3:* this stage begins when S_2 is turned ON. The energy stored in L_s and C_2 is transferred to the output load because $v_{Ls} = -v_2$. As shown in Fig. 4(a), this stage ends when the transformer current decreases to zero.

   At the end of this stage, a resonance occurs between the semiconductors' output capacitances (S_5–S_8) and the series inductance (L_s).
4) *Stage 4 [see Fig. 3(d)], t_3–$T_s/2$:* With L_s demagnetized, only C_2 supplies the output load because the transformer voltage is zero. This stage begins when the transformer current is zero and ends when S_3 is turned ON in the first stage of the negative half-cycle.

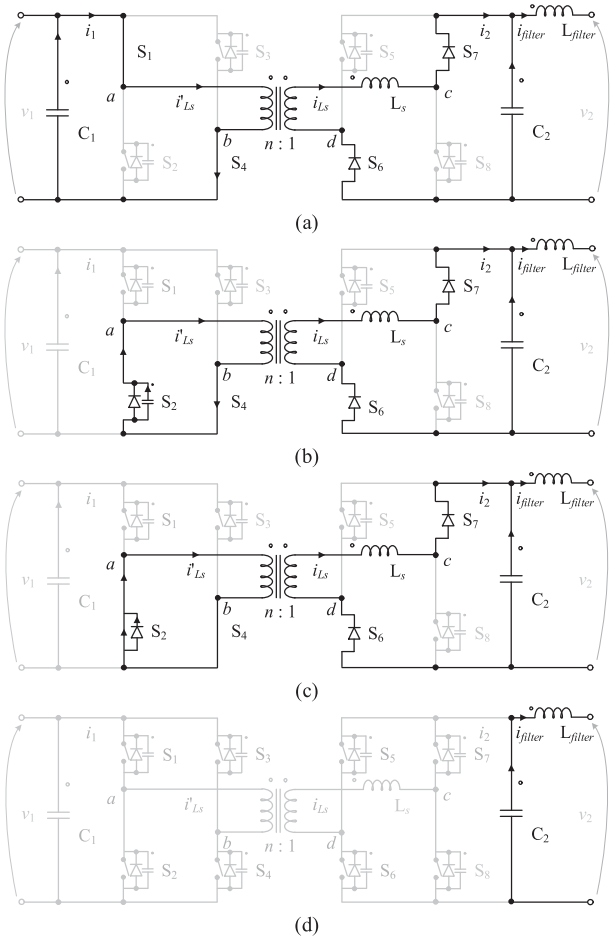


Fig. 3. Power stages of asymmetrical PWM DAB converter on step-down mode: (a) stage 1; (b) stage 2; (c) stage 3; (d) stage 4.

The voltage ratio for this operation mode is given as follows, where the conduction of S_1 and S_3 defines the duty cycle D:

$$\frac{v_2}{v_1} = \frac{1}{n}\frac{-\frac{v_2}{i_2} + \sqrt{\left(\frac{v_2}{i_2}\right)^2 + \frac{8 \cdot Ls \cdot v_2}{D^2 \cdot T \cdot i_2}}}{\frac{4 \cdot Ls}{D^2 \cdot T}}. \tag{2}$$

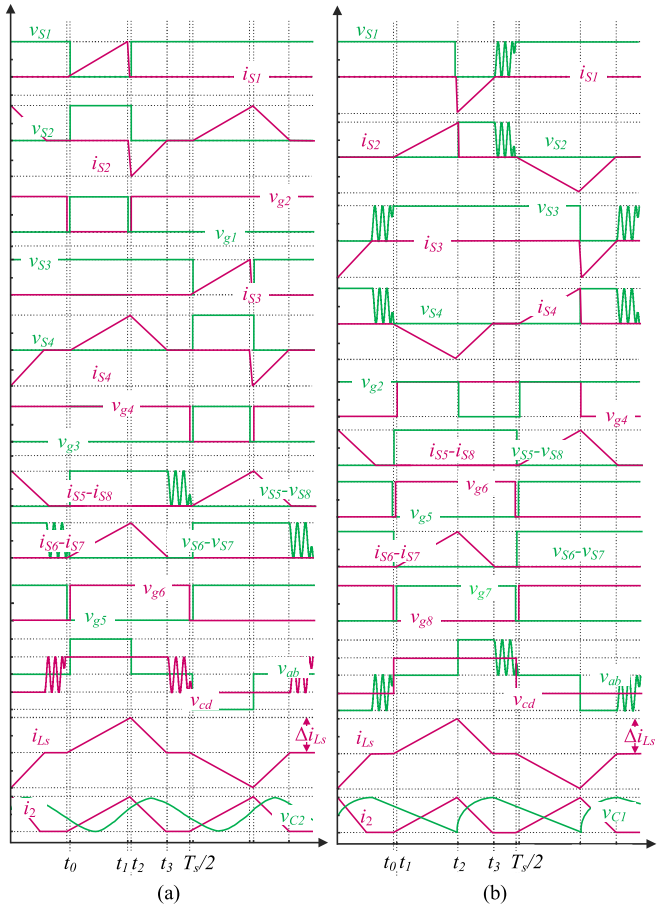


Fig. 4. Theoretical waveforms of asymmetrical PWM-DAB. (a) Step-down mode. (b) Step-up mode; $^{*}v_{gx}$: gate signals.

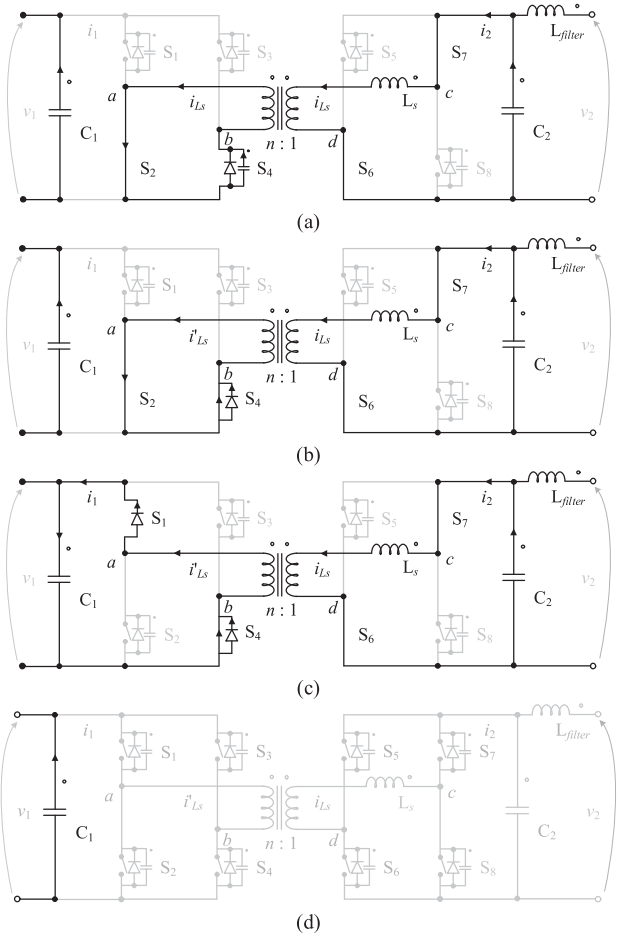


Fig. 5. Power stages of asymmetrical PWM DAB converter on step-up mode. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4.

B. Step-Up Mode

The step-up mode operates to increase the voltage (v_2) using the series inductances to store the energy from the LV side. For this operation mode, the LV bridge acts as an inverter to allow the reverse power flow.

The positive half-cycle of power flow has four power stages, as shown in Fig. 5. Fig. 4(b) shows the theoretical waveforms of the step-up mode. Again, the transformer current i_{Ls} has a TRM waveform. The gate signals (v_{g1}–v_{g8}) and the blocking voltages (v_{S1}–v_{S8}) are also showed to evaluate the modulation strategy.

1) *Stage 1 [see Fig. 5(a)], t_0–t_1:* This stage begins when S_6 and S_7 are turned on to establish a positive power flow through the transformer. Initially, the transformer current is zero. To increase i_{Ls}, S_2 is also turned ON so that $v_{Ls} = v_2$. The i'_{Ls} current flows through the output capacitor of S_4, which is discharged. When the capacitor of S_4 is completely discharged, their intrinsic diode is directly polarized to allow ZVS-ON.
2) *Stage 2 [see Fig. 5(b)], t_1–t_2:* This stage begins when the S_4 diode is directly polarized at t_1. Since their blocking voltage is zero, S_4 is turned ON under ZVS. The current i_{Ls} increases from zero to the peak of the transformer current. This stage ends when S_2 is turned OFF, as shown in Fig. 4(b).
3) *Stage 3 [see Fig. 5(c)], t_3–t_4:* When S_2 is turned OFF, the energy stored in L_s flows to the output capacitor (C_1) through the diode of S_1. According to the theoretical waveforms, the transformer current decreases from the peak value to zero because $v_{Ls} = v_2 - v_1/n$.
4) *Stage 4 [see Fig. 5(d)], t_4–$T_s/2$:* This stage begins when $i_{Ls} = 0$. The diode of S_1 is used to blocking a reverse current, and only the capacitor C_1 supplies the converter's output load.

In this stage, a resonance occurs between the output capacitances of HV side switches and the transformer inductance due to the discontinuous current i_{Ls}.

The voltage ratio for this operation mode is given by (3), where the conduction of S_2 and S_4 defines the duty cycle (D)

$$\frac{v_1}{v_2} = \frac{2 + \sqrt{n^2 + \frac{4 \cdot D^2 \cdot T \cdot i_1}{v_1 \cdot 2 \cdot Ls}}}{2}. \tag{3}$$

C. Effect of Devices Output Capacitances

The previous steady-state analysis explained the fundamental stages related to the modulation strategy. However, a resonance occurs between the output capacitors (C_{oss_Sx}) of S_1–S_8 and the

TABLE I
ZVS AND ZCS CONDITIONS OF ASYMMETRICAL PWM

Operation mode		S_1	S_2	S_3	S_4	S_5- S_8
Step-down	Turn-on	ZCS	ZVS	ZCS	ZVS	ZCS
	Turn-off	-	ZCS	-	ZCS	ZCS
Step-up	Turn-on	-	ZVS	-	ZVS	ZCS
	Turn-off	ZCS	-	ZCS	-	ZCS

transformer series inductance (L_s). This resonance is not related to the modulation and does not change the converter performance considerably. It only slightly modifies the operating waveforms during a few intervals (t_3–$T/2$), as shown in Fig. 4.

For both the step-down and step-up modes, the transformer current (i_{Ls}) reduces to zero in the fourth stage. The equivalent circuit is presented in Figs. 3(d) and 5(d), respectively.

For the LV-bridge (S_5–S_8), the total output capacitance is

$$\mathrm{C_{total}\text{-}HV} = \mathrm{C_{oss\_S1}}//\mathrm{C_{oss\_S4}} + \mathrm{C_{oss\_S2}}//\mathrm{C_{oss\_S3}}. \quad (4)$$

The series inductance (L_s) resonates with the output capacitances. The resonant frequency (ω_r) is given by

$$\omega_r = \frac{1}{\sqrt{\mathrm{L}s \cdot \mathrm{C_{total}}}}. \quad (5)$$

In these stages, the voltage across the switches capacitances are

$$\mathrm{v_{Sx}} = \frac{\mathrm{v_2}}{2} + \frac{\mathrm{v_2}}{2} \cdot \cos[\omega_\mathrm{r}(\mathrm{t} - \mathrm{T}/2)]. \quad (6)$$

Similar oscillations at identical resonant frequencies are obtained for the negative half-cycles. Analogous relations can also be obtained at the HV side for switches S_1-S_4.

D. Soft-Switching Conditions and Conduction Losses

The theoretical waveforms depicted in Fig. 4 shows that the high-voltage semiconductors present different switching conditions. For S_2 and S_4, it is easy to ensure the ZVS-ON because they are turned ON at the peak of i_{Ls}. It is necessary to ensure an adequate dead-band to discharge the output capacitances (C_o) of S_1 and S_3. Additionally, according to (1), the series inductance L_s must store sufficient energy to discharge/charge C_o. Considering the resonance frequency between L_s and C_o, the dead-band t_{db} is

$$t_{db} = \frac{1}{4} \cdot \frac{2\pi}{\omega_r} = \frac{1}{4 \cdot f_r}. \quad (7)$$

For the LV side, the zero current stage ensures the ZCS for both operation modes. It avoids losses due to the turn-off and reverse recovery current. Also, the ZCS condition is ensured to S_1 and S_3. Table I gives the switching conditions.

According to the power stages analysis, Table II gives the rms current of each power element. It allows evaluating the conduction losses after the converter design.

Tables I and II give that the converter has asymmetrical losses, but soft-switching conditions are ensured for a wide operating range. In the proposed modulation, the diode conduction is necessary to control the circulating current. It can impact the converter losses. However, it is not a concern, provided that the diode losses be less than a reactive power that could appear with no circulating current control.

E. Converter Design

The converter design has a compromise to ensure soft-switching conditions and reduce conduction losses. For this, L_s must be large enough to reduce rms current. At the same time, the discontinuous conduction mode must be kept.

The design of L_s considers the first stage of the step-down mode. Since both operation modes have similar power stages, the same results are obtained considering the step-down mode.

Initially, consider Δi_{Ls} the maximum variation of i_{Ls} in a half-cycle

$$\Delta i_{\mathrm{L}s} = \left(\frac{v_1/n - v_2}{\mathrm{L}s}\right) \cdot \frac{T_s}{2} \cdot D. \quad (8)$$

Observe that $v_{Ls} = v_1/n\text{-}v_2$, during a period ($\Delta t$) related to $D \cdot T_s/2$. On the critical conduction mode, the voltage conversion ratio (2) can be simplified as

$$\frac{v_2}{v_1} = \frac{D}{n}. \quad (9)$$

Considering v_1 as a constant value, (8) can be rewritten as (10), where f_s is the switching frequency

$$\Delta i_{Ls} = \frac{v_1/n \cdot \left(D - D^2\right)}{2 \cdot f_s \cdot \mathrm{L}s} = \frac{v_1/n \cdot \left(D - D^2\right)}{2 \cdot f_s \cdot \mathrm{L}s}. \quad (10)$$

Considering that $\Delta i_{Ls} = 2 \cdot i_2$ and (10), to keep the discontinuous conduction mode, the following relation must be satisfied

$$\mathrm{L}s \leq \frac{v_1/n \cdot \left(D - D^2\right)}{(2 \cdot f_s) \cdot (2 \cdot i_2)}. \quad (11)$$

Observe that smaller L_s will increase the *rms* converter current, which will impact the conduction losses. Therefore, L_s must be the highest possible value that satisfies (11). Also, it is necessary to note that L_s is the total converter inductance since an external series inductance can be added to increase the transformer leakage inductance.

To design the high-frequency filters (C_1-C_2-L_{filter}), Fig. 6 shows the voltage and current ripple waveforms. Fig. 6(a) presented the voltage (Δv_{C2}) and current (Δi_{filter}) waveforms for the battery charge (step-down mode), while Fig. 6(b) shows the dc bus voltage ripple (Δv_{C1}).

The capacitor C_2 is used to limit the voltage ripple on the battery side. The current i_{C2} has a similar waveform to i_2, however, with a zero average value. The capacitor charge variation ΔQ can be evaluated in the interval t_0-t_2, when the capacitor current is positive, as shown in Fig. 6(a). The value of ΔQ is equal to the area under the i_{C2} waveform during t_0-t_2. The area is evaluated through

$$\Delta Q = (t_2 - t_0)\,\frac{h}{2} \quad (12)$$

where h is the triangle height, given by

$$h = \Delta i_{Ls} - i_{filter_{(avg)}}. \quad (13)$$

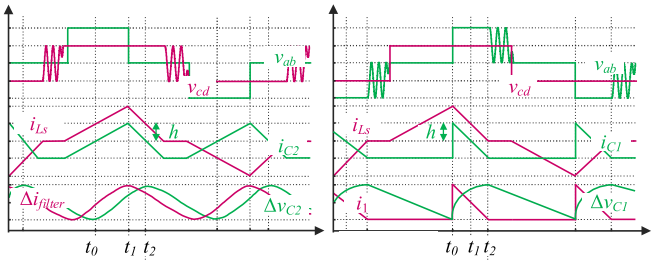


Fig. 6. Theoretical waveforms for the current and voltage ripples. (a) Step-down mode. (b) Step-up mode.

Also

$$t_1 - t_0 = \mathrm{L}s \cdot n \cdot \frac{\Delta i_{Ls} - i_{filter(avg)}}{v_1 - v_2 \cdot n} \tag{14}$$

$$t_2 - t_1 = \mathrm{L}s \cdot \frac{\Delta i_{Ls} - i_{filter(avg)}}{v_2}. \tag{15}$$

Therefore

$$\Delta Q = \left(\frac{n}{v_1 - v_2 \cdot n} + \frac{1}{v_2}\right) \cdot \frac{\mathrm{L}s \cdot \left(\Delta i_{Ls} - i_{filter(avg)}\right)^2}{2}. \tag{16}$$

Considering that $C = \Delta Q / \Delta v_C$, C_2 is given by

$$C_2 = \left(\frac{n}{v_1 - v_2 \cdot n} + \frac{1}{v_2}\right) \cdot \frac{\mathrm{L}s \cdot \left(\Delta i_{Ls} - i_{filter(avg)}\right)^2}{2 \cdot \Delta v_{C2}} \tag{17}$$

where Δv_{C2} is defined according to the design specifications.

The design of L_{filter} considers that $v_{L\mathrm{filter}}$ is approximated by a sine function given by

$$v_{Lfilter}(t) \approx \frac{\Delta v_{C2}}{2} \cdot \sin(2\pi f t). \tag{18}$$

Considering the equation of the inductor current, $i_L(t)$ is given by

$$i_L(t) = \int \frac{v_L(t)}{L} dt + i_{L(avg)} \tag{19}$$

and from (18), the current i_{filter} is

$$i_{filter}(t) = \frac{\Delta v_{C2}}{2} \cdot \frac{\cos(2\pi f t)}{2\pi f \cdot L_{filter}} + i_{filter(avg)}. \tag{20}$$

From (20), the maximum and minimum values of i_{filter} are

$$i_{filter-Max} = \frac{\Delta v_{C2}}{4\pi f \cdot L_{filter}} + i_{filter(avg)} \tag{21}$$

$$i_{filter-Min} = -\frac{\Delta v_{C2}}{4\pi f \cdot L_{filter}} + i_{filter(avg)} \tag{22}$$

From (21) and (22), the current ripple Δi_{filter} is obtained as

$$\Delta i_{filter} = \frac{\Delta v_{C2}}{2\pi f \cdot L_{filter}}. \tag{23}$$

The value of L_{filter} is defined as a function of Δi_{filter} rewriting (23) as

$$\mathrm{L}_{filter} = \frac{\Delta v_{C2}}{2\pi f \cdot \Delta i_{filter}}. \tag{24}$$

The capacitor C_1 is necessary to reduce the high-frequency ripple of the dc bus voltage. From the voltage waveform of v_{C1} in Fig. 6(b), t_0–t_1 defines ΔQ to design C_1. The result is given by (25), which is similar to the design methodology of C_2

$$C_1 = \left(\frac{n}{v_1 - v_2 \cdot n}\right) \cdot \frac{Ls \cdot \left(\Delta i_{Ls} - i_{1(\mathrm{avg})} \cdot n\right)^2}{2 \cdot n \cdot \Delta v_{C1}}. \tag{25}$$

IV. Comparison of Conventional Modulations and the Proposed Asymmetrical PWM

Table III gives a comparison of four different DAB converters in terms of the number of components, soft-switching requirements, control methods, and efficiency.

Individually, [20] offers good advantages since it is based on an improved DPSM and a CF-DAB to allow a higher voltage ratio and ZVS range. This topology includes two clamping diodes and two auxiliary inductors. Also, it employs a more complex control with two different modulations, selected according to the power level.

To the PSM, the main advantages are related to heavy loads. It occurs because it is easier to ensure the ZVS conditions for the highest power levels without a significant circulating current, especially when the voltage conversion ratio is unity. For low power levels, the circulating current assumes a high percentage of the processed power. Consequently, the converter efficiency is compromised at light loads [15], [23], [32].

In the DSPM, it is possible to ensure the ZVS conditions for an extended operating range. On the other hand, this approach increases the converter rms current for the highest power levels. Consequently, it is not easy to ensure high efficiency to heavy loads [20], [24], [25].

In hybrid approaches, the modulation scheme is not simple because it must be selected according to the power level.

A TPSM based DAB is proposed in [31]. In the TPSM, δ, D_1 and D_2 are used for the converter control. The result is that the converter performance depends on many factors, such as the power processing level and voltage conversion ratio. It occurs because the converter duty cycles (D_1 and D_2) may be unequal and variable. Also, their optimal choice depends on the converter operating point [16], [25], [27], [36].

The TPSM performance depends on converter optimization and multivariable analysis. Hence, the TPSM control is not easy to implement with high performance, and there is no unique solution in the current literature for its implementation.

A wide soft-switching operation is ensured in a-PWM, and high efficiency can be obtained due to the reducing circulating current. The main advantage is related to the simple implementation because only one controlled variable is used (D_1). It is possible because D_2 is defined as a fixed value, and no phase-shift is used in PWM approaches. The a-PWM's penalty is related to the conduction losses because asymmetrical losses result due the diodes conductions [33].

TABLE II
MAIN RMS CURRENTS OF THE DAB CONVERTER OPERATING WITH THE PROPOSED ASYMMETRICAL PWM

	$i_{S1\text{-}S3}(rms)$	$i_{S2\text{-}S4}(rms)$	$i_{S5\text{-}S6\text{-}S7\text{-}S8}(rms)$	Transformer current $i_{Ls}(rms)$
Step-down mode	$\frac{\Delta i_{Ls}}{n}\cdot\sqrt{\frac{D}{6}}$	$\frac{\Delta i_{Ls}}{n}\cdot\sqrt{\frac{D}{6}+\frac{2\cdot\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot v_2}}$	$\Delta i_{Ls}\cdot\sqrt{\frac{D}{6}+\frac{\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot v_2}}$	$\Delta i_{Ls}\cdot\sqrt{\frac{D}{3}+\frac{2\cdot\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot v_2}}$
Step-up mode	$\frac{\Delta i_{Ls}}{n}\cdot\sqrt{\frac{\Delta i_{Ls}\cdot L_S}{3\cdot T_S\cdot(v_1/n-v_2)}}$	$\frac{\Delta i_{Ls}}{n}\cdot\sqrt{\frac{D}{3}+\frac{\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot(v_1/n-v_2)}}$	$\Delta i_{Ls}\cdot\sqrt{\frac{D}{6}+\frac{\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot(v_1/n-v_2)}}$	$\Delta i_{Ls}\cdot\sqrt{\frac{D}{3}+\frac{2\cdot\Delta i_{Ls}\cdot L_S}{3\cdot T_s\cdot(v_1/n-v_2)}}$

TABLE III
COMPARISON OF CONVENTIONAL DAB CONVERTERS' MODULATIONS AND THE PROPOSED ASYMMETRICAL PWM

		[20]	[31]	[32]	Asymmetrical PWM
Number of components	Switches	8	8	10	8
	Diodes	2	-	-	-
	Capacitors	2	2	2	2
	External Inductors	3	1	3	1
Driver circuits	Isolated	4	4	6	4
	Non-Isolated	4	4	4	4
Transformer turn rations	(1:n)	(1:3.75)	(1:2)	(1:8.3)	(1:5)
Switching frequency		100 kHz	50 kHz	100 kHz	50 kHz
Soft-switch requirements	High voltage switches	ZVS-on	ZVS-on	ZVS-on	ZVS-on
	Low voltage switches	ZVS-on	ZVS-on	ZCS-off	ZCS-off
Soft-switch range (related to the nominal power)		6-100%	7-100%	Unvalued	2-100%
Power (and voltage) range		1 kW (42-56V/380V)	1 kW (200V/400V)	480 W (48V/400V)	500 W (42-56 V/380V)
Flat efficiency		Around 96%	Around 96%	Around 94.6%	Around 96%
Design specifications		Two clamping diodes and auxiliary inductors	Needed an offline optimization	Resonant cell with two switches and inductors	Asymmetrical losses
Control method	Modulation strategy	DPSM+EPSM	TPSM	EPSM	a-PWM
	Controlled variables	δ and D_1	δ, D_1 and D_2	δ and D_1	Only D_1

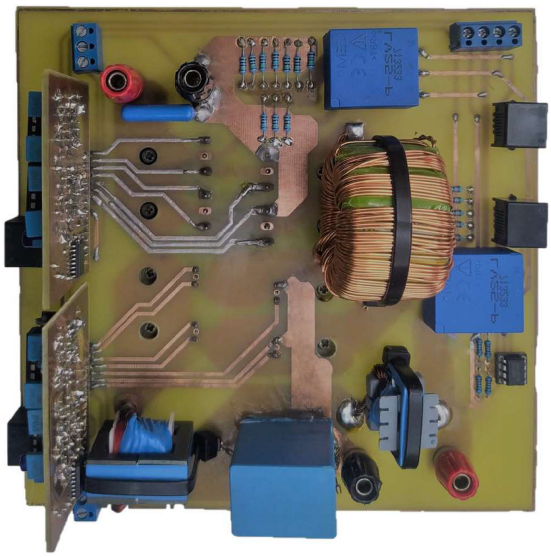


Fig. 7. Experimental prototype.

TABLE IV
PARAMETERS AND SPECIFICATIONS OF THE PROTOTYPE

Parameter/Component	Value/Detail
Nominal power (P_o)	500 W
dc bus voltage (v_1)	380 V
Battery bank (v_2)	42-56 V (20 Ah)
HF Transformer	Pri: 76 turns 2x#22 AWG (0.094 Ω) Sec: 15 turns 8x#22 AWG (0.005 Ω) Core: MMT520T40.31.10B
Serie inductor (L_s)	6.5 µH, Core: EE30/15/14 5 turns 32x#24 AWG (0.017 Ω)
L_{filter} (Δi=0.6 A)	1.50 µH, Core: EE20/10/5 3 turns 26x#26 AWG (0.006 Ω)
C_1 (Δv=38 V)	220 nF (Polyester 630 V)
C_2 (Δv=0.56 V)	70 µF (Film capacitor 60 V)
HV switches (S_1-S_4)	C3M0060065J (650 V/36 A)
LV switches (S_5-S_8)	IPP051N15N5 (150 V/120 A)
Switch frequency (f_s)	50 kHz
Driver circuit	IR2110

V. EXPERIMENTAL RESULTS

A 500-W prototype was used to verify the performance of the proposed modulation and design methodology. The experimental prototype is presented in Fig. 7. The parameters and specifications of the DAB converter are given in Table IV. The converter design considers a 48 V lithium-ion battery bank of 20 Ah. The constant current of 9 A is adopting for the battery charge. For the discharge, current and voltage levels vary according to the SoC. The converter design complies with other industrial applications [20], [31], [32] using a dc bus voltage of 380 V.

The design of the inductance L_s considers different voltage conditions of the battery bank. Fig. 8 presents the boundary limits evaluated from (11). Below the boundary, the converter

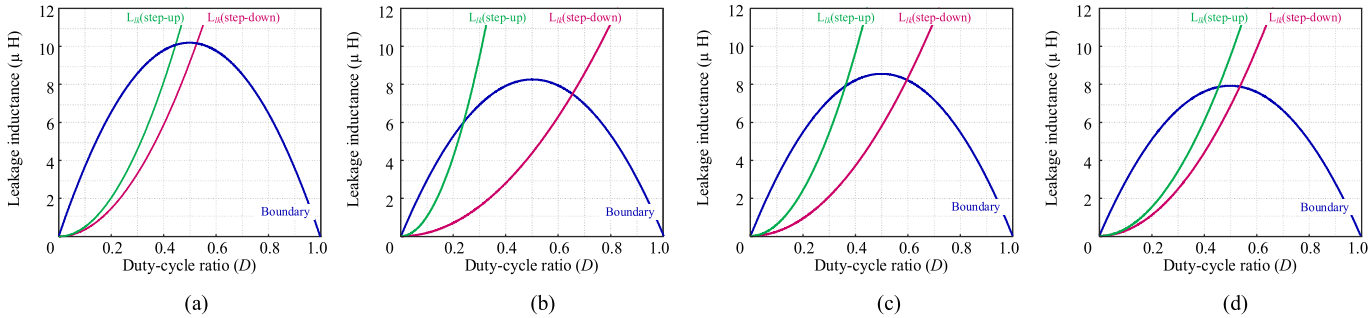


Fig. 8. Leakage inductance design to: (a) 42 V (v_2) and 9 A (i_{filter}). (b) 56 V (v_2) and 9 A (i_{filter}). (c) 48 V (v_2) and 10.42 A (i_{filter}). (d) 42 V (v_2) and 12 A (i_{filter}).

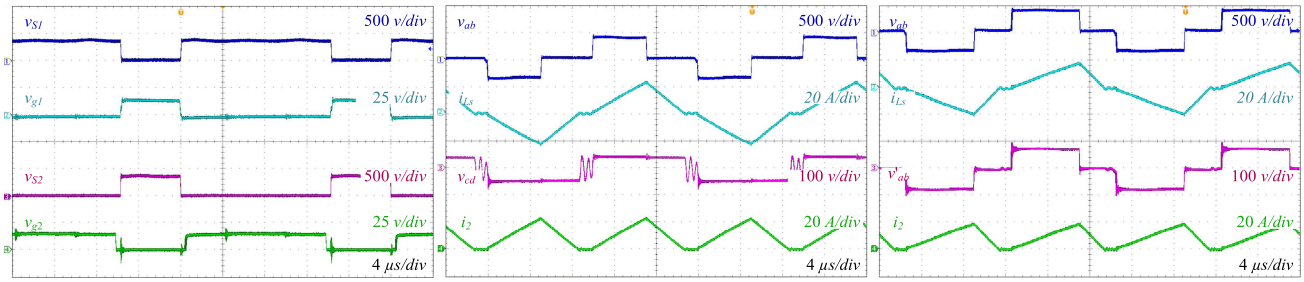


Fig. 9. Waveforms of step-down mode. (a) Gating signals (v_{g1}, v_{g2}) and blocking voltages (v_{S1}, v_{S2}). (b) Transformer voltages (v_{ab}, v_{cd}), leakage current (i_{lk}) and output current (i_2) to duty cycle 0.4. (c) Transformer voltages (v_{ab}, v'_{ab}), leakage current (i_{lk}) and output current (i_2) to duty cycle of 0.58.

operates in the discontinuous conduction mode (TRM waveform). Above the boundary, the converter operates in the continuous conduction mode (TZM waveform). The objective is to operate in the discontinuous mode to ensure all soft-switching conditions. Also, the turn ratio (n:1) is 5:1.

Based on the voltage ratios (2) and (3) for the step-down and step-up modes, respectively, the curves associated with L_s depicted in Fig. 8 were obtained.

The inductance L_s must be the highest possible value below the boundary curve, considering the worst scenario. The worst case is depicted in Fig. 8(d). It ensures the lowest Δi_{Ls} in discontinuous conduction mode and also the ZVS and ZCS conditions.

In the following, two subsections present the experimental results for each operation mode. The converter's waveforms were obtained with an oscilloscope Tektronix DPO4034 and efficiency with a power analyzer WT 1800.

To evaluate each operation mode individually, Section V-A presents the step-down mode, Section V-B the step-up mode, and Section V-C is used to verify the high-frequency ripples.

A. Step-Down Mode Results

Fig. 9 presents the main waveforms of step-down mode. Fig. 9(a) shows the gating signals (v_{g1} and v_{g2}) and the blocking voltages of semiconductors S_1 and S_2. It can be seen that the waveforms of blocking voltages are complementary as expected. A fixed dead-band of 250 ns is added between the gating signals to allow the ZVS-ON of all semiconductors. In the first test, the battery bank is discharged (42 V), and the duty cycle is defined as 0.4 to charge the batteries with 9 A_{rms}.

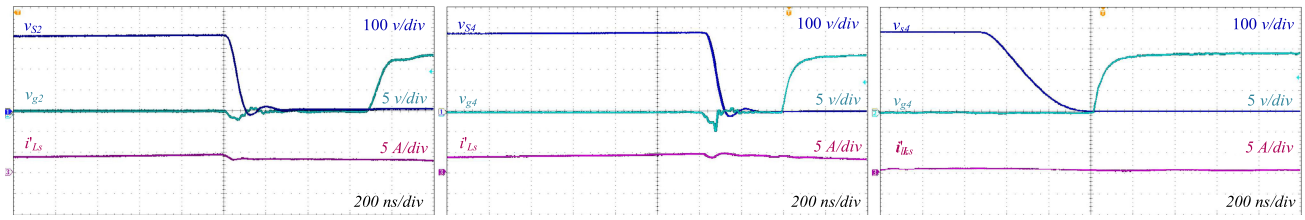
Fig. 9(b) shows the voltages v_{ab} and v_{cd}. The voltage v_{ab} has three levels, while voltage v_{cd} is almost a square wave. When the transformer current is zero, a resonance occurs between the output capacitances of LV switches and series inductances. Fig. 9(b) also shows the secondary transformer current (i_{Ls}) and the output current (i_2).

In a second test, the battery is completely charged, resulting in a higher voltage (56 V). Fig. 9(c) shows the voltage v_{ab} and its referred value to the LV side v'_{ab} to evaluate the transformer turn ratio (5:1). Besides, v_{ab} results in the largest duty cycle (0.58) due to the high battery voltage.

To evaluate the ZVS-ON range, Fig. 10 shows experimental results with the converter processing the nominal power (500 W) and a light load (10 W). Fig. 10(a) and (b) shows the leading and lagging legs ZVS-ON details at 500 W. The leading leg has the lowest ZVS-ON range. Finally, Fig. 10(c) shows the loss of the ZVS when the processed power is 10 W. At this power level, the transformer current does not satisfy the ZVS condition described by (1).

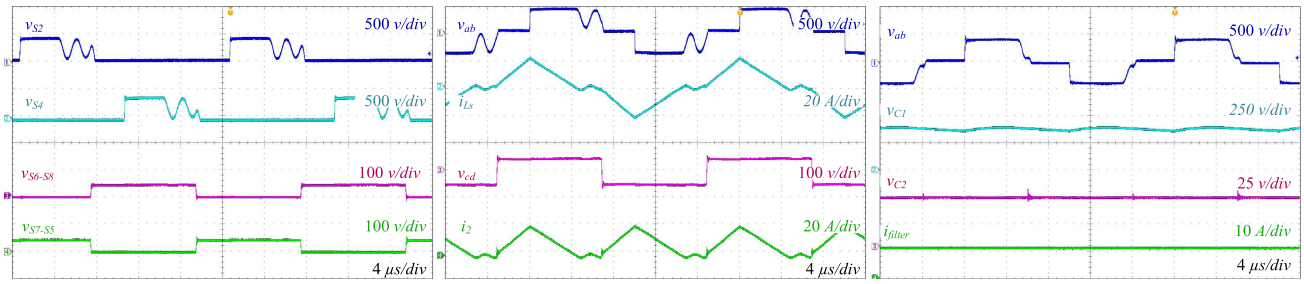
B. Step-Up Mode Results

Fig. 11 shows the main waveforms of the DAB converter operating in the step-up mode. Fig. 11(a) presents the blocking voltage of the main semiconductors. At the LV side, S_5–S_8 and S_6–S_7 result in a blocking voltage equal to v_2, and no resonance occurs. On the HV side, a resonance occurs due to the output capacitances of S_2 and S_4 and the series inductance (L_s). It can be reduced by choosing a semiconductor with the lowest possible output capacitance. However, the output capacitance is an intrinsic characteristic of the semiconductor, and other



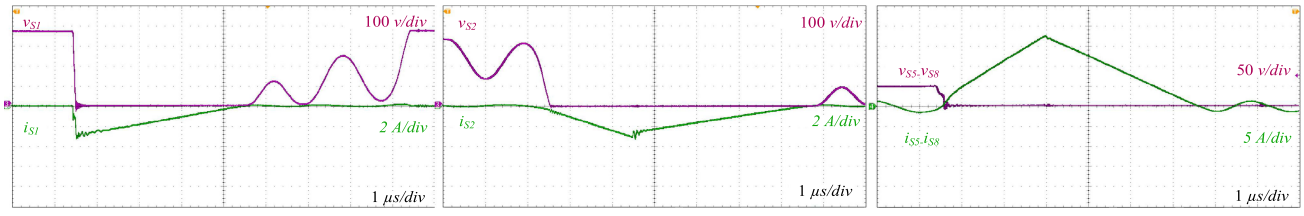
(a) (b) (c)

Fig. 10. Details of ZVS at turn-ON of step-down. (a) Leading leg. (b) Lagging leg. (c) Lagging leg ZVS lost at 10 W.



(a) (b) (c)

Fig. 11. Waveforms of step-up mode. (a) Semiconductors blocking voltages (v_{S1}, v_{S2}, $v_{S5\text{-}S8}$, $v_{S6\text{-}S7}$). (b) Transformer voltages (v_{ab},v_{cd}), leakage current (i_{lk}) and input current (i_2) to duty cycle 0.31. (c) Transformer voltages (v_{ab}), dc bus voltage (v_{C1}) and batteries discharge current (i_{filter}) and voltage (v_{C2}) to duty cycle of 0.39.



(a) (b) (c)

Fig. 12. Details of ZCS at turn-OFF for the step-up mode. (a) S_1 (b) S_2. (c) S_5–S_8.

aspects should also be weighted, such as the diode reverse recovery time and conduction losses.

Fig. 11(b) shows the HF transformer voltages v_{ab} and v_{cd}, the current of the transformer (i_{Ls}), and battery discharging current i_2. The first test considers the nominal voltage of the battery (48 V). Therefore, i_2 is 10.42 A_{rms}. Fig. 11(c) presents the results when the batteries are fully discharged with low SoC. In this situation, the battery bank voltage (v_2) is equal to 42 V. This result represents the highest processed current (12 A_{rms}), and consequently, the highest duty cycle (0.39). Also, Fig. 11(c) verify the voltage conversion ratio. For the dc bus, the measured average voltage is equal to 380 V.

In the last test, Fig. 12 shows the ZCS conditions of the main semiconductors. Since the ZCS-OFF occurs in all power range, only one test is presented considering a processed power of 250 W. Fig. 12(a) shows the S_1 switching, and Fig. 12(b) the details of S_2. Both cases illustrate details of ZCS-OFF and the resonances of output capacitances and L_s when the transformer current becomes zero. Finally, Fig. 12(c) shows the details of the ZCS-OFF at the LV side on the semiconductors S_5 and S_8.

C. High-Frequency Ripples Results

Fig 13 shows the experimental results of the high-frequency ripple obtained using the ac coupling. They depict the waveforms and the ripple amplitude for the dc-bus voltage, battery voltage, and current.

Fig. 13(a) shows the battery current (Δi_{filter}) and voltage (Δv_{C2}) ripple for the step-down mode with a duty cycle of 0.4 for a battery completely discharged. The battery voltage ripple (Δv_{C2}) is 0.50 V, while the current ripple Δi_{filter} is 0.56 A.

Fig. 13(b) shows the experimental results with a higher SoC battery and a duty cycle of 0.58. Again, similar results are obtained. The experimental ripples are below the defined design values $\Delta i_{filter} = 0.6$ A and $\Delta v_{C2} = 0.56$ V. Therefore, the design methodology is validated.

Fig. 13(c) shows the experimental results for the step-up mode considering a duty cycle of 0.39. The experimental dc bus voltage ripple (Δv_{C1}) is 35 V, while the defined design value is 38 V. Again, the filter design is corroborated.

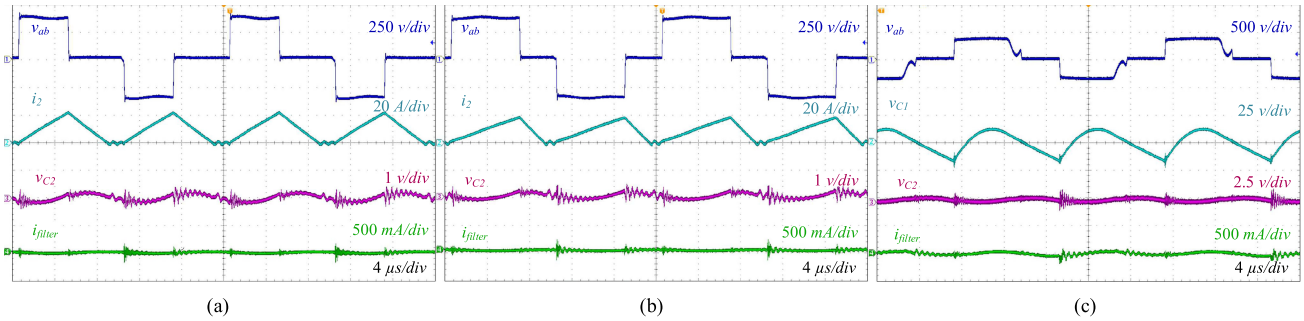


Fig. 13. High-frequency ripple results. (a) Step-down mode with duty cycle 0.4. (b) Step-down mode with duty cycle 0.58. (c) step-up mode with duty cycle 0.39.

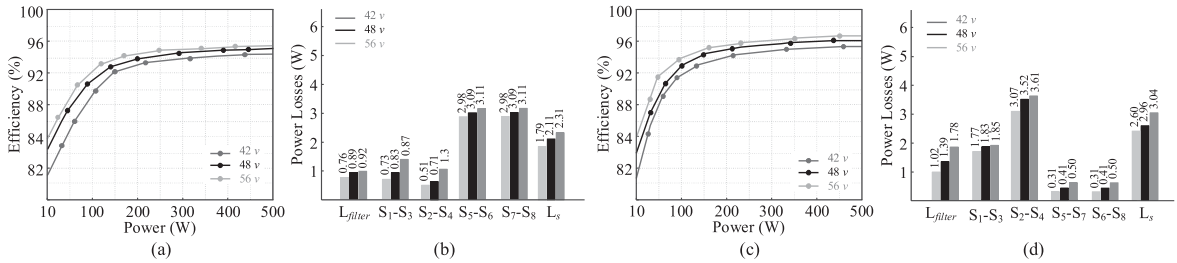


Fig. 14. Experimental efficiency and analysis of the losses. (a) Efficiency of step-down mode. (b) Estimated losses distribution of step-down mode at nominal conditions (380/48 V-500 W). (c) Efficiency of step-up mode. (d) Estimated losses distribution of step-up mode at nominal conditions (48/380 V-500 W).

D. Efficiency Analysis

The converter efficiency is evaluated at different operating points considering both operation modes and battery voltage levels (42, 48, and 56 V). Fig. 14(a) presents the measured efficiency in the step-down mode for different processed power. The asymmetrical modulation results in a flat efficiency, which includes the light loads where de minimum measured efficiency is 82.02%. At the nominal power, the maximum efficiency is 95.60%. For the step-up operation mode, similar results are shown in Fig. 14(c), where the minimum efficiency is 83.41%, and the maximum efficiency is 96.30% at nominal power.

The switching losses are almost constant due to the large ZVS and ZCS range. S_1 and S_3 operate on hard switching, equalizing S_2–S_4 losses in the step-down mode. In the step-up mode, the SiC-diodes reduces the reverse recovery losses at S_1–S_3, while S_2–S_4 has some conduction losses. Fig. 14(b) and (d) shows the converter losses distribution according to the *rms* currents, switching, and magnetic losses.

VI. Conclusion

In this article, a-PWM for the DAB converter was proposed to overcome the limitations of the usual PSM, DPSM, and TPSM, which operates with a restricted ZVS-ON range and excessive circulating current. Although the proposal allows both asymmetrical conduction losses and diode conduction, it ensures reducing the circulating current. Besides, SiC-MOSFETs were applied to reduce reverse recovery losses at the high-voltage side. The modulation strategy provides ZCS-OFF and ZVS-ON for a wide operation range between 2%–100% of the rated power, which reduces the switching losses significantly.

The experimental results demonstrate that it is possible to achieve improved results compared to conventional strategies previously presented in literature without extra hardware or multivariable control. The main advantages over other strategies are: simplicity, since the duty cycle D_2 remain permanently fixed at 0.5; lower design complexity concerning solutions based on multivariable control, offline optimizations, or auxiliary circuits; and also it is possible to obtain a more flat efficiency due to the extended soft-switching conditions.

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