Application of Soft-Switching Cell With Inherent Redundancy Properties for Enhancing the Reliability of Boost-Based DC–DC Converters

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***Abstract*—In this article, the inherent fault-tolerant capability of the soft-switching cell for boost-based dc–dc converters is investigated. The main switch of boost-based dc–dc converters withstands high-temperature stress, which is expected to be failed with a higher probability than other devices. Providing soft-switching condition for the main switch and employing fault-tolerant capability are effective approaches to solve this problem. When a fault occurs for the main switch, the proposed converter can be reconfigured such that the soft-switching cell can change its duty to continue the normal operation of the converter without interruption. Inherent redundancy, low failure rate, high integration, and high efficiency are the specifications of the presented converter. The reliability analyses are presented and the functionality of the active soft-switching cell to provide soft-switching condition and fault-tolerant capability are verified by experimental results.**

***Index Terms*—Active soft-switching cell, boost dc–dc converter, fault-tolerant capability, inherent redundancy feature, reliability.**

I. Introduction

POWER electronic converters are used to transfer power from energy sources to the loads. In applications such as aerospace systems, military devices, and medical equipments, in which loads must be continuously supplied, avoiding power interruption is very important. Thus, using converters with high reliability is necessary [1].

Power switch devices in dc–dc converters have a high risk of burning during the operation of converters, which challenges the reliability of the converters. Since most power electronic converters do not have the redundant capability, any unexpected fault that occurs to the switches would result in an interruption in converter operation [2]. To solve this problem, reducing failure rate and providing fault-tolerant capability are two important approaches to increase the reliability of dc–dc converters [3].

In modern applications, high efficiency and high power density dc–dc converters are required. To increase power density, the switching frequency must be increased. However, by increasing the switching frequency, the losses increase. This results in a reduction in the converter efficiency and reduces the life-time of the converter components. The approach to solving this problem is applying soft-switching methods. Using soft-switching methods not only reduces the switching loss drastically but also decreases the switches failure rate [3], [4].

When a fault occurs, the converter must use the fault-tolerant mechanisms to keep normal operation. To provide fault-tolerant capability, some solutions are addressed in the literature, which are generally divided into two categories.

The first approach is implementing fault-tolerant techniques without additional redundant power devices [5]–[8]. Interleaved structures belong to this fault-tolerant category in which if a fault occurs for the switches of a converter branch, other branches can take the tasks of the faulted branch [6]–[9]. Increasing the input and output voltage and current ripples, imposing additional electrical stresses to the power devices, and complex mechanisms of fault-managing system are the main problems of this method.

Another approach is to provide the fault-tolerant capability for dc–dc converters by adding circuitries that contain some redundant switches to the converter topologies [10]–[15]. In general, equipping converters with redundant power switches, legs, or modules [3] are the most desired solutions. In [13], by adding a redundant switch to the boost and buck converters, a new converter is introduced that can operate as a buck or boost converter in normal condition and can operate the same as a buck-boost converter under fault conditions. In [12], the cascade connection of z-source converters is used to reduce voltage stress of the components and also, to keep feeding load under fault conditions. Fault-tolerant single switch converters are presented in [14] and [15] using standby switch configurations. However, increasing the component counts, design complexity, and cost of the converter are some disadvantages of these methods. All the mentioned topologies have low efficiency in high switching frequencies and require large heat sinks to keep the junction temperature of the switches far from critical junction temperatures. Thus, their components failure rate is high. Besides, a

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long transition time between forward blocking mode to forward conduction mode is required in order to replace the redundant switch (e.g., TRIAC or relay) with the faulty switch in case of failures. The mentioned challenges are motivated to use inherent fault-tolerant configurations.

Adding soft switching and fault-tolerant circuitries to the power converters simultaneously causes a severe increase in the number of converter components. One of the approaches to reduce the components count is using soft-switching cells that can be acted as redundant structures when a fault occurs. Changing the task of the converter components according to different operating modes is a good solution to meet both improving the performance and increasing the integration of the converters.

So far, many soft switching techniques have been introduced in the literature. However, due to limitations in the structure of soft switched converters, by losing the main converter switch, the converter functionality would be missed [16]–[20]. In order for a soft-switching cell can provide inherent redundancy property, three essential requirements must be satisfied.

1) Its topology must contain at least one switch.
2) The soft-switching cell must have the capability to be placed in parallel with the main switch of the converter.
3) All components of the soft-switching cell must not disrupt the converter functionality in fault conditions.

In this regard, the zero-voltage-transition (ZVT) soft switching circuits have the ability to change their task under fault conditions. The ZVT circuits mostly consist of a capacitor, inductor, diode, and switch that are placed in the node in which the main converter switch is connected [21], [22]. This configuration of the soft switching circuits can act as the main switch of the boost converter when a fault occurs. Thus, the ZVT circuits can meet the reliability requirements by considering high-efficiency performance.

Enhancing the fault-tolerant capability of power converters by changing the role of active soft-switching cells is the main contribution of this article, which has not been considered in the previous literature. In this article, the ZVT boost converter reliability is analyzed, and its potential to have inherent redundancy in fault-tolerant conditions is investigated.

II. Application of the ZVT Cell in Boost Converter for Enhancing Reliability

So far, the ZVT cells have been used in many converters to provide soft-switching condition [21]–[39]. In general, the base of most ZVT circuits is derived from the references [21]–[26]. However, according to the aforementioned points, most ZVT cells cannot be utilized for reliability issues. In [32], [36], and [39], the ZVT cell does not place in parallel with the main switch of the converter. In [23]–[25], [27]–[31], and [35], the ZVT components disrupt the converter functionality in fault conditions. Although, by applying slight changes to most of the ZVT circuit topologies, they can operate under fault conditions. Moreover, according to the reliability design considerations, some other design considerations such as the number of components, voltage and current stresses, and soft-switching conditions must be considered to select the proper ZVT cell. In the following, a ZVT cell is selected and the topology derivation procedure of this cell to operate under fault conditions is discussed.

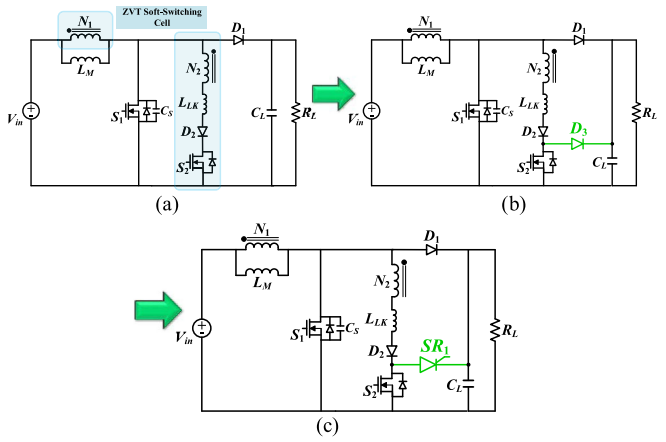

Fig. 1. Topology derivation of the proposed converter. (a) Conventional ZVT boost converter (C-ZVT). (b) Improved ZVT boost converter by utilizing clamping diode (I-ZVT-D). (c) Improved ZVT boost converter by utilizing thyristor (I-ZVT-SR).

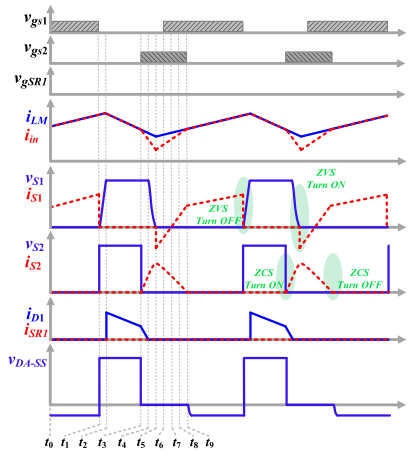

Fig. 2. Key waveforms of the ZVT boost converter under normal conditions.

In [21], a ZVT boost converter is introduced which is shown in Fig. 1(a). In this converter, S_1 is the main switch, D_1 is the output diode, and L_M acts as the inductor of the boost converter. The ZVT cell consists of N_1–N_2 coupled inductors ($n = N_2/N_1$) along with leakage inductance (L_{LK}), S_2 is the auxiliary switch, and D_2 is the auxiliary diode. In this converter, the coupled inductors technique is used. Thus, a single magnetic core is utilized in which the volume of the converter is reduced. Also, S_1 operates under zero-voltage-switching (ZVS) and S_2 operates under zero-current-switching. Fig. 2 shows the key waveforms of the ZVT boost converter under normal conditions. In [21], circuit analysis and design considerations are presented in detail.

In the conventional boost converter, the S_1 main switch has a high potential to burn. However, in the introduced ZVT boost converter, the ZVT cell can change its task and the auxiliary switch can operate instead of S_1. When a fault occurs for S_1, at first physical fault isolation unit [3] forces the damaged switch to be electrically isolated from the converter and eliminates

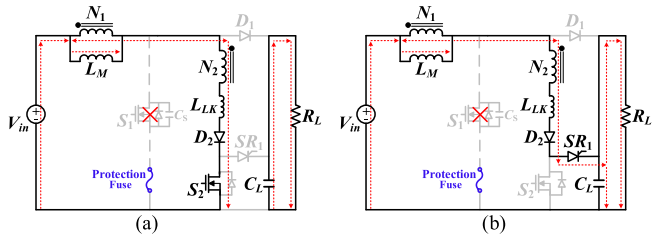

Fig. 3. Steady-state equivalent circuits of I-ZVT-SR converter when S_1 is failed due to the fault. (a) S_2 is in ON mode. (b) S_2 is in OFF mode.

its influence over the converter operation. Then the postfault reconfiguration would be activated. In this stage, the ZVT cell, which is connected in parallel with the main switch can continue the operation of the converter. Thus, the reconfigured converter can operate similarly to the conventional boost converter and supply the output load.

In the S_1 failure condition, S_2 operates as the main switch of the converter. At the turn-OFF instance, there is no path to discharge the stored energy in the leakage inductance series with the auxiliary switch. Thus, the leakage inductance generates spikes and increases the losses and voltage stress of S_2. Instead of over-designing the voltage stress of S_2, a simple practical solution is, clamping the v_{S2} on output voltage through a clamping diode (D_3) which is shown in Fig. 1(b). In the following, this converter is called I-ZVT-D converter. Although S_1 can operate under soft-switching conditions, but this diode disturbs the soft-switching operation of the S_2 in a normal state. To solve this problem, a technique must be used such that the voltage of S_2 be clamped to the output just in a fault condition. And, in normal conditions, it does not affect the soft-switching operation of the converter. Accordingly, the structure of Fig. 1(c) is proposed in which a thyristor (SR_1) is used instead of the clamping diode. In the following, this converter is called the I-ZVT-SR converter. In normal conditions, SR_1 is always OFF and the operation of the converter would be the same as the C-ZVT boost converter (see Fig. 2).

And, when a fault occurs, a constant trigger voltage would be applied to the gate of the thyristor. Through this method, the thyristor acts similarly to a diode. Thus, the operation of the converter in fault conditions would be similar to the conventional boost converter. And, a power flow path is provided to discharge the stored energy in the leakage inductance and the voltage stress of S_2 is clamped to the output voltage.

The steady-state operations and the key waveforms of the improved ZVT converter (I-ZVT-SR) under fault conditions are shown in Figs. 3 and 4, respectively. When S_2 is ON, the energy stores in magnetizing inductance and due to $n<1$, the less amount of current circulates in the primary side of the coupled inductors [see Fig. 3(a)]. And, when S_2 turns OFF, the stored energy in L_M transfers to the load [see Fig. 3(b)].

III. Reliability Analyses

In this section, the reliability analyses of the proposed converter are evaluated. At first, all possible operating states of the converter are investigated, and the graphical transitions of the

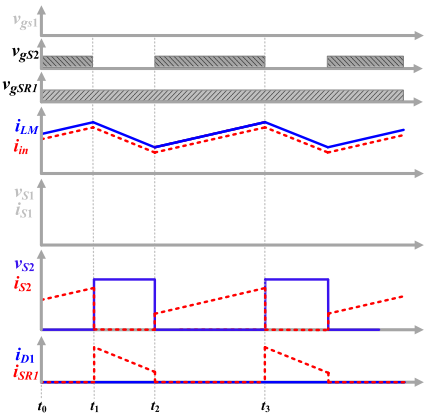

Fig. 4. Key waveforms of the ZVT boost converter under fault condition.

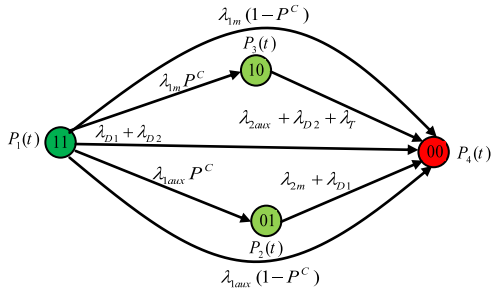

Fig. 5. Markov chain of the studied converter.

possible routes from one state to other states are presented. Then, the transition matrixes and mathematical equations to calculate the probability function of each state are derived. After that, the failure rates calculation method is introduced to derive the probability rate of transitions between each state.

A. The Markov Chain of the Proposed Converter

In a multistate system that may operate in different probability states, Markov chain theory can be employed to model stochastic changing of all states [40]. In [2], [8], [12], and [13], the Markov chain is used to derive reliability models of fault-tolerant converters. In the Monrovian theory, a Markov model of a system is built base on the probabilistic state-transition scheme of all operating conditions. In the proposed fault-tolerant converter, the health situation of the switches determines the operating states of the converter. The proposed converter can continue its duty in case of the main or auxiliary switch failures. Thus, two acceptable operating states are realized for the converter. After that, when the survived switch fails, the converter shuts down. According to [1], [12], [13], [41], and the results of this article, the failure rates of diodes and the thyristor are low enough to negligible in reliability analyses. However, to cover all possible events, the operation states of the proposed converter in case of these semiconductor devices failure are also considered in this section. Accordingly, four states can be considered in the Markov chain. Fig. 5 shows the Markov chain diagram for the studied converter. This diagram consists of four states as described in the following.

State 11: In this state, the main and the auxiliary switches and other semiconductor devices are healthy. In other words, the converter operates under normal soft-switching conditions.

State 10: If the main switch fails, the fault managing system must detect the fault, isolates the main switch, and reconfigures the converter to operate the auxiliary switch as the main converter switch. Therefore, the auxiliary switch tackles the main switch duty to feed load without interruption. The failure rate of the main switch and successful operation probability of the fault-managing system are denoted by $\lambda_{1\mathrm{m}}$ and P^{C}, respectively, in Fig. 5. The transition probability from state 11 to state 10 is $\lambda_{1m}P^{\mathrm{C}}$. The auxiliary switch, the D_2, and thyristor with the rates of (λ_{2aux}), (λ_{D2}), and (λ_T) may fail while the converter operates in state 10 which causes the converter shutdown.

State 01: It is possible that the ZVT cell would be lost due to the auxiliary switch fault. Therefore, this cell must be isolated by the fault-managing system. If the fault-managing system operates successfully with the rate of P^{C}, state 01 appears. The transition probability from state 11 to 01 is $\lambda_{1aux}P^{\mathrm{C}}$. In case of the main switch or output diode failure in state 01, the system would be OFF. Thus, the transition probability from state 01 to State 00 is $\lambda_{2m}+\lambda_{D1}$.

State 00: This state indicates the conditions in which there is no solution to supply the load power demand. If the main or auxiliary switch fails and the fault managing system cannot handle the faulty conditions, two possible transition paths from state 11 to 00 are realized. The transition rates from state 11 to 00 are determined by $\lambda_{1m}(1-P^{\mathrm{C}})$ and $\lambda_{1aux}(1-P^{\mathrm{C}})$, respectively. There is another path from state 11 to 00 that appears when the diodes fail with the rate of $\lambda_{D1}+\lambda_{D2}$.

According to the theoretical concepts of Markov chain analyses, a differential equation-based matrix is required to be derived. The general form of the matrix is presented by the following equation:

$$\frac{d}{dt}\begin{bmatrix}P_1(t)\\P_2(t)\\P_3(t)\\P_4(t)\end{bmatrix}=\begin{bmatrix}-\lambda_1-\lambda_D & 0 & 0 & 0\\ \lambda_{12} & -\lambda_{22} & 0 & 0\\ \lambda_{31} & 0 & -\lambda_{33} & 0\\ (1-P^C)\lambda_1+\lambda_D & \lambda_{22} & \lambda_{13} & 0\end{bmatrix}\begin{bmatrix}P_1(t)\\P_2(t)\\P_3(t)\\P_4(t)\end{bmatrix}. \tag{1}$$

To derive the matrix elements, some general simple rules are used as follows.

- To calculate λ_{ii}, all transition rates from state (i) to other states must be summed together. For example, (2) shows the calculation of λ_{11}as an example

$$\lambda_{11}=\lambda_{1m}P^C+\lambda_{1aux}P^C+(1-P^C)\lambda_{1m}+(1-P^C)\lambda_{1aux}+\lambda_{D1}+\lambda_{D2}. \tag{2}$$

By simplifying (2), we get

$$\lambda_{11}=(\lambda_{1m}+\lambda_{1aux})+(\lambda_{D1}+\lambda_{D2})=\lambda_1+\lambda_D. \tag{3}$$

- λ_{ij} is the transition rate from state (i) to (j). For example, considering Fig. 5, the operating state of the converter may change from State 11 to 01 with the rate of $\lambda_{1aux}P^C$. Thus, λ_{12} is equal to $\lambda_{1aux}P^C$. Considering the mentioned examples and rules, all elements of the matrix can be derived easily. In this matrix,$\lambda_{11}=\lambda_{1m}+\lambda_{1aux}$, $\lambda_{22}=\lambda_{2m}+\lambda_{D1}+\lambda_{D2}$, $\lambda_{33}=\lambda_{2aux}+\lambda_{D2}+\lambda_T$, $\lambda_D=\lambda_{D1}+\lambda_{D2}$ and λ_{13} is equal to $\lambda_{1m}P^C$.

According to Markov chain theory, the initial probability values of states are as follows:

$$\begin{bmatrix}P_1(0) & P_2(0) & P_3(0) & P_4(0)\end{bmatrix}=\begin{bmatrix}1 & 0 & 0 & 0\end{bmatrix}. \tag{4}$$

Since the converter can operate in states (11), (10), and (01), the reliability function of the studied converter is the summation of $P_1(t)$, $P_2(t)$, and $P_3(t)$. The reliability of the converter can be written as

$$R_p(t)=P_1(t)+P_2(t)+P_3(t). \tag{5}$$

The probability functions of different states can be derived by solving the differential equation-based matrix. By solving (1) and considering the initial conditions, the reliability function can be derived as follows:

$$R_p(t)=\begin{bmatrix}1-\frac{\lambda_{1m}P^c}{\lambda_{1m}+\lambda_{1aux}-(\lambda_{2aux}+\lambda_{D2}+\lambda_T)}\\ -\frac{\lambda_{1aux}P^c}{\lambda_{1m}+\lambda_{1aux}-(\lambda_{2m}+\lambda_{D1})}\end{bmatrix}e^{-(\lambda_{1m}+\lambda_{1aux}+\lambda_D)t}+\begin{bmatrix}\frac{\lambda_{1m}P^c}{\lambda_{1m}+\lambda_{1aux}-(\lambda_{2aux}+\lambda_{D2}+\lambda_T)}e^{-(\lambda_{2aux}+\lambda_{D2}+\lambda_T)t}\\ +\frac{\lambda_{1aux}P^c}{\lambda_{1m}+\lambda_{1aux}-(\lambda_{2m}+\lambda_{D1})}e^{-(\lambda_{2m}+\lambda_{D1})t}\end{bmatrix}. \tag{6}$$

Meant time to failure (MTTF) is another reliability index. MTTF predicts the elapsed time that the failure will occur for a converter. This index can be calculated as follows:

$$\mathrm{MTTF}=\int_0^\infty R_p(t) \tag{7}$$

where $R(t)$ is the reliability function [40], [42].

B. Failure Rate Analyses

The fault occurrence is a random phenomenon so that the converter can operate randomly at any operating state. To derive the reliability equation, failure rates of switches and other semiconductor devices must be calculated. The failure rates of switches are much more than other components [1], [4], [12], [13], [41]. Thus, the detailed failure rates of switches as the most vulnerable components are examined in this section. Different factors affect the calculated failure rates of switches. Each factor should be determined considering the environment and operating conditions of the studied converters.

- Considering the environmental situation in which the converter operates, the environmental factor π_{En}must be defined. It is assumed that the converter operates in the ground benign environment. Thus, $\pi_{En}=1$.
- The manufacturing process of components can be examined by some strict reliability standards. Depending on screening levels of power devices, heritage qualification factors (π_{QS}) of power components can be provided for industry communities. Nowadays, regular screening levels are implemented by the manufacturing factors, thus $\pi_{QS}=5.5$.

- HDBK-217F considers an application factor (π_{AS}) that depends on the power rate of the converter. In this article, $\pi_{AS} = 8$.
- The base failure rate value is another factor that is considered as a constant value for calculation failure rates. In this article, it is assumed that $\pi_b = 0.027(FIT)$.
- The junction temperature factor as a variable factor depends on the power profile of a switch, ambient temperature, and thermal resistance. According to HDBK-217F and some recent papers [12], [13], [41], this factor can be calculated by using the following equation:

$$\pi_t = \exp\left(\frac{a}{c} - \frac{a}{Tj + b}\right) \tag{8}$$

where $a = 1925$, $b = 273$, and $c = 298$ [41], [42].

For a switch that is mounted on a PCB board, it is excepted that the thermal factor and all other factors values are fixed duration operation of the switch as an active element of a converter. Thus, the failure rates (λ) of the power switches in the introduced converter are calculated as follows:

$$\lambda = \lambda_{base} \exp\left(\frac{a}{c} - \frac{a}{Tj + b}\right) \tag{9}$$

whereλ_{base} is the base failure rate and its value depends on the manufacturing process and historical failure rate data. It is constant for the main and auxiliary switches. To calculate the failure rates (λ), the junction temperature (Tj) of the power switch must be calculated. Thermal resistance between the junction and the case (R_{thJC}), the case and the switch heat sink (R_{thCS}), and the heat sink and ambient (R_{thSA}) should be known to calculate the junction temperature.$R_{thJC}$and R_{thCS} are given by the selected power switch datasheets. Also, the heat sinks datasheet determines the R_{thSA} value. The relationship between the junction temperature and power losses can be obtained as follows:

$$T_j = T_a + (R_{thJC} + R_{thCS} + R_{thSA}) \times P_{Losses} \tag{10}$$

where T_a is the ambient temperature and R_{th} is thermal resistance. The power losses of a switch consist of switching and conductions losses. Thus, the (10) can be reformed as

$$T_j = T_a + (R_{th})\,(\alpha P_{Loss\_Sw} + P_{Loss\_Cond}). \tag{11}$$

P_{Loss_Sw} and P_{Loss_Cond} are the switching and conduction losses of a switch, respectively. In (11), α is the soft switching factor. $R_{th}(= R_{thJC} + R_{thCS} + R_{thSA})$is total thermal resistance. Thus, by replacing (11) into (8), (9) can be rewritten as follows:

$$\lambda = \lambda_{base} e^{(a/c)} \exp \times \left(-\frac{a}{T_a + b + R_{th}(\alpha P_{Loss\_Sw} + P_{Loss\_Cond})}\right). \tag{12}$$

By applying soft-switching techniques, the value of α would be $0 \leq \alpha < 1$. If the switch operates under fully soft-switching conditions $\alpha = 0$, while for hard-switching conditions $\alpha = 1$. It is clear that the failure rate of the power switch has a direct relation with the switching losses. For fully soft-switching conditions, the total switching losses decrease. As a result, the failure rate of the switch would be decreased significantly. To determine the failure rates values, the switching and conduction losses must be calculated. The voltage stress of the switch (V_{DS}), the switch current (i_S) and the ON-state resistance of the switch (R_{DS}) are used to calculate the power losses. The mentioned losses can be calculated using the following equations:

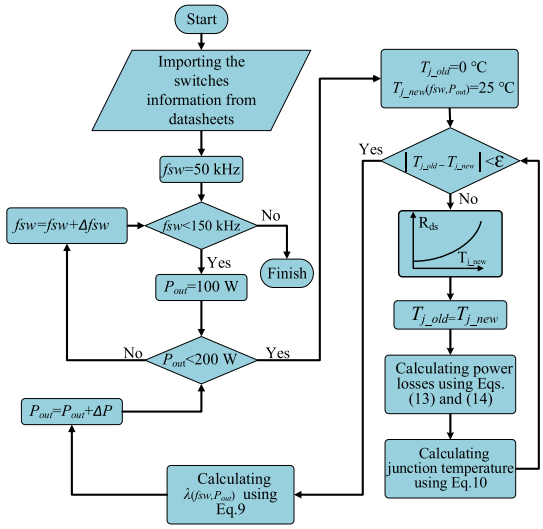

Fig. 6. Switches failure rates calculation flowchart.

$$P_{sw} = \frac{1}{T}\left[\int_0^T V_{DS} i_S(t) dt\right] \tag{13}$$

$$P_{Con} = \frac{1}{T}\left[\int_0^T R_{DS} i_s^2(t) dt\right]. \tag{14}$$

It should mention that the junction temperature (T_j) impacts on parasitic parameters of the switches are considered in failure rate calculations and the reliability analyses. With rising the junction temperature, the ON-state resistance of power switches would be increased. Thus, the losses increase. Then, the junction temperature rises further, which degrades reliability. The failure rates of diodes and the thyristor are evaluated the same as the process that is given in [2], [10], [12], [13], and [41]. To prevent prolongation, the failure analyses detail of diodes and thyristor are not reported in this section.

C. Reliability Evaluation Flowchart

In this section, the calculation procedure of the failure rates and MTTF of the studied converters in terms of different operating power levels and switching frequencies are presented. The flowchart shown in Fig. 6 indicates that how failure rate curves are achieved. In the first step of this flowchart, the switching frequency, operation power points of the converter, and the characteristics of each semiconductor device are initialized. Then, the junction temperature and failure rates for different output power levels and the switching frequency values are calculated. As the thermal resistance value depends on junction temperature, the junction temperature values are calculated in each iteration of

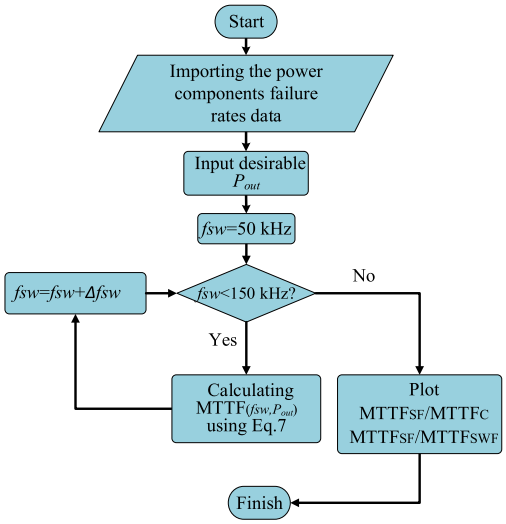

Fig. 7. MTTF calculation flowchart.

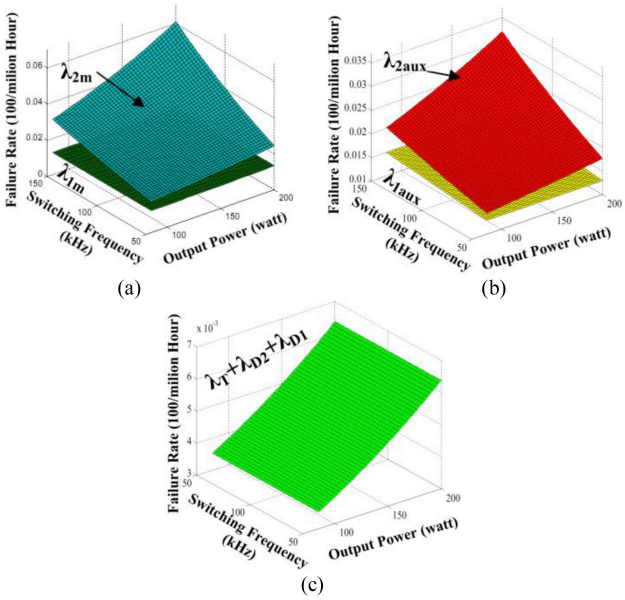

Fig. 8. Failure rate of I-ZVT-SR and conventional boost converter semiconductors. (a) S_1 failure rates. (b) S_2 failure rates. (c) Other semiconductor devices failure rates.

the flowchart loop. Using this flowchart, failure rates of switches are derived for defined power and switching frequency ranges.

To investigate the lifetime of the studied converters, the MTTF of the converters for specific operation points must be derived. Fig. 7 shows that how the MTTF values of the studied converters for different switching frequencies and the desired output powers are calculated.

D. Numerical Analyses

Fig. 8 illustrates the failure rates of the converter switches in different operating states. Fig. 8(a) shows that due to the operation of S_1 under the ZVS condition, the S_1 failure rate ($\lambda_{1\,m}$) is reduced drastically in comparison with the failure rate of the switch in the conventional converter ($\lambda_{2\,m}$) that operates under hard switching condition. Also, Fig. 8(b) indicates the failure rates of S_2 in the normal operation of the ZVT boost converter ($\lambda_{1\,aux}$) and its failure rate when S_2 operates in the faulty condition ($\lambda_{2\,aux}$). Fig. 8(c) shows the failure rates summation of the output and the clamp doides under different operating conditions in which, in comparison with the switches failure rates are negligible. Thus, the results show that soft switching reduces the failure rate of the boost converter main switch drastically. It should mention that the failure rates of main and auxiliary switches while operating under hard-switching conditions are not high, and the obtained failure rates are in the normal range [12], [13].

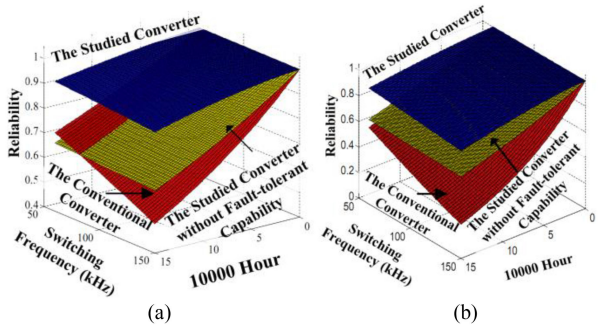

Fig. 9. Reliability comparison. (a) Half-load power. (b) Full-load power.

The reliability curves of the studied converter (for fair comparison and considering the failure of the fault-managing system, $P^{C} = 0.9$ is considered in this study), the reliability curves of the studied converter without fault-tolerant capability [$R_P(t) = P_1(t)$] and the conventional boost converter are shown in Fig. 9 for half-load and full-load operation modes. The results show that increasing the switching frequency affects reliability. The reliability of the hard-switched conventional boost converter is deteriorated by increasing the switching frequency. And, the ZVT boost converter has a more reliable structure for operating in high switching frequencies. As shown in Fig. 9, due to inherent redundancy, the ZVT boost converter in comparison with the conventional boost converter has better reliability in a wide range of the output power. Employing the ZVT cell without fault-tolerant capability cannot improve the reliability in the lower ranges of output power. Fig. 9(a) shows that in the half-load condition, the effect of using the extra switch in the ZVT boost converter dominates the effect of soft switching on reliability for low switching frequencies.

Fig. 10 compares the MTTF of the studied converters in different scenarios. In this figure, $\mathrm{MTTF_{SF}}$, $\mathrm{MTTF_{SWF}}$, and $\mathrm{MTTF_C}$ belong to the proposed converter, the converter without fault-tolerant capability and the conventional converter, respectively. According to Fig. 10, the $\mathrm{MTTF_{SF}/MTTF_C}$ proportion in full load condition has more improvement than in light load condition. However, due to the increased failure rate of the auxiliary switch in the case of operating as the main switch, the $\mathrm{MTTF_{SF}/MTTF_{SWF}}$ proportion has less improvement in the full load in comparison with operating in lower output power. Due to the use of soft-switching technique, the $\mathrm{MTTF_{SF}/MTTF_C}$

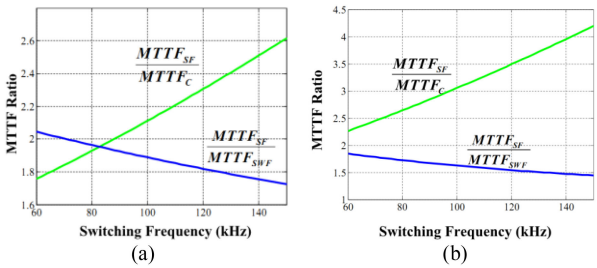

Fig. 10. MTTF comparison of the studied converters in different scenarios. (a) In half-load power. (b) In full-load power.

improvement ratio of the studied converter increases. Also, employing the inherent fault-tolerant capability of the ZVT cell causes the $\mathrm{MTTF_{SF}/MTTF_{SWF}}$ to increase.

IV. Proposed Converter Fault Tolerant Designs

The reliable performance of the converter is an important issue for the postfault conditions. In this regard, the power components must be selected according to the healthy and postfault conditions. Moreover, the reconfiguration steps and the functionality of the converter in postfault conditions must be investigated to guarantee normal or seminormal operations of the converter [43], [44].

A. Power Switches Parameters Design

The output voltage, the converter power rate, and the switching frequency are not changed in healthy and postfault conditions. Thus, redesigning the passive components is not required. However, the nominal current and voltage stresses of switches are changed as described in the following.

Voltage Stresses: during the healthy mode, the nominal voltage stress of the main and auxiliary switches are 100 and 120 V, respectively. While these values would be 100 V in fault conditions. Thus, the voltage stresses of the switches are not increased in fault conditions.

Current Stresses: the nominal rms current of the main switch in normal mode and the nominal rms current of the auxiliary switch in fault mode are almost the same and they are ≈4 A. The auxiliary switch tolerates low current stress in normal conditions. However, under fault conditions, this switch must tolerate the mentioned nominal current. Thus, the current rate of the auxiliary switch must be high to tolerate faulty conditions.

Efficiency: to achieve a high-efficiency converter, employing the switches with low ON-state resistance and low output capacitance for main and auxiliary switches are recommended. The selected power switches are listed in Table III.

Heat Sinks: the power losses of the switches are very low in normal conditions. However, the losses of the switch in fault conditions are high. In this article, to achieve an optimum design in fault conditions, it is tried to have minimum overdesigning. Therefore, the heat sinks are designed to keep the junction temperature of the switches far enough from the maximum critical junction temperature (0.7∗175°C≈120°C), which is determined by the switches datasheet [45], [46]. The desirable thermal resistances of heat sinks can be calculated by the following equation:

$$R_{th} < \frac{120 - T_a(=25^oC)}{P_{Losses}} - [R_{thJC}(=0.48) + R_{thCS}(=0.24)]. \quad (15)$$

The maximum power loss value for the switches under hard-switching condition is 3.9 W, thus

$$R_{th} < 23.64\,^{\circ}\mathrm{C}. \quad (16)$$

B. Fault Diagnosis

In this article, a simple method is presented to detect open-circuit and short-circuit faults (SCFs) of power switches. To implement the fault diagnostic system, only one additional voltage sensor is required to measure the summation of voltage across D_2 and S_2. Thus, the $V_{D2}+V_{S2} = V_{DA\text{-}SS}$ is measured by the voltage sensor. Considering the gate-driver signals of switches and the measured $V_{DA\text{-}SS}$, the type and occurrence time of the faults can be detected easily. Fig. 11 shows the different signs of $V_{DA\text{-}SS}$ values during healthy and different fault conditions. In this figure, the behavior of the $V_{DA\text{-}SS}$ signal under switch SCF, and switch open-circuit fault (OCF) is analyzed to detect the time and type of the switches faults. To detect the faults, the delayed signals of PWM pulses are used to ensure that the signals passed their transient states [47]. The conditions that the fault managing system can detect faults are also indicated in this figure. Table I summarizes these conditions. In this table, to simplify the analysis, each switch gate signal is denoted by "1" and "0" when the gate signal is high-level and low-level, respectively. According to the waveforms shown in Fig. 11 and analyses in Table I, the logical-based circuits are designed as shown in Fig. 12. When the output of each logic circuit function would be "1", the corresponding fault type can be detected.

C. Reconfiguration Strategy

After detecting the type and occurrence time of the faults, the reconfiguration strategy shown in Fig. 13 is executed. In the case of SCF of S_1 or S_2, SCFs can be cleared by fuses. After S_1 fault detection, whether fault type is open-circuit or short-circuit, the SR_1 is triggered and it would be ON forever. In the case of S_2 SCF fault, the leakage inductance current value would be high and its energy must be discharged after clearing S_2 SCF fault. Thus, SR_1 would be ON once that the fault is detected. It is not required to trigger the SR_1 in case of S_2 OCF fault. Thus, the converter can operate in reconfigured topology after faulty conditions.

V. Coupled Inductors Turns Ratio Design Considerations

The voltage and current stresses of semiconductor devices are formulated and listed in Table II. This table shows that the electrical stresses do not depend on the turns ratio in a fault condition. However, the turns ratio must be designed for healthy mode. Equations (17) and (18) present the soft switching resonance equations of the converter derived from a time interval

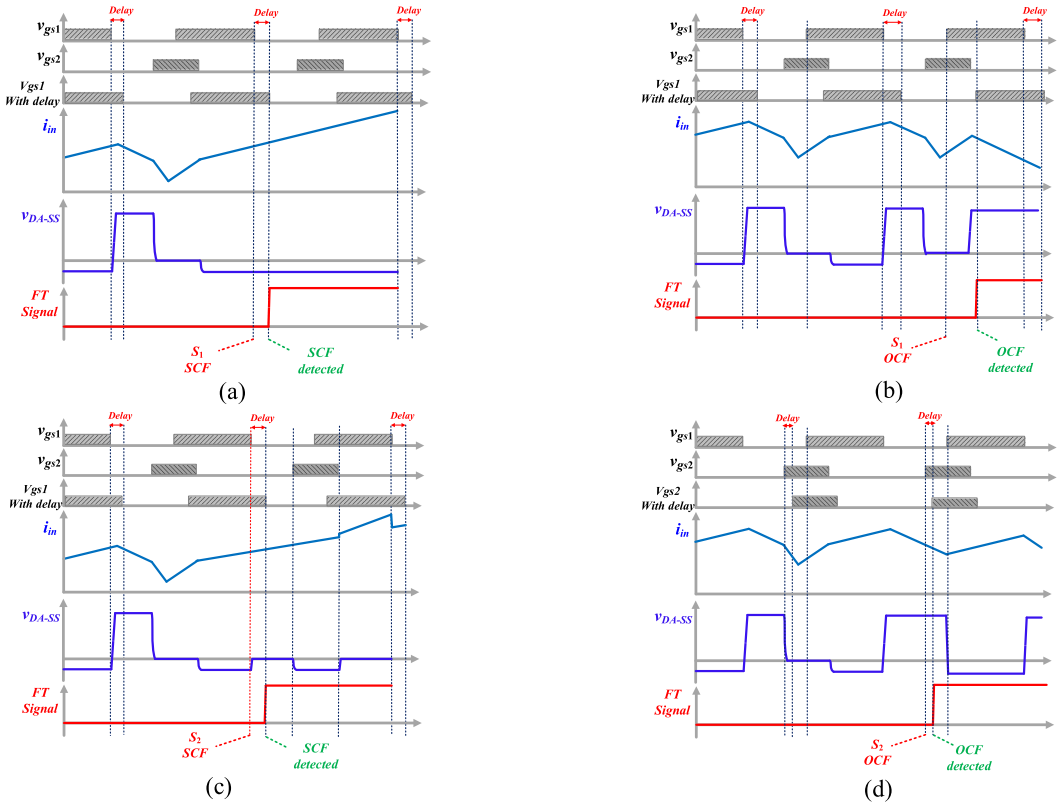

Fig. 11. Key waveforms from the healthy state to: (a) S_1 SCF, (b) S_1 OCF, (c) S_2 SCF, and (d) S_2 OCF.

TABLE I
EQUATIONS AND SIGN ANALYSES OF THE $V_{DA\text{-}SS}$ DURATION HEALTHY AND POSTFAULT CONDITIONS

Gate signals	$V_{DA\text{-}SS}$ in healthy conditions	Gate signals	$V_{DA\text{-}SS}$ in faulty conditions	
V_{gs1}: 0, V_{gs2}: 0	$V_{DA\text{-}SS}$=(1+n)V_O-nV_{in}	$V_{gs1\text{-with delay}}$: 0 , V_{gs2}: 0	S_1 is short-circuited $V_{DA\text{-}SS}\approx$ -nV_{in}	S_2 is short-circuited $V_{DA\text{-}SS}\approx$ -V_{DF}
V_{gs1}: 1, V_{gs2}: 0	$V_{DA\text{-}SS}$=-nV_{in}	$V_{gs1\text{-with delay}}$: 1 , V_{gs2}: 0	S_1 is open-circuited $V_{DA\text{-}SS}$=(1+n)V_O-nV_{in}	
V_{gs1}: 0, V_{gs2}: 1 V_{gs1}: 1, V_{gs2}: 1	$V_{DA\text{-}SS}$= -V_{DF}	V_{gs1}: 0, $V_{gs2\text{-with delay}}$: 1 , V_{gs2} :1	S_2 is open-circuited $V_{DA\text{-}SS}$=(1+n)V_O-nV_{in}	

V_{DF}: Diode forward voltage

(t_4–t_5) in Fig 2. In these equations, the turns ratio and leakage inductance participate in soft-switching conditions and increase the stresses. Thus, a tradeoff between the coupled inductors turns ratio and the value of leakage inductance must be established

$$v_{CS}(t) = \frac{n}{n+1}V_{in} + \left[-\frac{n}{n+1}V_{in} + V_O\right]\cos\omega(t-t_3) + [Z_0 I_{LM}(t_3) - Z_0(n+1)i_{LK}(t_3)]\sin\omega(t-t_3) \quad (17)$$

$$Z_0 = \frac{\sqrt{\frac{L_{LK}}{C_S}}}{n+1}, \quad \omega_0 = \frac{n+1}{\sqrt{L_{LK}C_S}}. \quad (18)$$

During the normal operating of the converter, S_1 is turned ON under ZVS condition through two steps of the resonance process (see Fig. 2). At first, when D_1 turns OFF, the voltage induced on the coupled inductors is applied to the leakage inductance and causes the leakage inductance current to increase and then discharges the C_S snubber capacitor. Thus, the voltage on the secondary side of the coupled inductors must be smaller than the output voltage

$$V_O \geq \left(\frac{2n}{1+n}\right)V_{in}. \quad (19)$$

This relation holds for any values of n>0. According to Table II, increasing the turns ratio contributes to S_2 rms current stress reduction. However, by increasing the value of n, the voltage stress of the S_2 increases. Equation (20) defines the current stress and (21) defines the voltage stress of S_2 in the normal condition. The current stress of the S_2 in normal conditions is low. Therefore, an optimum value for the turns ratio must be selected so that the voltage stress is reduced. Fig. 14 shows the relation between the turns ratio of the coupled inductors and

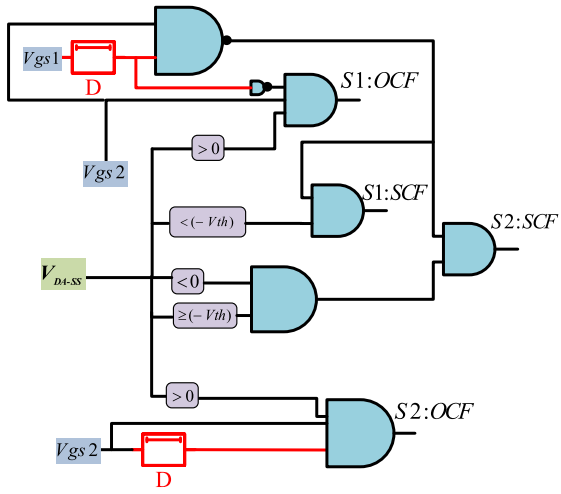

Fig. 12. Logic circuit functions of the fault-diagnostic system.

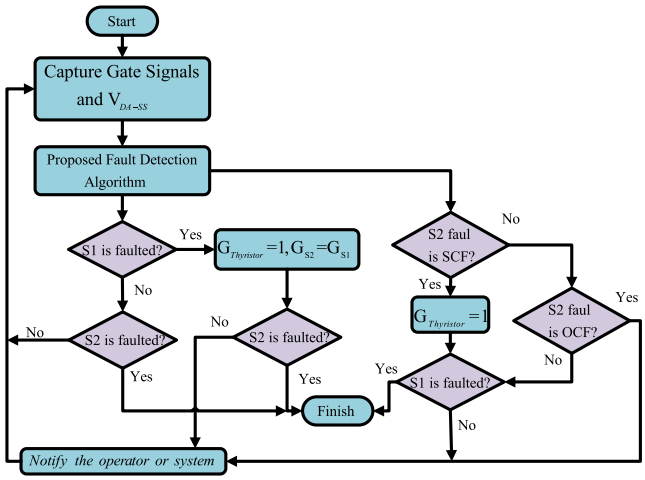

Fig. 13 Fault conditions managing diagram for the proposed converter.

TABLE II
COMPONENTS VOLTAGE AND CURRENT STRESSES

STRESSES	NORMAL MODE	FAULT MODE
S_1 voltage stress	V_o	$N.A$
S_2 voltage stress	$(1+n)V_o - nV_{IN}$	V_o
SR_1 voltage stress	V_o	V_o
D_1 voltage stress	V_o	V_o
D_2 voltage stress	nV_{in}	$0\ V$
S_1 RMS current stress	$\frac{P_{in}}{V_{in}}\sqrt{d_{S1}}$	$N.A$
S_2 RMS current stress	$(I_o + \frac{V_o}{Z_0})\sqrt{\frac{d_{S2}}{3}}$	$\frac{P_{in}}{V_{in}}\sqrt{d_{S2}}$
SR_1 average current stress	$0\ A$	$I_o(1-d_{S2})$
D_1 average current stress	$I_o(1-d_{S1})$	$0\ A$
D_2 average current stress	$\frac{1}{2}(I_o + \frac{V_o}{Z_0})d_{S2}$	I_o

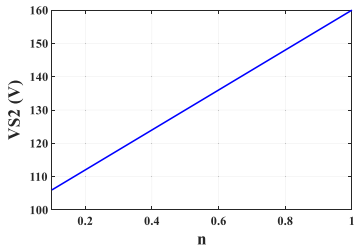

Fig. 14. Voltage stress of S_2 proportion to turn ratio in normal operating mode.

TABLE III
KEY PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Symbol	Value
L_M	150 µH
n	0.35
L_{LK}	1µH
C_1	2 nF
D_1, D_2	MUR1620
SR_1	TYN30Y-800T
S_1	IRF150P221
S_2	IRF250P225
C_L	100 µF
f_S	100 kHz
V_{in}	48 V
V_{out}	100 V

S_2 voltage

$$i_{S2\_RMS} = I_O + \frac{V_O}{Z_0}\sqrt{\frac{D_{S2}}{3}} \tag{20}$$

$$v_{S2}(t) = (n+1)V_O - nV_{in}. \tag{21}$$

VI. EXPERIMENTAL RESULTS

To confirm the theoretical analysis, a 200-W prototype of the I-ZVT-SR boost converter is implemented with specifications which are indicated in Table III. As seen in Fig. 9(a), the reliability of the soft-switching converter without fault-tolerant capability is more than the reliability of the conventional converter for f_S>83 kHz. For this reason and to have comparable experimental results, the 100 kHz switching frequency is selected.

Fig. 15 shows the experimental waveforms. Fig. 15(a) and (b) shows the waveforms of S_1 and S_2 under normal operation of the converter. And Fig. 15(c) shows that when the fault occurs and after isolation, S_2 operates similar to the main switch of the boost converter. Fig. 15(d) and (e) shows the key transition waveforms of the converter at the interval time in which a fault occurs, and then the converter continues the operation by the use of its inherent redundancy capability. As shown in Fig. 15(d) and (e), at first, the converter operates under normal conditions. Then, a fault occurs for $S_{1,}$ and S_1 is isolated from the converter. After that, S_2 continues the operation instead of S_1. To confirm the fault diagnostic system performance, the different fault detection scenarios are tested and shown in Fig. 16. According to the results, the I-ZVT-SR converter can supply the load uninterrupted under fault conditions.

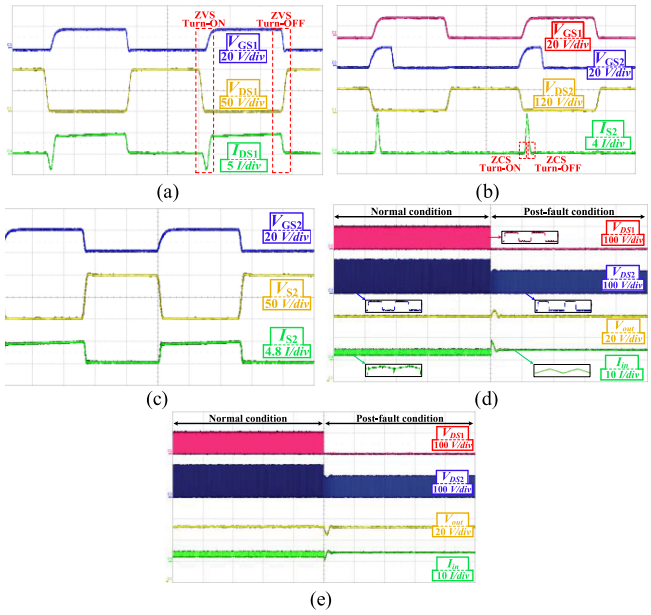

Fig. 15. Experimental waveforms (ts = time scale). (a) Operation of S_1 under soft switching condition in normal condition ($ts = 2$ μs/div). (b) Operation of S_2 under soft switching condition in normal condition ($ts = 2$ μs/div). (c) Operation of S_2 in fault condition ($ts = 2$ μs/div). (d) Transition waveforms between the normal mode and SCF mode ($ts = 5$ ms/div). (e) Transition waveforms between the normal mode and OCF mode ($ts = 5$ ms/div).

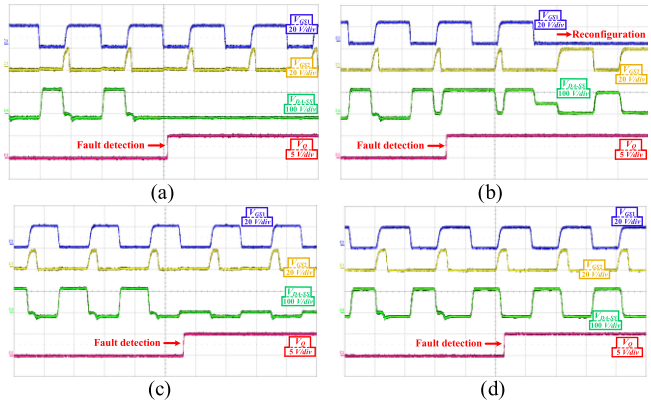

Fig. 16. Fault detection waveforms ($ts = 5$ μs/div). (a) S_1 short-circuit. (b). S_1 open-circuit. (c). S_2 short-circuit. (d). S_2 open-circuit.

VII. Comparison

A. Losses Improvement and Efficiency Evaluation

In Fig. 17, the switches losses and efficiency of the studied converters are evaluated. As mentioned, the leakage inductance in the C-ZVT converter shown in Fig. 1(a) causes power dissipation and increases voltage stress on S_2 in fault conditions. The solution to the problem is clamping the voltage of S_2 to the output voltage which can be done by a diode (I-ZVT-D) or a thyristor (I-ZVT-SR).

Clamping the voltage of S_2 in fault conditions can reduce the converter losses in three aspects. At first, when S_2 operates as the main switch, the energy of the leakage inductance can be conducted to the output. Also, the voltage of S_2, which

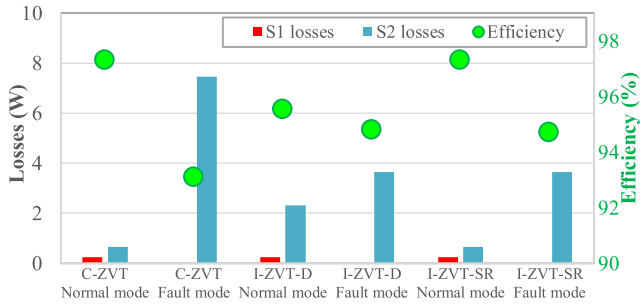

Fig. 17. Switches losses and converter efficiency in different modes.

has the most impact on the switching loss is reduced to the output voltage. And, by employing lower voltage stress switches, the MOSFETs with lower $R_{ds\cdot ON}$ can be used that reduces the conduction loss. To analysis the switches losses and efficiency of the studied converters, six cases are considered.

1) Case 1: The C-ZVT operates under normal condition.
2) Case 2: The C-ZVT operates under fault condition.
3) Case 3: The I-ZVT-D operates under normal condition.
4) Case 4: The I-ZVT-D operates under fault condition.
5) Case 5: The I-ZVT-SR operates under normal condition.
6) Case 6: The I-ZVT-SR operates under fault condition.

In cases 1, 3, and 5, the ZVT cell reduces the switching loss of the S_1 significantly. Thus, the overall losses of the S_1 are low. In case 3, due to the use of clamping diode in I-ZVT-D, S_1 operates under soft-switching condition, but soft-switching operation of the S_2 is missed. Thus, in comparison with case 1, S_2 losses are increased in case 3. However, in comparison with case 2, the S_2 losses decrease in case 4. Also, the efficiency of case 4 is better than case 2.

In I-ZVT-SR, due to the controllability of SR_1 to conduct current in different modes, the S_2 losses in case 5 are significantly decreased in comparison with case 3. Also, in case 6, the S_2 has fewer losses than case 2. As a result, by establishing a tradeoff between costs and S_2 losses, each of the studied converters can be used in different applications. Also, the power dissipation overhead on S_2 can be considered in the design of its heat sink. And in general, the I-ZVT-SR has the best efficiency and the least switches losses in both normal and fault conditions.

Also, the proposed method to use inherent redundancy properties of ZVT cell for enhancing the reliability of boost-based dc–dc converters has some advantages in comparison with the other reliability methods, such as adding redundant parallel modules to the converter. The ZVT boost converter, by changing the role of the converter components, not only provides reliability without adding extra circuits and increasing the costs but also increases the lifetime of converter switches, efficiency, and integration of the converter.

B. Performance Comparison of the Proposed Converter With Other Boost-Based Topologies

In this section, the effectiveness of the inherent redundancy of the ZVT cell on enhancing MTTF is investigated and compared with different fault-tolerant boost-based converters. To have a

TABLE IV
FEATURES COMPARISON OF THE PROPOSED CONVERTER WITH FAULT-TOLERANT BOOST BASED CONVERTERS

Converter	Efficiency		MTTF (Hours)		Number of components				
	Normal conditions	Faulty conditions	Critical $R_{th\_cr}{}^*$	$R_{th}{}^*$=8 ^{0}C/W	Switch	Diode & TRIAC& Thyristor	Capacitor	Inductor	Protection Devices
[12] (2 modules)	88.51	92.02	R_{th_cr} =12.8 MTTF=253225	383854	2	4	6	4	3 Relays
[13]	95.37	93.03	R_{th_cr} =18 MTTF=181332	380271	2	1	1	1	2 Fuses
[14]	96.18	96.18	R_{th_cr} =23.6 MTTF=148911	378562	2	1	1	1	2 Fuses
[15]	91.32	91.32	R_{th_cr} =8.9 MTTF=150295	168847	2	3	3	1	2 Fuses
Proposed Converter	97.26	94.85	R_{th_cr} =23.6 MTTF=424728	680564	2	3	1	1	2 Fuses

Critical $R_{th\_cr}{}^*$ is the maximum thermal resistance that the maximum junction temperatures of the switches are kept under 120 °C/W.

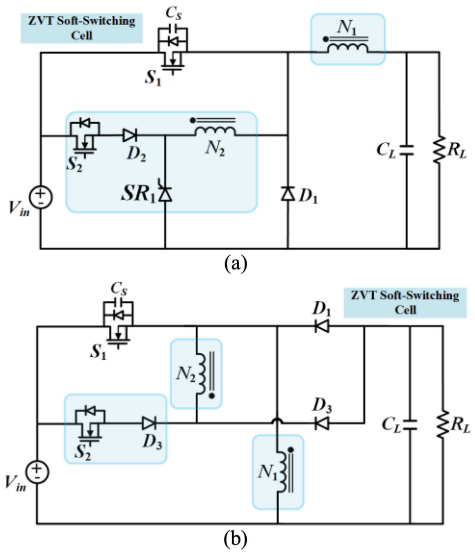

Fig. 18. Proposed family of ZVT converters with inherent redundancy property. (a) Buck converter. (b) Buck-boost converter.

fair comparison, similar conditions are considered for all studied converters as follows.

1) Input and output voltage levels, nominal power, and the switching frequency of all converters are the same.
2) In all converters, similar switches are used. In this case, the IRF250P225 switch is selected.

In Table IV, the proposed converter and other counterparts are compared in different aspects. According to the results of this table, the proposed converter has a better MTTF value than the other converters for different thermal resistance values. As a result, small-size heat sinks can be utilized. Moreover, due to soft switching operation, the proposed converter has the best efficiency in normal conditions.

VIII. FAMILY OF ZVT CONVERTERS WITH INHERENT REDUNDANCY PROPERTY

Similar to the boost converter, the ZVT technique can be applied to other basic buck and buck-boost nonisolated converters to enhance reliability, as shown in Fig. 18. In both converters, when S_1 is isolated due to the fault, S_2 can operate as the main switch of the converters and the converters can supply the load without interruption. In the buck and boost converters, to provide a discharging path for leakage inductance in a fault condition, a thyristor must be added to the converter. However, due to the topology of the buck-boost converter, it does not need to add any auxiliary thyristor. In all topologies, the theoretical operating modes are very similar to the operation of the ZVT boost converter explained in previous sections, and thus, further explanation is neglected.

It worth noting that the introduced ZVT cell can be applied to the wide range of step-up converters, which use coupled inductors in their structures [48] and enhances their reliability similar to the proposed converter.

IX. CONCLUSION

The aim of this article is to evaluate the potential of the ZVT soft-switching cell for improving the reliability of boost-based converters. Then, an improvement is applied to reduce the switches losses. In the normal condition, the ZVT cell provides soft-switching condition. And, in the fault condition, the converter is reconfigured so that the role of the ZVT cell switch is changed to operate instead of the faulty switch. The functionality of the converter under different operating modes is confirmed by experimental tests. Using the inherent properties of the ZVT boost converter, the performance of the convert in the aspects of reliability and efficiency are improved. Moreover, the circuit complexity and cost are decreased. The MTTF index shows that after the fault occurs, the converter would have a good lifetime. Also, the ZVT cell can apply to the buck, buck-boost dc–dc converters in order to improve the reliability.

It is recommended that for future research directions, the potential of the inherent redundancy property of other ZVT cells to enhance the reliability of power converters would be investigated. Another interesting research topic is to improve the performance of fault-tolerant ZVT converters by optimizing the efficiency and power density.

REFERENCES

[1] L. F. Costa and M. Liserre, "Failure analysis of the dc-dc converter: A comprehensive survey of faults and solutions for improving reliability," *IEEE Power Electron. Mag.,* vol. 5, no. 4, pp. 42–51, Dec. 2018.
[2] I. Koren and C. M. Krishna, Eds., *Fault-Tolerant Systems.* Burlington, VT, USA: Morgan Kaufmann, 2007.

[3] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.,* vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[4] T. Rahimi, S. H. Hosseini, M. Sabahi, M. Abapour, and G. B. Gharehpetian, "Three-phase soft-switching-based interleaved boost converter with high reliability," *IET Power Electron.*, vol. 10, no. 3, pp. 377–386, Mar. 2017, [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/iet-pel.2016.0211

[5] E. Pazouki, Y. Sozer, and J. A. D. Abreu-Garcia, "Fault diagnosis and fault-tolerant control operation of nonisolated DC–DC converters," *IEEE Trans. Ind. Appl.,* vol. 54, no. 1, pp. 310–320, Jan./Feb. 2018.

[6] E. Pazouki, J. A. D. Abreu-Garcia, and Y. Sozer, "A novel fault-tolerant control method for interleaved DC–DC converters under switch fault condition," *IEEE Trans. Ind. Appl.,* vol. 56, no. 1, pp. 519–526, Jan./Feb. 2020.

[7] N. Wassinger, E. Penovi, R. G. Retegui, and S. Maestri, "Open-circuit fault identification method for interleaved converters based on time-domain analysis of the state observer residual," *IEEE Trans. Power Electron.,* vol. 34, no. 4, pp. 3740–3749, Apr. 2019.

[8] T. Rahimi, L. Ding, R. Faraji, M. Kheshti, and J. Pou, "Performance improvement of a three-phase interleaved DC-DC converter without requiring anti-saturation control for post-fault conditions," *IEEE Trans. Power Electron.,* vol. 36, no. 7, pp. 7378–7383, Jul. 2021.

[9] T. Rahimi, L. Ding, M. Kheshti, and R. Faraji, "A ZVS three-phase interleaved DC-DC converter with SFM control method for the microgrid applications," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf.*, 2020, pp. 1–5.

[10] T. Rahimi, S. H. Hosseini, M. Sabahi, G. B. Gharehpetian, and M. Abapour, "Reliability evaluation of a fault-tolerant three-phase interleaved DC-DC boost converter," *Trans. Inst. Meas. Control,* vol. 41, pp. 1278–1289, Mar. 2019.

[11] S. Siouane, S. Jovanović, and P. Poure, "Open-switch fault-tolerant operation of a two-stage buck/buck–boost converter with redundant synchronous switch for PV systems," *IEEE Trans. Ind. Electron.,* vol. 66, no. 5, pp. 3938–3947, May 2019.

[12] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan, and M. Abapour, "Fault-tolerant and reliable structure for a cascaded quasi-z-source DC–DC converter," *IEEE Trans. Power Electron.,* vol. 32, no. 8. pp. 6455–6467, Aug. 2017.

[13] J. L. Soon, D. D. Lu, J. C. Peng, and W. Xiao, "Reconfigurable nonisolated DC–DC converter with fault-tolerant capability," *IEEE Trans. Power Electron.,* vol. 35, no. 9, pp. 8934–8943, Sep. 2020.

[14] E. Jamshidpour, P. Poure, and S. Saadate, "Photovoltaic systems reliability improvement by real-time FPGA-Based switch failure diagnosis and fault-tolerant DC–DC converter," *IEEE Trans. Ind. Electron.,* vol. 62, no. 11, pp. 7247–7255, Nov. 2015.

[15] Y. Zhang, L. Zhou, M. Sumner, and P. Wang, "Single-switch, wide voltage-gain range, boost DC–DC converter for fuel cell vehicles," *IEEE Trans. Veh. Technol.,* vol. 67, no. 1, pp. 134–145, Jan. 2018.

[16] M. Mohammadi, E. Adib, and M. R. Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Trans. Ind. Electron.,* vol. 62, no. 6, pp. 3473–3481, Jun. 2015.

[17] J. Kwon, W. Choi, and B. Kwon, "Single-switch quasi-resonant converter," *IEEE Trans. Ind. Electron.,* vol. 56, no. 4, pp. 1158–1163, Apr. 2009.

[18] Y. Zhao, W. Li, and X. He, "Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell," *IEEE Trans. Power Electron.,* vol. 27, no. 6, pp. 2869–2878, Jun. 2012.

[19] M. T. Outeiro, G. Buja, and D. Czarkowski, "Resonant power converters: An overview with multiple elements in the resonant tank network," *IEEE Ind. Electron. Mag.,* vol. 10, no. 2, pp. 21–45, Jun. 2016.

[20] R. Faraji, and H. Farzanehfard, "Fully soft-switched multiport DC–DC converter with high integration," *IEEE Trans. Power Electron.,* vol. 36, no. 2, pp. 1901–1908, Feb. 2021.

[21] J. P. Gegner, and C. Q. Lee, "Zero-voltage-transition converters using a simple magnetic feedback technique," in *Proc. Power Electron. Spec. Conf.*, 1994, pp. 590–596.

[22] G. Hua, C. S. Leu, and F. C. Lee, "Novel zero-voltage-transition PWM converters," in *Proc. Rec. 23rd Annu. IEEE Power Electron. Spec. Conf.*, 1992, pp. 55–61.

[23] K. Liu and F. C. Lee, "Zero-voltage switching technique in DC/DC converters," in *Proc. 17th Annu. IEEE Power Electron. Spec. Conf.*, 1986, pp. 58–70.

[24] G. Hua, E. X. Yang, Y. Jiang, and F. C. Lee, "Novel zero-current-transition PWM converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1993, pp. 538–544.

[25] J. G. Cho, J. A. Sabate, and F. C. Lee, "Novel full bridge zero-voltage-transition PWM DC/DC converter for high power applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1994, pp. 143–149.

[26] H. Guichao, L. Ching-Shan, J. Yimin, and F. C. Y. Lee, "Novel zero-voltage-transition PWM converters," *IEEE Trans. Power Electron.,* vol. 9, no. 2, pp. 213–219, Mar. 1994.

[27] H. N. Tran and S. Choi, "A family of ZVT DC–DC converters with low-voltage ringing," *IEEE Trans. Power Electron.,* vol. 35, no. 1, pp. 59–69, Jan. 2020.

[28] N. Altintaş, A. F. Bakan, and I. Aksoy, "A novel ZVT-ZCT-PWM boost converter," *IEEE Trans. Power Electron.,* vol. 29, no. 1, pp. 256–265, Jan. 2014.

[29] I. Aksoy, H. Bodur, and A. F. Bakan, "A new ZVT-ZCT-PWM DC–DC converter," *IEEE Trans. Power Electron.,* vol. 25, no. 8, pp. 2093–2105, Aug. 2010.

[30] B. Akın, "An improved ZVT–ZCT PWM DC–DC boost converter with increased efficiency," *IEEE Trans. Power Electron.,* vol. 29, no. 4, pp. 1919–1926, Apr. 2014.

[31] R. Fani, E. Farshidi, E. Adib, and A. Kosarian, "Analysis, design, and implementation of a ZVT high step-up DC–DC converter with continuous input current," *IEEE Trans. Ind. Electron.,* vol. 67, no. 12, pp. 10455–10463, Dec. 2020.

[32] B. Akhlaghi and H. Farzanehfard, "Efficient ZVT cell for interleaved DC???DC converters," *IET Power Electron.,* vol. 13, no. 10, pp. 1925–1933, Aug. 2020.

[33] B. Akhlaghi and H. Farzanehfard, "Family of ZVT interleaved converters with low number of components," *IEEE Trans. Ind. Electron.,* vol. 65, no. 11, pp. 8565–8573, Nov. 2018.

[34] B. Poorali, H. M. Jazi, and E. Adib, "Improved high step-up Z-Source DC–DC converter with single core and ZVT operation," *IEEE Trans. Power Electron.,* vol. 33, no. 11, pp. 9647–9655, Nov. 2018.

[35] M. L. S. Martins and H. L. Hey, "Self-commutated auxiliary circuit ZVT PWM converters," *IEEE Trans. Power Electron.,* vol. 19, no. 6, pp. 1435–1445, Nov. 2004.

[36] C.-M. Wang, C.-H. Su, and C.-H. Yang, "ZVS-PWM flyback converter with a simple auxiliary circuit," *IEE Proc., Electr. Power Appl.*, vol. 153, no. 1, pp. 116–122, Feb. 2006. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/ip-epa_20050123

[37] Y. Tang, H. Tong, R. Afzal, and Y. Guo, "High step-up ZVT converter based on active switched coupled inductors," *IEEE Access*, doi: 10.1109/ACCESS.2020.3041004.

[38] M. Rezvanyvardom and A. Mirzaei, "Zero voltage transition non-isolated bidirectional buck-boost DC-DC converter with coupled inductors," *IEEE J. Emerg. Sel. Topics Power Electron.*, doi: 10.1109/JESTPE.2020.2992007.

[39] R. Faraji, E. Adib, and H. Farzanehfard, "Soft-switched non-isolated high step-up multi-port DC-DC converter for hybrid energy system with minimum number of switches," *Int. J. Elect. Power Energy Syst.,* vol. 106, pp. 511–519, Jan. 2019.

[40] H. Pham, *Handbook of Reliability Engineering*. London, U.K.: Springer-Verlag, 2003.

[41] H. Tarzamni, F. P. Esmaeelnia, M. Fotuhi-Firuzabad, F. Tahami, S. Tohidi, and P. Dehghanian, "Comprehensive analytics for reliability evaluation of conventional isolated multiswitch PWM DC–DC converters," *IEEE Trans. Power Electron.,* vol. 35, no. 5, pp. 5254–5266, May 2020.

[42] *Reliability Prediction Models*: Reliability Information Analysis Center, 6000 Flanagan Rd, Suite 3, Utica, New York, NY, USA 13502-1348, RIAC-MIL- HDBK-217Plus, 2006.

[43] Y. Zhuang, F. Liu, X. Zhang, Y. Huang, X. Zha, and Z. Liu, "Short-circuit fault-tolerant topology for multiport cascaded DC/DC converter in photovoltaic power generation system," *IEEE Trans. Power Electron.,* vol. 36, no. 1, pp. 549–561, Jan. 2021.

[44] G. K. Kumar and D. Elangovan, "Review on fault-diagnosis and fault-tolerance for DC–DC converters," *IET Power Electron.,* vol. 13, no. 1, pp. 1–13, Jan. 2020.

[45] W. Martinez, C. Cortes, M. Yamamoto, J. Imaoka, and K. Umetani, "Total volume evaluation of high-power density non-isolated DC–DC converters with integrated magnetics for electric vehicles, "*IET Power Electron.*, vol. 10, no. 14, pp. 2010–2020, Nov. 2017.

[46] D. Christen, M. Stojadinovic, and J. Biela, "Energy efficient heat sink design: Natural versus forced convection cooling," *IEEE Trans. Power Electron.,* vol. 32, no. 11, pp. 8693–8704, Nov. 2017.

[47] H. Givi, E. Farjah, and T. Ghanbari, "A comprehensive monitoring system for online fault diagnosis and aging detection of non-isolated DC–DC converters' components," *IEEE Trans. Power Electron.,* vol. 34, no. 7, pp. 6858–6875, Jul. 2019.

[48] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 2, pp. 689–704, Jun. 2016.

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