An Improved Hybrid Frequency Pacing Modulation for Wireless Power Transfer Systems

Jiaqi Tang, Qianfan Zhang, *Member, IEEE*, Chao Cui, Tuopu Na, and Tengfei Hu

***Abstract*—Zero voltage switching (ZVS) techniques are widely utilized to increase efficiency and reduce electromagnetic interference of wireless power transfer (WPT) systems. Hybrid frequency pacing (HFP) is an excellent modulation method for WPT systems because it can achieve full-load range ZVS without changing the current frequency or adding auxiliary components. Another advantage of HFP is the average switching frequency reduction as decreasing output voltage so that it further reduces switching losses. This article provides an insight into the characteristics of HFP and points out that a large output ripple occurs under some reference conditions. To improve HFP, this article proposes an improved HFP (*i*HFP) method to minimize output ripple by optimally arranging the hybrid frequencies pulse sequence, but the implementation process of *i*HFP becomes more complicated. The reason for the unavoidable complicated calculation of HFP is the quantization error. In this viewpoint, this article proposes a modified sigma-delta modulation method with the quantization noise-shaping property for *i*HFP. As a consequence, the same pulse sequence can be generated by this simple modulator without complex calculations. Experimental results show that *i*HFP and Σ-Δ *i*HFP can reduce more than 60% voltage fluctuations compared with HFP. Under 0.2% input reference resolution, 66%–93% computational time reduction is achieved in going from HFP to Σ-Δ *i*HFP.**

***Index Terms*—Hybrid frequency pacing (HFP), sigma-delta modulation, wireless power transfer (WPT), zero-voltage switching (ZVS).**

I. Introduction

WIRELESS power transfer (WPT) is widely used in many applications, because of better safety and convenience and electrical isolation. Among all WPT technologies, the magnetic induction WPT technology is the most mature due to its transmission power, efficiency, and distance advantages [1], [2]. However, one of the reasons that limits WPT complete replacement of wired power transfer is lower efficiency than that by the wired one. The WPT system losses are mainly caused by coils, magnetic materials, capacitors, and converters [3]. To reduce the losses of the coupler, a lot of works have been done on the topologies and coils design [3]–[7]. Although advancements in materials technology and multilayer technology, the film capacitors are possibly replaced by the high-voltage multilayer ceramic chip capacitors (MLCC). MLCCs have extremely low equivalent series resistance so that the proportion of capacitor losses in the total losses is almost negligible.

Increasing the resonant frequency can dramatically improve the performance of the WPT coils, but the switching losses of converters limit the performance of systems. The main switching losses occur in the transmitter-side inverter. The pulsewidth modulation (PWM), also called phase-shift control in the full-bridge inverter, is widely used to regulate the output power of the transmitter, but this method perform hard-switching on the power devices, which reduces the inverter efficiency [9]. Even if wide bandgap power devices have lower output capacitance and reverse recovery charge, the soft-switching technique is still the most effective way to reduce switching losses.

The pulse frequency modulation (PFM) method adjusts the switching frequency in the range above the resonant frequency to achieve zero voltage switching (ZVS), but the whole system efficiency is relatively low under light load due to the increase in the current frequency [10], [11]. A combination of PWM and PFM methods is proposed to guarantee ZVS conditions in the literature. The complicated current phase feedback control is necessary for these methods. The pulse density modulation can achieve ZVS without the current frequency changed, but an additional passive branch for an inverter is added [12]. The ON-OFF keying modulation, another method does not change the current frequency, uses a low-frequency modulation signal to regulate output power, which enlarges the output ripple.

The hybrid frequency pacing (HFP) is an excellent modulation method for WPT systems, which can achieve ZVS operation without changing current frequency or adding auxiliary components [16], [17]. Compared with similar ON-OFF keying modulation, the HFP has a lower output ripple due to the shorter modulation periods. Another advantage is that the HFP can reduce average switching frequency as decreasing the output ratio, so that it further reduces switching losses. However, a characteristic of HFP is that the minimum modulated numbers of half-cycles will increase as the output ratio resolution increases, so the long pulse sequence causes a large output ripple.

To improve HFP, this article gives a detailed theoretical analysis of HFP and finds that the arrangement of pulse sequence can affect the output ripple, even if the pulse sequences have

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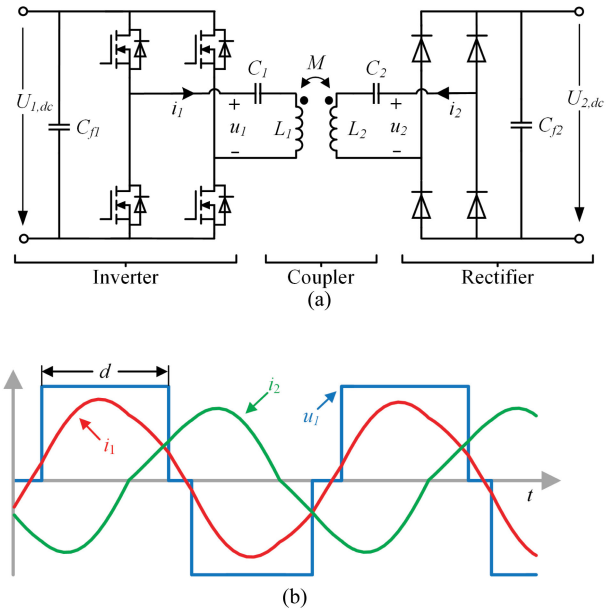

Fig. 1. (a) Series–series compensated WPT system with a full-bridge inverter comprising MOSFETs and a diode rectifier. (b) Calculated waveforms of the WPT system for duty cycle $d = 0.8$.

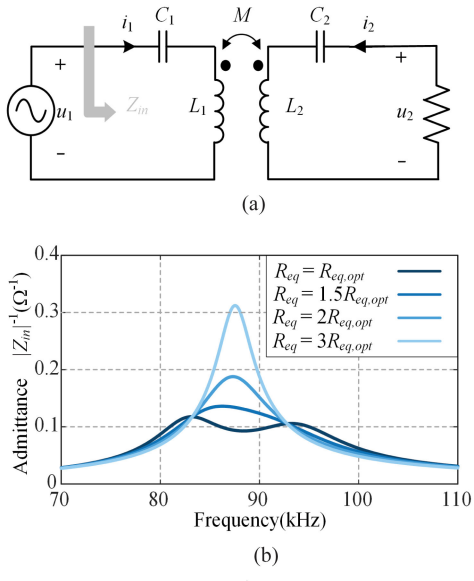

Fig. 2. (a) Equivalent circuit of a series–series compensated WPT system. (b) Magnitude of the input admittance is shown for different values of the equivalent load resistance.

the same minimum modulated numbers. Therefore, this article proposes an improved method for HFP to minimize the output ripple, which is achieved by the optimal frequencies arrangement and denominated as improved HFP (*i*HFP). However, the implementation process of *i*HFP becomes more complicated than HFP. Furthermore, HFP and *i*HFP have the uncertain times of division operations and program loops that are hard to fulfill high-frequency interrupt applications of the WPT systems.

In fact, the reason of the unavoidable complicated calculation is from the quantization error of HFP. In this viewpoint, a sigma-delta (Σ-Δ) modulation method to realize *i*HFP is proposed in this article. The advantage of this method is that the hybrid frequency pulse sequence is automatically generated by a few of basic function blocks so that it is easy to implement by the microcontroller of power electronics.

This article is structured into five sections. In Section II, the fundamental principles and the typical frequency characteristic of series–series compensated WPT systems are given. A detailed description of the operating principles and an improved method for HFP to reduce the output ripple are presented. In Section III, the basic principles of Σ-Δ modulator are reviewed and a modified Σ-Δ modulation method for *i*HFP is proposed. Section IV validates the proposed Σ-Δ modulation method for the HFP. Finally, Section V concludes this article.

II. HFP WPT System

A. Series–Series Compensated WPT System

A typical series–series compensated WPT system with a full-bridge inverter comprising MOSFETs and a diode rectifier is shown in Fig. 1(a). L_1 and L_2 are the self-inductances of the coupler. The mutual inductance M transfers the power from transmitter side to receiver side. The parasitic resistances of the coils are neglected because they have little effect on the waveforms.

PWM is the most widely used control scheme for full-bridge inverters. The inverter is operating at the resonant frequency f_0 of two *L*-*C* resonators, where

$$f_0 = \frac{1}{2\pi\sqrt{L_1C_1}} = \frac{1}{2\pi\sqrt{L_2C_2}} \tag{1}$$

The waveforms of inverter output voltage u_1 and the currents i_1 and i_2 of resonators are depicted in Fig. 1(b). Apparently, the duty cycle d can regulate the output voltage u_1. The Fourier series of u_1 is

$$u_1(t) = \frac{4U_{1,\mathrm{dc}}}{\pi}\sum_n \frac{1}{n} sin\left(\frac{n\pi d}{2}\right)\sin(2\pi f_0 t), \quad n = 1, 3, 5, \ldots, . \tag{2}$$

The currents i_1 and i_2 are almost sinusoidal wave due to the bandpass characteristics of the WPT system with the input impedance Z_{in}. To analyze the bandpass characteristics, the equivalent circuit of the WPT system is shown in Fig. 2(a). The output voltage $U_{2,\mathrm{dc}}$ and output power can be modeled by the equivalent resistance R_{eq} with

$$R_{\mathrm{eq}} = \frac{8}{\pi^2}\frac{U_{2,\mathrm{dc}}^2}{P_{\mathrm{out}}}. \tag{3}$$

To achieve maximum transmission efficiency of the WPT system, the equivalent resistance R_{eq} at rated load is approximately

equal to [3]

$$R_{\mathrm{eq,opt}} \approx k\omega_0 L_2 \tag{4}$$

where k is the coupling factor and ω_0 is the switching angular frequency. So, the condition $R_L < R_{\mathrm{eq,opt}}$ applies to the full load range.

Using the equivalent circuit model of Fig. 2(a), the circuit equations for the series-series (SS)-compensated WPT system are expressed as

$$\left(j\omega L_1 + \frac{1}{j\omega C_1}\right) i_1 + j\omega M i_2 = u_1 \tag{5}$$

$$j\omega M i_1 + \left(j\omega L_2 + \frac{1}{j\omega C_2} + R_{\mathrm{eq}}\right) i_2 = 0. \tag{6}$$

The transmitter-side input impedance Z_{in} can be derived as

$$Z_{\mathrm{in}} = \left(\frac{1}{j\omega C_1} + j\omega L_1\right) + \frac{\omega^2 M^2}{R_{\mathrm{eq}} + j\omega L_2 + 1/j\omega C_2}. \tag{7}$$

The magnitude of the input admittance is shown in Fig. 2(b) for different values of the equivalent load resistance R_{eq} according to (7). The curves show that only the harmonic components around the resonant frequency f_0 are contained in the inverter output current. Therefore, the bandpass characteristics of WPT systems can be utilized to achieve ZVS by HFP, and it will be given in the next paragraph.

B. Principle of HFP

The duty cycle d of PWM can be used to regulate the inverter output voltage u_1, but the hard-switching occurs in one half-bridge as d decreases. In contrast, HFP can maintain full-range ZVS operation. To give a more comprehensible explanation of HFP, this article proposes another representation of HFP, which is little different from that proposed in [16] and [17].

The control scheme of HFP is the operation at a constant duty cycle $d = 1$ and the different frequencies f_n to guarantee ZVS condition. So, the voltage waveform is a square wave, and the Fourier series of u_1 is

$$u_1(t) = \frac{4U_{1,\mathrm{dc}}}{\pi} \sum_n \frac{1}{n} \sin(2\pi n f t), \quad n = 1, 3, 5, \ldots, . \tag{8}$$

Suppose that only the harmonic components at the resonant frequency f_0 can generate current due to the aforementioned bandpass characteristic of WPT systems. Hence, the square wave at frequencies f_n can be selected to regulate the inverter output voltage, where

$$f_n = \frac{1}{T_n} = \frac{1}{n} f_0, \quad n = 1, 3, 5, \ldots, . \tag{9}$$

So, the square wave at frequencies f_n contains the component of harmonic frequency f_0 equal to

$$u_{1(1)} = \frac{4U_{1,\mathrm{dc}}}{n\pi}, \quad n = 1, 3, 5, \ldots, \tag{10}$$

where $u_{1(1)}$ denotes the harmonic components of the output voltage at f_0.

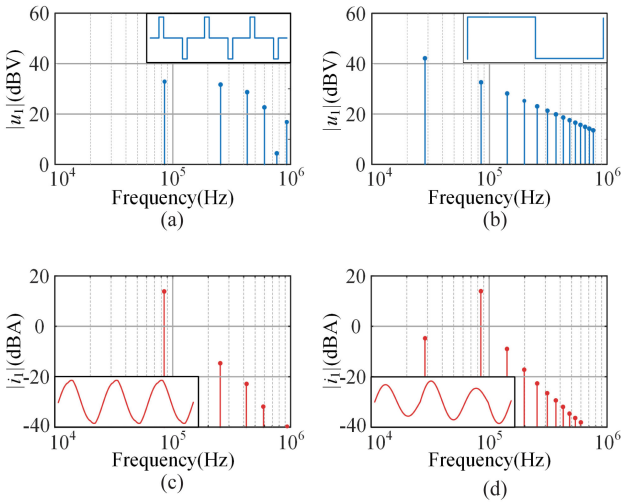

Fig. 3. Spectrums and waveforms of the output voltage $u_{1(1)} = 4U_{1,\mathrm{dc}}/(3\pi)$. (a) PWM. (b) HFP. Spectrums and waveforms of the inverter output current i_1 (c) PWM and (d) HFP.

Fig. 3(a) and (b) depicts the spectrums and waveforms of the output voltage $u_{1(1)} = 4U_{1,\mathrm{dc}}/(3\pi)$ regulated by PWM at frequency f_0 and HFP at frequency f_3. The spectrums of the transmitter current i_1 are given in Fig. 3(c) and (d). It is shown that the harmonic components of currents at the resonant frequency f_0 are equal, which are regulated by PWM and HFP. The other harmonic components of currents are more than 20 dBA lower that the harmonic components at f_0 because of the bandpass characteristic of the WPT system. Thus, the currents are almost sinusoidal wave.

According to (10), the resolution of output voltage by the HFP is too low when only one frequency is used. Combining different frequencies f_n into a pulse sequence is a way to increase the resolution of the average output voltage. To minimize the pulse sequence and the output ripple, HFP utilizes the half-cycles of different frequencies. For example, HFP involves two frequencies of f_1 and f_3 and combines them into a new pulse sequence and N_1 and N_3 denote the numbers of half-cycles of switching frequencies f_1 and f_3. So, the total pulse length is $T_p = (N_1 + 3N_3)T_0/2$ and the average output voltage of pulse sequence can be derived as

$$\overline{u_{1(1)}} = \frac{1}{T_p} \int_0^{T_p} u_{1(1)} dt = \frac{N_1 + N_3}{N_1 + 3N_3} \frac{4U_{1,\mathrm{dc}}}{\pi}. \tag{11}$$

The normalization output ratio δ can be used to denote the harmonic components of the average output voltage at f_0

$$\overline{u_{1(1)}} = \frac{4U_{1,\mathrm{dc}}}{\pi} \delta. \tag{12}$$

It is must be noted that (11) has multiple solutions and the numbers N_1 and N_3 are natural numbers. Thus, the minimum

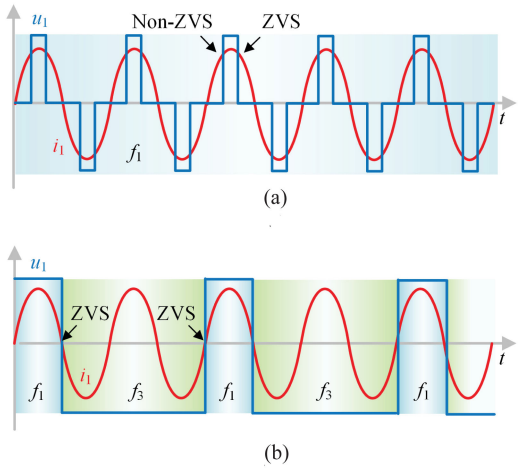

Fig. 4. Ideal voltage and current waveforms for the full-bridge inverter ($\delta = 0.5$). (a) PWM for duty cycle $d = 1/3$. (b) HFP for $N_1 = 1$ and $N_3 = 1$.

solution of (11) can minimize the pulse sequence and output ripple [16].

Fig. 4 depicts the ideal voltage and current waveforms for the full-bridge inverter ($\delta = 0.5$) under PWM for duty cycle $d = 1/3$ and HFP for $N_1 = 1$ and $N_3 = 1$. It is shown that hard-switching occurs in one half-bridge under PWM and the switching transition is always with zero current under HFP. Therefore, HFP also maintains a full-range ZVS against the variable output ratio δ. In practice, hard-switching also occurs if the switching transition is with zero current, because the output capacitances C_{oss} of MOSFETs need to be charged or discharged. If the current is insufficient to charge the output capacitances C_{oss} completely during the dead time interval, a part of energy stored in C_{oss} will dissipate. This case is named as incomplete ZVS [18]. Thus, to achieve ZVS, the input impedance of transmitter side must exhibit an inductive behavior.

Equation (11) can be extended to general form for a pulse sequence combined with different frequencies f_n, and the ratio δ is equal to

$$\delta = \frac{\sum_n N_n}{\sum_n nN_n}, \qquad n = 1, 3, 5, \ldots, \tag{13}$$

where N_n represents the numbers of half-cycles of switching frequencies f_n.

Another advantage of HFP is the average switching frequency reduction as decreasing output ratio, so that it further reduces switching loss. The average switching frequency $f_{\text{sw,avg}}$ can be derived as

$$f_{\text{sw,avg}} = \delta f_0. \tag{14}$$

The output ripple of HFP can be minimized by reducing the pulse sequence period, and the period depends on the modulated numbers of half-cycles N_n. The process for obtaining the shortest hybrid frequency pulse sequence for any given δ will be given here.

The modulated numbers of half-cycles N_n are calculated using (13). Suppose that HFP utilizes two switching frequencies of f_1 and f_3 and the range of the reference output ratio is $1/3 < \delta < 1$.

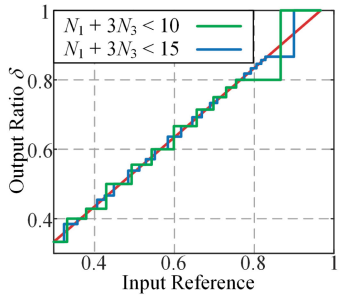

Fig. 5. Output ratio of all possible combinations for $N_1 + 3N_3 < 10$ and $N_1 + 3N_3 < 15$.

To get the integer solution, δ can be rewritten into fraction form with δ=2p/2q, where p and q are integers. The solution of (13) is

$$\begin{cases} N_1 = 3p - q \\ N_3 = q - p. \end{cases} \tag{15}$$

Equation (15) is not the minimum solution and it is easy to be demonstrated that the condition for the shortest sequence is N_1 and N_3 are coprime. The minimum solution can be obtained by finding the greatest common divisor of N_1 and N_3. It is a common question that can be solved by several methods, such as the long division method and Euclid's division algorithm [19].

The period of HFP T_{HFP} depends on the sum of N_n. If $N_1 + N_3$ is odd, the minimum HFP period T_{HFP} can be expressed as $T_{\text{HFP}} = N_1T_1 + N_3T_3$; if $N_1 + N_3$ is even, it can be expressed as $T_{\text{HFP}} = (N_1T_1 + N_3\ T_3)/2$ according to the half-cycle symmetrical characteristic.

The length of the hybrid frequency pulse sequence depends on the resolution of the reference δ. The output ratio of all possible combinations for $N_1 + 3N_3 < 10$ and $N_1 + 3N_3 < 15$ are shown in Fig. 5. The output step is not uniform, and the maximum step occurs around $\delta = 1$, where N_1 increases significantly for a certain resolution.

C. Improved HFP (iHFP)

A characteristic of HFP is that the output ripples may vary as the frequencies arrangement in the pulse sequences, even if two pulse sequences have the same minimum modulated numbers.

For instance, the voltage and current waveforms under original HFP for $N_1 = 7$, $N_3 = 2$, and $\delta = 9/13$ are depicted in Fig. 6(a). As a contrast, the waveforms of the pulse sequence with the same modulated numbers after another arrangement are depicted in Fig. 6(b), so they have the same output ratio. Apparently, the arrangement shown in Fig. 6(b) is better because the amplitude ripple of current under the original HFP is significantly larger.

The amplitude ripple of current i_1 is the beats phenomenon, which means that the harmonic components near the resonant frequency are large. Fig. 7(a) depicts the output voltage spectrum comparison between the two arrangements of HFP shown in Fig. 6. It shows that the components at f_0 under the different arrangements are equal, which proves that the arrangement does not affect the output ratio δ. However, the harmonics near f_0 are

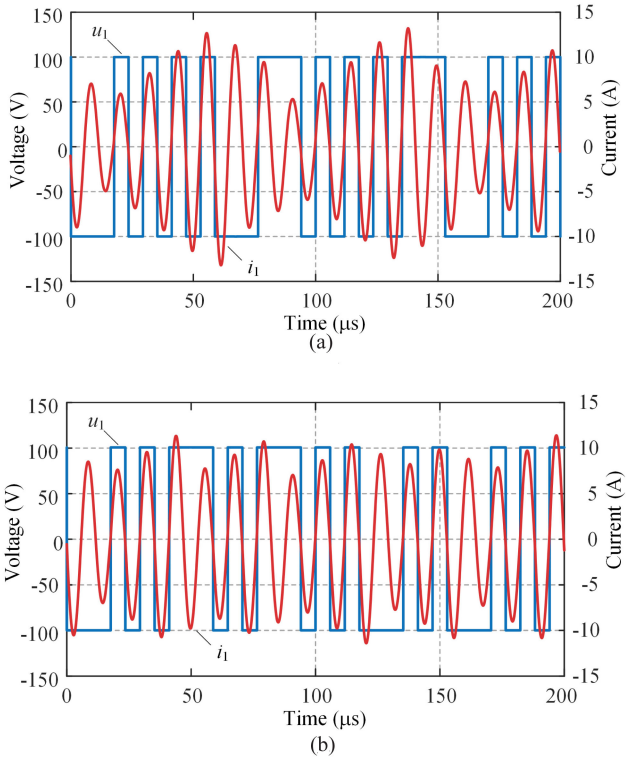

Fig. 6. Waveforms of voltage and current under HFP for $N_1 = 7, N_3 = 2$, and $\delta = 9/13$. (a) Original HFP without arranging. (b) Optimal arrangement.

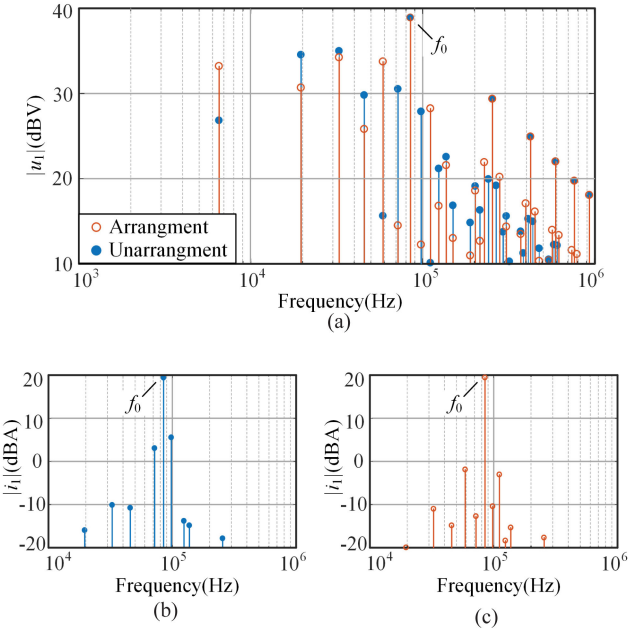

Fig. 7. (a) Output voltage spectrums comparison between the two arrangements of HFP. Spectrums of output currents under the two arrangements of HFP. (b) Original HFP without arranging. (c) Optimal arrangement.

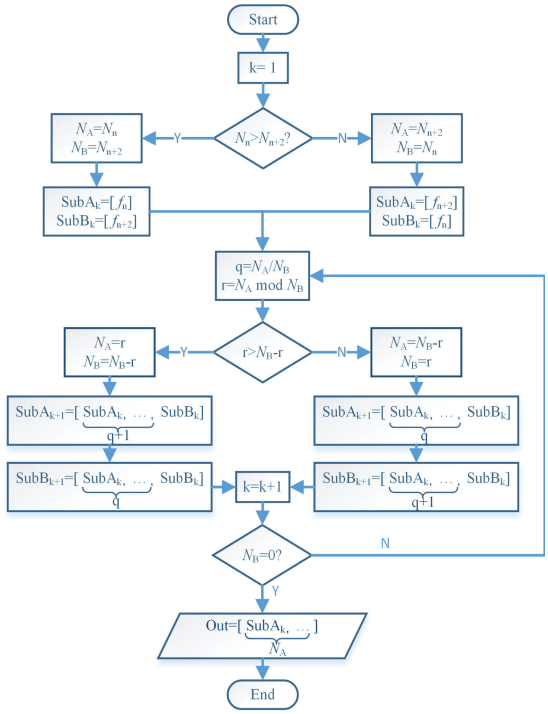

Fig. 8. Algorithm of proposed *i*HFP.

significantly different. The harmonics can be pushed far away from f_0, and the bandpass characteristics of the WPT system can filter them. Therefore, the current i_1 has a less dominant harmonic and output ripple after the optimal arrangement. The spectrums of output currents under the two arrangements of HFP are shown in Fig. 7(b) and (c).

According to this principle, an improved method for HFP to reduce the output ripple is proposed. The method is based on the optimal frequency arrangement and denominated as improved HFP (*i*HFP). The optimal frequency arrangement aims to interleave the two frequencies half-cycles. Furthermore, the local subsequence also needs to be interleaved.

This article proposes an arranging algorithm to achieve *i*HFP on microcontrollers, which is shown in Fig. 8. To explain this algorithm, the process instance for $N_1 = 11$ and $N_3 = 7$ is shown in Fig. 9. Although the input N_n is not the minimum solution of (13), the output pulse sequences are the same. Thus, calculating the minimum solution can be avoided in the proposed *i*HFP.

III. Sigma-Delta *i*HFP

HFP can realize the full-range ZVS and the proposed *i*HFP can reduce output ripple with the same ZVS condition. However, we are still not satisfied with them, because the implementation processes are not very suitable for microcontrollers owing to uncertain times of division operations and program loops. Especially, they are hard to fulfill the high-frequency interrupt application of WPT systems. So, this article aims to propose a simple modulation method that has the same performance as *i*HFP.

The aforementioned complex implementation processes of HFP and *i*HFP stem from the low output resolution using only one frequency. In other words, the quantization error is too big when only one frequency is utilized to regulate the output voltage. Unless some closed-loop control methods are applied

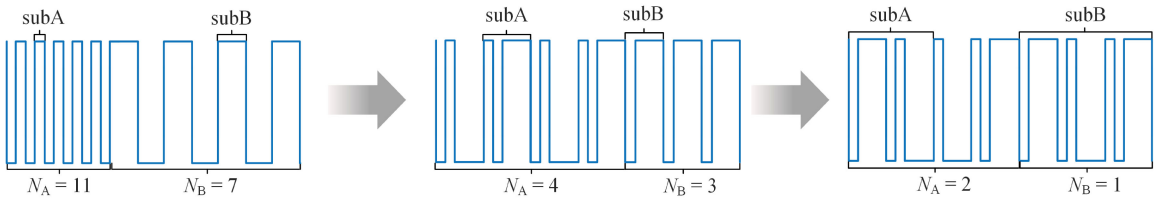

Fig. 9. Pulse sequence arranging progress of *i*HFP for $N_1 = 11$ and $N_3 = 7$.

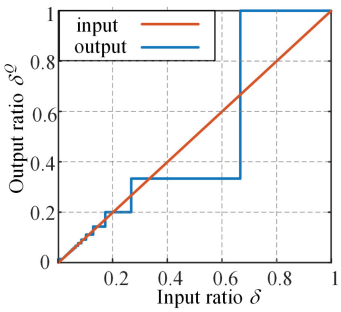

Fig. 10. Quantization error using one f_n.

such as hysteresis control, the complex calculation and sorting for averaging the output voltage have to be executed to increase the output resolution.

Σ-Δ modulation is a cost-effective technique, which is widely used for analog to digital (ADC) converters. Σ-Δ ADC requires only a 1-b comparator, but it can produce more than 16-b resolution. Σ-Δ modulation is based on oversampling techniques and noise shaping techniques. Oversampling can increase the resolution by oversampling the signal and subsequently low-pass filtering it. Noise shaping is a technique by which the feedback architecture allows the input signal to pass through, but the quantization noise is pushed out of the signal baseband by a high-pass filter [20]. Consequently, the output resolution can be increased by Σ-Δ modulation.

Some characteristics of WPT systems and HFP are similar to Σ-Δ ADC, so that the Σ-Δ modulation technique can be utilized to improve the HFP by some modification. First, the Nyquist frequency of the reference signal of the inverter output voltage is much less than the resonant frequency, so that the reference signal is oversampled. Second, the output resolution is low at only one frequency of HFP, and the noise shaping technique can reduce the quantization noise at low frequency. Last of all, the WPT system has low-pass characteristics from the transmitter voltage input to the receiver voltage output, which can filter the high-frequency quantization noise [21].

Because the harmonic components at the frequencies f_0 of HFP are used to regulate the output voltage, the quantization error using one f_n is shown in Fig. 10. HFP quantized output δ^Q is given by

$$\delta^Q = \delta + e \tag{16}$$

where e is the quantization error. The interval between successive levels is called the quantization step size. Therefore, the

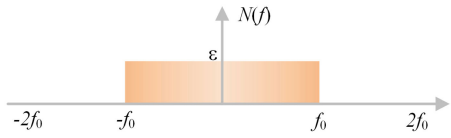

Fig. 11. Power spectral density of quantization error.

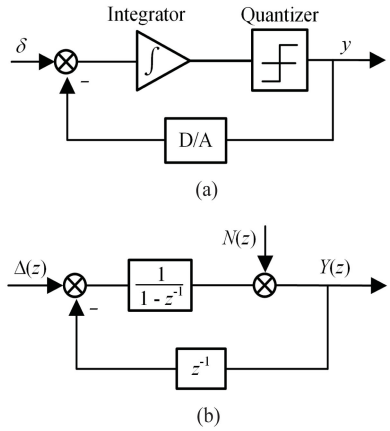

Fig. 12. (a) Classical first order Σ-Δ modulator. (b) z-domain analysis of Σ-Δ modulator.

quantization step size is nonuniformity and depends on the range of reference δ. Based on (10), the quantization step size q_n is given by

$$q_n = \frac{1}{n} - \frac{1}{n+2} \qquad n = 1, 3, 5, \ldots, . \tag{17}$$

It is generally assumed that the quantization error is random so that as discussed in [22] and [23], the noise power spread over the entire frequency range equally, which is shown in Fig. 11. The level of the power spectral density ε of quantization error at sampling frequency f_s can be given by

$$\varepsilon = \frac{q_n^2}{12 f_s}. \tag{18}$$

The classical first-order Σ-Δ modulator is shown in Fig. 12(a); it comprises a single-bit quantizer, an analog integrator, and a single-bit digital-to-Analog Converter (DAC). The discrete model can be represented in Fig. 12 (b). Therefore, the transfer function can be expressed as

$$Y(z) = \Delta(z) + \left(1 - z^{-1}\right) N(z) \tag{19}$$

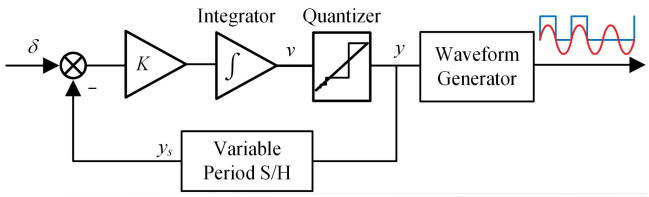

Fig. 13. Proposed Σ-Δ modulator structure for *i*HPF.

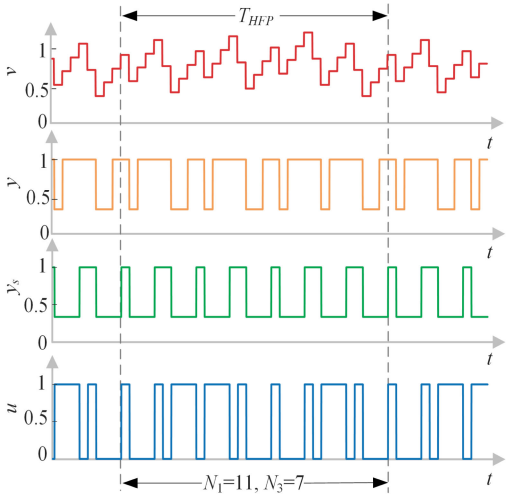

Fig. 14. Waveforms of the proposed Σ-Δ *i*HPF for $\delta = 7/16$.

where $\Delta(z)$, $N(z)$, and $Y(z)$ are the z-transforms of the reference, quantization noise, and output signals, respectively. It is clear that the modulator high-pass filters the quantization noise and does not change the reference signal. In other words, the modulator pushes the quantization noise into a higher frequency band [24]. As a result, the noise density at low frequency is decreased and the high-resolution reference signal can be extracted by a low-pass filter.

According to the principle of the Σ-Δ modulator, this article proposes a Σ-Δ modulator structure for *i*HPF, which is depicted in Fig. 13. Compared with the classical Σ-Δ modulator, the quantizer is nonuniform as shown in Fig. 10. The variable period sample and hold unit sample the value y and the duration T_s for holding the sample is variable, which can be given by

$$T_s = \frac{1}{2yf_0}. \tag{20}$$

The function of the waveform generator is output level toggle after period T_s, whereby the output value y is converted into the drive signal of the inverter. The gain K can regulate the filter characteristic of the Σ-Δ modulator. The simple structure of Σ-Δ *i*HFP can be easily implemented on a microcontroller unit. Σ-Δ *i*HFP can also run on a field-programmable gate array using a hardware description language (HDL). Thus, designing an application-specific integrated circuit for Σ-Δ *i*HFP is also feasible.

Fig. 14 shows the waveforms of the proposed Σ-Δ HFP modulator for the case of $\delta = 7/16$. According to noise shaping ability of proposed modulator, the modulated numbers of half-cycles

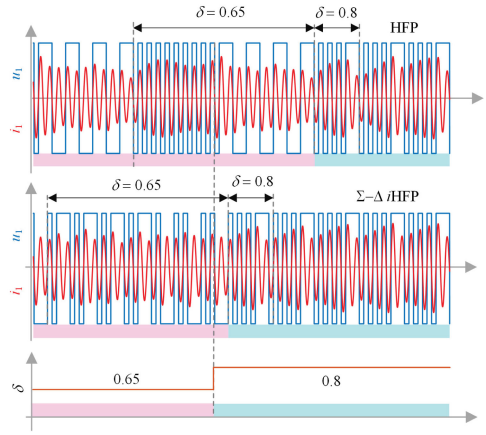

Fig. 15. Step response waveforms from δ=0.65 to δ=0.8 under HFP and Σ-Δ *i*HFP.

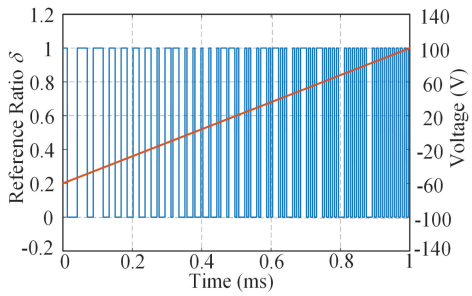

Fig. 16. Waveforms of the proposed Σ-Δ *i*HPF for a ramp reference.

N_n is the minimum solution, which is equal to the calculated result of HFP. Furthermore, the pulse sequence can be arranged optimally without complicated operations as the *i*HFP. Σ-Δ *i*HFP is only with several basic blocks, thus, it is very suited for various microcontrollers and high-speed interrupt WPT systems. The output of Σ-Δ HFP can be regulated at any time, unlike HFP and *i*HFP that need to wait until the end of a whole HFP period. Fig. 15 shows the step response waveforms from δ= 0.65 to δ= 0.8 under HFP and Σ-Δ *i*HFP. Because the reference step occurs at the intermediate stage of a HFP period, the valid output is regulated until the end of this HFP period. As a contrast, the response delay of Σ-Δ *i*HFP is short because of the interleaved pulses. Thus, the minimum update period of the reference δ is T_{HPF} for HFP, but it is T_s for Σ-Δ *i*HFP. The waveforms of δ and inverter output voltage u_1 for Σ-Δ HFP are illustrated in Fig. 16 when the reference is a ramp.

IV. Experimental Verifications

Based on the above-mentioned analysis and design, a prototype is implemented to verify the proposed *i*HFP and Σ-Δ *i*HFP. The system is shown in Fig. 17. The system parameters are listed in Table I. The resistance of transmitter and receiver coils is shown in Fig. 18.

To compare HFP and PWM, the inverter should have the ability to suffer hard-switching. The inverter was built with 200 V MOSFETs (IXFH80N20Q) at the dc-link voltage of 100 V. The

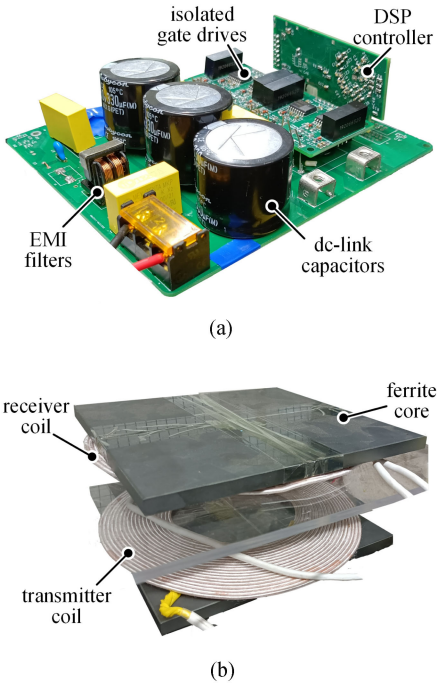

Fig. 17. Prototype WPT system. (a) Transmitter full-bridge inverter. (b) WPT coils.

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE PROTOTYPE.

Symbol	Description	Value
L_1	Transmitter coil inductance	131.1uH
L_2	Receiver coil inductance	124.0uH
C_1	Transmitter compensated capacitance	27.4nF
C_2	Receiver compensated capacitance	27.8nF
f_T	Transmitter resonant frequency	84.0kHz
f_R	Receiver resonant frequency	85.7kHz
R_L	Rated load resistor	20Ω
M	Nominal mutual inductance	34.2uH
d_1,d_2	Coils diameter	20cm
$d_{1\text{-}2}$	Coils distance	10cm
C_{f2}	Rectifier filter capacitance	20uF
$U_{1,dc}$	DC link voltage	100V

TABLE II
EXECUTION TIME IN CPU CYCLES

δ resolution	HFP	*i*HFP	Σ–Δ *i*HFP
1%	150-400	1000 - 20000	50
0.2%	150-800	1000 - 100000	50

rectifier is composed of four Schottky diodes (DSA120C150QB) to achieve high performance.

Table II shows the comparison of the approximated execution time in CPU cycles. The programs are implemented on DSP (TMS320F28377S) by C language. The program execution time of HFP and *i*HFP is a range which depends on the value and resolution of δ. Σ-Δ *i*HFP has a relatively fixed execution time

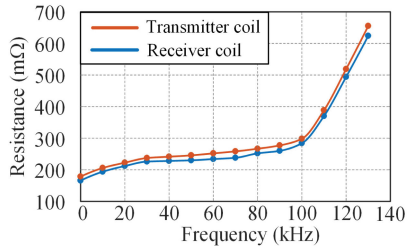

Fig. 18. Resistance of transmitter and receiver coils.

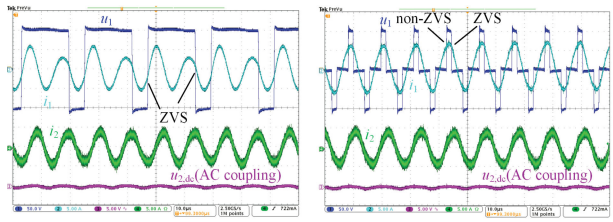

Fig. 19. Measured waveforms of a WPT system for $\delta = 0.5$. (a) HFP. (b) PWM. The waveforms of *i*HFP and Σ-Δ *i*HFP are same as that for HFP for $\delta = 0.5$. Scales: u_1 =50 V/div, i_1 = 5 A/div, $u_{2,\mathrm{dc}}$ = 5 V/div (ac coupling), i_2 = 5 A/div, time = 10 μs/div.

which is shorter than HFP and *i*HFP, so Σ-Δ *i*HFP is more suitable for microcontroller applications.

Fig. 19 shows the measured waveforms of the inverter output voltage u_1, transmitter coil current i_1, and output dc voltage $u_{2,\mathrm{dc}}$ ($\delta = 0.5$) under PWM for duty cycle $d = 1/3$ and HFP for $N_1 = 1$ and $N_3 = 1$. The waveforms of *i*HFP and Σ-Δ *i*HFP are the same as of HFP with output ratio $\delta = 0.5$. The output dc voltage $u_{2,\mathrm{dc}}$ is with a large dc offset. To measure the ripple of $u_{2,\mathrm{dc}}$ accurately, ac coupling mode on the oscilloscope channel 3 (purple line) is enabled to filter the dc component. The ZVS condition cannot be maintained as reducing duty cycle d under PWM. However, HFP maintains ZVS and reduces the equivalent switching frequency, which further improves the efficiency of the inverter. The only cost is increasing the current ripple.

The advantage of ripple reduction of *i*HFP and Σ-Δ HFP occurs at large N_n. For instance, for the reference ratio δ= 0.7, the optimal solution of HFP is $N_1 = 11$ and $N_3 = 3$. The measured waveforms for HFP are shown in Fig. 20(a). The peak-to-peak voltage of $u_{2,\mathrm{dc}}$ is 5 V. After optimal arrangement by *i*HFP, the peak-to-peak voltage of $u_{2,\mathrm{dc}}$ is reduced to 2 V, which is shown in Fig. 20(b). Σ-Δ *i*HFP can reduce the current fluctuations as well. The peak fluctuation (maximum peak minus minimum peak) of i_1 is reduced from 9 to 4 A and the peak fluctuation of i_2 is reduced from 8 to 3 A, which are shown in Fig. 20(c) and (d). When the reference ratio $\delta = 0.65$, the optimal solution of HFP is $N_1 = 19$ and $N_3 = 7$. The fluctuation of $u_{2,\mathrm{dc}}$ is reduced more than 60%. The current fluctuations are also reduced obviously. The waveforms of Σ-Δ *i*HFP are the same as that for HFP but the implementation procedure is easier. The spectrums of output currents i_1 for $\delta = 0.7$ are shown in Fig. 21. The frequency-domain analysis of current i_1 indicates that the dominant harmonics of Σ-Δ *i*HFP and *i*HFP are less than HFP so that the proposed methods reduce the output ripple.

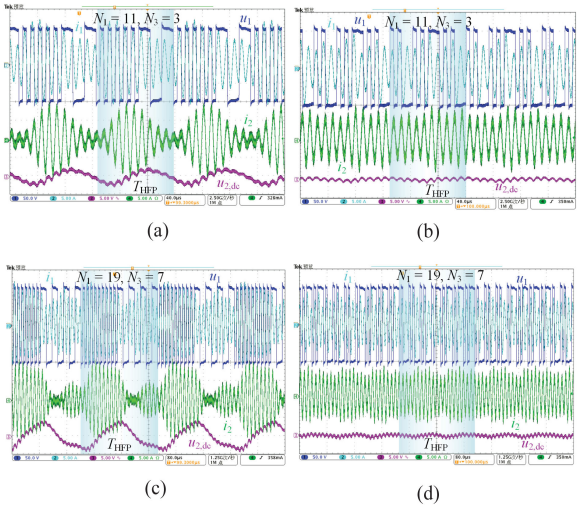

Fig. 20. Measured waveforms of the WPT system. (a) HFP and (b) *i*HFP and Σ-Δ *i*HFP. ($\delta = 0.7$) Time scale = 40 μs/div. (c) HFP. (d) *i*HFP and Σ-Δ *i*HFP. ($\delta = 0.65$) Time scale = 80 μs/div. Scales: $u_1 = 50$ V/div, $i_1 = 5$ A/div, $u_{2,\mathrm{dc}} = 5$ V/div (ac coupling), and $i_2 = 5$ A/div.

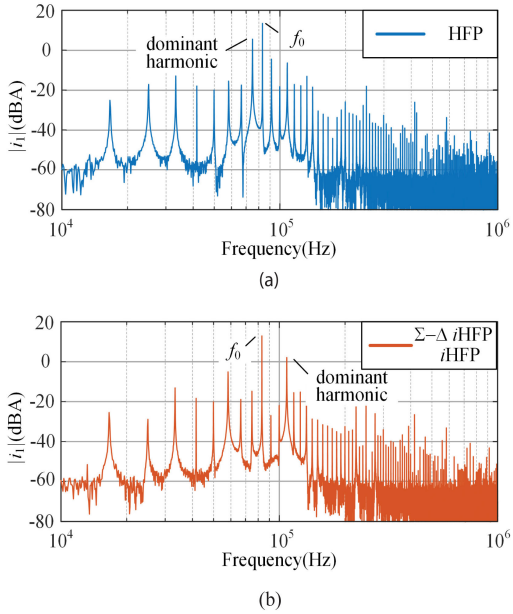

Fig. 21. Spectrums of output currents i_1 for $\delta = 0.7$. (a) HFP. (b) *i*HFP and Σ-Δ *i*HFP.

At last, the dc input power and the dc output power are measured with a power analyzer (Yokogawa WT5000, accuracy of the efficiency measurement 0.02%). The measurement results for the system efficiency of PWM and Σ-Δ *i*HFP are shown in Fig. 22(a) as a function of output power. Fig. 22(b) shows the power analyzer screenshot for Σ-Δ *i*HFP ($\delta = 0.5$). Channel 1 is the dc input power, channel 2 is the inverter output, and channel 3 is the dc output power. The system efficiency is shown in $\eta 1$. The two control methods have the same efficiency of 93.7% for achieving ZVS under a full load. The efficiency improvement of Σ-Δ *i*HFP occurs under light load, which is up to 17.8% than by PWM, because Σ-Δ *i*HFP can achieve full-range ZVS and reduce average switching frequency. The

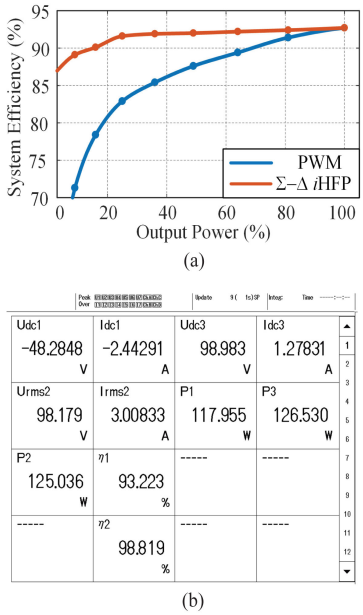

Fig. 22. (a) Measured system efficiencies of PWM and Σ-Δ *i*HFP. (b) Power analyzer screenshot for Σ-Δ *i*HFP ($\delta = 0.5$).

measurement efficiency of the WPT prototype using Σ-Δ *i*HFP can reach above 90% over a wide operating range from 16% load to full load.

V. Conclusion

In this article, an *i*HFP modulation has been proposed and verified for WPT systems. The proposed *i*HFP has the same advantage as HFP, such as full-range ZVS and switching frequency reduction ability. The improvement of *i*HFP is that it can reduce output ripple by optimal arranging pulse sequence. To simplify the implementation process of *i*HFP, Σ-Δ *i*HFP modulation has been proposed. The same pulse sequence as *i*HFP can be generated by Σ-Δ *i*HFP without complex calculations. Experimental results show that *i*HFP and Σ-Δ *i*HFP can reduce more than 60% voltage fluctuations compared with HFP. Under 0.2% input reference resolution, 66%–93% computational time reduction is achieved in going from HFP to Σ-Δ iHFP. The measurements efficiency of the WPT prototype using Σ-Δ *i*HFP can reach above 90% over a wide operating range from 16% load to full load.

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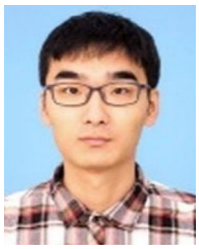

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