A Review of Multilevel Converters With Parallel Connectivity

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***Abstract*—Cascaded-bridge converters (CBCs) and modular multilevel converters (MMCs) enjoy growing popularity mostly due to modularity and scalability. Conventionally, their submodules allow only serial and bypass operation so that the use of low-voltage components for high-voltage output becomes possible. Dually, submodule parallelization adds the switched-capacitor behavior to CBCs/MMCs and has witnessed an upward trend in recent years. The salient advantages of parallel operation comprise sensorless voltage balancing, capacitance saving, current sharing, and system efficiency optimization. To capture the advancement in the field, this article reviews the state-of-the-art multilevel converters with parallel connectivity, covering various submodules, macrolevel circuit topologies, implementation challenges, and solutions, as well as control and optimization schemes. In particular, this article derives and classifies submodules as well as macro-level topologies according to basic H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules. On top of that, this article introduces strategies for the simplification of submodules and the creation of novel topologies yet maintaining parallel connectivity. We highlight the role of graph theory in creating new analytic and synthetic methodologies for multilevel converters. In addition, this article discloses the relationship between multilevel converters with parallel connectivity and switched-capacitor converters.**

***Index Terms*—Capacitance saving, cascaded-bridge converter (CBC), modular multilevel converter (MMC), submodule parallelization, switched-capacitor converter, topology, voltage balance.**

I. Introduction

MULTILEVEL converters have become a preferred technology choice in high-voltage dc/ac transmissions [1]−[3], motor drives [4]−[6], renewable energy generation [7]−[9], energy storage systems [10]−[12], power quality enhancement equipment [13]−[15], modular solid-state transformers [16]−[18], special power supplies [19]−[21], high-power amplifiers [22]−[25], electric vehicles [26]−[28], and high-power chargers [29]. Multilevel converters outweigh their two-level counterparts in terms of semiconductor voltage ratings, power quality, passive filter size, electromagnetic interference noise, and system redundancy. Cascaded-bridge converter (CBC), flying capacitor, and diode-clamped converters are three well-known multilevel converters [30]−[32]. Among them, CBCs stand out owing to their modularity and scalability and the avoidance of any additional diodes and high-voltage capacitors. Furthermore, we obtain modular multilevel converters (MMCs) by employing CBCs in replacement of individual active switches in two-level converters [33]. To this end, MMCs inherit benefits from CBCs, as MMC arms consist of CBCs. The breadth and speed of technological changes in MMCs in the past two decades are unprecedented [34]−[39].

Despite with obvious advantages, conventional CBCs or MMCs only exploit a portion of their submodules for desirable voltage synthesis, while the remaining submodules are dynamically bypassed [30], [33]. However, bypassed submodules contribute nothing but conduction power losses [40]. Furthermore, although the serial cascading of submodules breaks the output voltage into smaller portions for all module components, the current does not scale: each module—no matter how many—has to conduct the entire arm current.

In addition, the imbalance of submodule capacitor voltages poses a serious threat to the normal operation of CBCs and MMCs [41]. The mechanisms behind voltage imbalance often lie in the mismatch of charges and/or capacitances during certain periods [42]. Balancing is typically performed through circulating currents across the entire arm, which can add substantial losses in large systems [43], [44]. Especially, when supplying low-frequency voltages (e.g., for variable-speed motor drives), MMCs experience voltage drifts and hence significant submodule voltage imbalance [45]. As a straightforward solution, the use of large module capacitances appears practically viable. However, the module capacitors are bulky and expensive components that often largely determine converter size, weight, and cost [46], [47]. As such, there is a strong motivation for capacitance reduction rather than a further increase [48]. On top of the aforesaid features, system efficiency stays a key aspect of power converters [42]. Therefore, the pursuit of higher efficiency through conduction- and/or switching-loss reduction remains a paramount goal [42], [49]−[52].

Multilevel converters with parallel connectivity can mitigate the challenges and drawbacks mentioned in the previous paragraph [27], [40]. Flexible and dynamic transitions between series

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and parallel connection of modules add new features to CBCs and MMCs, known from switched-capacitor converters, while maintaining their own advantages, such as multiple inputs and outputs as well as voltage sharing among submodules [53]−[55].

As one way to enable parallelization without losing the advantage of low-voltage module components, a submodule can be tied to each of its neighboring submodules via two terminals. By proper activation of semiconductor switches, the bypassed submodules can now temporarily operate in parallel with active submodules [40], [56]. In many solutions for such parallelization, which will be elaborated further, several submodules can collectively share the arm current and thereby reduce conduction losses [27]. Moreover, dynamic parallelization can equalize submodule capacitor voltages, which is inherited as a feature intensively used in switched-capacitor converters [57]−[59]. As voltage equalization happens without the need for oversight, multilevel converters with parallel connectivity allow voltage balancing in a sensorless fashion [27], [40], [56], [60]. The hybrids of the switched capacitor and CBCs or MMCs allow compact converters with high reactive power capabilities and multilevel converters that can output ac down to 0 Hz, i.e., dc. The latter improves variable-speed motor drives, self-balancing or sensor consistency checking for safety-relevant systems, or dynamically reconfigurable battery systems, which in conventional CBCs suffer from pulsatile and reactive battery loads [61]−[69].

The removal of voltage sensors and the associated controllers can translate into significant improvements in system cost and reliability. Importantly, by providing an alternative way of voltage balancing, MMCs with serial and parallel connectivity (sometimes abbreviated as MMSPCs) can effectively mitigate voltage drifts in low-frequency applications, enabling the use of half-bridge MMCs even in dc microgrids [70]. Alternatively, the reduction of capacitor voltage ripple allows saving capacitance, such as in static compensator (STATCOM) applications, which in turn enables a further reduction of system cost and size [71]. Additionally, the added parallel states offer extra control freedom for converter efficiency optimization [40]. Because of the aforementioned benefits, multilevel converters with various ways to introduce parallel connectivity have received increasing attention in recent years [27], [40], [56], [70]−[73].

However, the option of parallelization typically increases the number of individual semiconductor switches, including their drivers; although in many topologies, the current rating per switch decreases on a similar level. For example, double-H-bridge submodules (namely, the H-bridge submodules that allow parallel connection) double the number of individual switches in multilevel converters [27]. A large quantity of active switches can increase the complexity of hardware and control. As not all connectivity modes and degrees of freedom are necessary for each application, submodules can be simplified, and the semiconductor count reduced [45], [56], [72]−[75]. Despite the tremendous growth of options, many submodules are application specific without obvious relationships.

This article reviews state-of-the-art multilevel converters with parallel connectivity. In particular, we derive submodules and macro-level topologies from three basic submodules viz., H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules. On top of that, novel strategies for circuit simplification while maintaining some forms of parallel connectivity are included. Also, we present strategies for the creation of novel topologies. Besides, the implementation challenges and solutions are covered. The remainder of this article is organized as follows. Section II presents the basic submodules of conventional multilevel converters. Section III derives the corresponding submodules for multilevel converters with parallel connectivity. Furthermore, Section IV introduces the strategies for submodule simplification, particularly for the reduction of semiconductors. Section V focuses on macro-level converter topologies. Section VI concentrates on implementation issues and solutions. Section VII discusses the control and optimization of multilevel converters with parallel connectivity. Finally, Section VIII provides concluding remarks.

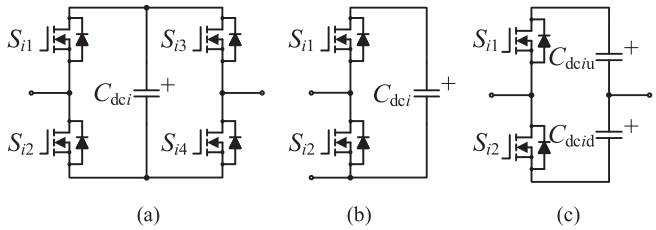

Fig. 1. Basic submodules of conventional multilevel converters. (a) H-bridge. (b) Asymmetrical half-bridge. (c) Symmetrical half-bridge.

II. Basic Submodules of Conventional Multilevel Converters

This section introduces three basic submodules of conventional CBCs and MMCs, which serve as the origins of multilevel converters with parallel connectivity.

Fig. 1 illustrates the schematic diagrams of three basic submodules of conventional multilevel converters—H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules [30], [33], [56]. As shown, each submodule consists of at least one energy storage element, such as capacitors, batteries, or any mix of them, as well as a plurality of semiconductor switches, including active switches, such as insulated-gate bipolar transistors (IGBTs) or field-effect transistors (FETs), and diodes. Current-source versions with unidirectionally conducting diode–transistor pairs or thyristors are rarer [76]−[79]. In conventional multilevel converters, submodules are connected in series for voltage sharing, thereby having two output terminals, each tied to one neighboring submodule [80]−[83].

As for H-bridge submodules [see Fig. 1(a)], the upper (S_{i1} or S_{i3}) and lower switches (S_{i2} or S_{i4}) typically operate complimentarily with dead times to avoid shoot through [70]. When diagonal switches S_{i1} and S_{i4} (or S_{i2} and S_{i3}) turn ON/OFF synchronously, we expect either a positive or a negative voltage (denoted as ± 1) from H-bridge submodules. Otherwise, the H-bridge submodule outputs a zero voltage (i.e., 0) given that its upper switches (or lower ones) turn ON simultaneously. In consequence, H-bridge submodules allow bipolar voltage outputs and bypass operation. During normal operation, H-bridge submodules use two switches to conduct load currents.

Regarding asymmetrical half-bridge submodules, as shown in Fig. 1(b), the two switches (S_{i1} and S_{i2}) operate complimentarily

TABLE I
METRICS OF BASIC SUBMODULES

Metrics	H-bridge	Asym half-bridge	Sym half-bridge
Submodule count	n	n	n
Switch count	$4n$	$2n$	$2n$
Cond. switch	$2n$	n	n
Capacitor count	n	n	$2n$
Polarity	Bipolar	Unipolar	Bipolar
Bypass operation	Yes	Yes	No
Parallel connection	No	No	No
Voltage levels	±1, 0	+1, 0	±1

[33], [83]. With S_{i1} ON and S_{i2} OFF, asymmetrical half-bridge submodules supply a positive voltage (+1). Alternatively, we obtain a zero voltage (0). As such, asymmetrical half-bridge submodules enable bypass operation yet only unipolar voltage outputs. Notably, unipolar voltage outputs prevent MMCs from operating during dc-side faults [81]. Besides, bipolar outputs are necessary for MMCs with certain macro-level topologies, such as H-bridges [82]. Nevertheless, asymmetrical half-bridge submodules save half of the switches compared with H-bridge submodules. Moreover, each asymmetrical half-bridge submodule carries the load current with only one switch, thus featuring lower conduction losses.

The symmetrical half-bridge submodule [see Fig. 1(c)] employs two switches and two energy storage elements [56], [71]. Upon S_{i1} ON and S_{i2} OFF, symmetrical half-bridge submodules yield a positive voltage (+1) contributed by their upper capacitors. Alternatively, with S_{i1} OFF and S_{i2} ON, symmetrical half-bridge submodules inversely output their lower capacitor voltages (−1). As a result, symmetrical half-bridge modules enable bipolar operation yet without any bypass state. Additionally, the balance of upper and lower capacitor voltages becomes a special problem associated with symmetrical half-bridge submodules and converters [56], [84]–[87].

Table I summarizes the key metrics of basic submodules, including the numbers or counts of switches, conducting switches, and dc energy storage elements (such as capacitors), as well as polarity, bypass operation, voltage levels, and parallel connectivity. Such metrics disclose important features of submodules. Ideally, submodules should allow bipolar and bypass operation with a large amount of output voltage levels as well as minimized numbers of switches, conducting switches, and energy storage elements.

III. DERIVED SUBMODULES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

This section presents three major derived submodules of multilevel converters with parallel connectivity, which are modified from basic submodules introduced in Section II. Submodules with local parallel connectivity are briefly discussed.

A. Submodules Derived From H-Bridge

Ilves *et al.* [80] introduced a double H-bridge submodule (see Fig. 2) that allows local parallel connectivity between two

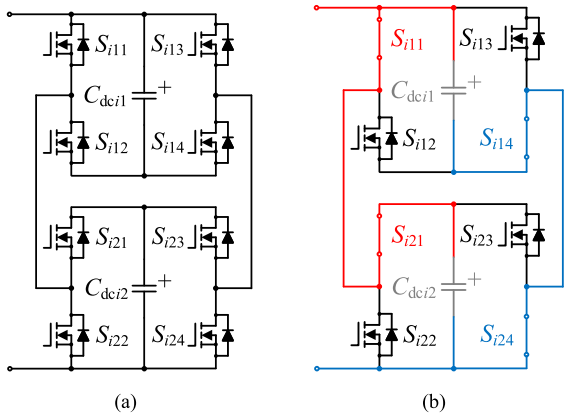

Fig. 2. Double H-bridge submodules of multilevel converters with local parallel connectivity. (a) Circuit topology. (b) Parallel state I.

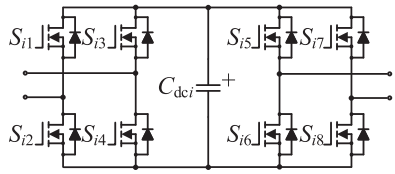

Fig. 3. Double-H-bridge submodules of multilevel converters with parallel connectivity.

capacitors, where two H-bridge circuits work collectively as one submodule. As shown in Fig. 2(a), the positive module rail of one H-bridge and the negative module rail of the other act together as output terminals, while their switching nodes are connected. When the corresponding diagonal switches S_{i11}, S_{i14} and S_{i21}, S_{i24} (or S_{i12}, S_{i13} and S_{i22}, S_{i23}) turn ON synchronously, double H-bridge submodules give a positive voltage (+1) contributed by two parallelized dc capacitors C_{dci1} and C_{dci2}, as exemplified by Fig. 2(b). Additionally, we can bypass the first H-bridge by turning ON its upper switches S_{i11} and S_{i13}. On the contrary, turning ON the lower switches S_{i22} and S_{i24} bypasses the second H-bridge. Combining these two bypass modes, we bypass the entire submodule (0). Alternatively, double H-bridge submodules yield their highest output voltage—the sum of two serial capacitor voltages (+2)—with S_{i12}, S_{i14}, S_{i21}, and S_{i23} ON. However, due to the topology asymmetry, double H-bridge submodules cannot output negative voltages, thereby featuring unipolar operation [80]. Moreover, as each double H-bridge submodule ties to an adjacent submodule via only one terminal, parallelization is only possible within but impossible across submodules. As such, the double H-bridge submodules in Fig. 2 only possess local parallel connectivity [80].

As a contemporaneously proposed alternative, a double-H-bridge submodule of multilevel converters with parallel connectivity is shown in Fig. 3, which consists of four switch pairs—eight switches, one energy storage element, and two pairs of output terminals (i.e., four terminals) [27]. One such submodule connects to its preceding or following submodule through a pair of (or two) output terminals instead of one as in conventional MMCs and CBCs. The pairwise module interconnection enables the parallelization of several submodules such that the switch

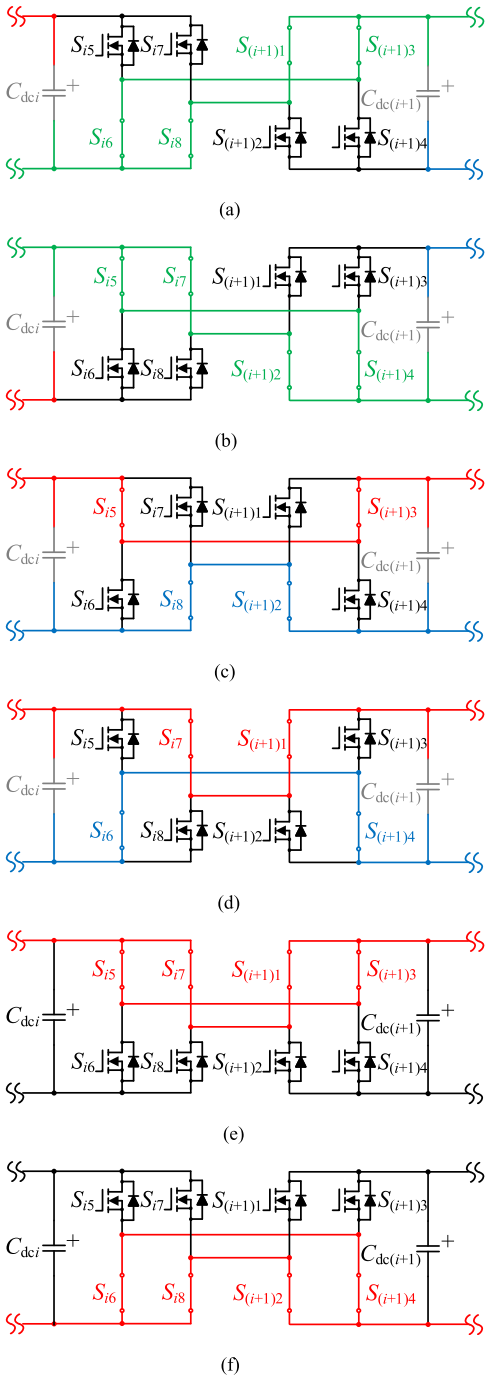

Fig. 4. Major operating states of double-H-bridge submodules. (a) Positive serial state. (b) Negative serial state. (c) Parallel state I. (d) Parallel state II. (e) Bypass state I. (f) Bypass state II.

utilization is still 50% and the blocking-voltage requirements for the modules' components do not increase.

Fig. 4 visualizes the six major operating states of double-H-bridge submodules, where only two adjacent submodules are shown for simplification [40]. Specifically, Fig. 4(a) and (b) demonstrates the positive (+2) and negative (−2) serial states, respectively. Notably, these two serial states are inherited from H-bridge submodules, except for single switches being replaced by two paralleled ones, leading to the reduction of

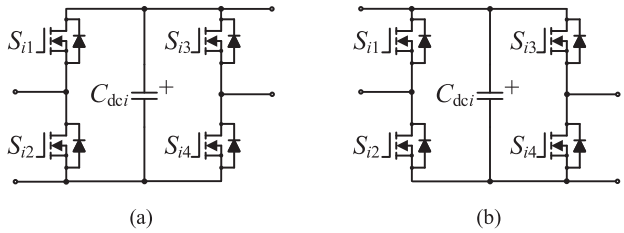

Fig. 5. Asymmetrical double-half-bridge submodules of multilevel converters with parallel connectivity. (a) Positive version. (b) Negative version.

conduction losses. In this case, the equivalent number of conducting switches is one. Additionally, Fig. 4(c) and (d) highlights the two parallel states. Under these conditions, two submodule capacitors are paralleled for voltage balancing and power loss reduction [27], [40]. Note that the maximum number of paralleled capacitors equals the number of double-H-bridge submodules, which is greater than two in general. Dependent on the states of remaining switches, either a positive (+1) or a negative (−1) voltage can be contributed by paralleled submodules. In addition, double-H-bridge submodules feature two bypass states, which give a zero voltage (0), as illustrated by Fig. 4(e) and (f). In short, double-H-bridge submodules allow bipolar, bypass, and parallel operation as well as large operating flexibility. The cost of flexibility is twice the number of individually controllable switches, although the utilization of switches is 50%. As the current can pass through two parallel transistors at each time, the total power rating of all semiconductor switches combined is exactly the same as that in conventional MMCs.

B. Submodules Derived From Asymmetrical Half-Bridge

By transplanting the same concept of parallelization into asymmetrical half-bridge submodules in Fig. 1(b), we obtain asymmetrical double-half-bridge submodules of multilevel converters with parallel connectivity, as shown in Fig. 5 [88], [89]. Here, we present two versions. Fig. 5(a) illustrates the unipolar positive version, which allows the two states of either a positive (+1) or a zero (0) output. In contrast, the negative version in Fig. 5(b) cannot yield positive voltages. Referring to Fig. 5, we notice that each asymmetrical double-half-bridge submodule comprises four switches and one energy storage element. Similar to double-H-bridge submodules, asymmetrical double-half-bridge submodules link neighbors via two terminals. Asymmetrical double-half-bridge submodules with local parallel connectivity follow the fundamental principle in Fig. 2 and are not detailed here [72].

Taking the positive version in Fig. 5(a) as an example, we present the major operating states of asymmetrical double-half-bridge submodules in Fig. 6 with two adjacent submodules included. Noticeably, the paralleled switches S_{i4} and $S_{(i+1)1}$ should switch together. Otherwise, turning ON only one of them translates into increased power losses. As such, we can lump the two switches into one, as will further be discussed later on [70]. Fig. 6(a) illustrates the serial state of submodules with their diagonal switches S_{i1}, S_{i4}, $S_{(i+1)1}$, and $S_{(i+1)4}$ ON. In this case, the submodules give their highest output voltage (+2) with 1.25 equivalent conducting switches (i.e., S_{i1} in series

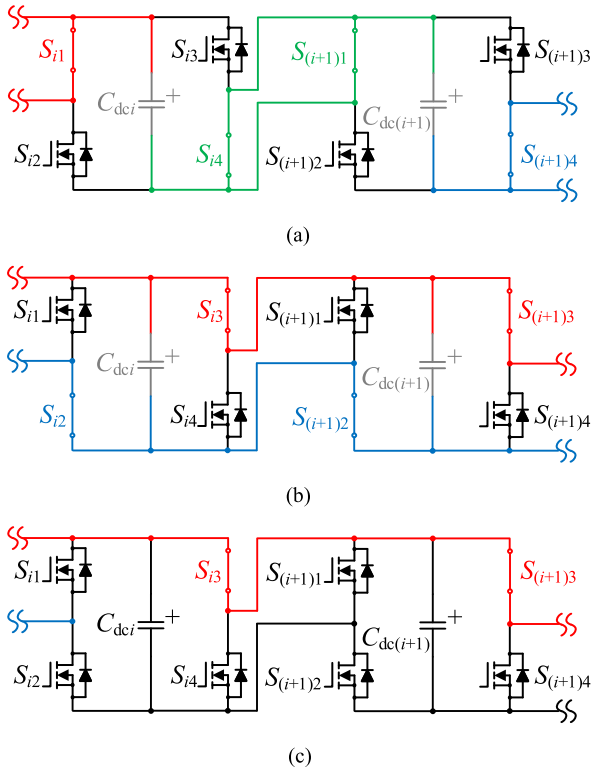

Fig. 6. Operating states of asymmetrical double-half-bridge submodules. (a) Serial state. (b) Parallel state. (c) Bypass state.

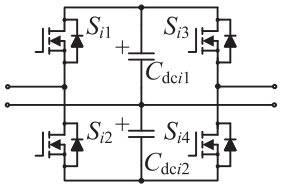

Fig. 7. Symmetrical double-half-bridge submodules of multilevel converters with parallel connectivity.

with shared $S_{i4}//S_{(i+1)1}$). Alternatively, by turning OFF the above-mentioned switches and turning ON the remaining ones, we derive the only parallel state (+1) in Fig. 6(b). Obviously, at least two module capacitors are parallelized in this manner. Under another condition, Fig. 6(c) shows the bypass state, where S_{i3} and $S_{(i+1)3}$ switch ON, leading to a zero output (0). In summary, asymmetrical double-half-bridge submodules enable parallel connectivity yet with unipolar voltage outputs.

C. Submodules Derived From Symmetrical Half-Bridge

Fig. 7 demonstrates symmetrical double-half-bridge submodules of multilevel converters with parallel connectivity [71]. As an extension of the symmetrical half-bridge submodule in Fig. 1(c), the symmetrical double-half-bridge submodule contains four switches, two energy storage elements, and four terminals. The addition of switches and terminals improves symmetrical half-bridge submodules in terms of flexibility, reliability, and performance.

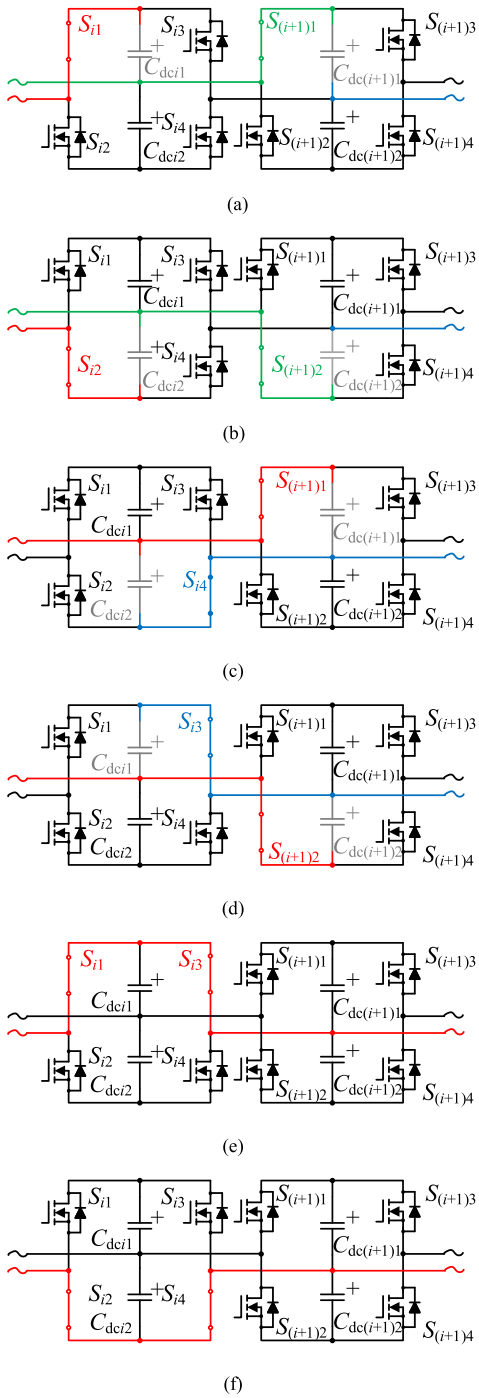

Fig. 8. Operating states of symmetrical double-half-bridge submodules. (a) Positive serial state. (b) Negative serial state. (c) Parallel state I. (d) Parallel state II. (e) Bypass state I. (f) Bypass state II.

Fig. 8 illustrates the six major operating states of symmetrical double-half-bridge submodules, where two adjacent submodules are incorporated. It is observed from Fig. 8(a) and (b) that symmetrical double-half-bridge submodules inherit positive (+2) and negative (−2) serial states from conventional symmetrical half-bridge submodules. More importantly, the additional parallel states [see Fig. 8(c) and (d)] allow the parallelization of diagonal capacitors C_{dci2} and $C_{dc(i+1)1}$ (or C_{dci1} and

TABLE II
METRICS OF DERIVED SUBMODULES

Metrics	H-bridge	Asym half-bridge	Sym half-bridge
Submodule count	n	n	n
Switch count	$8n$	$4n$	$4n$
Cond. switch count	n	$1.25n$	$0.5n$
Capacitor count	n	n	$2n$
Polarity	Bipolar	Unipolar	Bipolar
Bypass operation	Yes	Yes	Yes
Parallel connection	Yes	Yes	Yes
Voltage levels	±1, 0	+1, 0	±1, 0

$C_{\mathrm{dc}(i+1)2}$), which in turn provides an elegant way of balancing voltages between the upper and lower capacitors [71]. It should be emphasized that the parallel and serial states may appear simultaneously, where diagonal switches turn ON. As a result, parallel connectivity greatly saves on module capacitances in STATCOM applications [71], where multilevel converters compensate reactive power for voltage support [90]. Besides, symmetrical double-half-bridge submodules feature two bypass modes, as shown in Fig. 8(e) and (f). Notably, these bypass modes are excluded from conventional symmetrical half-bridge submodules [56].

Table II summarizes the key metrics of the submodules in Figs. 3, 5, and 7. As compared with Table I, the numbers of individual switches double, correspondingly. However, due to parallelization, the equivalent conduction switch count may even decrease. Parallelization improves the operating flexibility with more output voltage levels. It is possible to balance capacitor voltages and reduce voltage ripple in a sensorless way [27], [40]. Moreover, paralleled submodules share arm currents, resulting in the reduction of conduction power losses.

IV. SIMPLIFIED SUBMODULES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

This section presents strategies that reduce the number of active switches and simplify submodules of multilevel converters. The introduced strategies provide add-on benefits for the submodules introduced in Section III.

A. Diodes as a Replacement of Active Switches

In cases where unidirectional parallel connectivity is sufficient, we can replace some active switches, in combination with their drivers, by simpler diodes to save system costs and improve robustness.

Fig. 9(a) presents the schematic of double-H-bridge submodules with diodes, where one pair of active switches (i.e., S_{i7} and S_{i8}) is replaced by diodes. Notably, such a replacement is not unique. Fig. 9(b) and (c) demonstrates the two parallel states, which correspond to Fig. 4(c) and (d), respectively. However, parallelization occurs in a unidirectional pattern. To be specific, the capacitors $C_{\mathrm{dc}i}$ and $C_{\mathrm{dc}(i+1)}$ will be parallelized only when the voltage of $C_{\mathrm{dc}(i+1)}$ is greater than that of $C_{\mathrm{dc}i}$, namely,

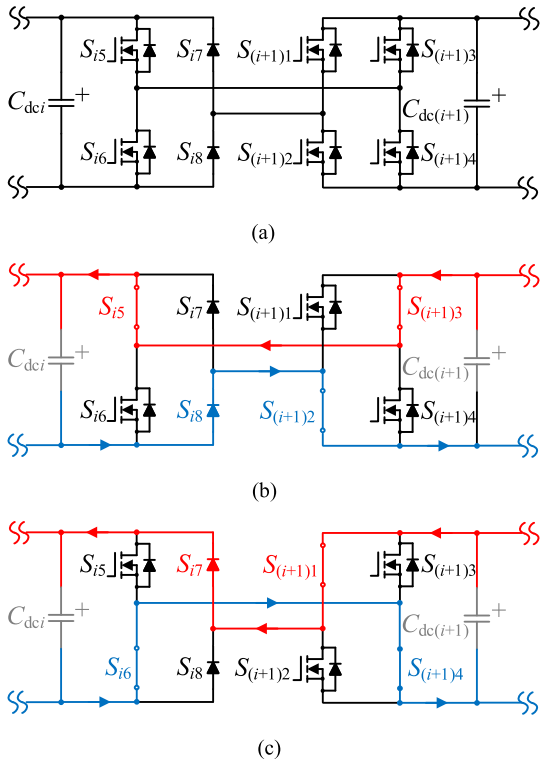

Fig. 9. Double-H-bridge submodules with diodes. (a) Circuit topology. (b) Parallel state I. (c) Parallel state II.

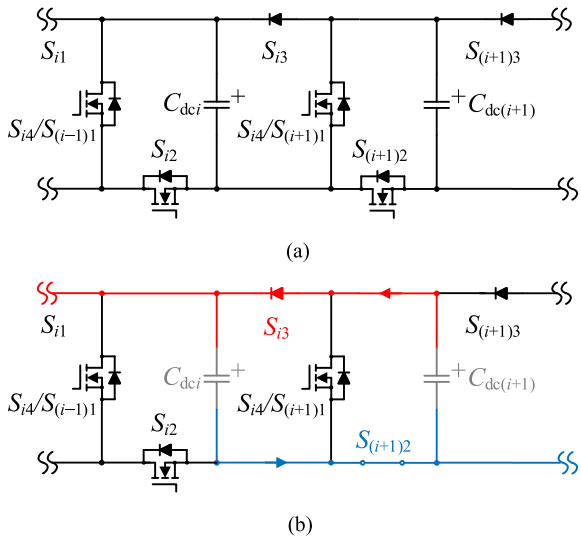

Fig. 10. Asymmetrical modified-half-bridge submodules with reduced switch count and diodes. (a) Circuit topology. (b) Parallel state.

$v_{\mathrm{dc}(i+1)} > v_{\mathrm{dc}i}$. Therefore, the use of additional diodes simplifies the circuits at the expense of operational flexibility.

By a generalization of the diode concept, Fig. 10 illustrates the asymmetrical modified-half-bridge submodules with parallel connectivity. As compared with Fig. 6, Fig. 10 first combines the two active switches S_{i4} and $S_{(i+1)1}$ into one single switch $S_{i4}/S_{(i+1)1}$ and then replaces the active switch S_{i3} by a diode. As a result, on the basis of the asymmetrical half-bridge topology, as shown in Fig. 1(b), each submodule

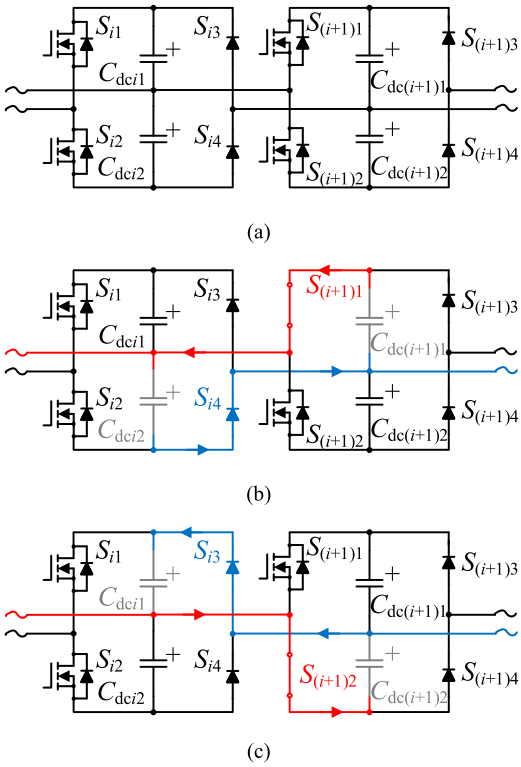

Fig. 11. Symmetrical double-half-bridge submodules with diodes. (a) Circuit topology. (b) Parallel state I. (c) Parallel state II.

uses only one additional diode to achieve parallelization, thereby greatly simplifying circuit hardware and control software [91]. However, the unidirectional property of diodes indicates that the parallelization only happens when $v_{\mathrm{dc}(i+1)} > v_{\mathrm{dc}i}$.

Similarly, Fig. 11 provides symmetrical double-half-bridge submodules with diodes, where two active switches (i.e., S_{i3} and S_{i4}) are replaced by diodes [56]. Once again, the parallel operation is unidirectional. Different from Figs. 9 and 10, it is worth noting that Fig. 11 involves different parallel capacitors ($C_{\mathrm{dc}i2}/C_{\mathrm{dc}(i+1)1}$ or $C_{\mathrm{dc}i1}/C_{\mathrm{dc}(i+1)2}$).

B. Removal of Redundant Active Switches

Returning to double-H-bridge submodules in Fig. 4, we note that two parallel states exist. Eliminating one redundant parallel state can reduce the number of active switches. For demonstration, Fig. 12 illustrates one asymmetrical modified-H-bridge submodule of multilevel converters with parallel connectivity [92]. It is clear from Fig. 12(a) that two active switches, along with their drivers and protection circuits, are removed. Fig. 12(b) represents the only remaining parallel state. Instead of positive module rails, the two interlinking active switches forming one bidirectional switch can likewise connect the negative module rails, although not shown here explicitly [92].

Fig. 13 illustrates the schematic of another set of asymmetrical modified-H-bridge submodules with two adjacent submodules [89], [93]. In this case, each submodule contains six active switches similar to that in Fig. 12. Interestingly, the associated parallel state [see Fig. 13(b)] implies that the parallelization

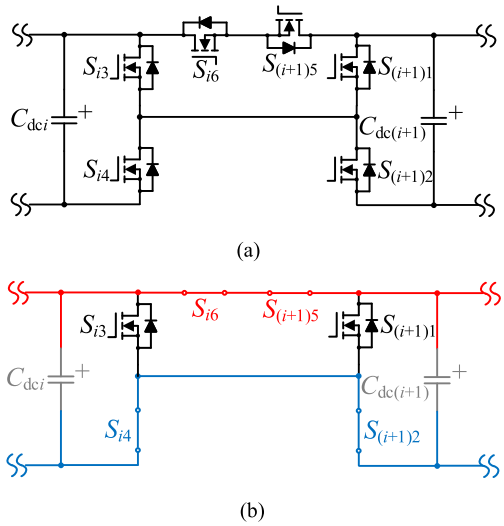

Fig. 12. Asymmetrical modified-H-bridge submodules with reduced switch count. (a) Circuit topology. (b) Parallel state.

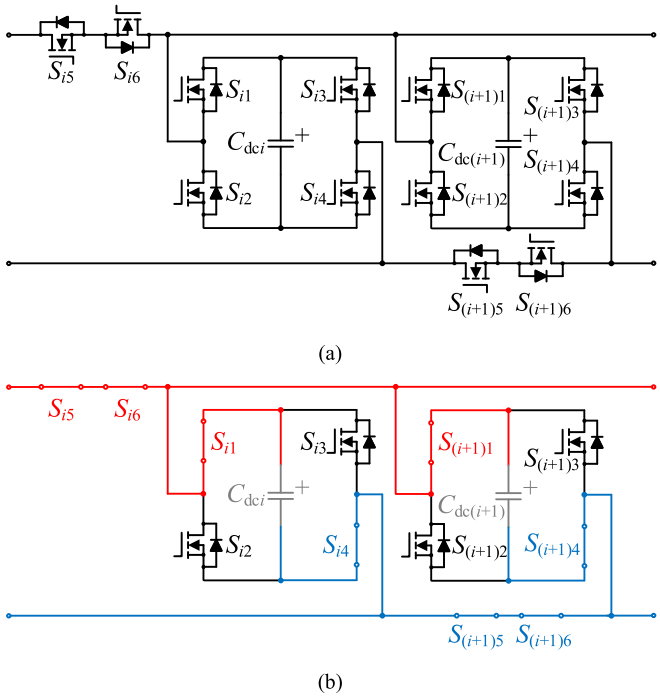

Fig. 13. Asymmetrical modified-H-bridge submodules with reduced switch count and parallel connectivity across submodules. (a) Circuit topology. (b) Parallel state.

is possible across submodules [93]. To be specific, keep the additional switches (i.e., S_{x5} and S_{x6}) ON, the submodules that are not adjacent can also be connected in parallel, as long as their diagonal switches (e.g., S_{i1}, S_{i4} and $S_{(i+2)1}$, $S_{(i+2)4}$) remain ON. The ability of parallelization across submodules enables a further improvement of system efficiency [89], [94]. However, submodules alternate in this case.

Fig. 14 demonstrates symmetrical modified-H-bridge submodules with reduced numbers of individual semiconductors. Clearly, each submodule comprises six active switches [89],

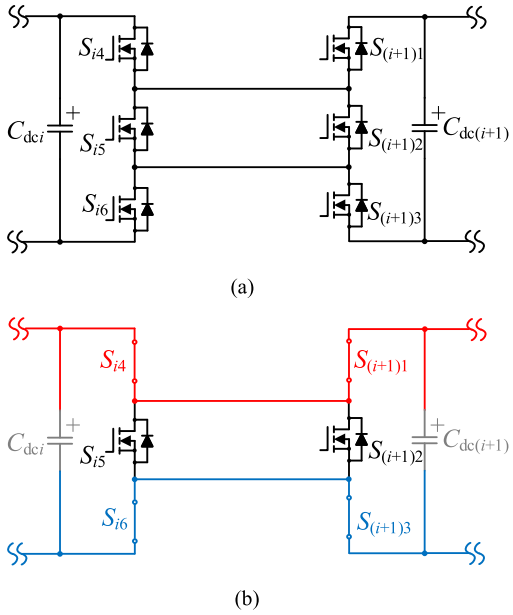

Fig. 14. Symmetrical modified-H-bridge submodules with reduced switch count. (a) Circuit topology. (b) Parallel state.

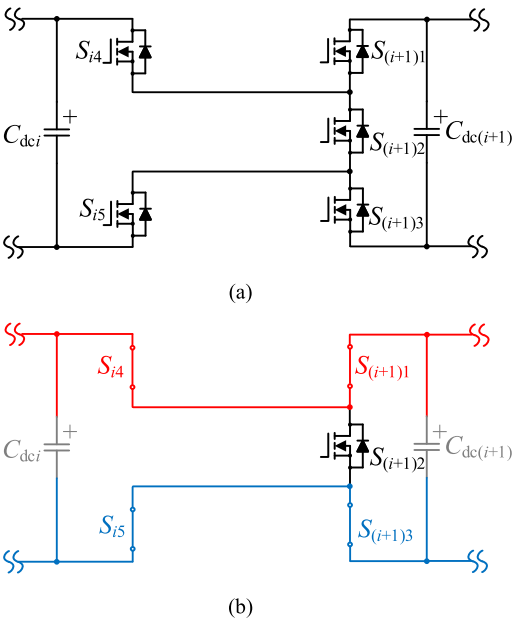

Fig. 15. Simplified symmetrical modified-H-bridge submodules with reduced switch count. (a) Circuit topology. (b) Parallel state.

[93]. As compared with Figs. 12 and 13, Fig. 14 achieves symmetry at the expense of higher conduction losses in serial states, where each symmetrical modified-H-bridge submodule features 2.5 equivalent conducting switches. By comparing Figs. 12(b) with 14(b), we find identical parallel states.

Furthermore, we simplify the two paralleled switches S_{i5} and $S_{(i+1)2}$ into one single switch $S_{(i+1)2}$, resulting in a reduction of the number of switches, as shown in Fig. 15 [89], [93]. In this case, each modified-H-bridge submodule employs only one more active switch on the basis of conventional H-bridge

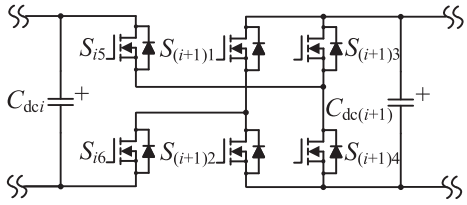

Fig. 16. Hybrid modified-H-bridge submodules.

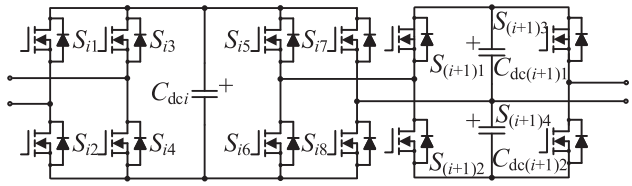

Fig. 17. Hybridization of double-H-bridge and symmetrical double-half-bridge submodules.

to enable parallel connectivity. However, three switches must simultaneously conduct in serial states to carry load currents.

C. Submodule Hybridization

An effective means of creating new multilevel converters with parallel connectivity and fewer active switches refers to hybridization. There are two levels of hybridization. First, we can obtain novel submodules through combinations of different parts of existing submodules. Second, we connect different submodules in a string to form novel CBCs or MMCs.

To illustrate the first way of hybridization, Fig. 16 presents a novel hybrid modified-H-bridge submodule that is contributed in part by the simplified symmetrical modified-H-bridge submodule (see Fig. 15) and partially by standard double-H-bridge submodules (see Fig. 3) [93], [95]. As expected, such hybrid submodules possess the features of both predecessors. In terms of switch numbers, hybrid submodules reduce two switches as compared with standard double-H-bridge submodules but increase one compared with simplified symmetrical modified-H-bridge submodules. Speaking of conducting switches, two switches conduct load currents, which is a compromise between the two predecessors once again.

Fig. 17 demonstrates the second aspect of hybridization, where two different submodules—standard double-H-bridge and symmetrical double-half-bridge submodules—are alternately connected in series, creating a novel hybrid multilevel converter with parallel connectivity, which so far has not been reported by any reference. Clearly, such hybridization reduces the average number of switches at the expense of modularity. In general, we can hybridize all the submodules, as shown in Figs. 3–16, that allow parallel connection mentioned in this article. Table III summarizes the metrics of derived submodules with reduced switch numbers.

D. Modularization

The modularization, i.e., where to split a phase unit and how to group ideally identical units, has often been a relatively arbitrary process. Early CBCs and MMCs were drafted bottom–up by

TABLE III
METRICS OF DERIVED SUBMODULES WITH REDUCED SWITCH NUMBERS

Metrics	Fig. 12	Fig. 13	Fig. 14	Fig. 15	Fig. 16
Submodule count	n	n	n	n	n
Switch count	$6n$	$6n$	$6n$	$5n$	$6n$
Cond. switch	$2n$	$2n$	$2.5n$	$3n$	$2n$
Capacitor count	n	n	n	n	n
Polarity	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar
Bypass operation	Yes	Yes	Yes	Yes	Yes
Parallel connection	Yes	Yes	Yes	Yes	Yes
Voltage levels	±1, 0	±1, 0	±1, 0	±1, 0	±1, 0

replicating known units, typically half- or H-bridges with capacitors [33], [96]. However, also a top–down modularization starting from the overall circuit is possible and shows that delimiters to form modules can be shifted relatively freely. Although such redefinition of modules appears topologically and theoretically irrelevant, modularization has large practical implications.

Most literature defines modules with a storage element inside and a switched, practically ac interconnection to the outside [74]. These interconnections typically follow the established half-bridge structures and entail the advantage that all low-side transistors of a module share the same source or emitter potential, which in turn allows to drive the gates of about half of the individual semiconductors of a module on the same potential. Topologies with a parallel mode, however, can introduce timing constraints for switching for adjacent modules and lead to a seemingly high number of module states, e.g., all combinations of bridges left and right of the storage element.

Alternatively, the module state definition can be per interconnection unit between two energy storage elements, which comprises half-bridges from two neighboring modules according to the more conventional definition above [40]. This step uncovers the high redundancy in the state definition per bridge and reduces the number of required (interconnection) states drastically, from m to approximately $\sqrt{m}$ [97]. All control operations, including modulation and module scheduling, can be performed in the interconnection space for simplification [88], [98]. If the state definition does not match the module definition, a mapping between both translates the control signals before they are sent to the modules; the first and the last bridges forming the outermost terminals of a module string can, although far apart, indeed be controlwise be united into one interconnection [88], [97].

The logical structure can also be used as the principle for modularization in hardware so that each interconnection between the module energy storage elements is entirely inside a module [45]. The module terminals become dc, the module states coincide with the interconnection states, and any timing conditions are simpler within a module.

V. MACRO-LEVEL TOPOLOGIES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

The selection of the best submodule depends largely on the application and how they are assembled to larger structures as the topologies of modules, thus the more macro-level topologies.

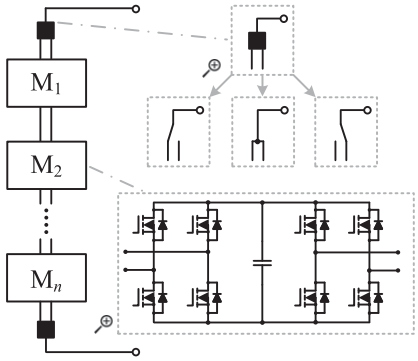

Fig. 18. CBCs or MMC arms with parallel connectivity.

As an example, the overall structure might limit the load on some or all of its arms, i.e., typically strings of modules, to mere dc voltage, although often still providing bipolar ac output at the converter terminals; in consequence, modules in such macro-level topologies only have to operate on two quadrants and be unipolar. Furthermore, the macro-level topology determines the balancing paths and can allow parallel connectivity across arms.

We start to derive macro-level topologies on the basis of the three submodules mentioned in Section II. Next, we present several special macro-level topologies. In particular, we introduce two approaches to generating novel macro-level topologies. Finally, the role of graph theory on macro-level topologies is pointed out.

A. Macro-Level Topologies Derived From Basic Submodules

Before proceeding to detailed topology derivations, we first present fundamental multilevel converters with parallel connectivity, i.e., CBCs or MMC arms with parallel connectivity, as depicted in Fig. 18, where n identical submodules (denoted by M_1, M_2, …, M_n) are connected in series similar to the conventional CBCs [30]. For the selection of submodules, it should be remembered that submodules must allow bipolar operation in typical applications of CBCs, such as STATCOMs [13]. The connection point of converter terminals allows several variants, as detailed in Fig. 18.

Next, we proceed to show macro-level topologies from fundamental submodules in Fig. 1. Recapping Fig. 1(a), we obtain macro-level H-bridge MMCs with parallel connectivity by replacing either switches (with paralleled diodes) or capacitors by CBCs in Fig. 18, as detailed in Fig. 19 [99]. Note that we remove bus capacitors in the left part of Fig. 19 such that the topology becomes totally symmetrical. This follows the concept of conventional macro-level H-bridge MMCs [82]. In contrast, the right-hand side schematic shows dc multilevel converters.

Fig. 20 presents macro-level asymmetrical half-bridge MMCs with parallel connectivity, which are derived from asymmetrical half-bridge submodules. Again, either switches or capacitors can be replaced by CBCs with parallel connectivity. Typically, macro-level asymmetrical half-bridge MMCs aim at dc–dc power conversion [75].

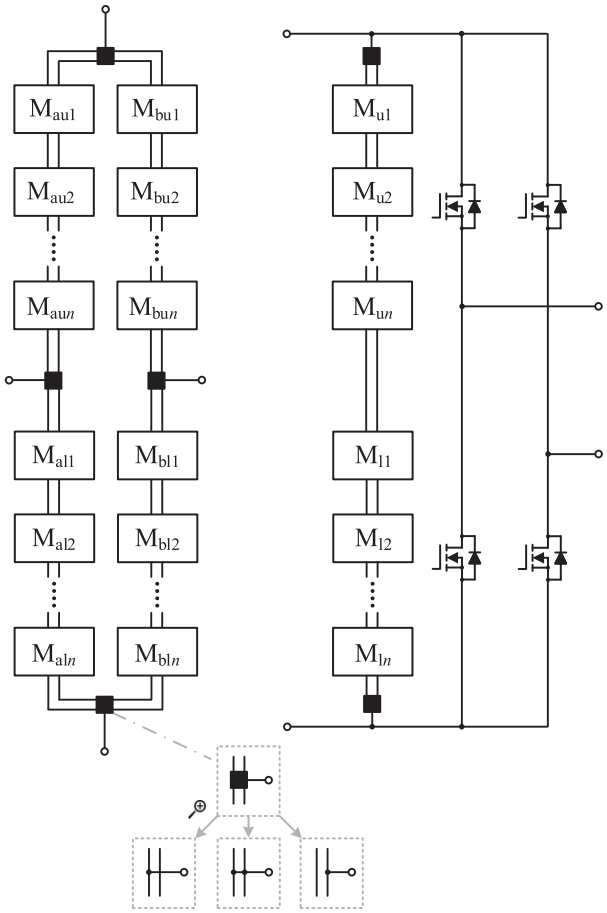

Fig. 19. Macro-level H-bridge MMCs with parallel connectivity.

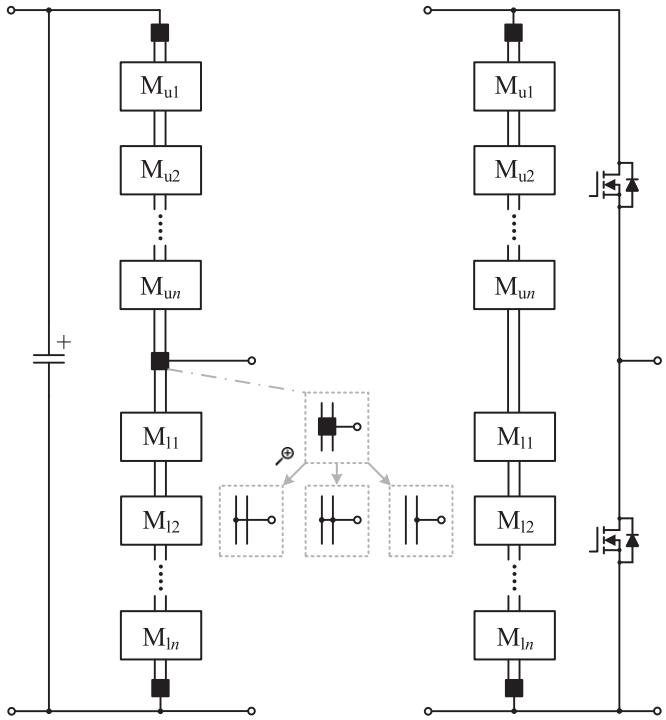

Fig. 20. Macro-level asymmetrical half-bridge MMCs with parallel connectivity.

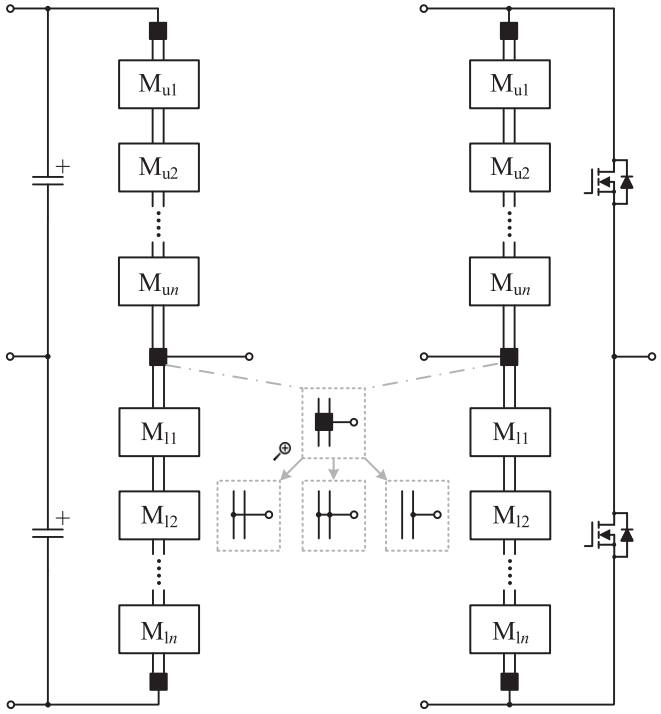

Fig. 21. Macro-level symmetrical half-bridge MMCs with parallel connectivity.

Fig. 21 illustrates macro-level symmetrical half-bridge MMCs with parallel connectivity. Remarkably, the corresponding MMC topologies without parallel connectivity have been widely used [100], [101]. One salient benefit of symmetrical half-bridge MMCs is that submodules with unipolar voltage outputs are still applicable, as voltage differences between the upper and lower arms determine the eventual output.

B. Macro-Level Topologies Derived From Other Submodules

In addition to basic submodules, three-phase two-level converters can also serve as macro-level topologies. As a notable example, Fig. 22 presents the macro-level three-phase MMCs with parallel connectivity, where either switches or bus capacitors of conventional three-phase two-level converters are replaced. The corresponding conventional MMCs have been extensively investigated [102]–[104].

Fig. 23 illustrates multilevel matrix converters with parallel connectivity, where the bidirectional switches of matrix converters are replaced by CBCs. As known, matrix converters allow direct ac–ac power conversion without intermediate power stages [105]. Therefore, multilevel matrix converters enable direct high-voltage ac–ac power transfer [102].

Fig. 24 presents another interesting type of macro-level three-phase MMCs (defined as hexagonal MMCs) with parallel connectivity [102], [106]. Similar to multilevel matrix converters, hexagonal MMCs also enable direct ac–ac power conversion yet with a reduced number of arms and compromised control flexibility [106].

Fig. 25 demonstrates a ring–star macro-level MMC with parallel connectivity [107]. Such MMCs are particularly suitable for

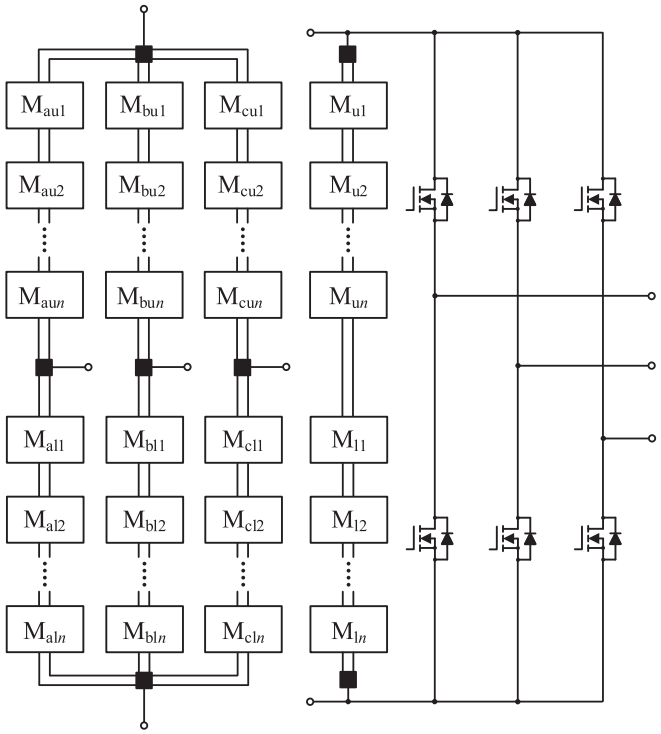

Fig. 22. Macro-level three-phase MMCs with parallel connectivity.

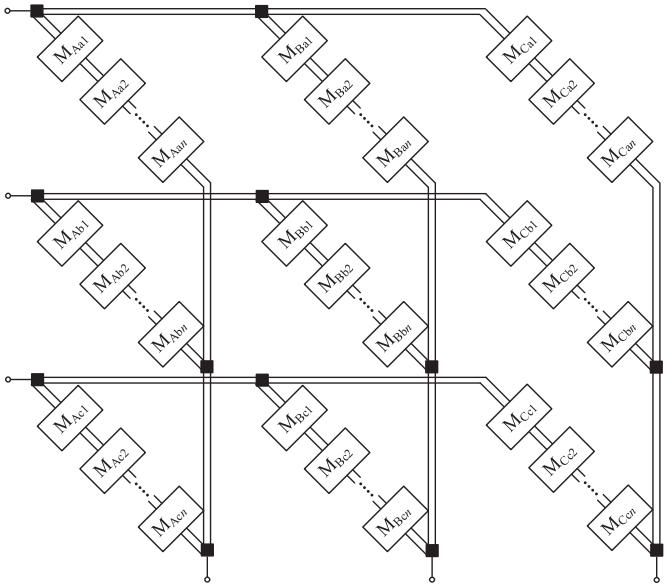

Fig. 23. Multilevel matrix converters with parallel connectivity.

poly-phase machine drives due to the decreasing phase-to-phase voltage, when phases are equivalently distributed along the ring [107]. Ring–star MMCs feature higher efficiency under light-load conditions due to parallel connectivity and desirable modulation indices. Moreover, the ring provides two mechanisms for flexible voltage balancing, specifically through capacitor parallelization and circulating currents.

In short, the majority of existing macro-level topologies of conventional MMCs are applicable to MMCs with parallel connectivity. Through the use of novel CBCs (see Fig. 18) as

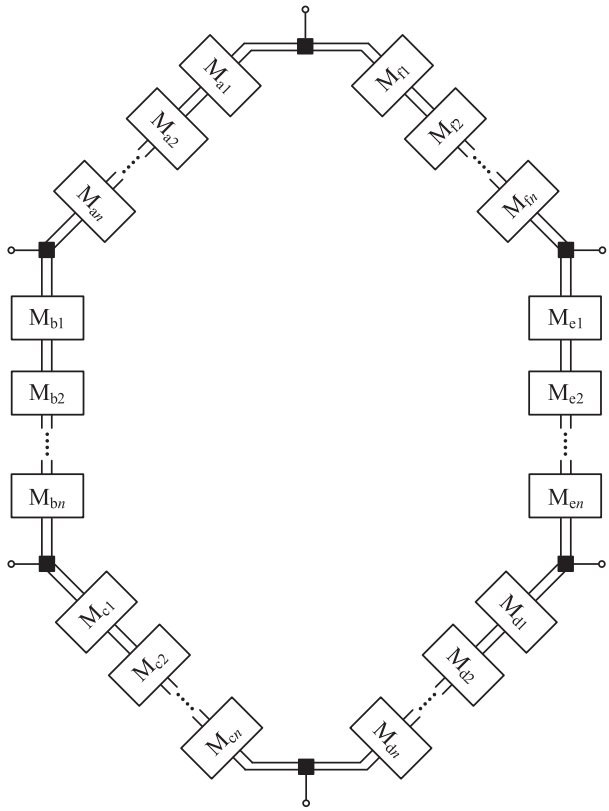

Fig. 24. Hexagonal MMCs with parallel connectivity.

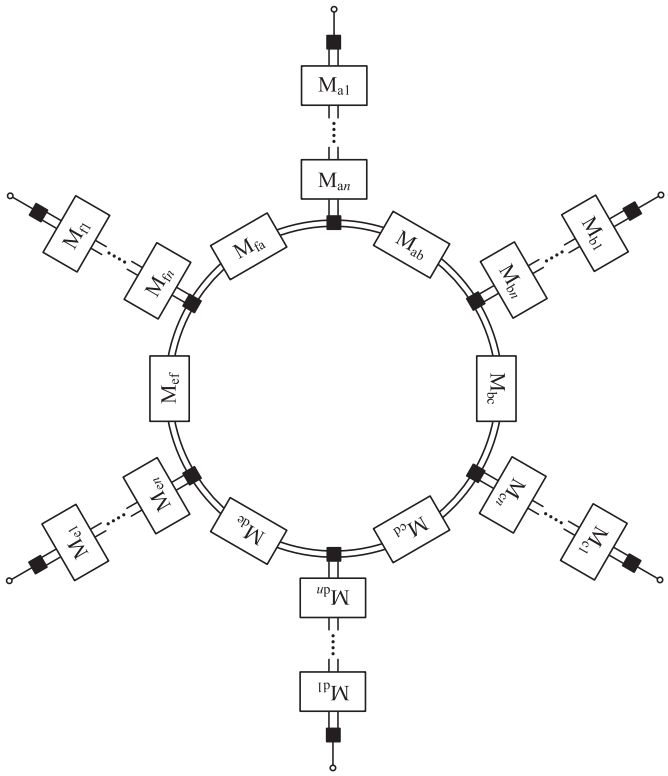

Fig. 25. Ring–star MMCs with parallel connectivity.

TABLE IV
METRICS OF MACRO-LEVEL TOPOLOGIES

MMC topologies	Arm count	Input	Output	Comments
CBC	1	–	DC/AC	–
H-bridge MMC	4	DC/AC	DC/AC	–
HB (aym) MMC	2	DC	DC	+1 cap
HB (sym) MMC	2	DC	DC/AC	+2 caps
3Φ MMC	6	DC	3ΦAC	–
Matrix MMC	9	3ΦAC	3ΦAC	–
Hexagonal MMC	6	3ΦAC	3ΦAC	–
Ring-Star MMC	6	3ΦAC	3ΦAC	+6 modules

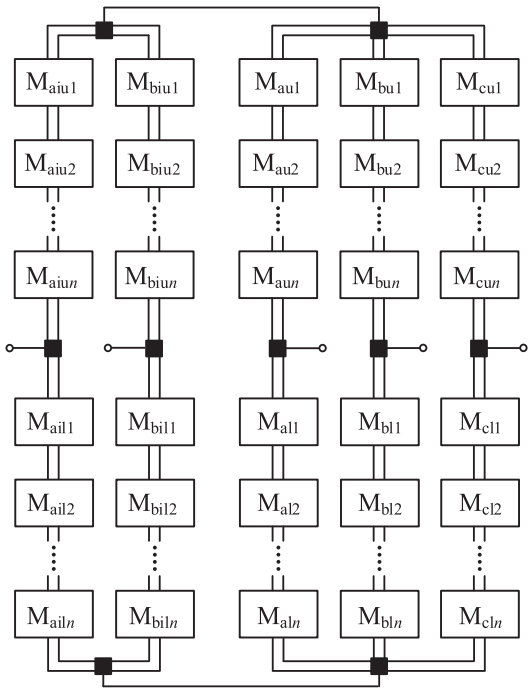

Fig. 26. Hybrid MMCs with parallel connectivity.

a replacement of conventional CBCs, we achieve the parallel connectivity of MMCs. Table IV summarizes the metrics of macro-level MMC topologies, including the arm count, input nature, output nature, and additional comments.

C. Creation of Novel Macro-Level Topologies

We have derived macro-level topologies based on single submodules/converters. In this section, we intend to create novel topologies through hybridization and nested structures.

Fig. 26 visualizes an example of macro-level hybridization, which consists of macro-level H-bridge and three-phase MMCs, both with parallel connectivity. Hybrid MMCs are potential candidates for connecting two ac grids (e.g., a single-phase grid and a three-phase grid). In principle, we can parallel multiple MMCs, CHBs, or hybridize other macro-level topologies as long as their terminals match [141], [142].

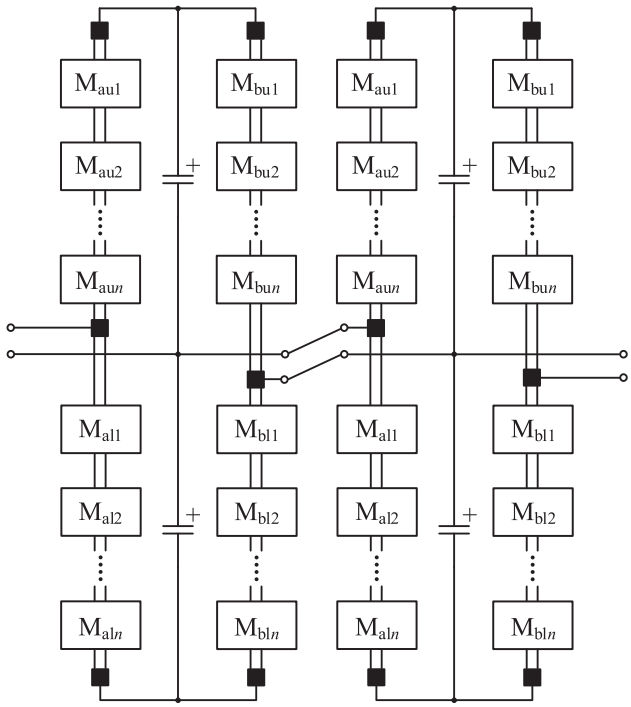

Fig. 27. Matryoshka multilevel converters based on symmetrical double-half-bridge.

Another interesting way of creating novel converters lies in the idea of nesting. Nested topologies create converters, also sometimes called Matryoshka converters [99], with more than one layer. Specifically, each layer consists of several submodules, which further comprise more submodules from sublayers. Fig. 27 provides novel Matryoshka multilevel converters on the basis of symmetrical double-half-bridge, where two top-layer symmetrical double-half-bridge submodules each incorporates a number of nested modules. Obviously, each top-layer submodule can be regarded as a macro-level MMC structure for the submodules in the second layer (represented as M_x), which may further be divided into more submodules [99]. Alternatively, nested modules can form the energy storage element of a nesting module while keeping discrete nesting-module transistors. Through nesting, macro-level (or micro-level) topologies become relative concepts. Other examples of Matryoshka multilevel converters can be found in [99].

D. Role of Graph Theory on Macro-Level Topologies

Graph theory is a valuable tool for the analysis and synthesis of macro-level topologies. For illustration, we provide an example to disclose the requirement of macro-level topologies on submodule voltage balancing via graph theory.

We begin the illustration with two simple ring MMCs, as shown in Fig. 28, where each MMC contains three submodules that allow parallel connectivity. In Fig. 28(a), the ring incorporates standard double-H-bridge submodules, thus allowing bidirectional voltage balancing. In contrast, the diodes in Fig. 28(b) only conduct in a unidirectional manner.

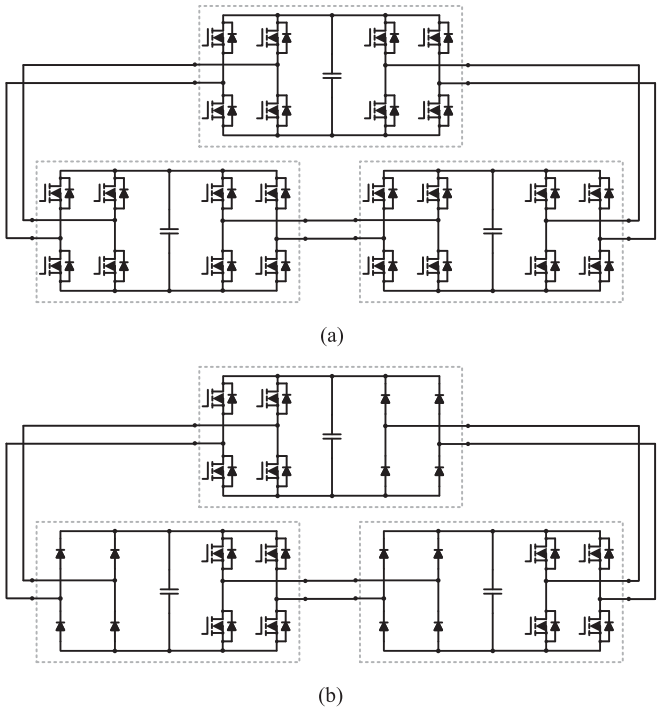

Fig. 28. Two simple ring MMCs for voltage balance study. (a) Standard double-H-bridge submodules. (b) Double-H-bridge submodules with diodes.

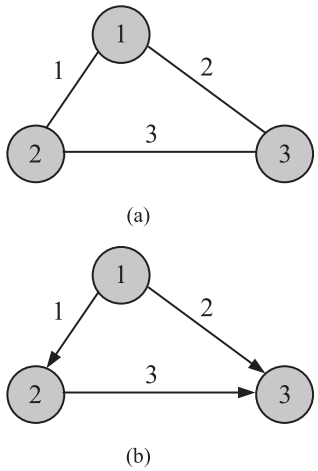

Fig. 29. Graph representations of two ring MMCs for voltage balance study. (a) Standard double-H-bridge submodules. (b) Double-H-bridge submodules with diodes.

Next, we simplify each submodule to a node and every pair of connection lines into an edge, leading to the graphs, as depicted in Fig. 29, where all the nodes and edges are sequentially numbered. Notably, Fig. 29(a) represents an undirected graph, where the edges without any arrow notation can be regarded as bidirectional edges. In contrast, Fig. 29(b) shows a directed graph with clearly marked arrows.

We define the graphs in Fig. 29 as the following triplets:

$$\mathbf{G_1} \triangleq (\mathbf{N_1}, \mathbf{E_1}, \mathbf{A_1}) \tag{1}$$

$$\mathbf{G_2} \triangleq (\mathbf{N_2}, \mathbf{E_2}, \mathbf{A_2}) \tag{2}$$

where $\mathbf{N_1}$ and $\mathbf{N_2}$, $\mathbf{E_1}$ and $\mathbf{E_2}$, and $\mathbf{A_1}$ and $\mathbf{A_2}$ stand for the sets of nodes, sets of edges, and adjacency matrices, respectively [108]. According to Fig. 29, they are expressed as

$$\mathbf{N_1} = \mathbf{N_2} = \{1, 2, 3\} \tag{3}$$

$$\begin{gathered}\mathbf{E_1} = \{(1,2),(1,3),(2,1),(2,3),(3,1),(3,2)\} \\ \mathbf{E_2} = \{(1,2),(1,3),(2,3)\}\end{gathered} \tag{4}$$

$$\mathbf{A_1} = \begin{bmatrix} 0\,1\,1 \\ 1\,0\,1 \\ 1\,1\,0 \end{bmatrix} = \mathbf{A_1}^{\mathbf{T}}, \quad \mathbf{A_2} = \begin{bmatrix} 0\,1\,1 \\ 0\,0\,1 \\ 0\,0\,0 \end{bmatrix} \neq \mathbf{A_2}^{\mathbf{T}}. \tag{5}$$

Notably, the elements of the edge sets $\mathbf{E_1}$ and $\mathbf{E_2}$ have two indices, which correspond to the source and sink nodes, respectively. In addition, the adjacency matrices $\mathbf{A_1}$ and $\mathbf{A_2}$ have a one-to-one mapping to the edge sets $\mathbf{E_1}$ and $\mathbf{E_2}$.

The prerequisite of random submodule voltage balance is that a (directed) path exists between every two nodes. Here, the path is defined as an ordered sequence of edges that links two nodes. For example, there are two paths from Node 1 to Node 3 in Fig. 29(b)—specifically {(1, 3)} and {(1, 2), (2, 3)}. The existence of paths between every two nodes is equivalent to the (strong) connectivity of graphs, which can be judged by the irreducibility of adjacency matrices [109]. By definition, $\mathbf{A}$ is an irreducible matrix if and only if the sum matrix of $\mathbf{A}^k$ ($k = 0, 1, 2, \ldots, n-1$) features all positive entries [109]. Specifically, $\mathbf{A_1}$ is irreducible as

$$\sum_{k=0}^{2} \mathbf{A_1}^k = \begin{bmatrix} 3\,2\,2 \\ 2\,3\,2 \\ 2\,2\,3 \end{bmatrix}. \tag{6}$$

Alternatively, $\mathbf{A_2}$ is found to be reducible since it contains zero entries, as proved by

$$\sum_{k=0}^{2} \mathbf{A_2}^k = \begin{bmatrix} 1\,1\,2 \\ 0\,1\,1 \\ 0\,0\,1 \end{bmatrix}. \tag{7}$$

Referring to Fig. 29(a), we observe that random voltage balance is possible. However, voltage balance from Node 2 (or 3) to Node 1 is impossible in Fig. 29(b).

The above example briefly demonstrates the role of graph theory on the analysis of MMC macro-level topologies for submodule voltage balance. In general, MMC macro-level topology analysis and synthesis through graph theory is a promising area.

VI. Implementation Challenges and Solutions

This section focuses on the implementation challenges and solutions of multilevel converters with parallel connectivity. The section first points out similarities and differences between multilevel and switched-capacitor converters. Next, it analyzes parallelization dynamics and discloses challenges due to capacitor parallelization. Furthermore, we analyze balancing energy losses. Finally, this section ends with strategies for current ripple suppression.

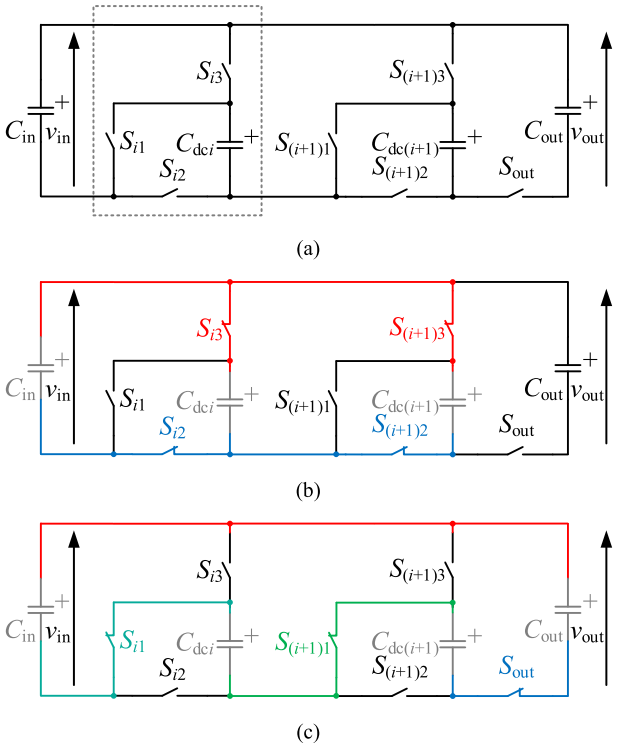

Fig. 30. Typical schematic and operation of switched-capacitor converters. (a) Circuit topology. (b) Parallel state. (c) Serial state.

A. Switched-Capacitor Converters

As the name suggests, switched-capacitor converters refer to power converters mainly consisting of semiconductor switches and capacitors, typically without magnetic components, such as inductors. As compared with inductors, capacitors can allow higher power and energy densities, thereby enabling lower power switched-capacitor converters to be implemented as integrated circuits [69]. Similar to multilevel converters with parallel connectivity, switched-capacitor converters balance capacitor voltages and transfer energy through parallelization [53]–[55]. By alternation between serial and parallel states, switched-capacitor converters can achieve very steep step-up or step-down ratios [110], [111].

Notably, multilevel converters with parallel connectivity and switched-capacitor converters can share very similar topologies. For example, Fig. 30(a) shows a typical topology of switched-capacitor converters, where the converter submodule is essentially the asymmetrical modified-half-bridge submodule with a reduced switch count (see Figs. 5 and 10) [57]. As shown in Fig. 19(b), the parallel state equalizes several selected capacitor voltages (i.e., $v_{\text{in}} = v_{\text{dc}i} = v_{\text{dc}(i+1)}$). On top of that, the serial state [see Fig. 19(c)] of switched-capacitor converters determines the remaining capacitor voltage(s) (i.e., $v_{\text{out}} = v_{\text{in}} + v_{\text{dc}i} + v_{\text{dc}(i+1)} = 3v_{\text{in}}$) [57].

Since the inputs and outputs of switched-capacitor converters are often capacitor voltages, whose relationships are fixed by serial and parallel states, switched-capacitor converters generally feature discrete (and sometimes unique) step-up or step-down ratios (e.g., 3 or 1/3). To achieve flexible voltage regulation, pulsewidth modulation (PWM) can be transplanted into switched-capacitor converters [112]. However, the usability of PWM greatly depends on parasitic resistors and equivalent series resistances of capacitors. Another methodology uses additional components, such as inductors, in switched-capacitor converters for voltage regulation [113]. In this case, switched-capacitor and conventional PWM converters overlap [114]. Along this direction, the combined operation of both modes is still under research [115], [116].

In contrast, multilevel converters with parallel connectivity typically select certain switching nodes (instead of capacitors), together with passive filters to smoothen current ripple, as inputs and outputs. As a result, flexible voltage regulation of multiple input/output ports can be expected similar to conventional MMCs [81]. Various modulation schemes for flexible voltage regulation will be introduced in the next section.

As mentioned, both switched-capacitor and multilevel converters with parallel connectivity can achieve voltage balance via capacitor parallelization. They encounter common challenges, as voltage sources (such as ideal capacitors) with very different voltages should not be directly connected in parallel [117]. We will elaborate on this point through the detailed analysis of parallelization dynamics.

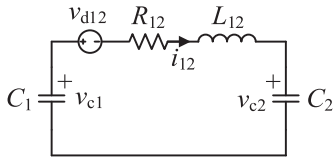

Fig. 31. Equivalent circuit for the analysis of parallelization dynamics.

B. Analysis of Parallelization Dynamics

In addition to paralleled capacitors, parasitic inductances, forward voltage drops, and equivalent resistances of semiconductors, capacitors, and cables determine parallelization dynamics [118]. For example, consider the case of two capacitors C_1 and C_2 for parallel connection in Fig. 31. As shown, v_{c1} and v_{c2} stand for the respective capacitor voltages. Elements v_{d12}, R_{12}, and L_{12} model the lumped voltage drop, resistance, and inductance, respectively; i_{12} denotes the current due to parallelization.

Parallelization dynamics are governed by the following differential equations of the serial *RLC* circuit

$$v_{\text{c1}}(t) = v_{\text{c2}}(t) + v_{\text{d12}} + R_{12}i_{12}(t) + L_{12}\frac{\text{d}i_{12}(t)}{\text{d}t} \text{ and} \quad (8)$$

$$i_{12}(t) = -C_1\frac{\text{d}v_{\text{c1}}(t)}{\text{d}t} = C_2\frac{\text{d}v_{\text{c2}}(t)}{\text{d}t} \quad (9)$$

whose theoretical bases are Kirchhoff voltage and current laws, respectively [117].

Before parallelization, assume that

$$v_{\text{c1}}(0) = v_{\text{c10}}, \quad v_{\text{c2}}(0) = v_{\text{c20}}. \quad (10)$$

Integration on both sides of (9) yields

$$C_1 v_{c1}(t) + C_2 v_{c2}(t) = C_1 v_{c10} + C_2 v_{c20}. \tag{11}$$

In the steady state, the two capacitors share an identical voltage, namely

$$v_{c1\infty} = v_{c2\infty} = \frac{C_1 v_{c10} + C_2 v_{c20}}{C_1 + C_2}. \tag{12}$$

Taking the derivative of (8), we obtain

$$\frac{\mathrm{d}^2 i_{12}(t)}{\mathrm{d}t^2} + \frac{R_{12}}{L_{12}} \cdot \frac{\mathrm{d}i_{12}(t)}{\mathrm{d}t} + \frac{(C_1 + C_2) i_{12}(t)}{L_{12} C_1 C_2} = 0. \tag{13}$$

The corresponding characteristic equation is

$$x^2 + 2\zeta\omega_0 x + {\omega_0}^2 = 0 \tag{14}$$

where

$$\omega_0 = \sqrt{\frac{(C_1 + C_2)}{L_{12} C_1 C_2}} \text{ and } \zeta = \frac{R_{12}}{2}\sqrt{\frac{C_1 C_2}{L_{12}(C_1 + C_2)}} \tag{15}$$

represent the natural angular frequency and damping factor, respectively. Alternatively, the damping factor can be quantified through

$$\alpha = \zeta\omega_0 = \frac{R_{12}}{2L_{12}}. \tag{16}$$

According to (14), we derive the two roots as

$$x_{1,2} = -\omega_0(\zeta \pm \sqrt{\zeta^2 - 1}) = -\alpha \pm \sqrt{\alpha^2 - {\omega_0}^2}. \tag{17}$$

The nature of roots and parallelization dynamics depend on the damping factor [119]. Specifically, as known from other oscillators, three cases exist.

1) *Overdamped Case ($\zeta > 1$):*

In this case, the two roots are both real numbers. The current due to parallelization is

$$i_{12}(t) = A_1 e^{x_1 t} + A_2 e^{x_2 t} \tag{18}$$

where the coefficients are determined by the following initial conditions:

$$i_{12}(0) = 0 \tag{19}$$

$$L_{12} \left.\frac{\mathrm{d}i_{12}(t)}{\mathrm{d}t}\right|_{t=0} = v_{c10} - v_{c20} - v_{d12}. \tag{20}$$

Substitution of (19) and (20) into (18) entails

$$i_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}(x_1 - x_2)}(e^{x_1 t} - e^{x_2 t}) \tag{21}$$

which varies monotonically.

2) *Critically Damped Case ($\zeta = 1$):*

We expect two identical roots under this condition. Correspondingly, the current takes the form of

$$i_{12}(t) = B_1 t e^{-\alpha t} + B_2 e^{-\alpha t}. \tag{22}$$

Considering (19) and (20), we can rewrite the current as

$$i_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}} t e^{-\alpha t}. \tag{23}$$

3) *Underdamped Case ($\zeta < 1$):*

In the underdamped case, the two roots are essentially one pair of conjugate roots, i.e.,

$$x_{1,2} = -\alpha \pm j\omega_d \tag{24}$$

where ω_d stands for the damped resonance frequency. Comparing (17) with (24), we can express ω_d as

$$\omega_d = \sqrt{{\omega_0}^2 - \alpha^2} = \omega_0\sqrt{1 - \zeta^2}. \tag{25}$$

Accordingly, the current becomes

$$i_{12}(t) = I_0 e^{-\alpha t}\sin(\omega_d t + \theta) \tag{26}$$

where the unknown parameters can be derived from (19) and (20), leading to

$$i_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}\omega_d} e^{-\alpha t}\sin(\omega_d t). \tag{27}$$

So far, we have introduced the expressions of currents [see (21), (23), and (27)] due to parallelization. According to (9) and (27), we can derive capacitor voltages (in the underdamped case) through integration as [120]

$$v_{c1}(t) = v_{c10} - \frac{(v_{c10} - v_{c20})C_2}{C_1 + C_2} \times \left[1 - e^{-\alpha t}\left(\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right)\right] \tag{28}$$

$$v_{c2}(t) = v_{c10} + \frac{(v_{c10} - v_{c20})C_1}{C_1 + C_2} \times \left[1 - e^{-\alpha t}\left(\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right)\right]. \tag{29}$$

In addition, it is of significance to know the maximum current during parallelization. Let the derivative of (27) equals zero, it gives

$$\left.\frac{\mathrm{d}i_{12}(t)}{\mathrm{d}t}\right|_{t=t_r} = 0 \Rightarrow \theta_r = \omega_d t_r = \arctan\left(\frac{1}{\alpha}\right) = \arctan\left(\frac{2L_{12}}{R_{12}}\right). \tag{30}$$

Considering (30) and setting $t = t_r$ in (27), we obtain the current peak as

$$i_{12\_\max} = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}\omega_d} e^{-\alpha\theta_r/\omega_d}\sin(\theta_r). \tag{31}$$

Clearly, we can reduce the maximum current by reduction of the capacitor voltage difference ($v_{c10} - v_{c20}$) and/or increment of the voltage drop v_{d12}. Alternatively, increasing inductors helps significantly in ripple suppression, as visualized in Fig. 32 and analyzed in [118]. The analyses of currents in other cases are similar and hence excluded. Strategies for current mitigation will be introduced in the following sections.

C. Analysis of Balancing Losses

As currents flow through resistors owing to parallelization, there will be energy losses associated with capacitor parallelization. Recapping (10), we express the initial energy that is stored

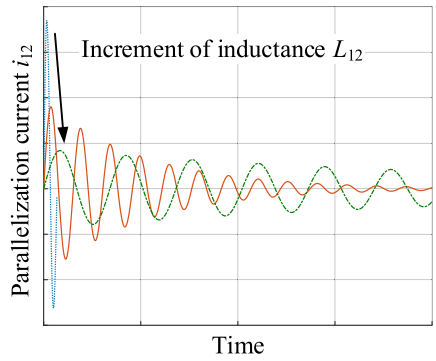

Fig. 32. Effect of inductors in suppression of currents due to parallelization.

in two capacitors as

$$E_0 = \frac{C_1 {v_{c10}}^2 + C_2 {v_{c20}}^2}{2}. \tag{32}$$

In steady state, two capacitor voltages equalize as in (12). Their energies amount to

$$E_\infty = \frac{(C_1 v_{c10} + C_2 v_{c20})^2}{2(C_1 + C_2)}. \tag{33}$$

Subtracting (33) from (32), we derive the expression of energy losses as

$$E_{\text{loss}} = E_0 - E_\infty = \frac{C_1 C_2 (v_{c10} - v_{c20})^2}{2(C_1 + C_2)}. \tag{34}$$

Under the assumption of identical capacitances, (34) reduces to

$$E_{\text{loss}} = \frac{C_1 {\Delta v_{c12}}^2}{2} \tag{35}$$

where $\Delta v_{c12} = v_{c10} - v_{c20}$.

Obviously, the energy loss due to parallelization E_{loss} increases quadratically with the increment of the voltage difference Δv_{c12} or linearly the capacitance C_1. Furthermore, Δv_{c12} is a function of C_1 and the accumulated charge difference ΔQ_{c12} in a cycle of parallelization (e.g., a switching period) per

$$\Delta v_{c12} = \frac{\Delta Q_{c12}}{C_1} \le \frac{\Delta I_{c12\_max} T_s}{C_1} \tag{36}$$

where ΔI_{c12_max} and T_s denote the maximum current difference and switching period, respectively. Substitution of (36) into (35) derives an upper limit of energy losses as

$$E_{\text{loss}} \le \frac{{\Delta I_{c12\_max}}^2 {T_s}^2}{2C_1}. \tag{37}$$

Interestingly, this first approximation is independent of the absolute module voltage. Equation (37) implies that fast switching (or reduced T_s) is key in the reduction of parallelization energy losses [27]. Alternatively, we can reduce the maximum current difference (i.e., ΔI_{c12_max}) and energy losses through well-organized charging and discharging fashions [40].

In general, energy losses owing to parallelization are notably lower than those caused by conducting and switching of semiconductor switches. As an example, with $\Delta I_{c12\_max} = 1000\,\text{A}$, $T_s = 10\,\mu\text{s}$, and $C_1 = 10\,\text{mF}$, the balancing loss of each submodule is calculated to be $E_{\text{loss}}/2 = 2.5\,\text{mJ}$ [27]. Assuming a moderate IGBT voltage drop of 1.5 V, the conduction loss per double-H-bridge submodule is found to be 60 mJ, which dwarfs the balancing loss by a factor of 24 [27]. The detailed loss analysis can be found in [27] and [40].

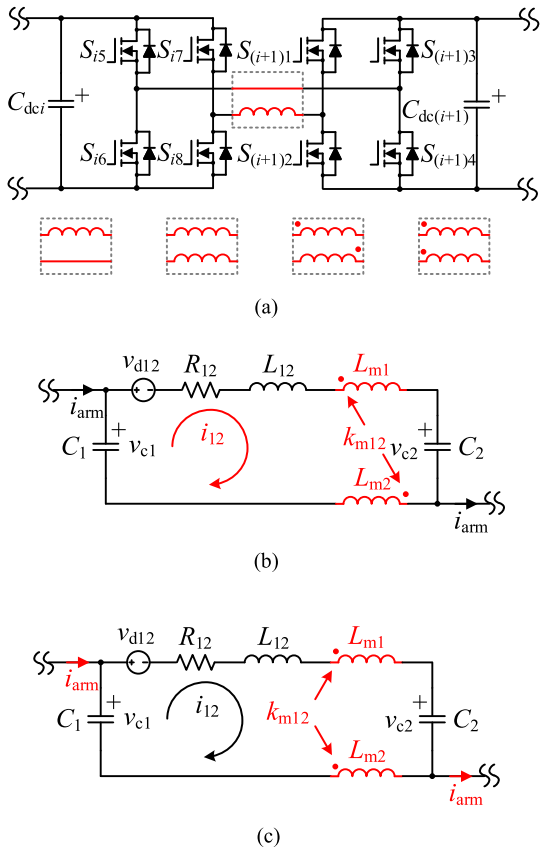

Fig. 33. Double-H-bridge submodules with interlinking inductors. (a) Schematic. (b) Equivalent circuit of negatively coupled inductors. (c) Equivalent circuit of positively coupled inductors.

D. Interlinking Inductors

As shown in Fig. 32, the increment of inductances reduces the balancing currents. Therefore, inserting small filtering inductors between submodules, as demonstrated in Fig. 33(a), can effectively suppress surge currents [121]–[123]. For this purpose, a converter can split the large, concentrated, arm inductor of conventional MMCs into smaller portions and distribute those across the module interconnections [45], [88]. The overall arm inductance would largely stay the same [88], [121].

In the case of two interlinking inductors, they can further be coupled for different applications [88]. When two inductors are negatively coupled [see Fig. 33(b)], they strongly attenuate the balancing current i_{12} via an equivalent total inductance of [124]

$$L_{\text{mp}} = L_{\text{m1}} + L_{\text{m2}} + k_{\text{m12}} \sqrt{L_{\text{m1}} L_{\text{m2}}} \tag{38}$$

where k_{m12} represents the coupling coefficient. Meanwhile, the coupled inductors pose no threat to arm currents and normal operation of MMCs [123]. In contrast, the positively coupled inductors in Fig. 33(c) mainly attenuate the arm current i_{arm}.

Another benefit of employing inductors refers to the independent control of submodule voltages, which can differ from each other [121]. Referring to Fig. 33(a), a bidirectional dc–dc converter (i.e., a buck-cascaded-boost converter) emerges provided that S_{i6} and $S_{(i+1)4}$ (or S_{i5} and $S_{(i+1)3}$) turn ON. In this case, we can regulate the voltages of $C_{\mathrm{dc}\,i}$ and $C_{\mathrm{dc}(i+1)}$ following the existing control methods of buck–boost converters [42]. With different submodule voltages, multilevel converters can yield more voltage levels with fewer submodules [121], [125].

Already with moderate switching, the inductors can be in the low microhenry range. Parasitic inductances of the module interconnections enhanced with ferrite cores have been demonstrated as effective [94].

VII. Control and Optimization of Multilevel Converters With Parallel Connectivity

This section focuses on the control and optimization of multilevel converters with parallel connectivity. The added parallel states not only greatly simplify control architectures but also allow further system efficiency optimization.

A. Control and Modulation

Previous sections introduced various topologies of multilevel converters that allow parallel connectivity. Although fundamental for multilevel converters, topologies and related hardware cannot successfully operate unless with the help of dedicated controllers. As such, this section concentrates on software implementations, including control and modulation as well as efficiency optimization.

For multilevel converters (and also those with parallel connectivity), control is closely related to modulation. To differentiate them, we refer to control as the generation of total output voltage and current references, while modulators and sometimes separate schedulers quantize those continuous reference commands and determine the activation of individual switches. In general, we classify control and modulation schemes into two groups—PWM control of individual submodules at high switching frequencies or at fundamental frequency—ideally with selective harmonic elimination [126].

Thanks to parallel charge exchange, PWM control is greatly simplified when applied to multilevel converters with parallel connectivity. This simplification is a result of dc voltage balancing that is achieved in a sensorless manner. Thus, once we regulate the dc voltage of a single submodule, all submodule dc voltages are successfully controlled.

Recapping Figs. 7 and 8, we take the multilevel converters based on symmetrical double-half-bridge submodules as an example to illustrate the control concept. Fig. 34 presents a controller for STATCOM applications, where the input reference signals $v_{\mathrm{dc\_ref}}$ and $i_{\mathrm{q\_ref}}$ are concerned with dc capacitor voltages and reactive current, respectively [71]. The grid voltage v_{grid} is measured and then passes through a phase-locked loop, yielding the phase angle information $\sin\theta$ and $\cos\theta$. Moreover, $G_{\mathrm{PI}}(s)$, $G_{\mathrm{PR}}(s)$, $G_{\mathrm{Fil\_1}}(s)$, and $G_{\mathrm{Fil\_2}}(s)$ stand for the complex frequency-domain transfer functions of proportional–integral (PI) controllers, proportional resonant (PR) controllers, notch

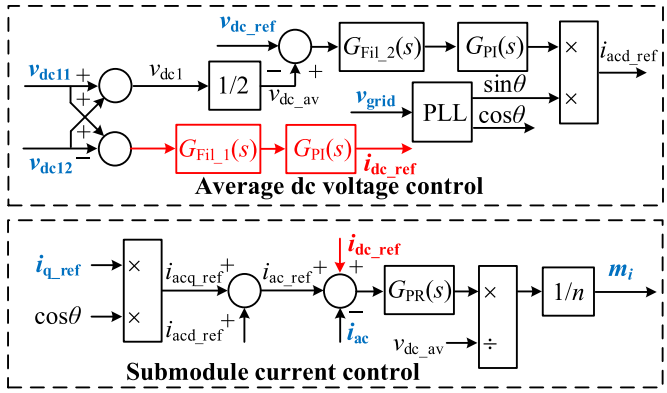

Fig. 34. Controllers of multilevel converters based on symmetrical double-half-bridge submodules operating as STATCOMs [71].

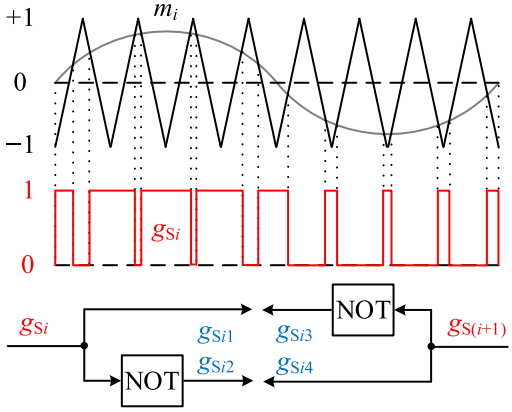

Fig. 35. Modulators of multilevel converters based on symmetrical modified-half-bridge submodules [71].

filters tuned to the second-order harmonic, and those at the fundamental frequency, respectively. With parallel connectivity, Fig. 34 implies that the controllers of multilevel converters become identical to those of conventional two-level converters, e.g., half-bridge controllers in [85]–[87] and [127].

In Fig. 34, the output signals m_i ($i = 1, 2, \ldots, n$) are sent to PWM drivers. For illustration, Fig. 35 demonstrates a simple way of modulation, where the individual m_i are compared with carrier waveforms to generate the gate signals $g_{\mathrm{S}i}$ ($i = 1, 2, \ldots, n$), and the carriers can be phase shifted for harmonic suppression [128]. Subsequently, $g_{\mathrm{S}i}$ produces $g_{\mathrm{S}i1}$ and $g_{\mathrm{S}i2}$, which further drive the corresponding upper switch S_{i1} and lower switch S_{i2} in Fig. 7, respectively [71]. The gate signals $g_{\mathrm{S}i3}$ and $g_{\mathrm{S}i4}$ deserve attention, as they come from $g_{\mathrm{S}(i+1)}$ of an adjacent submodule. As a result, diagonal switches turn ON and OFF simultaneously given that dead times are ignored, leading to the parallel states, as shown in Fig. 8(c) and (d). The relevant simulation and experimental results can be found in [71].

Regarding fundamental frequency controllers, the only necessary adaptation for multilevel converters with parallel connectivity is in principle the replacement of some or all bypass states by parallel states [27]. However, the organization of parallel states can affect system efficiency, which will be discussed in Section VII-B.

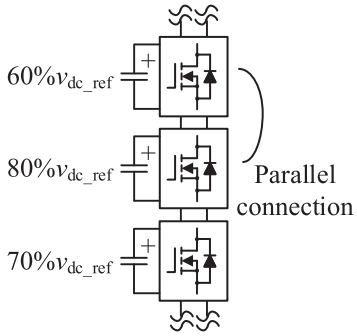

Fig. 36. Multilevel converters with three submodules illustrating efficiency optimization.

General concepts of the existing control and modulation schemes of conventional multilevel converters remain valid in multilevel converters with parallel connectivity. Notable examples include but are not limited to space-vector PWM [129], direct torque control [130], model predictive control [131], reduced switching frequency modulation [132], circulating current control [102], fault-tolerant control [133], and virtual synchronous machine control [134]−[136]. In addition, multilevel converters with parallel connectivity also allow the delivery of grid-supportive services [137]−[140].

B. Efficiency Optimization

The sequence of parallel operations affects the system efficiency of multilevel converters. Detailed optimization methodologies can be found in [27] and [40]. In this section, we briefly introduce the fundamental idea behind efficiency optimization through the reduction of parallel energy losses. For demonstration, Fig. 36 shows a multilevel converter with three exemplified submodules that can clear their voltage differences through parallelization. As revealed by (35), energy losses due to parallelization are the quadratic functions of voltage differences. Referring to Fig. 36, we choose to parallelize the upper two submodules. This leads to equalized dc voltages and a total energy loss of $0.005\, C_1\, v_{\mathrm{dc\_ref}}^2$ according to (35). Instead, if we first parallelize the lower two submodules and then parallelize them together with the first submodule, the resultant power loss amounts to $0.0125\, C_1\, v_{\mathrm{dc\_ref}}^2$, which exceeds that of the first case by a factor of 2.5. This example demonstrates the importance of balancing sequences.

VIII. Conclusion

This article provides a comprehensive review of multilevel converters with parallel connectivity. It begins with the introduction of three basic submodules—H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules. Subsequently, we derive the corresponding submodules for multilevel converters that allow parallel operation. Furthermore, we simplify such submodules via systematic techniques, including the replacement of active switches by diodes, removal of active switches, and hybridization. These submodules can furthermore form various macro-level topologies of multilevel converters as reviewed. Novel macro-level topologies can emerge through hybridization and nested structures. In addition, the role of graph theory on macro-level topologies is pointed out. Furthermore, implementation challenges and solutions related to parallel operation are detailed. Finally, we briefly review control and optimization strategies for multilevel converters with parallel connectivity. In general, the advance of power electronics promises parallelization as an enabling technology for future multilevel converters.

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