A High Power Density Multilevel Bipolar Active Single-Phase Buffer With Full Capacitor Energy Utilization and Controlled Power Harmonics

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***Abstract*—Active power decoupling in single-phase conversion systems reduces the required capacitance for twice-line frequency power ripple buffering by operating the energy buffering capacitors with high energy utilization ratios. The bipolar active buffer is the buffer topology that can achieve 100% energy utilization ratio. Yet, the conventional two-level full-bridge designs suffer from high switching and conduction loss and large filter inductor size due to the direct connection of the buffer across the high voltage dc-bus. Moreover, the high voltage swings across the buffer capacitor impose challenges for the control to regulate harmonics in the system. This article improves the power density and the efficiency of the bipolar active buffer through a buffer architecture incorporating the flying capacitor multilevel topology. Moreover, control techniques to regulate harmonics in the buffer are proposed to maintain low ripple in the dc-side current. The use of two common types of capacitors, the metal film capacitor and the X6S multilayer ceramic capacitor (MLCC) as buffer capacitors, is addressed with different harmonic control schemes. With MLCCs, we have also achieved a total passive component volume that is almost three times smaller than state-of-the-art solutions. The proposed approach is validated using a compact hardware for a 2-kW, 400-V dc-bus, 60-Hz single-phase inverter application.**

***Index Terms*—AC–DC, active buffer, capacitors, flying capacitor multilevel converters, single-phase.**

I. Introduction

In SINGLE-PHASE ac–dc or dc–ac systems, large dc-link capacitors are usually required to buffer the twice-line frequency pulsating power mismatch between the dc side and the ac side. However, due to the small dc-bus ripple requirements in many practical implementations, the energy utilization ratio (EUR) of the dc-link capacitor is typically very low, leading to large physical size. Moreover, since most of the capacitor bank solutions are implemented with electrolytic capacitors, the dc-link capacitors are usually the weakest link in the system due to the short lifetime and aging concerns, in particular at elevated temperatures and for large rms current [1]. Active decoupling methods in general improve the EUR of the capacitors by allowing larger voltage ripple on the capacitors, while decoupling such large ripple from the dc bus voltage with the help of extra power converters [2].

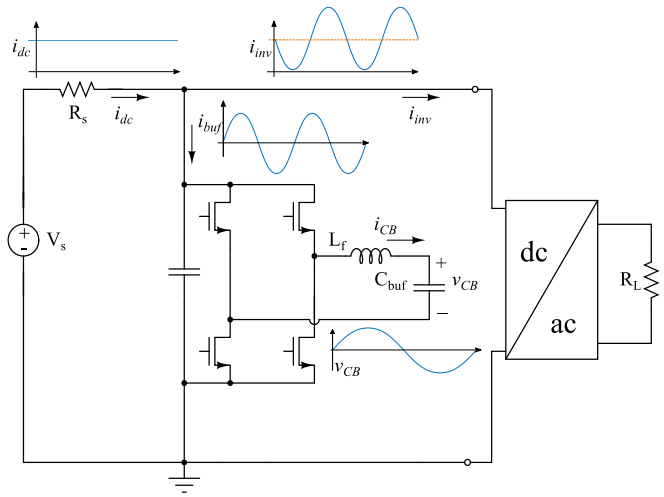

Fig. 1. Schematic drawing and key waveforms of the bipolar ripple-port active buffer in single-phase inverter applications.

The bipolar ripple port converter [3] in Fig. 1 is a type of active decoupling solutions that apply a line-frequency sinusoidal voltage onto the buffer capacitor with a full-bridge dc–ac inverter to provide the reactive power for active decoupling. Because the buffer capacitor is fully discharged to zero volt at every zero crossing of the sinusoidal voltage, the EUR is 100%. That is, all the energy in the capacitor is used to compensate for the power difference between the dc and ac side in one half 120-Hz cycle. If the buffer capacitor voltage swings with the amplitude up to the full bus voltage, the required capacitance for decoupling is minimized. However, because of the high voltage stress and high rms current through the buffer capacitor, implementing the full-bridge converter with a conventional two-level design suffers from large filter inductor size, high voltage stress on the switches, and higher device count compared to half bridge unipolar ripple port. As a result, high loss and large inductor size usually offset the benefit of the small capacitance for the conventional two-level bipolar ripple port.

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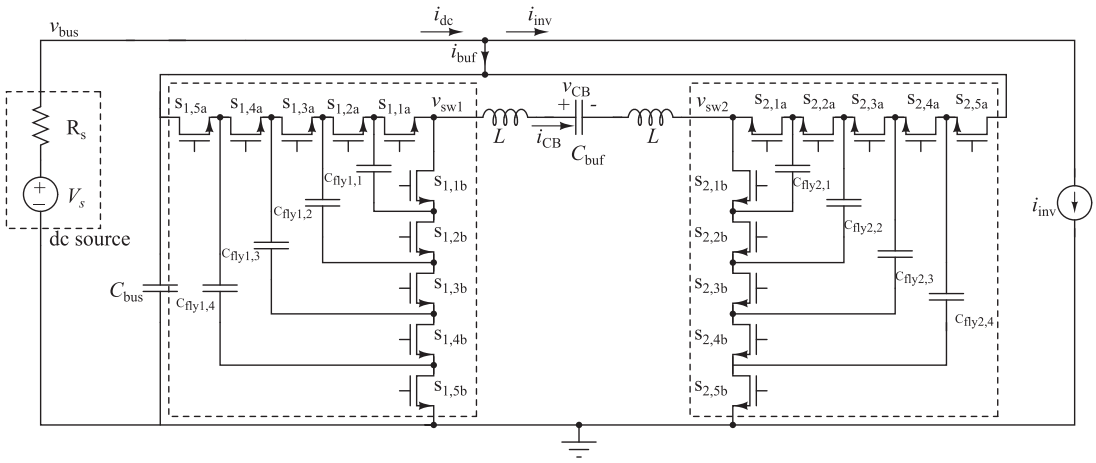

Fig. 2. Schematic drawing of the bipolar active buffer implemented with two 6-level FCML converters.

To shrink the converter size and improve efficiency, different active decoupling solutions have been proposed to improve upon the bipolar ripple port converter, which generally incur a trade-off of lower energy utilization ratio of the capacitor. For example, the unipolar half-bridge power pulsating buffer [4], [5] has half the device count of the full-bridge bipolar ripple port. However, if the dc-bias voltage of the capacitor is zero to achieve 100% EUR, the inductor current is not continuous at the voltage zero-crossings. To avoid high current slew rate and high peak current in the actual implementation, the buffer capacitor typically holds high dc bias such that the inductor current is continuous and has lower amplitude, which lowers the EUR and requires higher buffer capacitance as a trade-off. Other solutions such as the series-stacked buffer configuration [6]–[8] reduces the power processed by the full-bridge converter to reduce the overall loss by connecting a bulk capacitor in series to block the high dc-bus voltage. However, the main buffering bulk capacitor is biased with the dc-bus voltage, which means the allowed ripple is limited by the voltage rating of the physical capacitor. As a result, higher total buffer capacitance is also needed. In the practical designs of [4]–[6], the energy utilization ratio of the buffer capacitors are all below 50%. To achieve high power density with higher buffer capacitance, instead of using low-energy-density film capacitors, many single high-energy-density multilayer ceramic capacitors (MLCC) are connected in parallel and packaged as large capacitor blocks. While MLCCs brings benefits such as high energy density and efficiency, they also raise two major concerns.

The first concern is that they are very sensitive to mechanical and thermal shocks, which could cause cracks inside the ceramic layers and lead to various electrical defects or failures [9]. Such properties of MLCC require advanced packaging process to ensure performance and limit the operating conditions and environment of the converter.

Another concern with common X6S, X7S MLCCs is that they do not have a constant capacitance. Instead, the capacitance depends on the voltage bias. As a result, if ideal sinusoidal voltages derived using constant capacitance for normal buffer operations were applied, the capacitor current would be strongly distorted, and so would be the power flowing through the capacitor [10], [11]. Consequently, unwanted harmonics will be present on the dc-side current. This is another reason why buffers implemented with MLCCs in [4] and [6] are operated with limited voltage swings and high dc biases such that the capacitance change within the operating voltage range is negligible and thus does not introduce extra harmonics in the system.

In this article, we seek to overcome the limitations of the conventional bipolar ripple port converter by implementing the dc–ac buffer converter with two flying capacitor multilevel (FCML) converters, as shown in Fig. 2. With FCML converters, the filter inductor size and the overall passive component volume are much reduced. The high efficiency and high power density characteristics of the FCML in various low-to-medium-voltage applications have recently been demonstrated in [12]–[14]. Furthermore, in two-level active buffers, the filter inductors are so large that their reactive power has to be considered at the line frequency [4], [5], which complicates the calculation for ideal capacitor voltage. With much smaller inductors in the FCMLs, as can be demonstrated in this article, the ideal capacitor voltage can be directly applied without considering the reactive power of the filter inductors.

For the buffer capacitor, different design targets and applications would prefer the use of film capacitor or MLCC over the other. For instance, film capacitors are preferred in more demanding operating conditions such as automotive applications, while MLCCs are more desirable to achieve high power density. In this work, expanding upon the buffer design in [15] with only the film capacitors, the use of both film capacitors and X6S MLCCs are explored and demonstrated with corresponding control techniques. Compared to [15], tradeoffs among different buffer designs such as volume, input current ripple, and loss distribution are discussed in more details. The proposed buffer topology, control, and modulation schemes are implemented and verified with a compact hardware prototype rated for 2-kW and 400-V dc-bus. The major contributions of this article are as follows.

1) The first hardware demonstration of the bipolar ripple port implemented with FCMLs in full-bridge configuration.

2) The tested condition of 2 kW at 400 Vdc is higher than any prior work on the bipolar ripple port with film capacitors as the buffer capacitor. A full voltage control scheme with regulation and harmonic compensation is proposed to minimize the harmonics in the capacitor voltage, thus in the dc-side current.
3) The first hardware demonstration of using MLCCs as the buffer capacitor in a bipolar ripple port, with a high voltage swing that is close to the full dc-bus voltage. For X6S MLCCs tested in this work, a novel control technique is proposed to eliminate the harmonics in the MLCC's power by actively injecting voltage harmonics in the capacitor voltage, under very high voltage swings. The resulting low harmonic capacitor power is able to maintain a low ripple in the input dc current.
4) With the MLCCs, the buffer capacitor volume is three to four times smaller than the state-of-the-art solutions designed for the same conversion specifications (Google LittleBox Challenge Specifications [16]: 2 kW, 400 V dc-bus, 20% dc current ripple).

II. Ideal Operation of the Bipolar Active Buffers

The single-phase conversion scenario with the bipolar active buffer is depicted in Fig. 1. The dc source is modeled as a voltage source V_s with a source resistance R_s. The fundamental frequency content of the inverter input current is at the twice-line frequency regardless of the switching frequency [3], [6]. As such, the single-phase inverter load on the dc-bus is modeled as a current load. For simplicity, the ac side of the inverter is considered with unity power factor in this work, but the proposed solution works equally well with nonunity power factor. With unity-power-factor inverter load, the inverter current can be found as

$$i_{\text{inv}} = I_{\text{dc}} - I_{\text{dc}} \sin(2\omega_L t). \tag{1}$$

To cancel the twice-line frequency component in the inverter current, the buffer current has to be (2) such that $i_{\text{buf}} + i_{\text{inv}}$ is a dc constant.

$$i_{\text{buf}} = I_{\text{dc}} \sin(2\omega_L t). \tag{2}$$

For the buffer to draw such current, a line-frequency sinusoidal voltage has to be applied to the buffer capacitor C_{buf}. Using the power balancing relation of the buffer converter, the differential equation using fundamental capacitor voltage/current relation can be found as

$$V_{\text{bus}} i_{\text{buf}} = v_{\text{CB}} i_{\text{CB}}$$

$$V_{\text{bus}} I_{\text{dc}} \sin(2\omega_L t) = C_{\text{buf}} v_{\text{CB}} \frac{\mathrm{d}v_{\text{CB}}}{\mathrm{d}t}. \tag{3}$$

Separating two variables and integrating both sides, we can obtain

$$V_{\text{bus}} I_{\text{dc}} \int \sin(2\omega_L t)\mathrm{d}t = C_{\text{buf}} \int v_{\text{CB}} \mathrm{d}v_{\text{CB}}$$

$$\frac{V_{\text{bus}} I_{\text{dc}}}{2\omega_L}(k - \cos(2\omega_L t)) = \frac{1}{2} C_{\text{buf}} v_{\text{CB}}^2 = E_{\text{Cbuf}}. \tag{4}$$

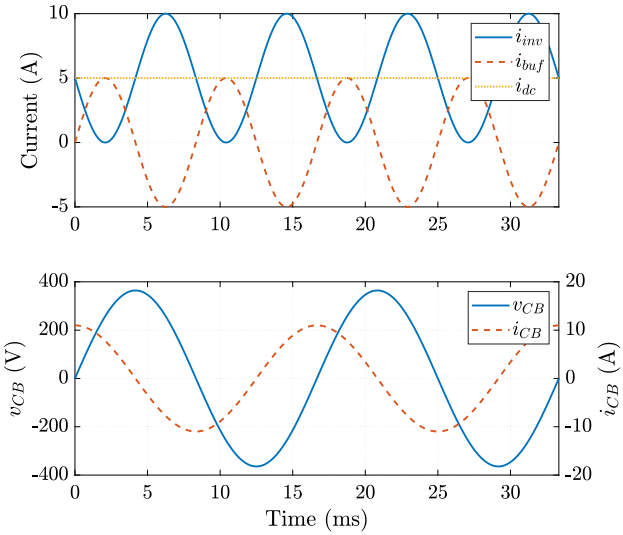

Fig. 3. Ideal waveforms of the bipolar active buffer $V_{\text{S}} = 450$ V, $i_{\text{dc}} = 5$ A, $R_s = 10\ \Omega$, and $C_{\text{buf}} = 80\ \mu$F.

Since the capacitor energy E_{Cbuf} is always greater than zero, the constant k from the indefinite integral cannot be lower than one. If the capacitor voltage is discharged to zero after each twice line cycle, the EUR of the capacitor is 100%. In other words, by setting the initial energy $E_{\text{Cbuf}}(0) = 0$ in (4), $k = 1$ for the 100% EUR [5], which is true for the bipolar ripple port considered in this work. Assuming the buffer capacitance C_{buf} is constant, the solution to the differential equation with $k = 1$ is

$$v_{\text{CB}} = V_{\text{CB}} \sin(\omega_L t) = \sqrt{\frac{2V_{\text{bus}} I_{\text{dc}}}{\omega_L C_{\text{buf}}}} \sin(\omega_L t) \tag{5}$$

where V_{CB} is the magnitude. The ideal waveforms of i_{inv}, i_{buf}, i_{dc}, v_{CB}, and i_{CB} are plotted in Fig. 3. From (5), we can also derive the minimum capacitance needed for buck type ripple port buffers by setting $V_{\text{CB}} = V_{\text{bus}}$ as

$$C_{\text{buf, min}} = \frac{2P_0}{\omega_L V_{\text{bus}}^2} \tag{6}$$

where P_0 is the single-phase system power $V_{\text{bus}} I_{\text{dc}}$, V_{bus} is the dc-bus voltage, and ω_L is the line angular frequency.

III. Control of the Buffer With Film Capacitors

If film capacitors were used as the buffer capacitor, the ideal voltage in (5) could be directly applied because of the constant capacitance. Thus, the goals for the buffer control scheme are as follows.

1) Generate reference capacitor voltage based on (5) with correct frequency, phase, and magnitude to buffer the needed power in the overall dc–ac system.
2) Regulate the output voltage of the dc–ac buffer converter (i.e., capacitor voltage v_{CB}) with low harmonics such that no unwanted harmonic contents are induced in the dc-side input current.

The full control scheme of the buffer converter with film capacitors is shown in Fig. 4. It comprises three main elements: generation of an ideal voltage reference for buffer capacitor

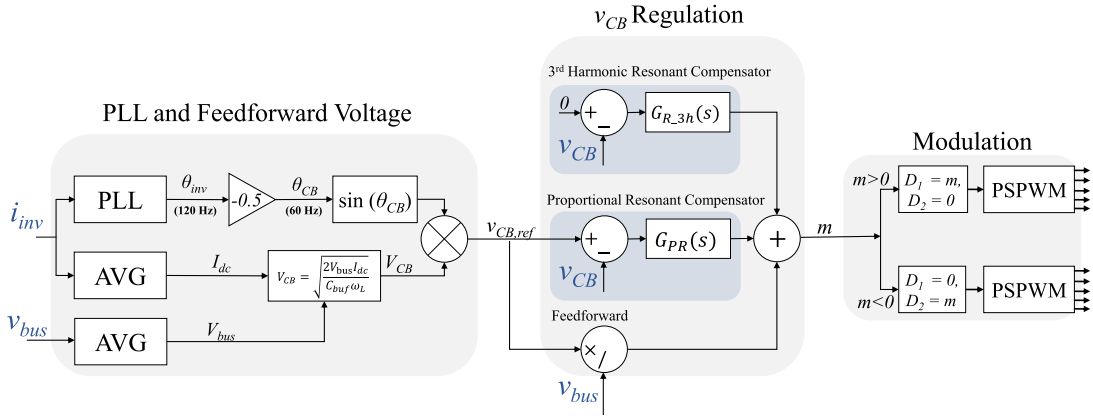

Fig. 4. Control diagram of the proposed buffer control scheme for film capacitors. The sensed parameters are in blue font.

voltage $v_{\rm CB}$, regulation of $v_{\rm CB}$ and modulation, i.e., generation of the appropriate phase-shifted pulse-width-modulation (PSPWM) signals.

A. Buffer Capacitor Voltage v_{CB} Reference

To generate a low-harmonic and low-noise reference voltage for the buffer capacitor, a phase-locked loop (PLL)-based control is implemented as shown in Fig. 4 [17]. From (1) and (5), the angular relation between the inverter current and buffer voltage can be determined. If the angle of the ac portion of the inverter current is $\theta_{\rm inv} = -2\omega_L t$, the angle for the buffer capacitor voltage is then $\theta_{\rm CB} = \omega_L t = -0.5\theta_{\rm inv}$. In other applications where the buffer control is integrated with the main inverter or power factor correction (PFC) control [13], [18], the angle can also be obtained from the main ac voltage.

The inverter current $i_{\rm inv}$ is sensed, and a PLL based on digital notch filters is designed to detect the angle $\theta_{\rm inv}$. Once $\theta_{\rm CB}$ is calculated from $\theta_{\rm inv}$, the magnitude $V_{\rm CB}$ can be calculated based on (5). To do so, the average dc current $I_{\rm dc}$ is obtained by averaging $i_{\rm inv}$, and the dc-bus voltage $V_{\rm bus}$ is also sensed and calculated. $C_{\rm buf}$ and ω_L are known parameters to the system. The square-root function in the DSP controller can then be used to calculate $V_{\rm CB}$.

B. Regulation of v_{CB}

In the ideal case, $v_{\rm CB}$ can be generated by feedforwarding the calculated reference using (5). However, as the voltage and current swings on the buffer capacitor become larger as the load increases, the actual $v_{\rm CB}$ will be distorted, which means the capacitor power is also distorted. As can be seen from the power balancing relation in (3), any distortion on the capacitor power will result in discrepancy between the actual $i_{\rm buf}$ and the ideal buffer current $I_{\rm dc}\sin(2\omega_L t)$, which means the ripple component in $i_{\rm inv}$ will not be perfectly canceled. As a result, there will be unwanted ripple component in the dc-side current as

$$\begin{aligned} i_{\rm dc} &= i_{\rm inv} + i_{\rm buf} \\ &= I_{\rm dc} - I_{\rm dc}\sin(2\omega_L t) + i_{\rm buf} \\ &= I_{\rm dc} - I_{\rm dc}\sin(2\omega_L t) + \frac{v_{\rm CB} i_{\rm CB}}{V_{\rm bus}}. \end{aligned} \tag{7}$$

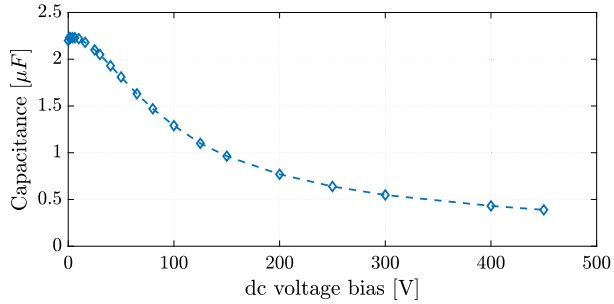

Fig. 5. Capacitance derating with voltage bias curve of TDK C5750X6S2W225K250KA.

Since the peak-to-peak ripple of the dc-side current is usually restricted to a certain limit (e.g., $\leq 20\%$ of the dc average current) for many practical applications [16], it is necessary to regulate $v_{\rm CB}$. To obtain a low-harmonic $v_{\rm CB}$, a regulation scheme with feedforward, a proportional-resonant (PR) compensator $G_{\rm PR}$ at the fundamental 60 Hz frequency, and a resonant compensator at 180 Hz (third harmonic) $G_{\rm R\_3h}$ is implemented [19]. The transfer function for the $G_{\rm PR}$ is

$$G_{\rm PR}(s) = K_P + K_{i1}\frac{s}{s^2+\omega_L^2} \tag{8}$$

and the transfer function for third harmonic resonant compensator is

$$G_{\rm R\_3h}(s) = K_{i3}\frac{s}{s^2+(3\omega_L)^2} \tag{9}$$

where K_P is the proportional gain, and K_{i1} and K_{i3} are the gains for resonant compensators at the fundamental line frequency (60 Hz) and the third harmonic (180 Hz), respectively. As will be presented in the experiment results, third harmonic resonant compensator is essential to maintain low harmonics in the dc-side current.

IV. Control of the Buffer With X6S MLCCs

A. Challenges of Using MLCC in the Bipolar Active Buffer

To demonstrate the challenges of using MLCC as the buffer capacitor, the TDK C5750X6S X6S MLCC is used as a design example. The capacitance derating curve of TDK C5750 is

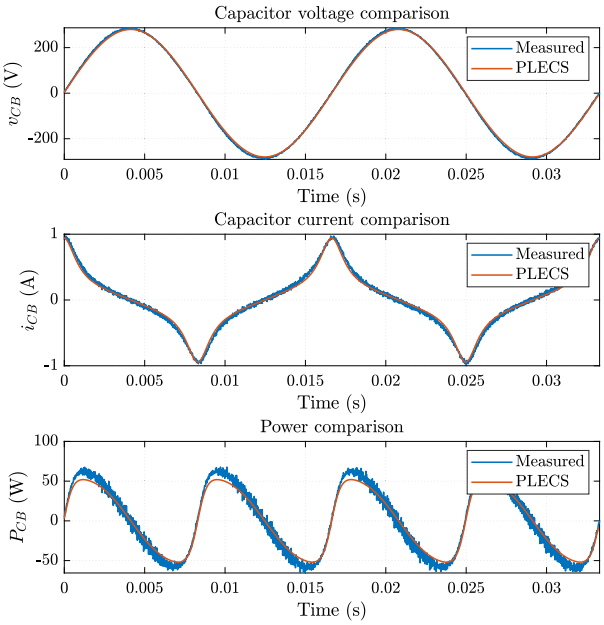

Fig. 6. Experimental and simulated waveforms of four TDK C5750X6S under 200 V_{rms}, 60 Hz ac voltage.

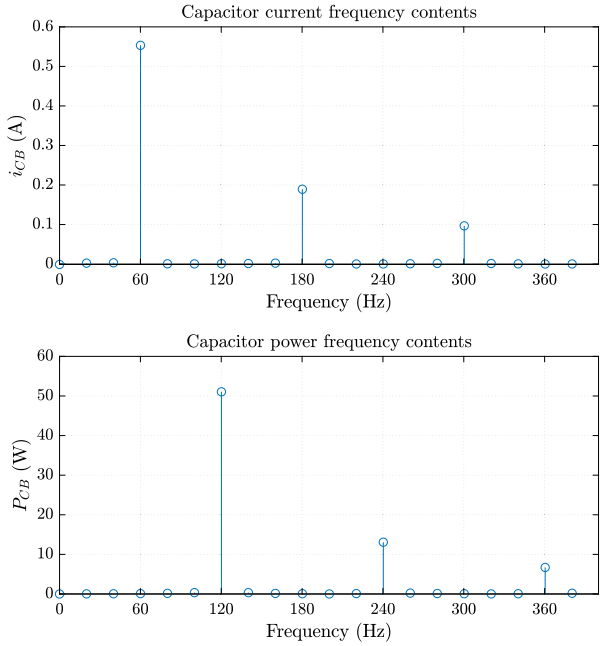

Fig. 7. Harmonic contents of the tested TDK C5750X6S ceramic capacitor current and power.

shown in Fig. 5. As can been seen, the capacitance deceases to 20% of the zero-bias capacitance at 400 V dc-bias. The capacitor current equation $i = C\frac{dV}{dt}$ thus has to be modified such that $C(V)$ is the capacitance at V bias. To understand the effect of capacitance derating on the capacitor current and power, four TDK C5750 capacitors in parallel are tested with 200 V_{rms}, 60 Hz pure sinusoidal voltage with an ac power supply, which has sufficient voltage swing to introduce a significant change in capacitance. Meanwhile, a corresponding simulation-based model of a variable capacitor based on the derating curve in Fig. 5 is implemented in the simulation software PLECS. The experimental and simulated results are plotted and compared in Fig. 6. As can be observed, the model in PLECS can predict the actual capacitor current fairly well. Most importantly, both the capacitor current and power contain significant harmonic distortion. The frequency contents of the capacitor current and power are plotted in Fig. 7. It can be seen that the current contains only odd harmonics (third, fifth,...), while the power contains even harmonics of 60 Hz (fouth, sixth,...).

For the bipolar active buffer, if TDK C5750 is used as the buffer capacitor, the resulting capacitor power will contain even harmonics if the sinusoidal voltage in (5) is applied. As derived in (7), the even harmonics in the capacitor power will cause even harmonics in the buffer current i_{buf}, which eventually will appear as components of the dc-side current. The effects using other capacitor types with different characteristics are discussed in [20].

B. Proposed Control Scheme to Eliminate Harmonics in the MLCC's Power

As discussed in Section IV-A, we cannot simply replace linear film capacitors with nonlinear MLCCs as the buffer capacitor using the same control, otherwise there will be even harmonics in the dc-side current caused by the nonlinear capacitance. Intuitively, if the capacitance of the MLCCs is the function of the voltage bias, by incorporating a voltage-dependent capacitance function $C(V)$ into the differential equation (3), an explicit voltage expression in time domain can be solved for MLCCs similar to (5). However, this approach first requires a good curve fitting to find an expression for the $C - V$ curve in Fig. 5. As the derating curve is nonlinear, higher order terms are needed for more accurate modeling, which will make the differential equation (3) much more difficult to solve and the final result much more complicated than constant capacitance. Moreover, the fitting parameters will vary for individual MLCCs. As such, it is not realistic nor effective to first derive an ideal buffer voltage expression with voltage-dependent capacitance and to directly apply such voltage in the control. In this work, utilizing the harmonic analysis in Fig. 7, instead of trying to solve for the correct capacitor voltage in time domain, a control scheme is proposed such that the buffer capacitor voltage is reconstructed and controlled in frequency domain.

Fundamentally, even harmonics in the capacitor power originate from the product of the odd-harmonic current and the fundamental-frequency voltage. To eliminate the even harmonics in the capacitor power, thus in the input dc current, odd voltage harmonics with opposite signs need to be injected to the capacitor voltage. Detailed mathematical derivation is given in the Appendix. Consequently, a feedback system to regulate the ripple components in i_{dc} cannot be realized with only linear compensators such as proportional-integral (PI) or proportional-resonant (PR) controllers in [4], as they do not change the frequencies of the signals in the system. More specifically, if the errors from sensing i_{dc} contain only even harmonics, the output from the compensators will also contain only even harmonics.

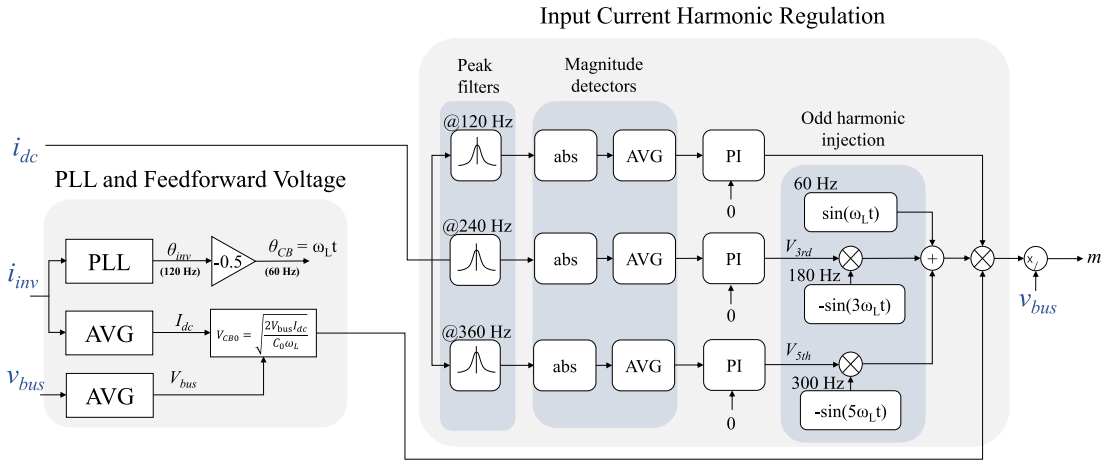

Fig. 8. Control diagram of the proposed buffer control scheme for MLCCs. The sensed parameters are in blue font.

Thus, injecting even-harmonic voltages cannot eliminate the even harmonics in the capacitor power, and, in fact, introduces undesirable extra odd harmonics. To overcome the limitation of linear controllers, the control scheme in Fig. 25 is proposed.

Similar to the control with film capacitors, i_{inv} and v_{bus} are sensed to generate the phase reference and feedforward voltage magnitude. The feedforward voltage term is calculated using the zero-bias capacitance of the MLCCs. Next, i_{dc} is sensed and the its harmonics are regulated as follows. First, with three peak filters centered at 120, 240, and 360 Hz, even harmonic contents in i_{dc} are extracted independently. The peak filters are implemented in the DSP with the parameters calculated from the second-order infinite impulse response (IIR) filter function `iirpeak` in Matlab with sampling frequency of 150 kHz and bandwith of 24 Hz, which are plotted in Fig. 8.

Following that, the magnitude of each harmonic content is calculated by averaging the absolute value of the ripple. Each harmonic magnitude is then regulated to zero with a PI controller with zero reference. The outputs from PI controllers for 240 and 360 Hz contents scale the third (180 Hz) and fifth (300 Hz) harmonic voltage injection. The output of the PI controller for 120 Hz scales the overall magnitude to cancel the main twice-line frequency ripple. The exact relation among three scaling factors are derived in the Appendix.

The conversion scenario with 100 parallel-connected TDK C5750, for 400 V dc-bus and 2 kW conversion, is simulated in PLECS with the proposed control. The voltage, current, and power waveforms and frequency contents are plotted in Figs. 9 and 10 respectively. As can be observed in Fig. 9, the capacitor voltage is not a pure 60 Hz sinusoidal voltage anymore. Instead, the controller is able to determine the correct magnitude for the third and fifth harmonics to inject into the capacitor voltage, as shown in the spectrum plot in Fig. 10. As a result, the capacitor power has very low even harmonic content except for the main 120-Hz content for twice-line frequency power buffering.

Note that because the magnitude of the 60 Hz component is much larger than that of the 180 and 300 Hz components, to better visualize them in the same plot, the capacitor voltage in Fig. 10 is plotted in dB. The expression for the capacitor voltage

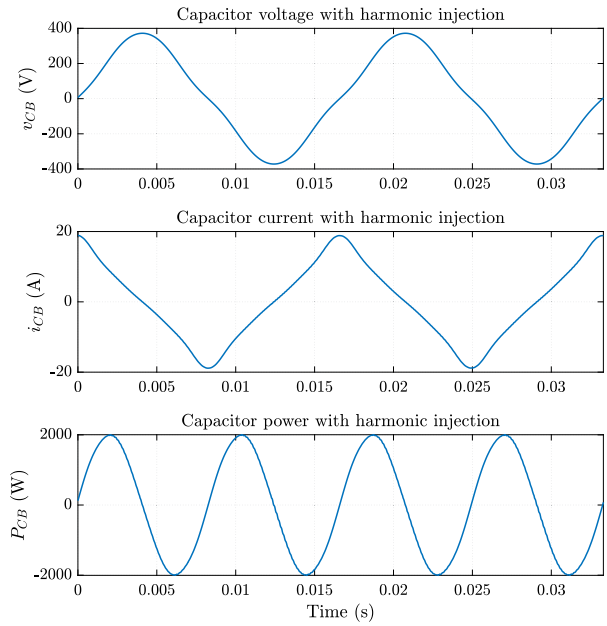

Fig. 9. Simulated waveforms for single-phase buffering scenario with 2-kW system power and 400-V dc-bus using X6S MLCCs as the buffer capacitor.

in Volts is

$$v_{\text{MLCC,2kW}}(\text{V}) = 345\sin(\omega t) - 31.5\sin(3\omega t) - 5.35\sin(5\omega t) \tag{10}$$

which has a peak voltage of 371.2 V. Correspondingly, the peak current is 18.2 A.

The transient behavior of the power harmonic elimination control is also simulated in PLECS for a load step from 2 to 1 kW system power in Fig. 11. And the voltage magnitude commands for the fundamental, third, and fifth harmonic contents are shown in Fig. 12. As can be seen in both figures, the controller is able to adjust the magnitudes of the fundamental and odd harmonic voltages to suppress the ripple term in the dc input current to zero within a few line cycles after the load step. More optimization on the PI parameters can be done to improve the dynamic performance.

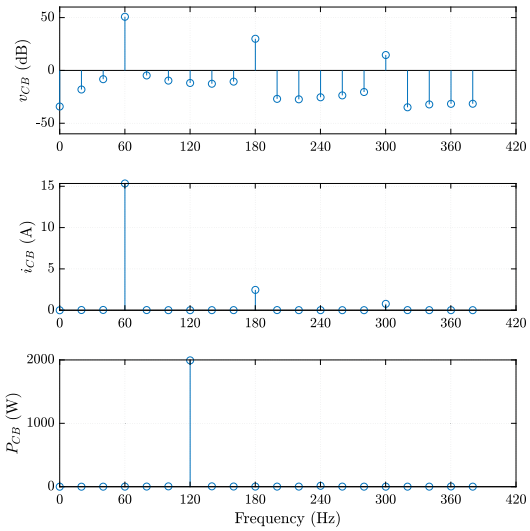

Fig. 10. Harmonic contents of the capacitor voltage, current and power with the proposed control for 2 kW system power and 400 V dc-bus using X6S MLCCs as the buffer capacitor. As can be observed, the capacitor power has very minimal high harmonic contents.

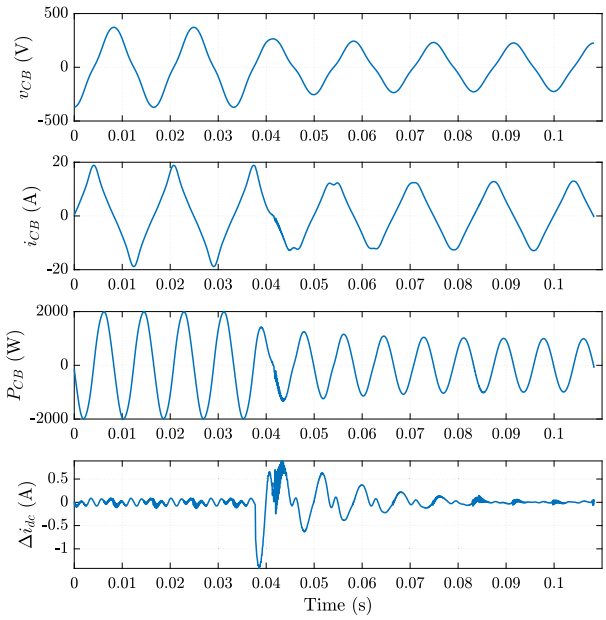

Fig. 11. MLCC buffer capacitor voltage, current, power and corresponding dc-side current ripple during a load step from 2 kW to 1 kW dc power.

V. Buffer Converter Design

A. FCML Component Sizing

The dc–ac converter in the buffer is implemented with two 6-level FCMLs in a full-bridge configuration. For FCMLs, it is critical for the flying capacitor voltages to maintain close to the ideal balanced voltage levels to avoid high voltage stress on the switches and extra switching harmonics. While active balancing techniques are more robust [21], [22], they require additional sensing and computing capabilities. As such, in this work, the FCMLs rely on the strong natural balancing strength of the even-level FCMLs to maintain good voltage balancing [23], as will

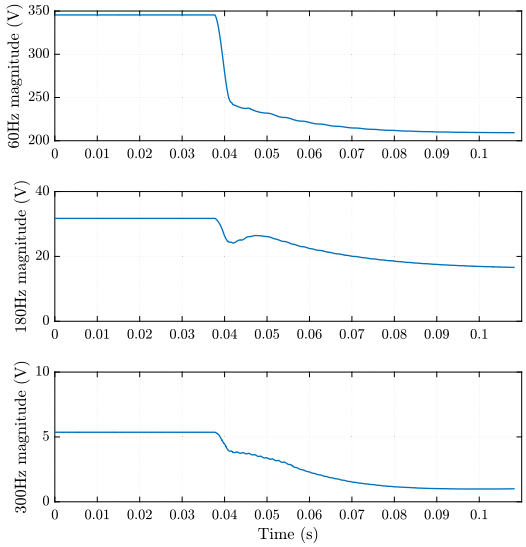

Fig. 12. Capacitor voltage magnitudes of each frequency contents during a load step from 2 to 1 kW dc power.

be seen in the experiment results. It should be noted that this work demonstrates strong natural balancing for simplicity, and the proposed control technique is fully compatible with active balancing, should one wish to use such methods. More detailed operation and sizing of passive components for the FCML can be found in [14], [24]–[27]. Yet, there are a few specifications that are worth noting for this particular application.

Unlike the FCML inverters tested in [12], [14], the output voltage and current of the buffer dc–ac converter are 90° out of phase, and contain high-order harmonics with the MLCCs. As such, the inductor current ripple and flying capacitor voltage ripple have to be specifically calculated in one line cycle with the buffer voltage and current to determine the ratings for the inductor, capacitors, and switches.

With the equations in [14], [27], the calculated inductor current ripple Δi_{L} and flying capacitor voltage ripple (peak-to-average) Δv_{cfly} with 150 kHz switching frequency and 3 μF flying capacitor, and 13.6 μH inductor are plotted in Fig. 13. The voltage stress seen by each switch is

$$v_{\mathrm{sw,\,rating}} = V_{\mathrm{nom}} + \Delta v_{\mathrm{cfly}} \tag{11}$$

where V_{nom} is the nominal flying capacitor voltage $\frac{V_{\mathrm{bus}}}{5} = 80$ V for the 6-level FCML. Therefore, the peak switch voltage stress is 87 V for this design. The top envelope of the inductor current is

$$i_{\mathrm{L,\,top}} = i_{\mathrm{CB}} + 0.5\Delta i_{\mathrm{L}} \tag{12}$$

whose maximum is the peak inductor current in one line cycle. The saturation limit of the inductor current rating is thus calculated to be 18.4 A.

B. Hardware Implementation

The dc–ac full-bridge FCML converter in the buffer is implemented with two 6-level FCML modules in Fig. 14. The FCML module is designed with ten 100 V GaN System FETs, isolated

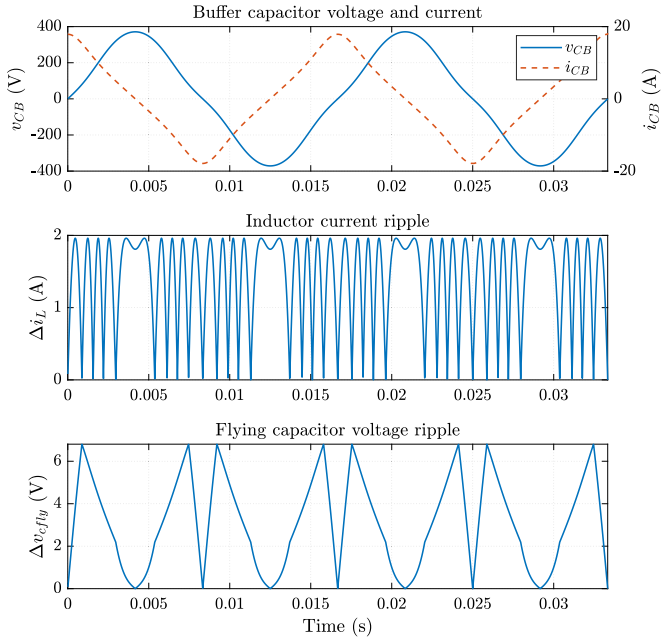

Fig. 13. Calculated inductor current ripple and flying capacitor voltage ripple in two line cycles with MLCC buffer capacitor for 2-kW, 400-V dc-bus.

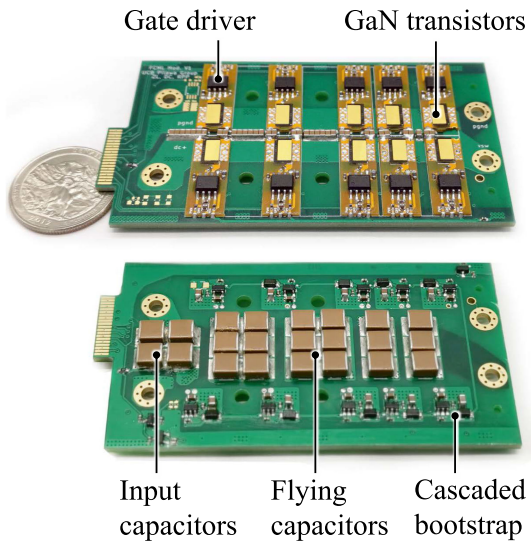

Fig. 14. 6-Level FCML module with a US quarter for size reference.

gate drivers, and cascaded bootstrap method for floating gate driving power [28]. The dimensions of the FCML module are 87 mm $\times$ 49 mm $\times$ 6.4 mm, which correspond to 27.3 cm ^{3} of box volume. The full buffer hardware prototype is constructed with two FCML modules mounted on a control and sensing board as shown in Fig. 15. Two LT1999 current amplifiers are placed on the ground return path to sense i_{dc} and i_{inv} with 5 mΩ shunt resistors as shown in Fig. 16. The proposed control scheme and all the PWM signals are digitally implemented in the Texas Instruments C2000 Delfino DSP. The output terminals for v_{CB} are connected to the buffer capacitor. For the buffer capacitor, the film capacitors tested in this article are two 450-V, 40-μF TDK B32776G4406K, which result in a maximum voltage V_{CB}

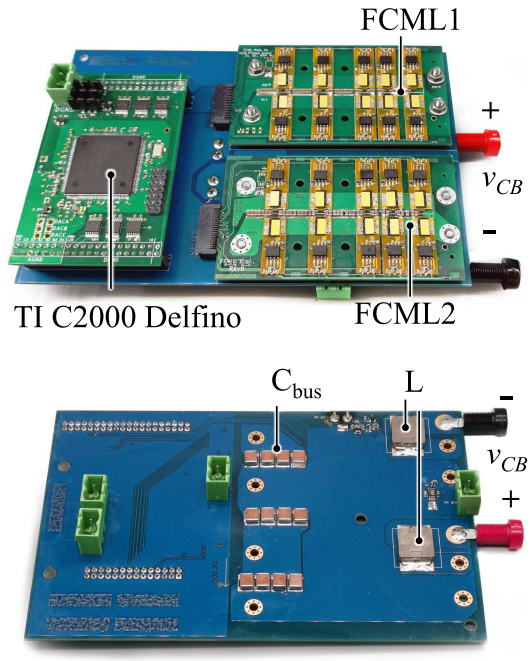

Fig. 15. Tested buffer hardware. The dc–ac converter is implemented with a full-bridge converter with two FCML legs.

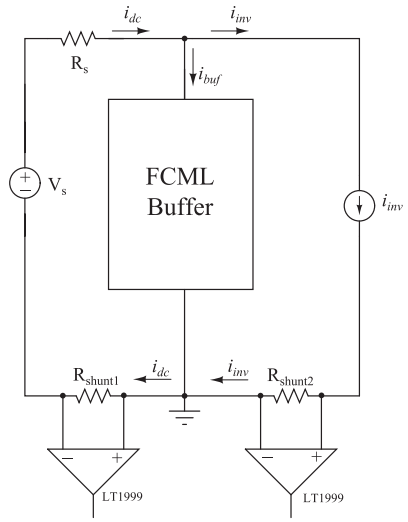

Fig. 16. Current sensing circuitry with two shunt resistors and current amplifiers.

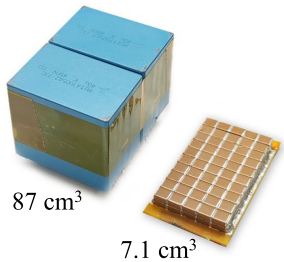

Fig. 17. Buffer capacitor size comparison between the tested film capacitors (TDK B32776G4406 K) and MLCCs (TDK C5750X6S).

TABLE I
KEY COMPONENT LIST OF THE BUFFER CONVERTER

Component	Part number	Parameters
GaN transistors	GaN Systems GS1008T	100 V, 7 mΩ
GaN gate driver	Silicon Lab Si8271	
Flying capacitors	TDK C5750X6S × 36	2.2 μF, 450 V
dc-bus capacitors	TDK C5750X6S × 20	2.2 μF, 450 V
Inductors	Vishay IHLW5050 × 2	6.8 μH, 18 A
Buffer capacitors	TDK B32776G4406K (film) × 2	40 μF, 450 V
	TDK C5750X6S (MLCC) × 100	2.2 μF, 450 V

TABLE II
VOLUMES OF PASSIVE COMPONENTS

Passive components	Volume (cm^3)
C_{buf} (Film)	87.02
C_{buf} (MLCC)	7.1
C_{fly}	2.87
C_{bus}	1.60
L	1.13

of 364 V at 2 kW dc power based on (5). In the case with MLCCs, 100 TDK C5750 capacitors are connected in parallel and constructed as a single block. As simulated in Fig. 9, the corresponding peak voltage for 100 TDK C5750 is 371 V. The two buffer capacitors are shown in Fig. 17 for size comparison. The filter inductors and other key components are listed in Table I. For the 2-kW test, the buffer is tested with no heatsink attached to the FCML modules and only airflow from an electric fan.

Accounting for the volume of all the passive components (C_{bus}, C_{buf}, filter inductors, flying capacitors) in the main power stage, the power density of the hardware by passive component volume is 21.6 W/cm^3 (354 W/in^3) with film capacitors, and 157.5 W/cm^3 (2581.1 W/in^3) with MLCCs. The volume breakdown of passive components in the main power stage is listed in Table II.

VI. EXPERIMENTAL VERIFICATIONS

The experimental setup includes a dc voltage source of 450 V, a 10 Ω source resistor, and an electronic load operated in current load mode to emulate an inverter load with unity power factor. The buffer converter is tested up to 2 kW with no heatsink, and the efficiency is measured with Keysight PA2201 A power analyzer. It should be noted that the buffer efficiency in this work is the two-port efficiency used in [4], [29]. With two-port efficiency, the buffer is treated as a cascaded stage between the dc source and the inverter. As a result, the buffer efficiency can be directly multiplied for calculating the system efficiency with the inverter or PFC stage.

A. Results With Film Capacitors

Figs. 18 and 19 show the steady-state operation under the condition of 400 V dc-bus, and 2-kW dc power, using film capacitors as C_{buf}. DC source current i_{dc}, buffer capacitor voltage v_{CB} and i_{CB}, and the differential FCML switching node

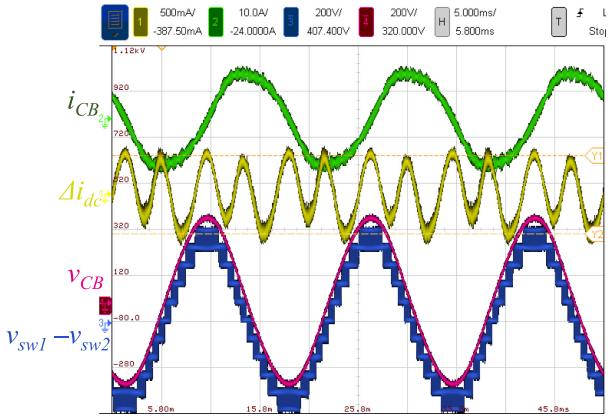

Fig. 18. Experimental waveforms of the proposed buffer with film capacitors controlled with only feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. Without third harmonic compensation, the dc current ripple is 850 mA. Test condition: 400 V dc bus, 2 kW dc power.

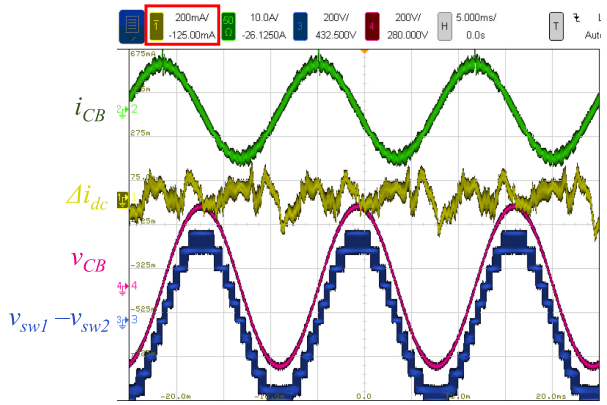

Fig. 19. Experimental waveforms of the proposed buffer with film capacitors controlled with additional third harmonic compensation, along with feedforward and PR compensator. The dc source current i_{dc} is ac-coupled to showcase the ripple component. As shown, the dc-side current has much lower ripple component of only 200 mA with third harmonic compensation. Test condition: 400 V dc bus, 2 kW dc power.

voltage $v_{sw1} - v_{sw2}$ are monitored. In both figures, the switching node voltages demonstrated excellent voltage balancing of the flying capacitors through natural balancing alone. As can be seen in Fig. 18, with only feedforward and PR compensator at the line frequency, the buffer capacitor's voltage and current are obviously distorted, and the buffer converter is not able to perfectly cancel the twice-line frequency component in i_{inv}, resulting in 850 mA ripple on the dc-side current. With an additional third harmonic resonant compensation term, the buffer capacitor voltage is less distorted, and the resulting ripple component in the dc-side current is reduced to 200 mA, as shown in Fig. 19. The corresponding ripple current ratio is 4%, which is significantly lower than the common limit of 20% [16]. This ripple ratio is equivalent to having a 6.6 mF physical capacitor at the dc-bus, if a passive capacitor bank solution is used. The harmonic can be further suppressed if resonant compensator at higher order of harmonics is included [19]. While the presented voltage control method for the film capacitor has already managed to suppress

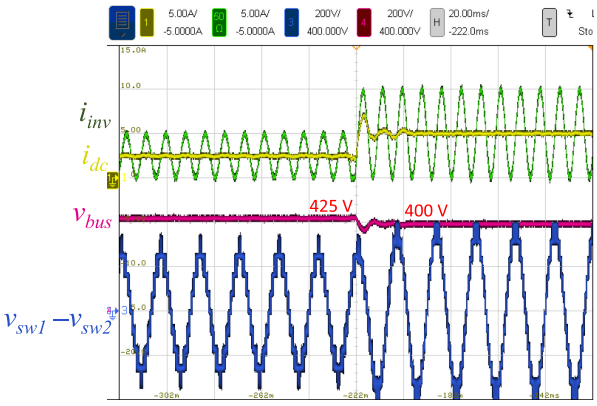

Fig. 20. Experimental waveforms of the proposed buffer during load step up. The dc-side current steps from 2.5 to 5 A.

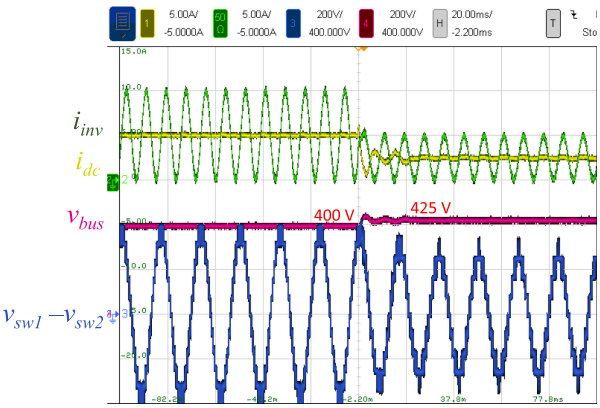

Fig. 21. Experimental waveforms of the proposed buffer during load step down. The dc-side current steps from 5 to 2.5 A.

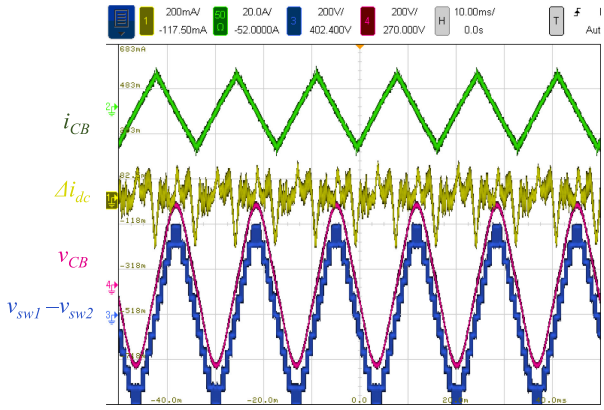

Fig. 22. Experimental waveforms of the buffer with MLCCs controlled with the proposed power harmonic elimination scheme. The dc source current i_{dc} is ac-coupled to showcase the ripple component. As shown, the dc-side current has low ripple component of only 300 mA, resulting from the low-harmonic buffer power. Test condition: 400 V dc bus, 2 kW dc power.

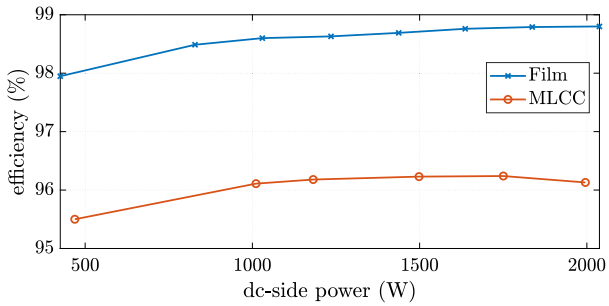

Fig. 23. Measured buffer efficiencies of using both film capacitor and MLCC as buffer capacitors.

the ripple ratio to 4% using ideal constant capacitance value in the control software, to compensate for slightly different capacitance due to part variation and aging, a feedback loop can be designed to monitor the ripple content in the dc-side current.

Figs. 20 and 21 show the transient behavior of the buffer during load stepup and stepdown, respectively. The emulated single-phase inverter power steps from 1 to 2 kW in Fig. 20 and steps down from 2 to 1 kW in Fig. 21. In both cases, the control is able to adjust the magnitude of v_{CB} to the new load condition after one line cycle and suppress the harmonic in v_{CB} to minimize the dc current ripple. Note that the dc-bus voltages changes accordingly due to the 10 Ω source resistance.

B. Results With X6S MLCCs

The steady-state operating waveform with the MLCCs as the buffer capacitor at 2 kW and 400 V dc-bus is shown in Fig. 22. It can be seen that with the proposed power harmonic elimination technique, the dc-side current has only 300 mA ripple component, which is 6% of the dc average current. The low ripple indicates that the buffer power contains low harmonic, demonstrating the effectiveness of the proposed control.

C. Loss Comparison

The tested buffer efficiencies of using both film capacitors and MLCCs are plotted in Fig. 23. As can be seen, the buffer with the film capacitors maintains higher efficiency than the MLCCs across the full load range.

While both the peak voltage and current in the FCML converters are slightly higher in the case with the MLCCs, which leads to higher loss in the converters, the major difference in the overall loss is from the MLCC buffer capacitors. The large voltage swing on the MLCCs induces high dielectric hysteresis loss besides the ESR conduction loss. As tested in [11], the loss density of the TDK C5750 under 60 Hz, 400 V peak-to-peak sinusoidal voltage at 60°C is 3 W/cm^3. At 2 kW in the bipolar buffer, the peak-to-peak voltage swing on the buffer capacitor is 742 V, and thus a loss density higher than 3 W/cm^3 is expected for the buffer application.

The estimated loss composition at 2 kW of both buffers is provided in Fig. 24. The individual contributions from the device switching, device conduction, inductors, and buffer capacitors are also labeled on the sides of the stacked bar diagram. The

TABLE III
COMPARISON TO OTHER HIGH-PERFORMANCE ACTIVE BUFFERS

Reference	[4]	[6]	This work (film cap)	This work (X6S MLCC)
Power rating (kVA)	2	2	2	2
Buffer capacitor type	MLCC	MLCC	Film	X6S MLCC
Effective buffer capacitor energy density	0.38 J/cm^3	0.41 J/cm^3	0.06 J/cm^3	0.74 J/cm^3
Total effective buffer capacitance	150 μF (350 V)	100 μF (450 V)+ 430 μF (80 V)	80 μF	77.5 μF (effective with 371 V peak)
Total capacitor volume (cm^3)	**24.6**	**28.1**	**87**	**7.1**
Total passive volume (cm^3)	**31.2**	**32.9**	**92.6**	**12.7**
Energy utilization	49%	46%	100%	100%
Efficiency @ 2 kW	98.65%	99.3%	98.8%	96.12%
Dc-side ripple ratio @ 2 kW	$<$ 3%	15%	4%	6%

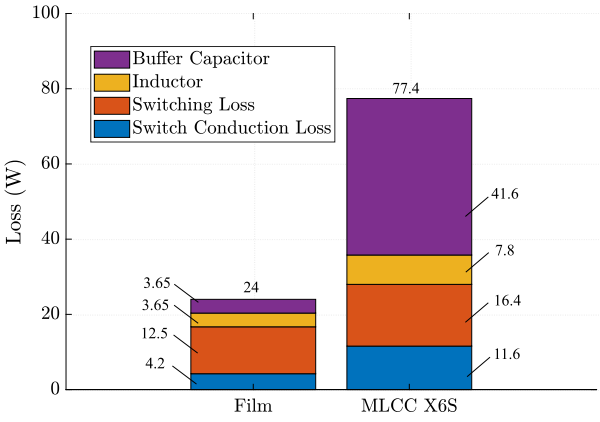

Fig. 24. Estimated loss composition of the buffer converters with film capacitor and MLCC.

loss on the buffer capacitors are estimated by subtracting the converter loss from the total loss. The estimated loss density of MLCC is thus $\frac{41.6\text{W}}{7.1\text{cm}^3} = 5.9$ W/cm^3. On the other hand, the loss on the film capacitors is estimated to be 3.65 W, which is consistent with the tested high efficiencies (>99.5%) of film capacitors in [10].

Comparison of key performance metrics with other high power density active buffer solutions are presented in Table III. The efficiency with the film capacitors are comparable to other high-performance buffer solutions. With the MLCC, the volume of the buffer capacitor is three to four times smaller, yet the high dielectric loss led to relatively low overall buffer efficiency.

VII. CONCLUSION

The proposed multilevel bipolar active power pulsation buffer allows minimum energy storage on the buffer capacitor for single-phase conversion, while shrinking the switching-frequency filtering passive component size with the FCML topology. The proposed active decoupling control schemes are able to regulate dc-side current with low ripple contents for both linear film capacitors and nonlinear MLCCs. We have also demonstrated that the proposed control schemes with multiple compensators, digital filters, and tens of PWM signals can be implemented with a commercially available DSP controller.

APPENDIX

A. Mathematical Proof of Odd Voltage Harmonic Injection to Eliminate Power Harmonics for MLCC

As shown in the simulation and experimental results, injecting the correct amount of negative odd harmonics in the voltage results in the elimination of even harmonics in the power for MLCC. As shown in Fig. 6, the strongest harmonics in the MLCC current with pure sinusoidal capacitor voltage are the third and fifth harmonics. As such, to simplify the calculation, the capacitor voltage v_{MLCC} is normalized to be $\sin(\omega t)$, and the current is normalized and represented as

$$i_{\text{MLCC}} = \cos(\omega t) + A\cos(3\omega t) + B\cos(5\omega t) \tag{13}$$

where A and B are positive numbers to reconstruct the current waveform in Fig. 6. Consequently, the MLCC power is

$$\begin{aligned} P_{\text{MLCC}} &= v_{\text{MLCC}} i_{\text{MLCC}} \\ &= \sin(\omega t)(\cos(\omega t) + A\cos(3\omega t) + B\cos(5\omega t)) \end{aligned} \tag{14}$$

which can be simplified using product-to-sum trigonometric identities as

$$\begin{aligned} P_{\text{MLCC}} = \frac{1}{2}((1-A)\sin(2\omega t) + (A-B)\sin(4\omega t) \\ + B\sin(6\omega t)). \end{aligned} \tag{15}$$

As can be observed, the power contains unwanted contents at fourth and sixth harmonics, which are related to the third and fifth current harmonic magnitude A and B. Moreover, the magnitude of the main 120 Hz component is also reduced by A. To cancel the fourth and sixth harmonics in the power, additional terms are needed to cancel the fourth harmonic term $(A-B)$ and sixth harmonic term B. By injecting negative third and fifth voltage harmonic, the voltage is modified to be

$$v_{\text{MLCC,inject}} = K(\sin(\omega t) - X\sin(3\omega t) - Y\sin(5\omega t)) \tag{16}$$

where X and Y are the magnitudes of the injected third and fifth voltage harmonic, respectively, and K is the overall scalar to adjust the main 120 Hz power component. In reality, the injected third and fifth voltage harmonics will introduce new current harmonics at higher frequencies. However, since the magnitudes of the injected third and fifth voltage harmonics are much lower than the fundamental voltage, the newly introduced harmonic contents can be neglected for this calculation. The

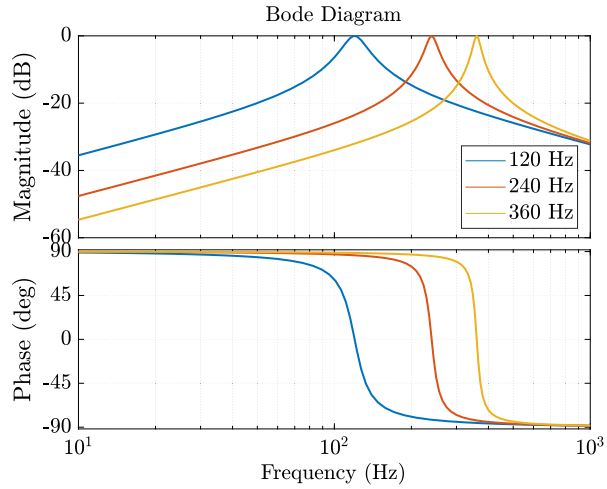

Fig. 25. Bode plots of three peak filters with center frequencies at 120, 240, and 360 Hz.

resulting capacitor power is

$$P_{\text{MLCC,inject}} = \frac{K}{2}((1 - A - X + BX - AY)\sin(2\omega t) + (A - B - X - Y)\sin(4\omega t) + (B - AX - Y)\sin(6\omega t)). \quad (17)$$

The resulting eighth and tenth harmonics are omitted for simplicity in this expression as their magnitudes are small. With the correct values of X and Y, the terms $(A - B - X - Y)$ and $(B - AX - Y)$ can be zero to eliminate the fourth and sixth harmonics in the power. The proposed control in Fig. 25 can determine the values of X and Y with the feedback loop by sensing the fourth and sixth harmonic contents in the input dc current. Furthermore, for the main 120 Hz power ripple to match the pulsating power in the overall single-phase system, K is also adjusted by the feedback loop by sensing the 120 Hz component in the dc current.

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