A Family of Dual-Boost Bridgeless Five-Level Rectifiers With Common-Core Inductors

Hui Ma, *Member, IEEE*, Kaitong Zheng, Hao Jiang, and Hongpeng Yin

***Abstract*—In this article, a family of dual-boost bridgeless five-level rectifiers with common-core inductors is proposed, which is composed of two coupled inductors, one bidirectional switch unit, and the dual-boost bridgeless power factor correction (PFC) rectifier. A bidirectional switch unit is embedded in the midpoint between the two capacitors and the bridge arm of the dual-boost bridgeless PFC (DBBL-PFC) to directly generate the five-level waveforms in each line cycle. The proposed topologies have the characteristics of lower voltage/current stresses and low total harmonic distortion. Additionally, the proposed five-level rectifiers employ a pair of common-core coupled inductors at the input side to replace the inherent independent inductors to improve the core utilization and the power density. First, the characteristics of the proposed topologies are analyzed and compared, and one of the topologies is taken as an example to illustrate its operating principle. Second, the modulation strategy with strong topology applicability and control system is designed for the proposed topologies. The advantage of the proposed pulsewidth modulation method is that it only needs to change the pulse distribution of the five-level topology to realize the five-level rectification, and the program debugging is simple. Then, the coupled inductors are designed, compared, and analyzed by the equivalent model in detail. Finally, a rated output of 1 kW/400 V experimental prototype is built, and the experimental results are presented to demonstrate the performance and effectiveness of the proposed topologies.**

***Index Terms*—Coupled inductor, five-level bridgeless power factor correction (PFC) circuit, pulsewidth modulation (PWM), single-phase rectifier.**

I. Introduction

RECENTLY, there are increasing demands for achieving lower total harmonic distortion (THD), higher power factor, high power density, and high reliability in a variety of power factor correction (PFC) rectifiers, such as motor drive, frequency conversion air conditioning system, and electric vehicles [1]–[4].

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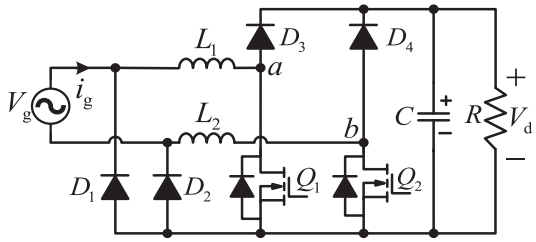

Fig. 1. Schematic diagram of DBBL-PFC.

Among many PFC rectifiers, the bridgeless PFC is popularly used due to its simple structure, continuous input current, and high power factor characteristics [5]–[7].

The bridgeless PFC can not only improve the power factor and reduce the input current THD but also play an important role in improving the overall efficiency of the system due to eliminating the diode bridge [9]–[11]. Usually, bridgeless PFC circuits mainly include the basic bridgeless PFC, the dual-boost bridgeless PFC (DBBL-PFC), as shown in Fig. 1, and the totem-pole dual-boost PFC [5]–[7]. Especially, the DBBL-PFC rectifier, as shown in Fig. 1, produces a dual-boost circuit in every half-cycle and has lower common-mode noise than the basic bridgeless boost PFC rectifier [13], [14]. However, the major drawback of the DBBL-PFC is that both of the inductors are operating at each half-cycle alternately, which increases the size and weight of the total rectifier system. Hence, in order to reduce the volume and increase the utilization of the magnetic material, it is an effective solution of employing an integrated dual-coupled inductor to replace two independent inductors [15], [16].

The semiconductor devices in the DBBL-PFC suffer from the excessive voltage and current stresses, causing more burden of the high conduction losses. In order to improve the efficiency and the system performance, the multilevel technology has been widely considered as a better solution, and the multilevel PFC rectifiers have lower switching losses and lower harmonic components compared with the three-level rectifiers [17]–[19]. In addition, the multilevel PFC rectifiers generate a multilevel voltage waveform between two bridge arms on the input side, which can decrease the harmonic content with a small-size L filter. Also, the multilevel rectifiers can increase the power density and reduce the filter with low current ripples. Both semiconductor components and gate driving circuits of the multilevel rectifiers are more than that used in three-level rectifiers, and the control circuit becomes relatively complicated. Hence, how

to realize a multilevel PFC rectifier with high efficiency, low cost, and low THD is still a challenge. The derived multilevel topologies based on the three-level Vienna rectifier technique achieve not only multilevel voltage but also utilize a smaller number of active switches compared with the conventional diode neutral point clamped (NPC) multilevel structure [20]–[23]. After analyzing both of the applications, the NPC-PFC can enable operation in bidirectional power, so it is a fact that the quantitative comparison of active switches is not enough, and the application and hardware costs need to be considered too. In unidirectional power applications, the tradeoff between the multilevel performance and cost needs to be considered for deducing the multilevel topologies. As a result, the multilevel topologies of the bridgeless PFC with better performance and lower cost are expected, especially in the lighting power and communicated power.

Based on the above description, the three-level PFC rectifiers have been replaced by multilevel PFC technologies, especially in medium-voltage applications. Therefore, a family of five-level bridgeless PFC topologies, derived from the DBBL-PFC using the bidirectional switch, have been proposed in this article, and that considers the size and the cost of the total rectifier system; two common-core coupled inductors are applied to the proposed topologies, which reduces the use of a pair of magnetic cores, reduces the cost, and the weight and volume of the rectifier, as shown in Fig. 2. The proposed dual-boost bridgeless five levels are named, respectively, according to the topological structure characteristics; Fig. 2(a)–(c) are uniformly defined as bridgeless five-level rectifiers with bidirectional switch (BFR-BS), where the topology is shown in Fig. 2(a) as BFR-BS-I, in 2(b) as BFR-BS-II, and in 2(c) as BFR-BS-III; and Fig. 2(d) and (e) show that a bridge arm in the bridgeless five-level rectifiers topology has four ports [as shown in the dotted box in Fig. 2(d) and (e)], which are defined as bridgeless five-level rectifier with four-port cell (BFR-FC), where the topology, as shown in Fig. 2(d), is defined as BFR-FC-I and in 2(e) as BFR-FC-II.

The organization of this article is listed as follows. A family of dual-boost bridgeless five-level rectifiers with common-core inductors is proposed, the characteristics of the proposed topologies are analyzed and compared, and one of the topologies is taken as an example to illustrate its operating principle in Section II. More importantly, Section III proposes a novel carrier-based sinusoidal pulsewidth modulation (NCB-SPWM) method with strong topology versatility and applicability that ensures efficient and stable operation of the rectifier system, and the desired five-level waveform can be finally obtained by selecting the appropriate operation mode. In addition, the proportional–resonant (PR) controller is applied to the current loop, which is also designed and that can realize the zero-error tracking of source variables in the fundamental frequency. Two common-core coupled inductors are also designed by analyzing the mechanism under the coupling effect, and the effect of leakage inductance and magnetic core mismatch causing input current ripple are discussed in detail in Section IV. The experimental results are presented in Section V. Finally, Section VI presents the conclusion in this article.

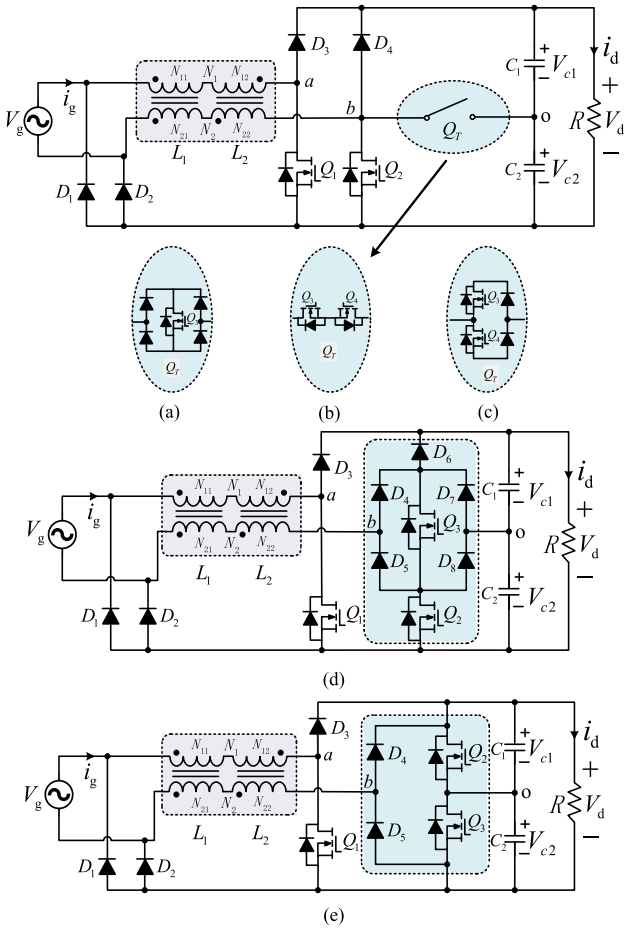

Fig. 2. Family of dual-boost bridgeless five-level rectifiers with common-core inductors. (a) BFR-BS-I. (b) BFR-BS-II. (c) BFR-BS-III. (d) BFR-FC-I. (e) BFR-FC-II.

TABLE I
VOLTAGE STRESS ANALYSIS OF MOSFET FOR THE PROPOSED TOPOLOGIES

Voltage stress	BFR-BS-I	BFR-BS-II	BFR-BS-III	BFR-FC-I	BFR-FC-II
$0.5V_o$	Q_3	Q_3、Q_4	Q_3、Q_4	Q_2、Q_3	Q_2、Q_3
V_o	Q_1、Q_2	Q_1、Q_2	Q_1、Q_2	Q_1	Q_1

II. TOPOLOGIES COMPARISON AND OPERATION PRINCIPLE

A. Topology Characteristics and Comparison

Table I presents the voltage stress analysis results of MOSFETs used in the five proposed topologies. It can be seen from Table I that three switches (Q_1, Q_2, and Q_3) are required for BFR-BS-I, BFR-FC-I, and BFR-FC-II, respectively. For BFR-BS-I, the number of switches with the voltage stress of 0.5 V_o accounts for one-third of the total number of switches, while for BFR-FC-I and BFR-FC-II, the number of switches with voltage stress of 0.5 V_o accounts for two-third. Four switches (Q_1, Q_2, Q_3, and Q_4) are required for BFR-BS-II and BFR-BS-III, and the number of switches withstanding the voltage stress of $0.5V_o$ and V_o accounts for half, respectively. From the point of view of a small number of switches and low voltage stress, BFR-FC-I and BFR-FC-II have significant advantages.

TABLE II
NUMBER OF POWER DEVICES AND THE RATED VOLTAGE IN THE CURRENT PATH UNDER DIFFERENT LEVELS

Levels	Device (Number×Rated voltage)				
	BFR-BS-I	BFR-BS-II	BFR-BS-III	BFR-FC-I	BFR-FC-II
$+V_o$	3×*D*6	3×*D*6	3×*D*6	2×*D*4, 2×*D*6	3×*D*6
$-V_o$	3×*D*6	3×*D*6	3×*D*6	2×*D*4, 2×*D*6	3×*D*6
$+0.5V_o$	2×*D*4, 2×*D*6, 1×*Q*4, 1×*Q*6	1×*D*4, 2×*D*6, 1×*Q*4, 1×*Q*6	1×*D*4, 2×*D*6, 1×*Q*4, 1×*Q*6	2×*D*4, 2×*D*6, 2×*Q*4	3×*D*6, 1×*Q*4
$-0.5V_o$	2×*D*4, 2×*D*6, 1×*Q*4	1×*D*4, 2×*D*6, 1×*Q*4	1×*D*4, 2×*D*6, 1×*Q*4	2×*D*4, 2×*D*6, 1×*Q*4	3×*D*6, 1×*Q*4
+0	2×*D*6, 1×*Q*6	2×*D*6, 1×*Q*6	2×*D*6, 1×*Q*6	2×*D*4, 1×*D*6, 1×*Q*6	2×*D*6, 1×*Q*6
-0	2×*D*6, 1×*Q*6	2×*D*6, 1×*Q*6	2×*D*6, 1×*Q*6	1×*D*4, 2×*D*6, 2×*Q*4	3×*D*6, 2×*Q*4
Total	4×*D*4+4×*D*6+1×*Q*4+2×*Q*6	2×*D*4+2×*D*6+2×*Q*4+2×*Q*6	2×*D*4+4×*D*6+2×*Q*4+2×*Q*6	5×*D*4+3×*D*6+2×*Q*4+1×*Q*6	5×*D*6+2×*Q*4+1×*Q*6

Note: *D*4 and *D*6 represent the diodes with rated voltages of 400 V and 600 V, respectively; *S*4 and *S*6 represent the switches with rated voltages of 400 V and 600 V, respectively.

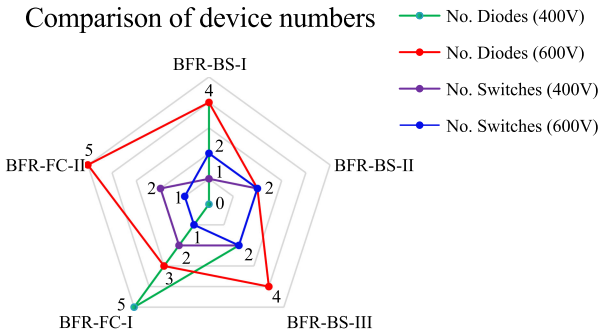

Fig. 3. Comparison of the number and rated voltage of power devices in different topologies.

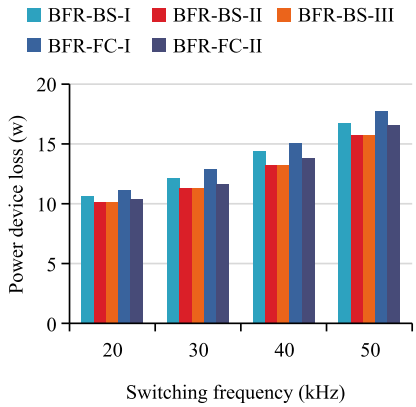

Fig. 4. Device losses distribution of the proposed five topologies under different switching frequencies.

Table II presents the number of switching devices in the current paths of the five proposed topologies at different levels as well as the rated voltage and the total number of power devices required for each topology. From the analysis in the table, it can be seen that the number of conductive devices in the current path of the BFR-BS-II and BFR-BS-III topologies in all levels is the same, so the switching losses of the two are similar. At $\pm 0.5V_o$ levels, BFR-BS-I has one more diode in the conduction state than BFR-BS-II and BFR-BS-III, respectively, so the loss is slightly higher. In the multilevel state, the number of conductive devices in the current path of BFR-FC-I topology is more than that of BFR-FC-II, so the loss is slightly higher than that of BFR-FC-II. In addition, the BFR-FC-II has a flexible structure, and its modulation form has two types of A and B. The main difference lies in the $\pm 0.5V_o$ level, as shown in the pulse distribution diagram in Fig. 7. Therefore, from the perspective of modulation flexibility, the BFR-FC-II topology is simpler and the pulse distribution is flexible.

In order to clearly show the total number and rated voltage of power devices used in the proposed five topologies, a comparative analysis of the number of devices is carried out in combination with Table II and Fig. 2, as shown in Fig. 3. In terms of total switch number, BFR-BS-II uses two less diodes than BFR-BS-III, but compared with BFR-BS-I, BFR-BS-II reduces the use of four diodes and only adds one switch, so the cost of BFR-BS-II is lower. The number of diodes used in BFR-FC-I is three more than that in BFR-FC-II, while the number of switches used is the same, all of which are three. In terms of cost, BFR-FC-I is higher than BFR-FC-II.

The switching loss plays an important role in the overall efficiency of a rectifier, which mainly includes the losses of MOSFETs and diodes, especially the turn-ON loss, turn-OFF loss, and conduction loss account for a relatively high proportion. The detailed loss calculation method and device losses distribution at different switching frequencies are given in [24], which verifies that the proposed five-level topologies have lower switching loss at the low switching frequency. The device loss distribution of the proposed five topologies under different switching frequencies is shown in Fig. 4. It can be seen from Fig. 4 that, under the condition of rated output power, as the switching frequency increases, the switching loss gradually increases. The theoretical calculation results in Fig. 4 are consistent with the analysis in Table II. Topologies BFR-BS-II and BFR-BS-III have the same and lowest switching loss. Topologies BFR-BS-I and BFR-FC-II have slightly higher switching losses. Among all topologies, topology BFR-FC-I has the highest switching loss, which is mainly related to the number of devices in the current flow path and the operating mode in each mode.

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGIES WITH OTHER FIVE-LEVEL TOPOLOGIES

Parameter	Topology								
	BFR-BS-I	BFR-BS-II	BFR-BS-III	BFR-FC-I	BFR-FC-II	In [12]	In [19]	In[20]	In[26]
No. of switches	3	4	4	3	3	4	6	3	8
No. of diodes	8	4	6	8	5	6	2	8	4
No. of inductors	2	2	2	2	2	1	2	1	1
No. of capacitors	2	2	2	2	2	2	3	4	2
No. of gate drivers	3	4	4	3	3	4	6	3	8
Power flow	UPF	UPF	UPF	UPF	UPF	UPF	BPF	UPF	BPF

Note: UPF - Unidirectional power flow; BPF - Bidirectional power flow.

B. Compared With Other Multilevel PFC Rectifiers

A family of dual-boost bridgeless five-level rectifiers with common-core inductors is derived from the topology DBBL-PFC, which retains and improves the characteristics and performance of the topology DBBL-PFC and uses fewer switching devices to achieve multilevel. Table III presents the number comparison of the components between the proposed topologies and other five-level topologies. Compared with the articles presented in [12], [18], and [25], the number of switches of the proposed five topologies is significantly reduced, especially the number of switches in topologies BFR-BS-I, BFR-FC-I, and BFR-FC-II uses only three, respectively. For the number of diodes used, the proposed topologies BFR-BS-II and BFR-FC-II have the most advantages. The number of inductors has little difference, while the number of capacitors is more used in [18] and [19]. The gate driver circuits are more used in [18] and [25], and least used in topologies BFR-BS-I, BFR-FC-I, BFR-FC-II, and the article presented in [19], which also reduces the hardware cost. The proposed five topologies can realize unidirectional power flow, reduces the use of devices, avoids power backflow, and improves power supply reliability.

Therefore, combined with the comparative analysis of Section II-A and B, it can be selected and applied according to the following topological characteristics.

1) Cost advantage: Topologies BFR-BS-II or BFR-FC-II can be preferred.
2) Modulation flexibility: Topology BFR-FC-II can be given priority.
3) Switching loss advantage: Topologies BFR-BS-II and BFR-BS-III can be considered first.
4) Lower switching voltage stress: Topologies BFR-FC-I and BFR-FC-II are more advantageous.
5) Low common-mode noise: The proposed topologies all have this advantage, and the main reason is that the existence of diodes D_1 and D_2 makes the output terminal and the input terminal connected [5], [14].

C. Operation Principle

In order to further understand the features of the proposed dual-boost bridgeless five-level rectifiers with common-core inductors, the BFR-BS-I, as shown in Fig. 2(a), is taken as an example to analyze the operation principle, and the BFR-BS-I topology is composed of an ac voltage source V_g, two coupled inductors (L_1 and L_2), two capacitors (C_1 and C_2), three switches (Q_1, Q_2, and Q_3), and eight diodes (D_1–D_8). Fig. 5 presents the current paths of the six operation modes, and this circuit operates symmetrically during the positive and negative half-cycle. Moreover, the switch states are listed in Table IV, where "1" and "0" indicate the "ON" and "OFF" states of the power switches, respectively. In the following, the six operation modes of the BFR-BS-I are analyzed in detail.

TABLE IV
SELECTION OF SWITCH STATE AND SYSTEM PARAMETERS UNDER SIX OPERATION MODES

Modes		Switching states			System parameters					
		Q_1	Q_2	Q_3	i_1	i_o	i_2	C_1	C_2	V_{ab}
$i_g > 0$	1	0	0	0	i_g	0	i_g	Charge	Charge	$V_{c1}+V_{c2}$
	2	0	1	1	i_g	$-i_g$	0	Charge	Discharge	V_{c1}
	3	1	0	0	0	0	0	Discharge	Discharge	+0
	4	0	1	0	0	0	0	Discharge	Discharge	-0
$i_g < 0$	5	0	0	1	0	i_g	i_g	Discharge	Charge	$-V_{c2}$
	6	0	0	0	i_g	0	i_g	Charge	Charge	$-(V_{c1}+V_{c2})$

Mode 1: When the voltage V_{ab} is $+V_d$, all the active switches are OFF. The positive line current i_g charges both capacitors C_1 and C_2 to achieve voltage $V_{ab} = V_{c1}+V_{c2} = +V_d$, and the dc-side currents $i_1 = i_2 = i_g$ and $i_o = 0$. The equivalent circuit of this mode is shown in Fig. 5(a).

Mode 2: Q_2 and Q_3 are ON. At this time, capacitor C_1 is charged by the positive line current i_g, and the dc load current discharges the capacitor C_2. During this state, the voltage $V_{ab} = +V_{c1} = +V_d/2$, correspondingly, and the dc-side currents $i_1 = i_g$, $i_o = -i_g$, and $i_2 = 0$ as the equivalent circuit are shown in Fig. 5(b).

Mode 3: The switch Q_1 turns ON to obtain the bridge-arm voltage $V_{ab} = +0$. In this mode, the positive line current i_g is linearly increasing. Meanwhile, two capacitors C_1 and C_2 are discharging and supplying power to dc load R. The dc-side currents $i_1 = i_2 = i_o = 0$ as the equivalent circuit are shown in Fig. 5(c).

Mode 4: In this mode, Q_2 is ON, and the voltage V_g is short circuited through the coupled inductor, as shown in Fig. 5(d). During this period, the capacitors C_1 and C_2 discharge energy to the load R and the voltage $V_{ab} = -0$. The dc-side currents are $i_1 = i_2 = i_o = 0$.

Mode 5: Q_3 turns ON to obtain the bridge-arm voltage $V_{ab} = -V_{c2} = -V_d/2$. At the same time, the negative line current

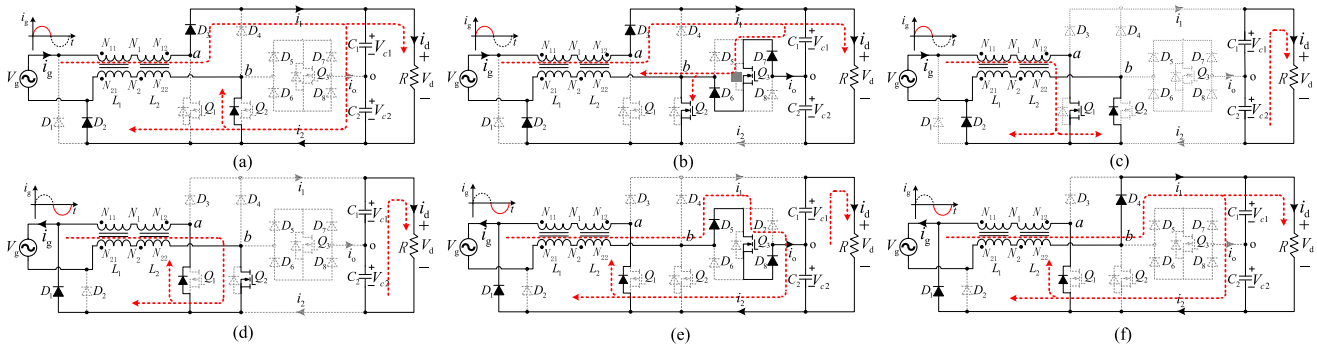

Fig. 5. Current flow path during different output voltage levels. (a) $V_{ab} = +V_d$. (b) $V_{ab} = +V_d/2$. (c) $V_{ab} = +0$. (d) $V_{ab} = -0$. (e) $V_{ab} = -V_d/2$. (f) $V_{ab} = -V_d$.

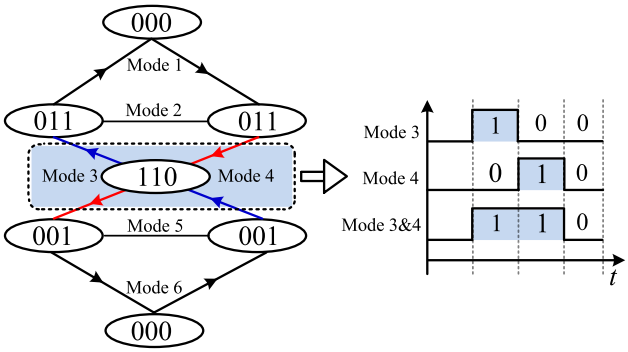

Fig. 6. Circulation process diagram of six operation modes.

charges the capacitor C_2 and the capacitor C_1 is discharged by the dc load. The dc-side currents $i_1 = 0$, and $i_o = i_2 = i_g$ as the equivalent circuit are shown in Fig. 5(e).

Mode 6: During this operating state, all switches are OFF to obtain the bridge-arm voltage $V_{ab} = -V_{c1} - V_{c2} = -V_d$. At the moment, capacitors C_1 and C_2 are charged by the negative line current and current i_g decreases linearly. The dc-side currents $i_o = 0$, and $i_1 = i_2 = i_g$ as the equivalent circuit are shown in Fig. 5(f).

There are two current return paths. In the positive half-cycle, the sum of induced voltages at both ends of the same direction series' windings N_{21} and N_{22} located in the negative half-cycle is zero. Similarly, in the negative half-cycle, the sum of induced voltages at both ends of the reverse series' windings N_{11} and N_{12} located in the positive half-cycle is also zero, which is equivalent to the independent dual inductors operating in the positive and negative half-cycle. It means that the energy in the coupled inductor flows from the primary side to the secondary side in one cycle.

From the above operation analysis, the proposed dual-boost bridgeless five-level rectifiers can produce six voltage levels, which are obtained by the proper pulsewidth modulation (PWM) scheme of each switch. In addition to these states, the cycle process of the six operating modes is also shown in Fig. 6, where the bridge-arm voltages $+0$ and -0 are generated by modes 3 and 4, respectively. In order to reduce the control complexity of the commutation process and the transition process of switching action, the bridge-arm voltages $+0$ and -0 are superimposed to complete the "0" level state output, which will be analyzed in detail in the proposed modulation scheme (in Section III-A).

III. Modulation Scheme and Control Strategy

A. Modulation Scheme

Fig. 7 shows the specific PWM modulation process block diagram of the proposed five topologies, which mainly include three parts: logic comparison module (LCM), mode selection module (MSM), and pulse distribution module (PDM). The proposed modulation principle is similar to the conventional CB-SPWM modulation method, all using multicarrier modulation technology; the conventional CB-SPWM algorithm generates pulse sequence waves by comparing sine modulation waves with multicarriers, which is directly used as switch pulse driving signal to achieve multilevel output. However, in the process of modulation, there are obvious differences between the implementation steps of the proposed NCB-PWM modulation and CB-PWM. In the LCM, the four in-phase and equal amplitude triangular carriers v_i (i = 1, 2, 3, 4) are logically compared with the modulation wave $V_{\rm ref}$, and the reference voltage signal $V_{\rm ref}$ output by the inner loop of the control system is a sine wave in phase with the input voltage V_g and current i_g. The sine modulation wave expression is written as

$$V_{\rm ref} = M \sin(\omega t + \theta) \tag{1}$$

where M is the modulation wave coefficient, the variation range of M is [0,1], and the angular frequency of the modulation wave is ω. The four carrier signals are represented as follows:

$$v_i = \begin{cases} v_1 \in [0.5, 1] \\ v_2 \in [0, 0.5] \\ v_3 \in [-0.5, 0] \\ v_4 \in [-1, -0.5] \end{cases} \quad (i = 1, 2, 3, 4)\,. \tag{2}$$

Five groups of level signals with an amplitude of 1 are generated through the LCM and the LCM waveform, as shown in Fig. 8(a). In order to obtain the five step level waveforms, as shown in Fig. 7, the amplitude gain of each group of level signals is 1, 2, 3, 4, and 5 times, respectively, and then accumulate the amplitude of the five levels after gain to obtain the

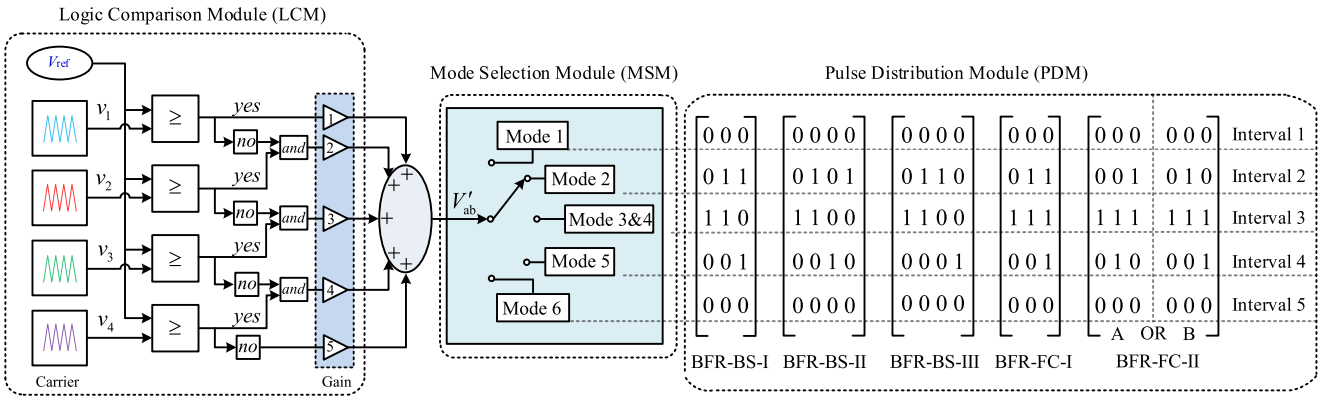

Fig. 7. PWM modulation process block diagram.

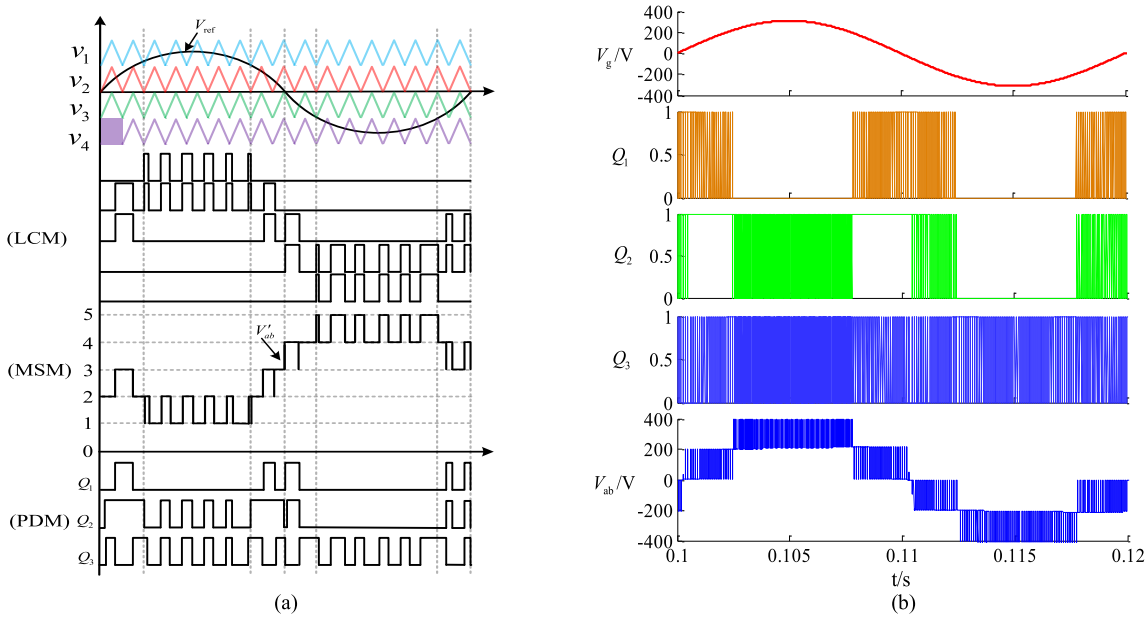

Fig. 8. Theoretical waveform and the simulation results of the proposed PWM technology. (a) Theoretical waveform. (b) Simulation results ($M = 0.9$).

quasi-step level waveform V'_{ab}, which is the phase opposite to the bridge-arm voltage V_{ab} and the V'_{ab} waveform, as shown in Fig. 8(a).

In this LCM, using this design method is to divide the state interval of the five-level waveforms in one line cycle, which is similar to the SVPWM sector division principle. The sinusoidal quasi-step level waveform is obtained in the previous stage LCM in order to achieve a high-frequency five-level waveform V_{ab} in phase with the input voltage and current between the bridge arms a and b; in the MSM, the five-level states after pulse synthesis are sorted according to Mode 1→Mode 2→Mode 3 and 4→Mode 5→Mode 6 to adjust the level output. The interval divisions, level states, and the switch pulses distribution results of the five topologies in this article are shown in Fig. 7 (PDM). The implementation principle of the switch pulse distribution result corresponds to the level switching process and pulse synthesis method in Fig. 6. Among them, there is only one pulse distribution method of topologies BFR-BS-I, BFR-BS-II, BFR-BS-III, and BFR-FC-I, while the topology BFR-FC-II pulse distribution method has two types, A and B, with high flexibility of pulse distribution.

As described above, the drive and control of switches (Q_1, Q_2, and Q_3) for BFR-BS-I can be achieved by further selecting the sequence of the operating modes. In fact, mode 3 and mode 4 are the same state quantity for level "0 " state output. As a consequence, the ideal five-level voltage V_{ab} waveform of the bridge arm can be generated. The pulse distribution waveforms of three switches in BFR-BS-I are shown in Fig. 8(a), and the corresponding simulation waveforms are shown in Fig. 8(b). It can be seen that the adopted PWM method has strong versatility and verifies the correctness of the PWM strategy. In addition, for different five-level rectifiers, as long as their pulses are allocated correctly, this method can be used for modulation, which greatly simplifies the process of programming and debugging, and reduces the hardware cost; it has certain engineering application value.

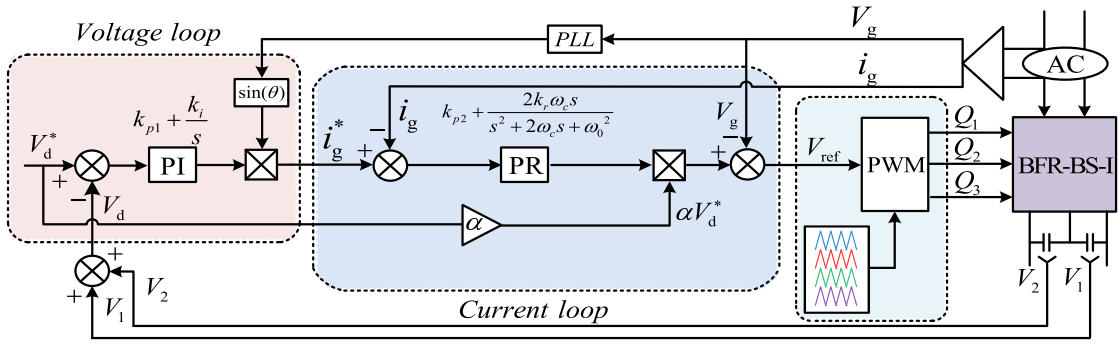

Fig. 9. Simplified control diagram of the BFR-BS-I rectifier system.

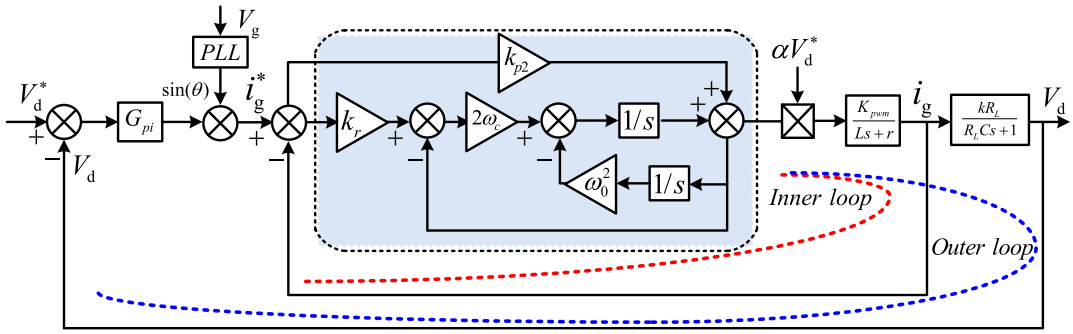

Fig. 10. Block diagram of the system transfer function.

B. Control Strategy

Fig. 9 shows a simplified control block diagram of the BFR-BS-I system. The topologies proposed in this article should focus on achieving the current balance control of the two inherent coupled inductors on the input side. If the tracking effect of current is not ideal, the harmonic content will greatly increase, which directly leads to a rapid decline in power factor. Furthermore, once out of control, a large peak current will be generated, the balance ability of the two capacitors will be affected, and even damage the equipment in serious cases. To improve the tracking ability of the control system to the ac reference and dc reference, a combined control strategy of the voltage outer loop (proportional Integral (PI) controller with the characteristic of tracking dc reference without static error) and current inner loop (PR controller with the characteristic of tracking ac reference without static error) is adopted in this article. The voltage loop is used to maintain the dc output voltage constant by employing a PI controller. The output signal of the voltage loop is taken as the input current reference of the current inner loop. The reference current signal output by the outer loop voltage control and the phase-locked loop can be expressed as

$$i_g^* = [k_{p1}(V_d^* - V_d) + k_i \int (V_d^* - V_d)dt] \frac{V_g}{|V_g|} \sin(\theta) \quad (3)$$

where k_{p1} is the proportional gain, k_i denotes the integrational gain, and $|V_g|$ and $\sin(\theta)$ are the amplitude and phase information of the mains voltage V_g, respectively.

The detailed block diagram of the inner loop and the outer loop transfer function is shown in Fig. 10. The current loop is used to control the input current by taking the advantage of the proportional–resonance (PR) control to accurately track the reference current signal and ensure that it is in phase with the mains voltage. In addition, in order to avoid the effect of mains voltage disturbance on the normal operation of the system, a voltage feedforward compensation link is introduced to take into account the dynamic- and steady-state performance of the rectification control system. The transfer function of the PR controller is as follows:

$$G_{\rm pr}(s) = k_{p2} + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_0{}^2} \quad (4)$$

where k_{p2} is the proportional gain, k_r is the resonance gain, ω_0 is the resonant frequency, and ω_c is the cutoff frequency.

As described above, in order to study the impact of PR controller parameters on the system performance, one of the parameters will be changed, while the other parameters will remain unchanged. Fig. 11 shows the bode diagram of the PR controller at different parameter values k_{p2}, k_r, and ω_c. First, the magnitude–phase relationship is given in Fig. 11(a) when k_r changes. It can be seen that the gain of the proportional–resonant controller increases with the increase of k_r, while k_r has little effect on the resonant bandwidth. Therefore, the gain of the controller peak value is proportional to the k_r value. Considering the influence of cutoff frequency ω_c on the system performance, let $k_{p2} = 1$ and $k_r = 100$, and the bode diagram of the PR controller changes with ω_c, as shown in Fig. 11(b). It can be

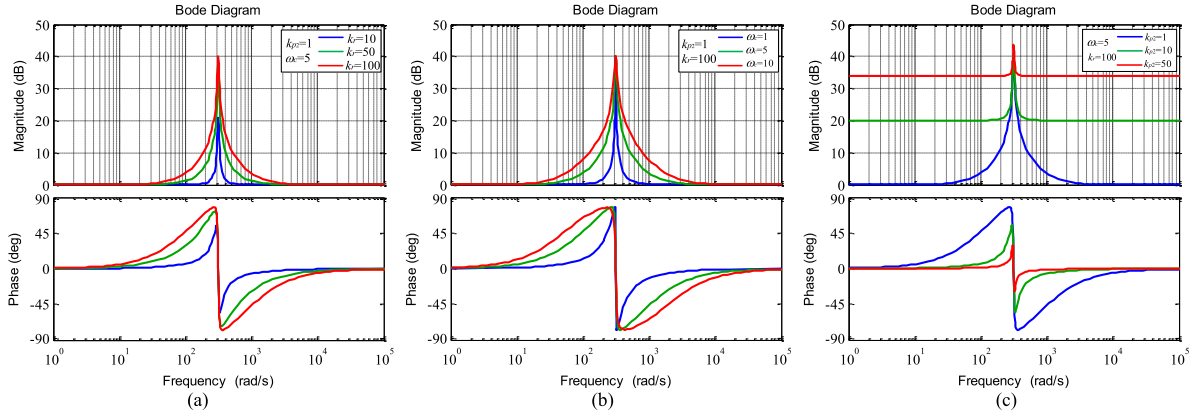

Fig. 11. Bode diagram of PR controller at different parameter values K_p, K_r, and ω_c.

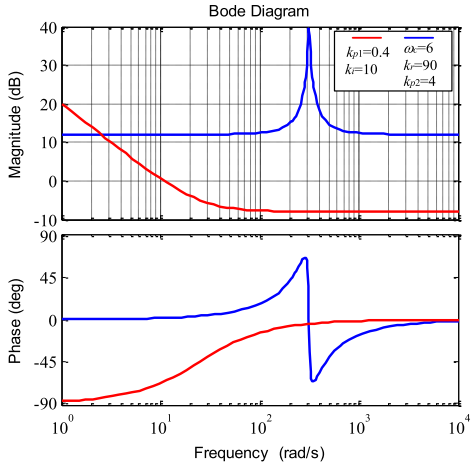

Fig. 12. Bode diagram of PI (in red) +PR (in blue) control system based on the experimental parameters.

seen that the change of ω_c will not only cause the change of gain but also changes the bandwidth of the controller. When k_{p2} changes, let $\omega_c = 5$ and $k_r = 100$, and the bode diagram is shown in Fig. 11(c). It can be seen from the figure that the change of k_{p2} does not change the resonance bandwidth and resonance gain, indicating that the role of the resonance link does not increase indefinitely with the increase of k_{p2} value. After a certain limit, the resonance link tends to a stable state. k_{p2} mainly affects the gain of the controller at the nonresonant frequency, so the disturbance can be suppressed by choosing a proper proportional coefficient.

In order to get a better performance in the experiment, the bandwidth is adjusted appropriately to adapt to the influence of power grid frequency change, which is helpful to suppress the generation of harmonics. The controller parameters are selected as follows: $k_{p1} = 0.4$, $k_i = 10$, $\omega_c = 6$, $k_r = 90$, $k_{p2} = 4$, and $\omega_o = 100\pi$, and the bode diagram of the controller is shown in Fig. 12. It can be seen that the PI controller has infinite gain at zero frequency, which improves the steady-state performance of the system. Compared with the PI controller, the amplitude–frequency characteristic of the PR controller at the fundamental frequency is $A(\omega_0) = 40$ dB, and the phase angle margin is infinite, so it can achieve zero steady-state error and has good steady-state margin and transient performance.

The goal of the controller is to minimize the error between the desired control objectives and their references; for this reason, the design of the closed-loop control parameters of the system is also very important. Without considering the slight disturbance of the grid voltage, the current closed-loop transfer function in this control system is

$$G_{\mathrm{cl}}(s) = \frac{\alpha V_d^* K_{\mathrm{pwm}} G_{\mathrm{pr}}(s)/(Ls+r)}{1+\alpha V_d^* K_{\mathrm{pwm}} G_{\mathrm{pr}}(s)/(Ls+r)} = \frac{1}{1+(Ls+r)/(\alpha V_d^* K_{\mathrm{pwm}} G_{\mathrm{pr}}(s))} \tag{5}$$

where L is the inductive filter value, r is the line impedance, K_{pwm} is the equivalent gain of the PWM rectifier bridge, and α is the reference voltage proportional coefficient ($\alpha = 0.55$). The relationship among the output dc voltage, the load, and dc capacitor can be expressed as

$$G_{\mathrm{rec.out}}(s) = \frac{V_d}{i_s} = \frac{kR_L}{R_L C s + 1}. \tag{6}$$

Based on Figs. 9 and 10, the open-loop transfer function of the whole system can be given as

$$G_{\mathrm{ol}}(s) = G_{\mathrm{pi}}(s) G_{\mathrm{cl}}(s) G_{\mathrm{rec.out}}(s) = \frac{G_{\mathrm{pi}}(s) G_{\mathrm{rec.out}}(s)}{1+(Ls+r)/(\alpha V_d^* K_{\mathrm{pwm}} G_{\mathrm{pr}}(s))}. \tag{7}$$

Then, the closed-loop transfer function of the whole system control loop can be expressed as

$$G_{\mathrm{wl}}(s) = G_{\mathrm{ol}}(s)/\left(1+G_{\mathrm{ol}}(s)\right). \tag{8}$$

IV. Design and Analysis of Coupled Inductors

A. Design of Coupled Inductors

A family of dual-boost bridgeless five-level rectifiers with common-core inductors is proposed in this article, and all have the characteristics of multilevel output. In order to make the proposed topologies have better operating performance in the

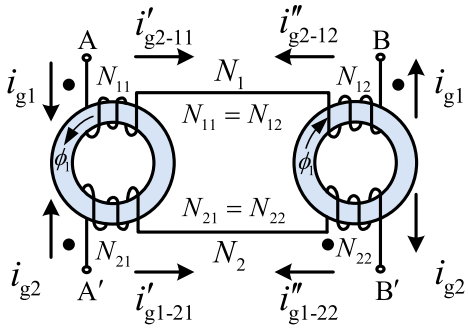

Fig. 13. Dual-coupled common-core inductors.

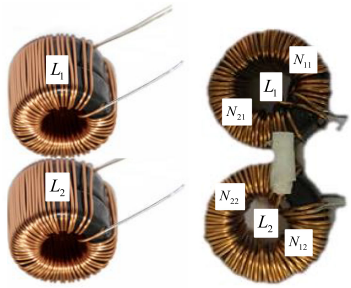

Fig. 14. Picture of the constructed two types of inductance structure. (a) Dual-core winding type. (b) Single-core coupled type.

positive and negative half-cycle, the structure model of the dual-coupled common-core inductors is drawn in Fig. 13. The specific process of coupled inductor design is as follows.

The turn ratio of the four windings is N_{11}:N_{12}:N_{21}:$N_{22} = 1$ in which the windings N_{11} and N_{21} are wound in the same direction by a common magnetic core. Nevertheless, the windings N_{12} and N_{22} are wound in the opposite direction by a common magnetic core. In fact, the leakage inductance of each winding is much lower than the magnetizing inductance, and the coupling coefficient is approximately $k_1 = k_2 = 1$, which means that the leakage inductance can be ignored. In other words, the coupled inductor can be regarded as an ideal transformer with a turn ratio of 1:1 and a magnetizing inductance L_m in parallel. During the positive half-cycle operation, the input current i_{g1} flows through the windings N_{11} and N_{21}, according to the principle of electromagnetic induction, and equal magnetic flux $\phi_1(t) = N_{11}i_{g1}(t) = N_{12}i_{g1}(t)$ will be generated in the two cores. The induced current of windings N_{21} and N_{22} can be calculated as

$$\begin{cases} i'_{g1-21}(t) = \frac{N_{11}}{N_{21}} i_{g1}(t) \\ i'_{g1-22}(t) = \frac{N_{12}}{N_{22}} i_{g1}(t). \end{cases} \tag{9}$$

The opposite induced currents i'_{g1-21} and i'_{g1-22} are generated in winding N_2 as the winding direction of winding N_{21} is opposite to that of N_{22}, as shown in Fig. 13; the total induced current i_{g1-2} of winding N_2 is 0 ($i_{g1-2} = i'_{g1-21} + i'_{g1-22} = 0$). Similarly, the total induced currents i_{g2-1} generated in the winding N_1 by current i_{g2} flowing through winding N_2 are 0 during the negative half-cycle ($i_{g2-1} = i'_{g2-11} + i'_{g2-12} = 0$).

TABLE V
INDUCTANCE PARAMETERS IN TOPOLOGIES

Parameters	Fig. 14(a)	Fig. 14(b)
Core size (mm)	44 (OD)*28 (ID)*30 (HT)	40 (OD)*22 (ID)*14 (HT)
Core material	High flux, TYH series	High flux, TYH series
Coil parameters	AWG#16	AWG#15
Turns (N)	N_{L1}=N_{L2}=60	N_{N11}=N_{N12}=N_{N21}=N_{N22}=32
Number of cores	4	2
Volume ratio	3:1	

Fig. 14 shows two types of inductance structures. Fig. 14(a) is a dual-core winding type and Fig. 14(b) is a single-core coupled type. Table V presents the inductor materials and coil winding methods used in the DBBL-PFC rectifier and the proposed five-level rectifiers with common-core inductors. It can be seen that in terms of the number of turns and the material of the winding, the difference between the two is not obvious, but the single-core coupled type reduces the use of a pair of magnetic cores, and the volume ratio in Fig. 14(a) and (b) is about 3:1 by calculation. Compared with the dual-core winding type, the size of the coupled inductor used is significantly reduced. As demonstrated in [15] and [16], the number of magnetic components can be reduced by integrating magnetic components, such as transformers and inductors on the same core. Therefore, it can be seen from the analysis of Fig. 14 and Table V that the coupled inductors reduce the use of a pair of magnetic cores, so the utilization rate of magnetic cores is significantly improved.

In summary, the induced current and voltage generated by two identical coupled inductors can cancel each other in one line cycle, which is of great benefit to reduce the inductance loss. Consequently, the magnetizing inductor L_m can be idealized as the energy storage filter inductor L for theoretical analysis, and the topologies proposed in this article can achieve the same operation performance as the DBBL-PFC with independent dual inductors by rationally designing the winding method of inductance coil and turns ratio of the dual-coupled common-core inductors.

B. Equivalent Inductance Model

Under the actual condition, the main performance of the coupled inductors is limited by the manufacturing level, accompanied by a small amount of leakage inductance and magnetic core mismatch. In the derivation, the relevant analysis is as follows: In the steady-state operation mode, obviously, the coupled inductors can be regarded as a parallel combination of a magnetizing inductance and an ideal transformer, and then in series with a leakage inductance. The equivalent structure is shown in Fig. 15, where L_{m11}, L_{m21}, L_{m12}, and L_{m22} are the magnetizing inductances, L_{k11}, L_{k21}, L_{k12}, and L_{k22} are the leakage inductances, and M is the mutual inductance coefficient.

Based on the design of the coupled inductor in Section IV-A above, the voltage and current relationship ($u_{11} = u_{21}$, $u_{12} = -u_{22}$, $i_{11} = -i_{21}$, and $i_{12} = i_{22}$) in each winding can be obtained from the principle of the transformer, where each winding is the same (including the number of turns and material of winding),

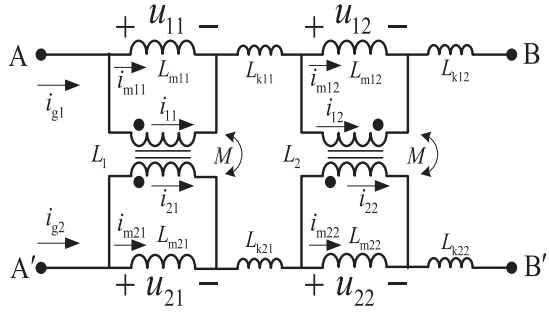

Fig. 15. Equivalent structure of the dual-coupled common-core inductors with leakage inductance.

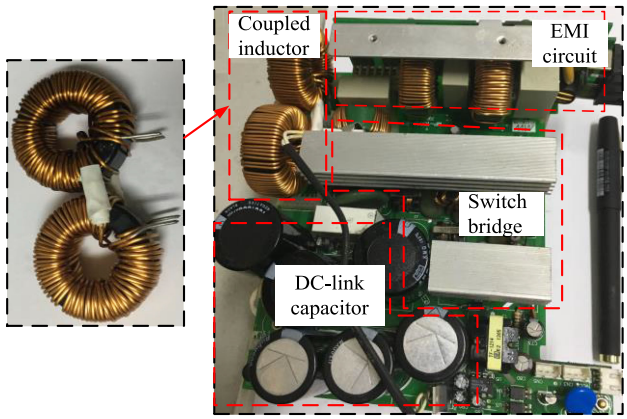

Fig. 16. Experimental prototype platform.

that means $L_{m11} = L_{m21} = L_{m1}$, $L_{m12} = L_{m22} = L_{m2}$, and the direction of each parameter is depicted in Fig. 15. The input current relationship of the proposed rectifiers during the positive and negative half cycles by applying Kirchhoff's law can be expressed as

$$\begin{cases} i_{g1} = i_{m11} + i_{11} = i_{m12} + i_{12} \\ i_{g2} = i_{m21} + i_{21} = i_{m22} + i_{22}. \end{cases} \tag{10}$$

The voltage relationship of magnetizing inductance on each winding is as follows:

$$\begin{cases} u_{11} = L_{m1} di_{m11}/dt = u_{21} = L_{m1} di_{m21}/dt \\ u_{12} = L_{m2} di_{m12}/dt = -u_{22} = -L_{m2} di_{m22}/dt. \end{cases} \tag{11}$$

According to (3), i_{m11}=i_{m21} and i_{m12}=$-i_{\mathrm{m22}}$ can be derived, and then the two equations are, respectively, substituted into (10); combined with formulae i_{11}=$-i_{21}$ and i_{12}=i_{22}, the following expressions are obtained by adding and subtracting i_{g1} and i_{g2}.

$$\begin{cases} i_{g1} + i_{g2} = i_{12} + i_{22} = i_{m11} + i_{m21} \\ i_{g1} - i_{g2} = i_{11} - i_{21} = i_{m12} - i_{m22}. \end{cases} \tag{12}$$

For the convenience of analysis, i_{m1} and i_{m2} are introduced to represent the current relationship as follows:

$$\begin{cases} i_{m1} = i_{12} = i_{22} = i_{m11} = i_{m21} \\ i_{m2} = i_{11} = -i_{21} = i_{m12} = -i_{m22}. \end{cases} \tag{13}$$

According to (12) and (13), the positive and negative half-cycle currents are simplified as

$$\begin{cases} i_{g1} = i_{m1} + i_{m2} \\ i_{g2} = i_{m1} - i_{m2}. \end{cases} \tag{14}$$

Since the sum of the induced voltages on the two coupled inductors in each mode is zero, the voltages at the A–B terminal and A′–B′ terminal are expressed as

$$\begin{cases} u_{\mathrm{A'B'}} = u_{21} + u_{22} + L_{k2} di_{g2}/dt = 0 \\ u_{\mathrm{AB}} = u_{11} + u_{12} + L_{k1} di_{g1}/dt = 0 \end{cases} \tag{15}$$

where $L_{k1} = L_{k11}$+L_{k12} and $L_{k2} = L_{k21}$+L_{k22}. Substituting (11), (13), and (14) into (15), the relationship of i_{m1} and i_{m2} can be derived as (16) and (17) by further integrating and simplifying

$$i_{m1} = ((L_{m2} + L_{k2}/2)/(L_{m1} + L_{k2}/2))\, i_{m2} \tag{16}$$

$$i_{m2} = -((L_{m1} + L_{k1}/2)/(L_{m2} + L_{k1}/2))\, i_{m1}. \tag{17}$$

Substituting (16) and (17) into (14), eliminating i_{m1} and i_{m2}, the expressions of the induced current ripple can be derived by the positive and negative half-cycle currents i_{g1} and i_{g2} in the corresponding windings, as follows:

$$\begin{cases} i_{g2-1} = ((L_{m2} - L_{m1})/(L_{m1} + L_{m2} + L_{k1}))\, i_{g2} \\ i_{g1-2} = ((L_{m2} - L_{m1})/(L_{m1} + L_{m2} + L_{k2}))\, i_{g1}. \end{cases} \tag{18}$$

Equation (18) shows the relationship between the induced currents (i_{g1-2}, i_{g2-1}), input currents (i_{g1}, i_{g2}), magnetizing inductors (L_{m1}, L_{m2}), and leakage inductances (L_{k1}, L_{k2}). From the above analysis, it should be noted from (18) that the current in the coupled inductors circuit has no effect on each other when $L_{m1} = L_{m2}$. Ignoring the leakage inductance in the analysis of the rectifiers, the difference ΔL_m between L_{m1} and L_{m2} is limited to 5% ($\Delta L_m = |L_{m1}{-}L_{m2}|{<}5\%L_m$). According to (18), the range of induced current ripple in each winding can be calculated, as shown in (19), taking into account the filtering ability of inductance on current; the induced current in each winding is very small and has little effect on the sinusoidalization and harmonic content of input current. That is, the induced current ripple can be ignored.

$$\begin{cases} 0 \le i_{g2-1} \le 2.43\% i_{g2} \\ 0 \le i_{g1-2} \le 2.43\% i_{g1}. \end{cases} \tag{19}$$

V. Experimental Verifications

In this section, the main experimental results obtained with the BFR-BS-I are presented. The controller adopts DSP TMS320F28335, and the experimental waveforms are acquired with a Puyuan DS1054Z oscilloscope. The experimental circuit of the BFR-BS-I is shown in Fig. 16, and the parameters of the experimental circuit are listed in Table VI.

Fig. 17 shows the pulse distribution diagram of switches Q_1, Q_2, and Q_3. The PWM signal is amplified by the optocoupler isolation chip ACPL-W341 to a 15 V/20 kHz pulse signal to directly drive the three MOSFET switches. The time that Q_1 is in the switching action is relatively short, which can reduce the switching loss in the main loop. Q_2 has a moderate proportion of switching time, and Q_3 is always in the high-frequency operation state. However, according to Table I, it can be seen that Q_3 withstands the switching voltage of the half dc output voltage,

TABLE VI
PARAMETERS OF THE EXPERIMENTAL CIRCUIT

Parameters	Values
Input voltage V_g	220V
Output voltage V_d	400V
Grid frequency f_g	50Hz
Coupled inductors L_1/L_2	2mH
Capacitors C_1/C_2	990μF
Switching frequency f_s	20kHz
Rated power P_o	1kW
Diode	RHPR3060
High-voltage MOSFET	STW26NM60N
Controller chip	TMS320F28335

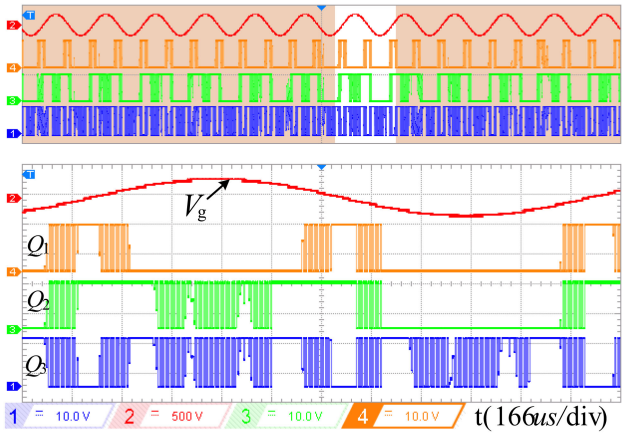

Fig. 17. Pulse distribution waveform of three switches in BTR-BS-I.

and the switching loss is also reduced due to low voltage stress. The pulse distribution in Fig. 17 corresponds to that in Table IV and Fig. 8, which is consistent with the theoretical analysis.

Fig. 18 shows the experimental waveform of BFR-BS-I topology operating in a steady state at 1 kW rated power. Fig. 18(a) shows the voltage and current of the grid side and two branch currents of the coupled inductors. From Fig. 18(a), the input voltage V_g in phase with the input current i_g and unity power factor is approximately realized. The currents i_{g1} and i_{g2} of the two branches of the coupled inductor are in a balanced state and operate alternately in the positive and negative half cycles with a peak value of about 6.43 A. Fig. 18(b) shows the voltage V_{ab} between the bridge arms a and b, the upper and lower capacitors voltage, and the dc output voltage waveforms. In Fig. 18(b), it can be seen that the voltage between the two bridge arms conforms to the operating characteristics of the five-level circuit, which is consistent with the theoretical analysis. The two capacitors' voltage waveforms are in dynamic balance, and the dc output voltage V_d is controlled stably at 400 V.

The THD analysis of the grid current is carried out at a rated power of 1 kW. Fig. 19(a) shows that, during the stable operation of the system, the grid-side voltage and current waveforms remain in phase to achieve a unity power

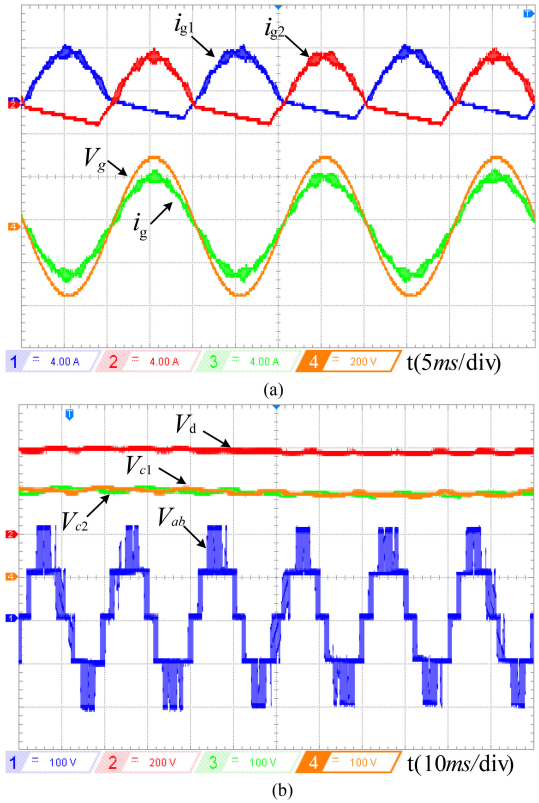

Fig. 18. Voltage and current waveform in steady state. (a) Grid-side voltage and current, and dual-coupled inductor current. (b) Input bridge-arm voltage V_{ab}, the dc output voltage V_d, and the capacitor voltage V_{c1} and V_{c2}.

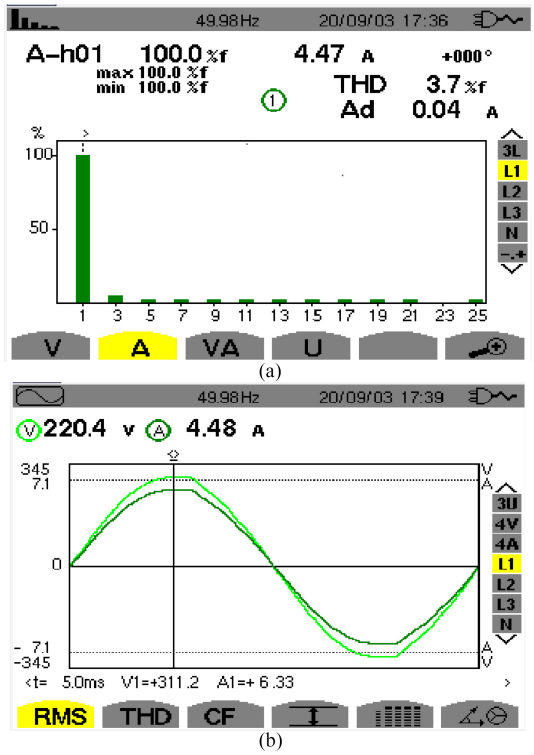

Fig. 19. THD analysis of grid current. (a) THD analysis. (b) Grid current and voltage waveform.

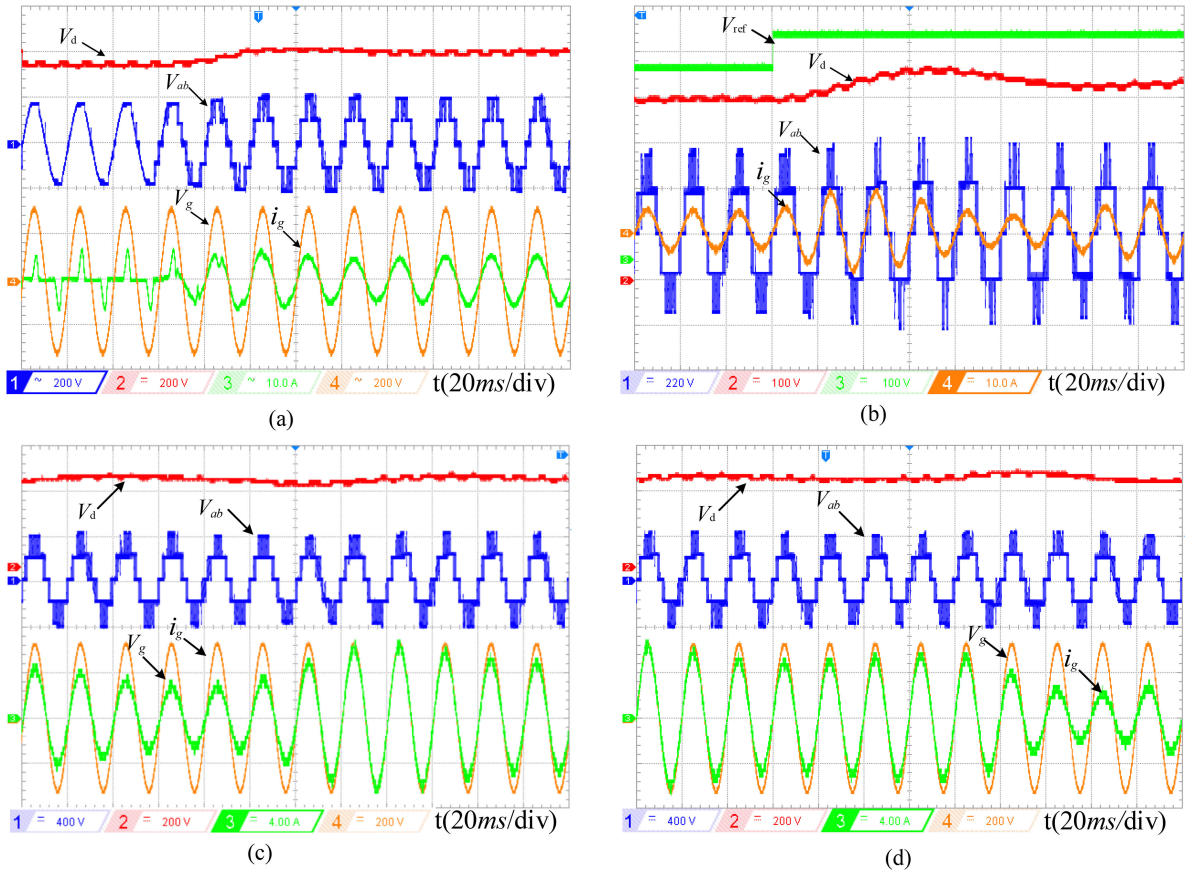

Fig. 20. Voltage and current waveforms in a dynamic state. (a) DC output voltage V_d, grid voltage V_g, input bridge-arm voltage V_{ab}, and input current i_g from startup to steady state. (b) Test results during V_{ref} increase from 400 to 450 V. (c) Test results during load from 160 to 80 Ω. (d) Test results during load from 80 to 160 Ω.

factor. Fig. 19(b) shows that the THD value of the proposed rectifier under the implemented controller is 3.70%, which meets the IEC 61000-3-2 standard and realizes the unity power factor.

Fig. 20 shows the relevant dynamic waveforms of the BFR-BS-I circuit. First, the BFR-BS-I circuit device is precharged for 30 s, and then the controller sends out a switching pulse after precharging. Fig. 20(a) shows the voltage and current waveforms of the BFR-BS-I during the process from uncontrollable to controllable. The device reaches a steady state after about two power supply cycles. The input current i_g has small distortion in the dynamic process and keeps in phase with the input voltage V_g; meanwhile, the voltage V_d is stable at 400 V. In the steady state of the BFR-BS-I circuit, when the reference voltage of dc side jumps from 400 to 450 V, as shown in Fig. 20(b), the voltage V_d changes with its reference value, and it takes about five power supply cycles to stabilize at about 450 V. The main reason is that there are two inductors in the input side of the topology, which leads to a relatively slow current change and a long stability process at the dc side.

The advantage is that the voltage V_d has a slightly inconspicuous overshoot process and the process is capable of coping with the impact of disturbance. It can be seen from Fig. 20 that when the reference value of dc voltage changes, the proposed five-level PFC topology can keep the input current in phase with the input voltage, realize unity power factor, and stabilize the dc voltage.

Fig. 20(c) and (d) shows the relevant voltage and current waveform with the load changes. The load is doubled from the rated power, that is, the load R jumps from 160 to 80 Ω in Fig. 20(c), and then jumps to the rated power state in Fig. 20(d). During the whole load jump process, the input current i_g and voltage V_g still maintain in phase, the current increases and decreases, and there are two power cycle fluctuations and the voltage V_d has gentle fluctuations. It can be seen from Fig. 20 that the proposed five-level PFC topology can still achieve unity PFC when the power fluctuates within twice the power range.

In order to further evaluate the quality of the input current, the input current harmonic spectrum of the proposed topology [see Fig. 2(a)] and the topology DBBL-PFC (see Fig. 1) is shown in Fig. 21, which was tested by using C.A 8335 under different operating frequencies at full load. It can be seen that the proposed topology has lower harmonic content at 20 and 50 kHz compared with the DBBL-PFC, and the test results show that it is below IEC 61000-3-2 standard.

Fig. 22 shows the efficiency comparison curves at different switching frequencies. It can be seen that the efficiency of the proposed topology decreases with the increase of switching frequency, which is due to the increase of power device loss caused by the increase of switching frequency. At 50 kHz, the

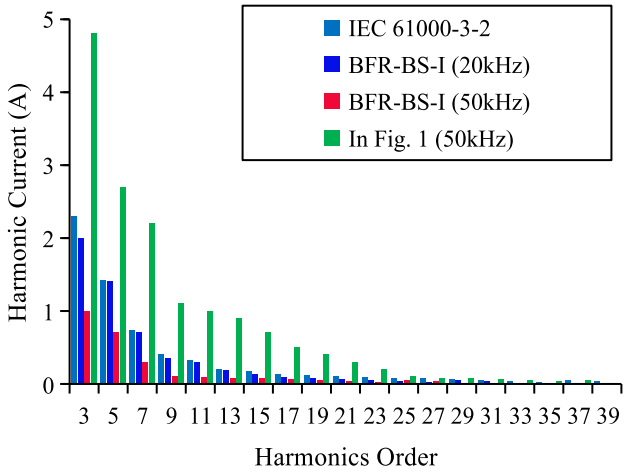

Fig. 21. Comparison of input current harmonics under different operating frequencies at full load.

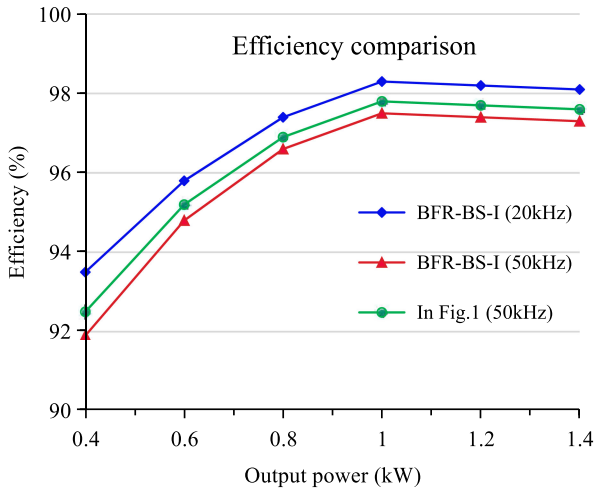

Fig. 22. Efficiency comparison curves at different switching frequencies.

TABLE VII
PERFORMANCE EVALUATION BETWEEN THE TOPOLOGY BFR-BS-I AND OTHER FIVE-LEVEL TOPOLOGIES

Test parameter	In [12] (3kW)	In[17] (1kW)	In [19] (395W)	In[20] (420W)	BFR-BS-I (1kW)
$\text{Efficiency}_{(max)}$	98.00%	99.05%	96.20%	95.13%	98.30%
THD	2.18%	3.50%	2.60%	5.60%	3.70%
Dynamic response	fast	normal	normal	low	fast
Switching frequency	140kHz	20kHz	20kHz	50kHz	20kHz
Grid frequency	60Hz	60Hz	50Hz	60Hz	50Hz

efficiency of the proposed topology is slightly lower than that of the circuit in Fig. 1. However, the system operates at 20 kHz, and the efficiency is significantly higher than that of the circuit in Fig. 1, which further verifies that the proposed topology can operate under low switching frequency conditions with high efficiency.

Table VII presents the performance between the proposed topologies and the other five-level topologies. The main test parameters are the maximum efficiency of the topology and the corresponding THD value. The test results show that different five-level topologies obtain different maximum efficiencies under different switching frequencies and power output levels. At the switching frequency of 140 kHz, the efficiency of the topology in [12] is 98.00% (3 kW and THD = 2.18%); when the switching frequency is 50 kHz, the efficiency of topology in [19] is 95.13% (420 W and THD = 5.60%). Under the same switching frequency (20 kHz), the efficiency of the pieces of literature [17] and [18] is 99.05% (1 kW and THD = 3.50%) and 96.20% (395 W and THD = 2.60%) respectively; the efficiency of the proposed topology BFR-BS-I is up to 98.30% at low switching frequency (20 kHz) and rated output power of 1 kW, and the current THD is 3.7%. The results show that the proposed topology has perfect dynamic performance, high efficiency, and low THD, and meets the system performance requirements.

VI. CONCLUSION

Based on the three-level dual-boost bridgeless rectifier, this article proposed a family of dual-boost bridgeless five-level rectifiers with common-core inductors, which can reduce the voltage stress of switch devices and improve core utilization and power density. Take the dual-boost bridgeless five-level rectifier (BFR-BS-I) as an example to explain its operating principle, modulation method, and controller design. An experimental prototype with a power of 1 kW was built, and the experimental results in steady state, step-up and step-down loads, and dc-link voltage reference variation have been experimented to verify that the proposed topologies can be good candidates for rectifiers with acceptable performance. Compared with the three-level dual-boost bridgeless rectifier, the proposed topologies can achieve sinusoidal current under low switching frequency conditions, and the current THD and switching loss are low and the working efficiency is higher.

REFERENCES

[1] K. S. B. Muhammad and D. D.-C. Lu, "ZCS bridgeless boost PFC rectifier using only two active switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2795–2806, May 2015.

[2] M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A soft-switching bridgeless AC–DC power factor correction converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.

[3] M. Alam, W. Eberle, D. S. Gautam, C. Botting, N. Dohmeier, and F. Musavi, "A hybrid resonant pulse-width modulation bridgeless AC–DC power factor correction converter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1406–1415, Mar./Apr. 2017.

[4] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.

[5] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.

[6] Y. Jang and M. M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.

[7] K. K.-M. Siu, Y. He, C. N. M. Ho, H. S.-H. Chung, and R. T.-H. Li, "Advanced digital controller for improving input current quality of integrated active virtual ground-bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3921–3936, Apr. 2019.

[8] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1833–1843, Jul./Aug. 2011.
[9] X. Liu *et al.*, "A high-efficiency single-phase AC/DC converter with enabling window control and active input bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2912–2924, Jun. 2012.
[10] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.
[11] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," *IET Power Electron.*, vol. 1, no. 2, pp. 194–202, Jun. 2008.
[12] A. D. B. Lange, T. B. Soeiro, M. S. Ortmann, and M. L. Heldwein, "Three-level single-phase bridgeless PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2935–2949, Jun. 2015.
[13] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
[14] A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martínez-Salamero, "Loss-free resistor-based power factor correction using a semi-bridgeless boost rectifier in sliding-mode control," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5842–5853, Oct. 2015.
[15] I. Laird, D. D.-C. Lu, and V. G. Agelidis, "High-gain switched-coupled-inductor boost converter," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 2009, pp. 423–428.
[16] T.-T. Nguyen, H. Cha, B. L.-H. Nguyen, and H.-G. Kim, "A novel single-phase three-level dual-buck inverter," *IEEE Trans. Power Electron.,* vol. 35, no. 4, pp. 3365–3376, Apr. 2020.
[17] J.-S. Kim, S.-H. Lee, W.-J. Cha, and B.-H. Kwon, "High-efficiency bridgeless three-level power factor correction rectifier," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1130–1136, Feb. 2017.
[18] V. Monteiro, J. C. Ferreira, A. A. N. Meléndez, and J. L. Afonso, "Model predictive control applied to an improved five-level bidirectional converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5879–5890, Sep. 2016.
[19] M. A. F. de Souza Kohler and D. F. Cortez, "Single-phase five-level flying-capacitor rectifier using three switches," *IEEE Open J. Power Electron.*, vol. 1, no. 1, pp. 383–392, Sep. 2020.
[20] H. Vahedi and K. Al-Haddad, "A novel multilevel multioutput bidirectional active buck PFC rectifier," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5442–5450, Sep. 2016.
[21] D. Liu, Y. Wang, F. Deng, and Z. Chen, "Balanced power device currents based modulation strategy for full-bridge three-level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 2008–2022, Feb. 2020.
[22] Z. Tang *et al.*, "Modulation for the AVC-HERIC inverter to compensate for deadtime and minimum pulsewidth limitation distortions," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2571–2584, Mar. 2020.
[23] D. Bao, X. Pan, and Y. Wang, "A novel hybrid control method for single-phase-input variable frequency speed control system with a small DC-link capacitor," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9016–9032, Sep. 2019.
[24] L. Zhang, K. Sun, Y. Xing, and J. Zhao, "A family of five-level dual-buck full-bridge inverters for grid-tied applications," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7029–7042, Oct. 2016.
[25] X. Zhang, G. Tan, T. Xia, Q. Wang, and X. Wu, "Optimized switching finite control set model predictive control of NPC single-phase three-level rectifiers," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10097–10108, Oct. 2020.

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