A 3-Leg Inverter-Based High-Frequency Welding Power Supply Capable of AC 220 and 440-V Operation

Duk-Hyeon Yun, Woo-Seok Lee, Jun-Young Lee, and Il-Oun Lee

***Abstract*—In this article, a dc/dc topology is proposed for welding power supply that achieves a high conversion efficiency of over 94%, requiring ac 220 and 440 V operation. The secondary-side structure of the proposed topology is the same as that of conventional welding power supplies but the primary side consists of a three-leg inverter structure and a high-frequency transformer with two primary windings connected in series. Due to this structure, it is possible to operate in a wider input voltage range than conventional welding power supplies without significant loss of performance. In addition, it has the advantage of achieving high conversion efficiency over the entire input voltage range by reducing primary current stress and secondary rectifying voltage stress due to an increase in turn-ratio, and a reduction in circulating current. This advantage allows the use of MOSFETs rather than insulated gate bipolar transistor (IGBTs) with low operating frequency, which are often used in conventional welding power supply applications. Using a MOSFET reduces the size of the power-stage passive devices, thereby reducing the overall system size. The performance of the proposed topology is verified in prototypes with a switching frequency of 100 kHz, an input voltage of 311/622 V, an output of 50 V, and a 6.0 kW class specification.**

***Index Terms*—Phase-shifted full-bridge topology, three-leg inverter, welding power supply.**

I. Introduction

WITH THE recent development of the steel, metal and material industries and the development of large-capacity power devices, a great deal of interest in the welding field has become focused on miniaturization, weight reduction, efficiency improvement, and precise output current control of welding power supplies [1]–[5]. Especially, in some areas such as shipbuilding, the distance between welding location and welding machine is very far due to their heavy weights so that loss dissipated in cable occupies 20%∼30% of total input power. To save this loss, welding power supply in welding machine should be light and small enough to be installed anywhere on welding location. In addition, it shall be possible to produce the output required for welding even at any input voltages including the output of a generator for the convenience of mobility. To meet these requirements, welding power supplies should be operated at high frequency without much loss of efficiency and be capable of operating with a wide input voltage range.

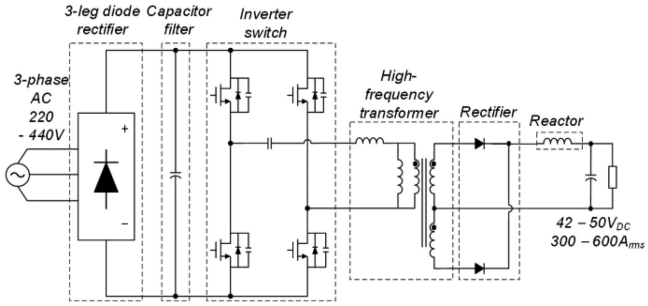

Fig. 1. Conventional welding power supply.

Fig. 1 shows the structure of conventional inverter-based welding power supplies. The welding power supply is a device that receives a three-phase system voltage as input and generates the low voltage output of 42–50 V and high current of 300–600 A required for welding industry [4], [5]. As shown in Fig. 1, it consists of a three-leg diode rectifier that rectifies the three-phase grid voltage, a filter capacitor for dc voltage smoothing, an inverter switch circuit, a high-frequency ferrite transformer, a high-frequency diode rectifier, and an inductor called reactor [6]–[8]. The circuit from the input filter capacitor to the output reactor can be seen as an isolated dc/dc converter. The voltage rectified through the three-leg bridge diode rectifier becomes the input voltage of the insolated dc/dc converter, which is about 311 V for ac 220 V and 622 V for ac 440 V. The isolated dc/dc converter for welding mainly adopts a phase-shift manner suitable for low voltage and high current output applications, and insulated gate bipolar transistor (IGBTs) suitable for high power are used as switching device. Due to the hard switching problem caused by IGBT current tailing, the switching frequency is generally around 10–20 kHz [9]–[11].

Despite the demand for welding machines with a wide input voltage range, conventional welding power supplies have been mainly developed with a single grid voltage specification of ac 220 or 440 V, not a specification that can use both ac 220/440 V

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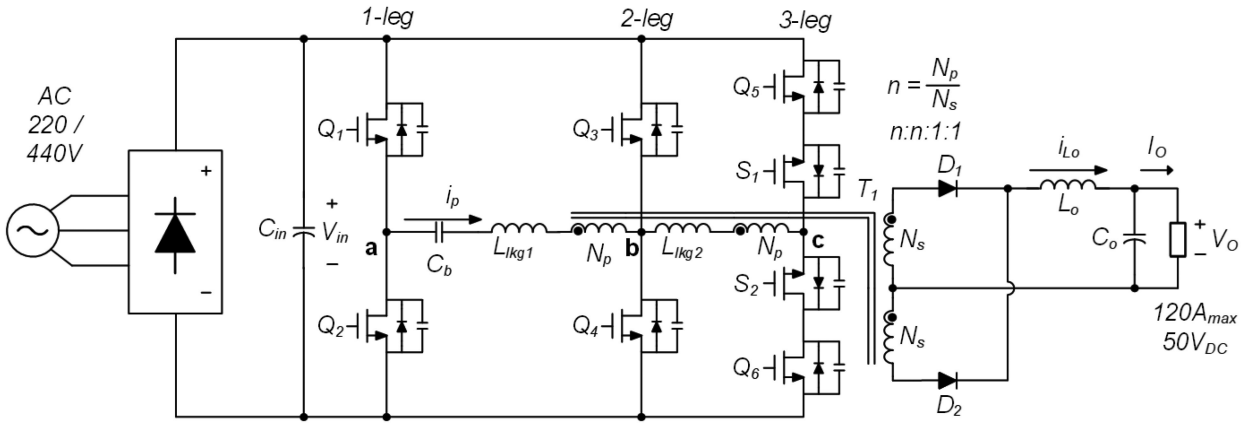

Fig. 2. Proposed topology for welding power supply.

grid voltage. This is because the structure in Fig. 1 makes power-conversion efficiency very poor due to large circulating current on the inverter side and high voltage stress on the rectifier side under a wide input voltage range, resulting in big size due to the generated heat [12]–[18]. To implement it without significant loss of performance in the structure in Fig. 1, a passive method of adjusing the tap according to the input voltage conditions after placing a tap on the transformer has been used until now. However, this method requires the operator to open the case of welding power supply to adjust the tab, resulting in a lot of working time. In addition, improperly adjusted tab can lead to problems that result in faulty power supply and insufficient power consumption. Another way is to place a dc/dc converer between the three-leg diode rectifier and the inverter switch circuit to stablize the inverter input voltage against any gird voltages. This method provides convenience that does not require operator intervention in gird voltages. However, inducors and capacitors in the added converter are very bulky and heavy, resulting in poor power-density and the increase of size and weight of welding machine.

In this article, a three-leg inverter-type topology capable of operating at both ac 220 and 440 V while achieving high efficiency without additional passive components is proposed for welding power supply applications. The secondary-side structure of the proposed topology is the same as that of the conventional welding power supply, but the primary-side structure consists of a three-leg inverter structure and a high-frequency transformer with two primary windings in series. Due to this structure, the proposed topology can operate in a wider input voltage range than the conventional dc/dc topology in Fig. 1, while guarantying that maximum duty operation is always possible at both ac 220 and 440 V. As a result, the circulating current decreases, and the primary-side current and secondary-side rectifier voltage stress are drastically reduced, enabling high-efficiency operation in all input voltage conditions. This efficiency improvement makes it possible to increase the switching frequency of the proposed topology and to apply MOSFETs suitable for high-frequency operation to the proposed welding power supply topology. Use of high frequency made it possible to reduce the size of passive elements, such as inductors, transformers, and capacitors, which occupy very large volumes in the welding power supply, and it became possible to design a welding current controller with a much wider bandwidth than conventional IGBT-based welding power supply devices. The performance of the proposed topology with a wide input voltage range for a high-frequency welding power supply is verified using prototypes with a switching frequency of 100 kHz, an input voltage of 311/622 V, an output voltage of 50 V, and a 6.0 kW class specification, and the experimental results are presented in this article.

The structure of this article is as follows. In Section II, the principle of operation and analysis of the proposed dc/dc topology are presented. Section III gives the design details of the proposed topology, and in Section IV, the results of the comparison and analysis of the conventional and proposed dc/dc topologies are presented. Finally, the conclusion is made in Section V.

II. Proposed Welding Power Supply

A. Topology Description

Fig. 2 shows a dc/dc topology proposed for welding power supply applications capable of operating at both ac 220 and 440 V. As seen in Fig. 2, the secondary-side structure of the proposed topology is the same as that of a conventional dc/dc topology. Meanwhile, a third leg is added to the primary inverter part of the proposed topology, and switches S_1 and S_2 are arranged in series to Q_5 and Q_6, respectively, so that a current path is not formed in the third leg when the input voltage is 311 V. Also, the additional winding is arranged between the second and third legs using the same number of turns as the winding N_p between the first and second legs. Since the drain-source voltage stress of the switches is more than 622 V, the first and second legs and the added switching leg (third leg) use SiC-MOSFETs as the switching element. The use of SiC-MOSFETs reduces the size of passive devices such as transformers, inductors, and capacitors with high breakdown voltage, high drain current featuring very low ON-resistance, and fast switching cycles. In addition, the added winding is driven by a transformer rather than an ordinary inductor. If two transformers are manufactured with a general center-tap structure and connected in series on the primary side and in parallel on the secondary side, the volume becomes problematically large. Therefore, in order to reduce the volume, a four-winding structure is adopted in which one more winding

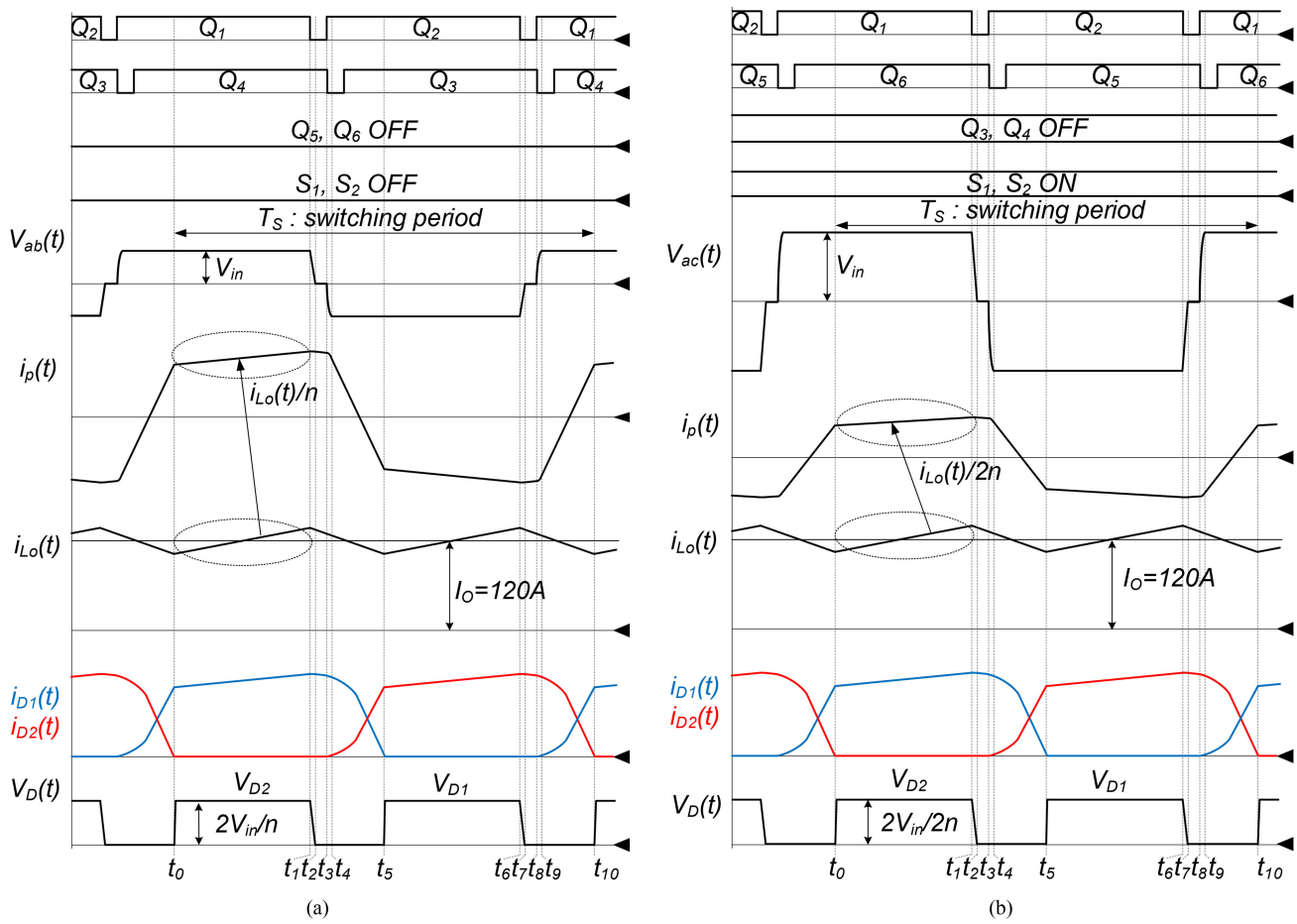

Fig. 3. Key waveforms according to the input voltage of the proposed topology. (a) When the input voltage is 311 V. (b) When the input voltage is 622 V.

is wound around transformer T_1 with the existing center-tap structure.

B. Operating Principles

Fig. 3 shows the main operating waveforms of the proposed topology when the input voltages are 311 and 622 V in the steady state. Fig. 4 shows the current path according to each input voltage of the proposed topology. As can be seen in Figs. 3(a) and 4(a), the input voltage 311 V operation of the proposed topology runs to the first and second legs, as in a conventional dc/dc topology [19]. At this time, all switches (Q_5, Q_6, S_1, and S_2) of the third leg are in the OFF state. Therefore, the 311 V input voltage operation of the proposed dc/dc topology has the same performance as the 311 V operation of a conventional dc/dc topology. Figs. 3(b) and 4(b) show the main operation waveforms of the proposed topology operated with an input voltage of 622 V. As can be seen in these figures, switches S_1 and S_2 of the third leg of the proposed topology are always ON during 622 V operation. This results in improved performance compared to a conventional topology operated at an input voltage of 622 V. The operation modes of the proposed topology at 622 V are as follows.

1) *Mode 1 [t_0, t_1]:* This is a power transmission section. Both of the primary-side windings are used and the turn-ratio is $2n$, a twofold increase from the previous one. Mode 1 is ended when switch Q_3 is switched OFF. The transformer voltage $V_{\rm ac}$ is the input voltage and the primary current i_p is shown as

$$V_{\rm ac}\left(t\right) = V_{\rm in} \tag{1}$$

$$\frac{di_{L_O}\left(t\right)}{dt} = \frac{\frac{V_{\rm in}}{2n} - V_o}{\left(L_{\rm lkg1} + L_{\rm lkg2}\right)/4n^2 + L_o} \tag{2}$$

$$i_p\left(t\right) = \frac{i_{L_O}\left(t\right)}{2n}. \tag{3}$$

2) *Mode 2 [t_1, t_2]:* This is the charging and discharging section of the leading leg switches. The sum of the output inductance L_O reflected to the primary side and the transformer leakage inductances ($L_{\rm lkg1} + L_{\rm lkg2}$) resonate with the parasitic capacitances $C_{\rm OSS1}$ and $C_{\rm OSS2}$ of the switches. Mode 2 ends when $C_{\rm OSS1}$ and $C_{\rm OSS2}$ are fully charged and discharged respectively. $V_{\rm ac}$ is the voltage of $C_{\rm OSS2}$ and i_p is shown as

$$V_{\rm ac}\left(t\right) = V_{\rm in} - \frac{i_{L_O}\left(t_1\right)}{2n} Z_a \sin\omega_a\left(t - t_1\right) \tag{4}$$

$$i_p\left(t\right) = \frac{i_{L_O}\left(t_1\right)}{2n} \cos\omega_a\left(t - t_1\right) \tag{5}$$

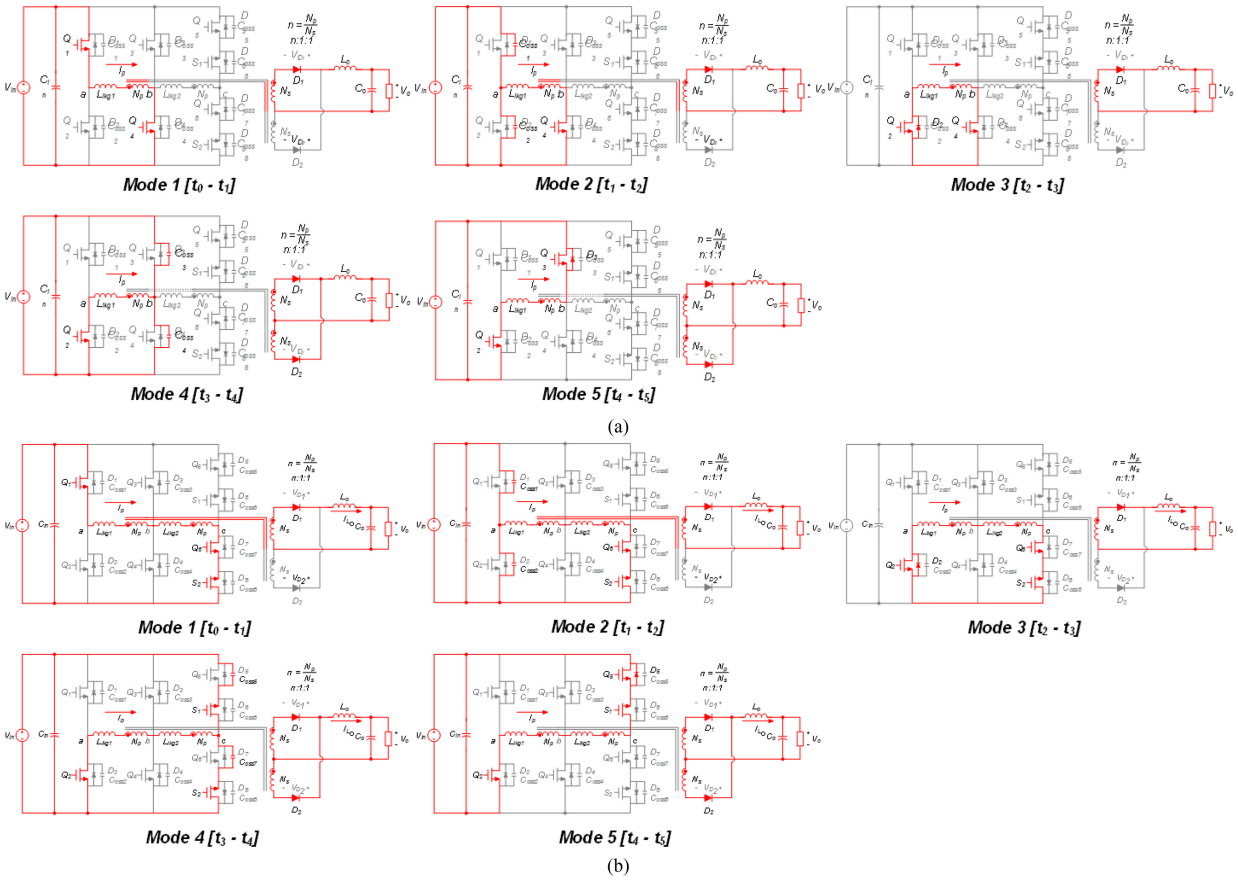

Fig. 4. Current path according to the input voltage of the proposed topology. (a) When the input voltage is 311 V. (b) When the input voltage is 622 V.

$$\omega_a = \frac{1}{\sqrt{2L_a \mathrm{C_{OSS}}}}, Z_a = \sqrt{\frac{L_a}{2\mathrm{C_{OSS}}}} \tag{6}$$

$$L_a = 4n^2 L_O + L_{\mathrm{lkg1}} + L_{\mathrm{lkg2}}. \tag{7}$$

3) *Mode 3 [t_2, t_3]:* This is the freewheeling section. Mode 3 starts when C_{OSS2} discharge is completed. Then, the conduction of the body diode of Q_2 is completed, and when the gate signal is applied, Q_2 achieves zero-voltage switching (ZVS). In addition, both diodes on the secondary side are conducting and enter the free-wheeling mode. During this mode, voltage and current waveforms can be expressed as

$$V_{\mathrm{ac}}(t) = 0 \tag{8}$$

$$\frac{di_p(t)}{dt} = -\frac{V_O}{2nL_O} \tag{9}$$

$$i_{L_O}(t) = i_{L_O}(t_2) - \frac{V_O}{L_O}(t - t_2). \tag{10}$$

4) *Mode 4 [t_3, t_4]:* This is the charging and discharging section of the lagging leg switches. Mode 4 starts when Q_6 is turned OFF. In this mode, the parasitic capacitors of Q_5 and Q_6 discharge and charge respectively, and the secondary diodes start to change their roles. Therefore, the output inductance is not projected to the primary side, and C_{OSS5} and C_{OSS6} discharge and charge due to the current flowing through the primary-side leakage inductances. Mode 4 ends when C_{OSS5} completes discharging. The primary-side current and the voltage across the inverter are as

$$V_{\mathrm{ac}}(t) = -i_p(t_3) Z_b \sin\omega_b (t - t_3) \tag{11}$$

$$i_p(t) = i_p(t_3)\cos\omega_b (t - t_3) \tag{12}$$

$$\omega_b = \frac{1}{\sqrt{2L_b \mathrm{C_{OSS}}}}, Z_b = \sqrt{\frac{L_b}{2\mathrm{C_{OSS}}}} \tag{13}$$

$$L_b = L_{\mathrm{lkg1}} + L_{\mathrm{lkg2}}. \tag{14}$$

5) *Mode 5 [t_4, t_5]:* This is the commutation section of the secondary-side diodes. Mode 5 starts when the C_{OSS5} voltage is discharged and the drain-to-source voltage of Q_5 is zero. Then, the body diode of Q_5 is passed through, and when the gate signal is applied before the current is reversed, Q_5 achieves ZVS. At this mode, the input voltage is applied to the primary windings of the transformer, but the secondary side does not deliver power with the rectifier diodes plowed, causing loss of duty-ratio. In practice, the applied input voltage appears on transformer leakage inductances, not effective primary windings and it changes the orientation of the primary-side current, resulting in a rapid gradient reduction. This section is analyzed as

$$V_{L_b}(t) = -V_{\mathrm{in}} \tag{15}$$

$$\frac{di_p(t)}{dt} = -\frac{V_{\mathrm{in}}}{L_{\mathrm{lkg1}} + L_{\mathrm{lkg2}}} \tag{16}$$

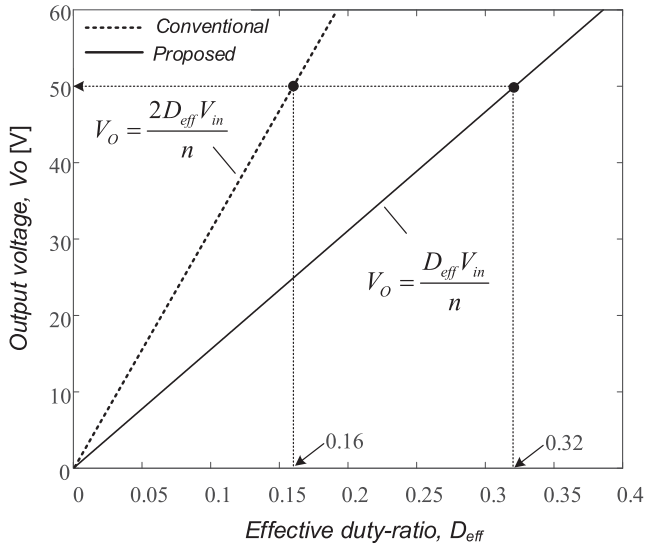

Fig. 5. Output voltage of the conventional and proposed topologies according to the effective duty-ratio at $V_{\rm in} = 622$ V and $n = 8$.

TABLE I
PRIMARY-SIDE RMS CURRENT STRESS

Input Voltage	Conventional	Proposed
311V	$\frac{1}{n}\sqrt{2D_{eff}I_O^2 + 2(1-D_{eff})I_{O.pk}^2}$	Same as before
622V		$\frac{1}{2n}\sqrt{2D_{eff}I_O^2 + 2(1-D_{eff})I_{O.pk}^2}$

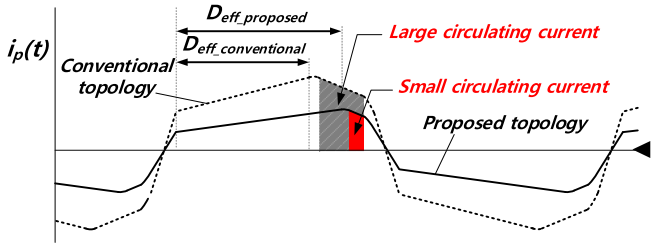

Fig. 6. Comparison of primary-side current stress of the conventional and proposed topologies at $V_{\rm in} = 622$ V.

$$i_p(t) = i_p(t_4) - \frac{V_{\rm in}}{L_{\rm lkg1} + L_{\rm lkg2}}(t - t_4). \tag{17}$$

C. Voltage Gain Analysis

When operating at a high input voltage like 622 V, the proposed topology's output inductor builds up with a slope of $V_{\rm in}/2n$-V_O in mode 1 and demagnetizes it with a slope of -V_O in modes 2 and 3. Using the voltage-second condition for each mode, the voltage gain of the proposed topology can be obtained as

$$\frac{V_O}{V_{\rm in}} = \frac{D_{\rm eff}}{n}. \tag{18}$$

On the other hand, the conventional topology operating at the high input voltage has the gain of

$$\frac{V_O}{V_{\rm in}} = \frac{2D_{\rm eff}}{n}. \tag{19}$$

Fig. 5 shows the output voltage of the conventional and proposed topologies according to the effective duty-ratio at the condition of $V_{\rm in} = 622$ V and $n = 8$. As can be seen in Fig. 5, the proposed topology operates with a wider duty-ratio than the conventional topology for the output of 50 V. This means that the proposed topology has much smaller time-interval which the circulating current flows, compared to conventional topology.

D. Primary Current Stress

Table I gives the analysis of the primary-side current stress of the conventional and proposed topologies according to the input voltage. Fig. 6 shows a comparison of the primary-side current stress at the input voltage of 622 V. As can be seen in Fig. 6, the conventional topology is designed to have the maximum effective duty-ratio at the low input voltage of 311 V. As a result, the topology works with a much lower effective duty-ratio as shown in Fig. 5 at 622 V input voltage and experiences large circulating current on the primary side. On the other hand, as can be seen in Fig. 5, the effective duty-ratio of the proposed topology at 50 V, which is the output voltage specification of this article, is larger than that of the conventional topology; thus, the proposed topology is superior to the conventional topology in terms of the circulating current of the primary current waveform. In addition, due to the double increase in the turn-ratio because of the added winding, the load current projected from the secondary side to the primary side decreases, thereby reducing the overall primary-side current stress by 50% as given in Table I. Thus, the proposed topology can greatly reduce conduction losses in the switches and transformer, and is highly efficient at a high input voltage.

E. Output Inductor Current Ripple

Increasing the effective duty-ratio, the advantage of the proposed topology mentioned above, reduces the output inductor current ripple by

$$\Delta i_{Lo} = (1 - 2D_{\rm eff})\frac{T_S}{2}\frac{V_O}{L_O}. \tag{20}$$

Fig. 7 shows a graph of the output inductor current ripple according to the input voltage when the output inductance is 14.125 μH based on (20). In a conventional topology, as the input voltage increases, the output inductor current ripple increases, and the same is true in the proposed topology. However, when the input voltage is 622 V, the turn-ratio of the proposed topology changes and the ripple is reduced by about 50% compared to that in the conventional topology. If the output inductor current ripple is equal at 622 V operation, the inductance value of the proposed topology can be up to 50% smaller than that of the conventional topology. As a result, the volume of the output inductor is reduced, and the power density is improved. However, in this article, to enable a comparison between the two topologies, the proposed topology is designed with the same output inductance as the conventional topology.

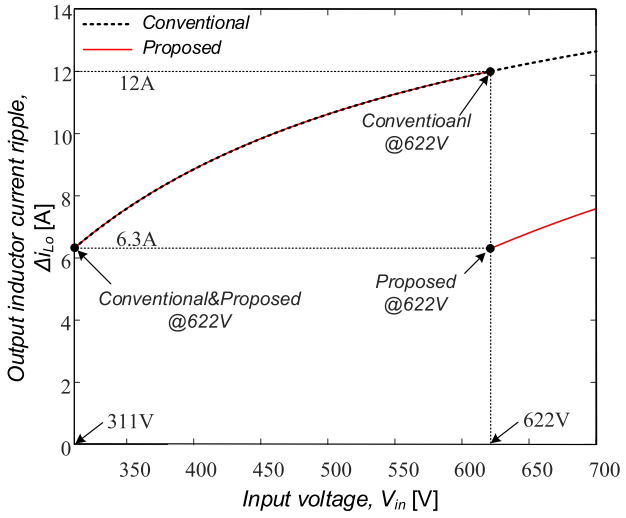

Fig. 7. Output inductor current ripple of the conventional and proposed topologies according to input voltage with $L_o = 14.125$ Mh.

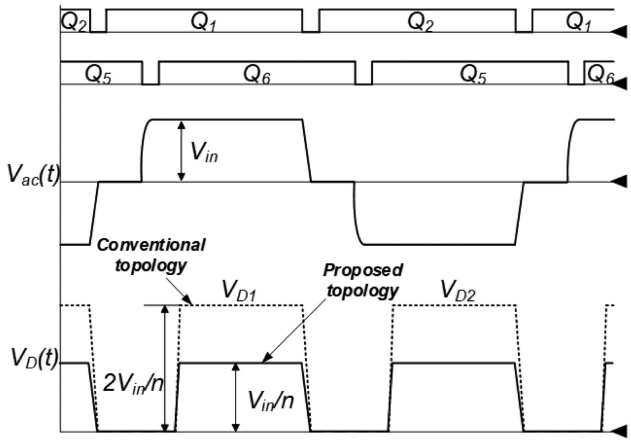

Fig. 8. Comparison of the secondary-side rectifier voltage stress in the conventional and proposed topologies at $V_{\rm in} = 622$ V.

F. Voltage Stress of the Rectifier Diodes

Fig. 8 shows a comparison of the voltage stress of the secondary-side rectification stage of the conventional and proposed topologies at the input voltage of 622 V. As can be seen in Fig. 8, in conventional topologies, as the input voltage increases, the voltage stress of the secondary-side rectifier increases. In addition, in order to solve the ringing problem caused by the parasitic capacitors in the secondary-side rectification stage, a snubber circuit is generally added to the secondary-side rectification stage; the snubber circuit is designed to be disadvantageous in terms of power density and efficiency due to its volume and loss. Meanwhile, as given in Table II, the proposed topology has a 50% reduction in voltage stress at the secondary rectifying stage compared to the conventional topology. At the input voltage of 622V, the proposed topology utilizes the first and third legs but not the second leg. Therefore, power is transmitted using both windings on the primary side. As a result, the voltage stress of the secondary rectification stage can be reduced by 50% compared to that of the conventional topology, and the existing snubber circuit can be removed, or a diode with a small breakdown voltage and a small forward voltage drop can be used. Due to this advantage, the proposed topology shows reduced snubber or diode losses at a high input voltage, thereby enabling high-efficiency operation.

TABLE II
SECONDARY-SIDE RECTIFIER PEAK VOLTAGE STRESS

Input Voltage	Conventional	Proposed
311V	$\frac{2V_{in}}{n} + ringing$	Same as before
622V		$\frac{V_{in}}{n} + ringing$

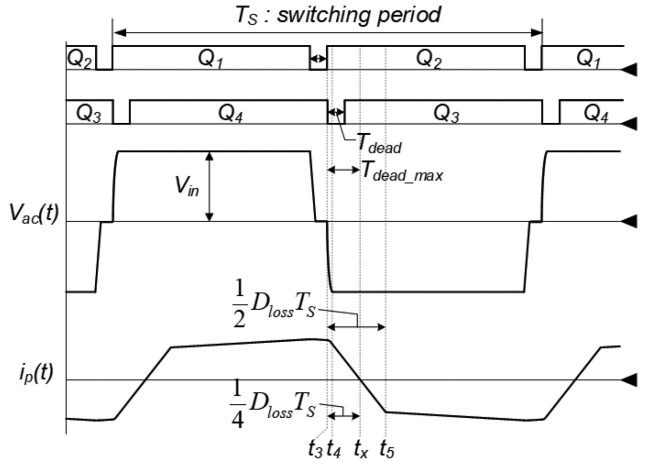

Fig. 9. Dead-time range for ZVS.

G. Zero-Voltage Switching Condition

The proposed topology has the same operating principles as a conventional phase-shifted full-bridge converter [20], [21]. Therefore, the ZVS condition is also analyzed in the same manner. Fig. 9 shows the dead-time range between switching operations for ZVS. According to the operation mode analysis, the gate signal must be turned on before the primary-side current is reversed. Then, the ZVS condition can be defined as

$$T_{\rm dead} \le T_{\rm dead\_max} = \frac{1}{4} D_{\rm loss} T_S = \frac{L_{\rm lkg} I_O}{n V_{\rm in}}. \tag{21}$$

From (21), the required primary inductance $L_{\rm lkg}$ in series with the transformer for ZVS operation can be obtained from

$$L_{\rm lkg} \ge \frac{n V_O V_{\rm in} T_{\rm dead}}{P_O} \times 10^6 [\mu{\rm H}]. \tag{22}$$

Fig. 10 shows the inductance in series with T_1 for ZVS according to the load conditions with the input voltage of 622 V and a dead time 175 ns. As can be seen in Fig. 10, the proposed topology additionally requires twice the inductance as the conventional topology. In order to compare the performance of the two topologies under equivalent conditions, inductances with a ZVS starting load of 2.5 kW are selected and reflected in the prototype.

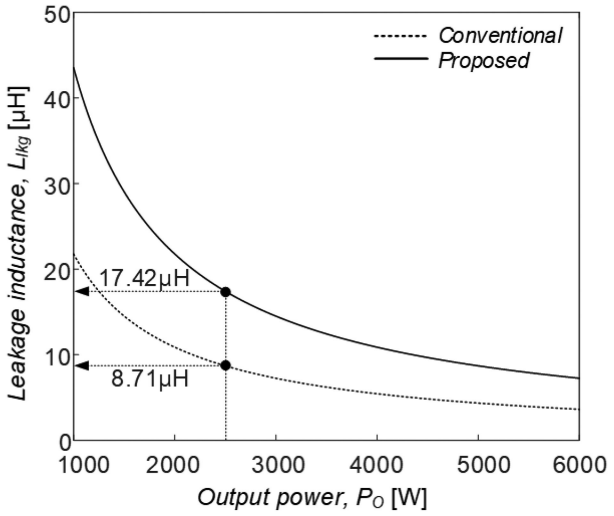

Fig. 10. Inductance in series with the transformer for ZVS according to load conditions at $V_{\text{in}} = 622$ V.

TABLE III
DESIGN SPECIFICATION

Parameter	Value	Unit
Input voltage, V_{in}	311/622	V
Output voltage, V_O	50	V
Output current, I_O	120	A
Switching frequency, f_s	100	kHz
Output current ripple, Δi_O	10	%
Output voltage ripple, ΔV_O	1	%

III. PROPOSED TOPOLOGY DESIGN

The proposed topology for welding power supply applications is compared with a conventional topology. To secure the validity of the comparison, the design standard is the same as that of the conventional topology. Table III gives the input and output specifications of the conventional and the proposed topologies. As can be seen from the table, it receives 311 V, which is a voltage rectified from ac 220 and 622 V, which is rectified from ac 440 V, as an input voltage. Output specifications are 50 V, 6.0 kW, the output current ripple is 10.0%, and the output voltage ripple is 1.0%.

A. Transformer

The turn-ratio is required for the transformer design of the proposed topology and it should be designed at the minimum input voltage of 311V. At that condition, it can be derived from the gain (19) of the conventional topology because the proposed topology works with a single primary winding. However, the operating effective duty-ratio is 0.32 at the 311 V input condition, not 0.16 as in the conventional topology. Then the turn-ratio is determined by

$$n = \frac{2D_{\text{eff\_max}}V_{\text{in\_min}}}{V_O} = \frac{2 \times 0.32 \times 311}{50} = 4. \quad (23)$$

Considering the core loss in the high frequency, it is preferable to choose a ferrite core with a smaller B-H loop area. The energy capacity of the core size for the transformer is selected based on the area product A_p, which is a function of generally used as follows [15], [22]:

$$A_p = W_a A_c \geq \left[\frac{11.1P_O/\eta}{K\Delta B f_s}\right]^{1.31} \geq \left[\frac{11.1 \times 6000/0.95}{0.165 \times 0.24 \times 100 \times 10^3}\right]^{1.31} = 43.15\,[\text{cm}^4]. \quad (24)$$

In (24), the output power P_O is 6.0 kW, conversion-efficiency η is 0.95, switching frequency *fs* is 100 kHz, topology factor *K* is 0.165, and the maximum magnetic flux density is selected as 0.12 T for small core loss. The magnetic core meeting the result of (24) is EE8076S cores, which have the A_p of 44.99 cm^4 consisting of the winding area W_a of 11.22 cm^2 and the cross-sectional area A_c of 4.0 cm^2 [22].

The number of turns on the primary side of the transformer can be derived by Faraday's law; it is as follows:

$$N_p \geq \frac{V_{in\_\min} t_{on\_\max}}{\Delta B A_c/10^3} = \frac{311 \times 4.86 \times 10^{-6}}{0.24 \times 4/10^3} = 16. \quad (25)$$

The next step is to select a coil. To find the winding thickness, the root-mean-square (rms) current stress of the primary and secondary windings is calculated at the minimum input voltage and is shown in (26) and (27). At the calculation, D_{eff} is 0.32, I_O is 120 A, and $I_{O,\ pk}$ is 132 A

$$I_{\text{pri(RMS)}} = \frac{1}{n}\sqrt{2D_{\text{eff}}{I_O}^2 + (1 - 2D_{\text{eff}}){I_{O.pk}}^2} \approx 31\,[\text{A}] \quad (26)$$

$$I_{\text{sec}(RMS)} = \sqrt{2D_{\text{eff}}{I_O}^2} \approx 70\,[\text{A}]. \quad (27)$$

In general, winding thickness can be selected by (28) [22]. In (28), *J* is current density and the litz-wire is used to ignore skin-effects in this design

$$\phi = 2\sqrt{\frac{I}{J\pi}}. \quad (28)$$

If the primary current density of 250 A/cm^2 for small coil loss is substituted for (28) it is possible to calculate the thickness of 0.12 mm, 1062 strands for the primary-side windings and the secondary current density of 420 A/cm^2 is calculated the thickness of 0.12 mm, 1685 strands for the secondary-side windings. The calculated secondary-side winding thickness is so thick that a core with a larger window area should be selected. However, since none of the existing EE cores are larger than EE8076S, the core should be stacked to increase the cross-sectional area of the core or ΔB to reduce the number of primary-side turns.

In this article, transformer design is performed by stacking cores. Finally, a transformer is manufactured using the 2 stacked

TABLE IV
DESIGNED TRANSFORMER PARAMETER

Transformer	
Core	EE8075C 2 stacked / PL7
Method	Center-Tap
Primary windings	0.12mm / 1000 strands / 8 turns / 8 turns
Secondary windings	0.12mm / 825 strands / 2 parallel / 2 turns
Magnetizing inductance	891.23mH
Leakage inductance	8.69μH

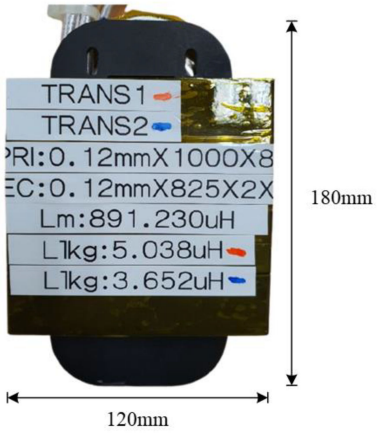

Fig. 11. Manufactured transformer.

EE8075Cs, and its specifications are given in Table IV. Fig. 11 shows a manufactured transformer.

B. Power Semiconductor

The maximum voltage and current stresses of the primary-side switches and the secondary-side diodes in the proposed topology are expressed as follows.

1) Primary switches (Q_1, Q_2, Q_3, Q_4)

$$I_{\text{peak.max}} = \frac{(I_O + \Delta i_{Lo})}{n}$$
$$I_{\text{rms.max}} = \frac{1}{n}\sqrt{(0.5 - D_{\text{eff}})\, {I_{O.\min}}^2 + D_{\text{eff}} {I_O}^2}$$
$$V_{\text{peak.max}} = V_{\text{in}}. \tag{29}$$

2) Primary switches (Q_5, Q_6, S_1, S_2)

$$I_{\text{peak.max}} = \frac{(I_O + \Delta i_{Lo})}{2n}$$
$$I_{\text{rms.max}} = \frac{1}{2n}\sqrt{(0.5 - D_{\text{eff}})\, {I_{O.\min}}^2 + D_{\text{eff}} {I_O}^2}$$
$$V_{\text{peak.max}} = V_{\text{in}}. \tag{30}$$

3) Secondary diodes (D_1, D_2)

$$I_{\text{peak.max}} = I_O + \Delta i_{Lo}$$
$$I_{\text{avg.max}} = \frac{I_O}{2}$$
$$I_{\text{rms.max}} = 0.707 I_O$$

TABLE V
CALCULATED VOLTAGE AND CURRENT STRESSES

Current and Voltage Stress	Switch Q_1, Q_2, Q_3, Q_4	Switch Q_5, Q_6, S_1, S_2	Diode
Maximum peak current, $I_{peak.max}$	33A	16A	132A
Maximum RMS current, $I_{rms.max}$	28A	14A	85A
Maximum AVG current, $I_{avg.max}$	-	-	60A
Maximum peak voltage, $V_{peak.max}$	622V	622V	311V

TABLE VI
DESIGNED OUTPUT INDUCTOR SPECIFICATION

Output inductor	
Core	CH740125 2 stacked
Windings	0.12mm X1150 strands X 2 parallel X 5.5 turns
Inductance	14.16μH

$$V_{\text{peak.max}} = \frac{V_{\text{in}}}{n} + V_{\text{ringing}} \approx 2\frac{V_{\text{in}}}{n}. \tag{31}$$

Table V gives the calculated current and voltage stresses. Considering the power loss of less than 15 W, a voltage margin of 1.8 times, and a current margin of 1.6 times based on the electrical stress, the primary switches are selected with SCT50N120, which have the specifications of 1200 V, 65 A, and 59 mΩ. To maximize the performance comparison of the proposed topology, the diodes of the proposed topology is selected the same as the diodes of the conventional topology. As a result, the DFE240X600NAs, which have the rating of 600 V, 240 A, and 1.3 V voltage drop, are used for the diodes in the rectifier stage.

C. Output Inductor and Capacitor

The output inductor of the proposed topology is designed by (32) considering the output current ripple

$$L_o \geq \frac{(1 - 2D_{\text{eff}})\, V_O}{2 f_S \Delta i_{Lo}} = \frac{(1 - 0.32) \times 50}{2 \times 100 \times 10^3 \times 12} = 14.16\,[\mu\text{H}]. \tag{32}$$

According to (32), the output inductance should be 14.16 μH or more, and the CH740125 core is selected in consideration of the core loss of the inductor and the dc superposition characteristic [22], [24]. In consideration of the output current specification and the window area of the core, as given in Table VI, an output inductor is manufactured with two stacks of cores and 5.5-turns.

The output capacitor is designed in consideration of the ripple specification of the output voltage. Equation (33) shows the design equation and the capacitance should be 15 μF or more. The RMS stress of the current flowing through the capacitor is

$$C_O \geq \frac{\Delta i_{Lo}}{16 f_S \Delta V_O} = \frac{12}{16 \times 100 \times 10^3 \times 0.5} = 15\,[\mu\text{F}] \tag{33}$$

$$I_{C_O} = \frac{\sqrt{3}\Delta i_{Lo}}{6} = 3.46\ [\text{A}]. \tag{34}$$

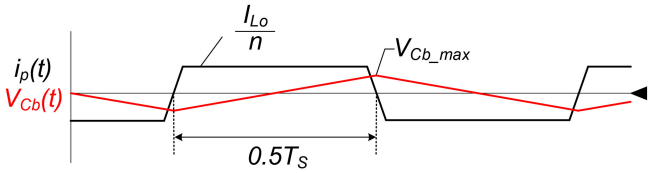

Fig. 12. Current waveform of dc-blocking capacitor.

The selected output capacitor is the "22201C106M4Z2A" multilayer ceramic capacitor which it has a 10 μF, 100 V capacity that is better in terms of insulation resistance, equivalent series resistance (ESR), and volume than electrolytic capacitors. In addition, considering (33) and (34), five parallel capacitors are selected so that matches 15 μF more of the capacitance and the conduction loss per a capacitor by (34) is less than 1.0 W considering the life-time.

D. DC Blocking Capacitor

The dc-blocking capacitor removes dc-offset occurring in the transformer caused by the operation of abnormal switches. In the case of phase-shifted full-bridge topologies, the smaller value of the dc-blocking capacitor increases the voltage drop across the dc-blocking capacitor and reduces the topology voltage gain. Then the desired output voltage cannot be obtained. In addition, the ZVS operation can be failed due to the dc-offset. Therefore, it is necessary to select an appropriate capacitance that does not affect both the ZVS operation and voltage gain. Fig. 12 shows the approximated current and voltage waveforms of the dc-blocking capacitor. The dc-blocking capacitor is inserted in series with the primary-side of the transformer, and the current flowing through it is the same as the primary-side current of the transformer. Therefore, when selecting a dc-blocking capacitor, a capacitor of the metallized polypropylene (MKP) film capacitors-type with high current capacity is selected. Equation (35) gives the value of the minimum blocking capacitance

$$V_{C_{b\_}\max} \le V_{\text{in\_min}} - nV_O$$
$$C_b \ge \frac{I_O}{4nV_{C_{b\_}\max} f_S}$$
$$\ge \frac{120}{4 \times 4 \times (311 - 4 \times 50) \times 100 \times 10^3} = 0.67\,[\mu\text{F}]. \quad (35)$$

In this article, TDK's "B32674D1225" with specifications of 750 V, 2.2 μF, and 9 A is selected, and four parallels are performed considering the primary-side current stress of 30 A. Therefore, a total capacitance of 8.8 μF is selected.

IV. Experimental Results

To verify the validity of the proposed topology, the conventional and proposed prototypes are made with the components given in Table VII. Figs. 13 and 14 show photos of each of the manufactured prototypes. As seen in Figs 13 and 14, a bulky snubber circuit is used at the secondary side of the conventional topology, but not in the proposed topology. The two prototypes were regulated by a DSP, TMS320F28335-based controller with both of output voltage and current control algorithms, and resistance loads were used to confirm the steady-stage performance of each topology.

Figs. 15 and 16 show the experimental waveforms for the conventional and proposed topologies, respectively, under 311 or 622 V and full load conditions. As shown in Figs. 15 and

TABLE VII
COMPONENTS USED FOR PROTOTYPES

Device	Conventional	Proposed
Rectifier, C_{in}	Electrolytic capacitor 220μF / 600V / 2 Series 2 Parallel	
Switch, $Q_{1\sim4}$	SCT50N120 (1200V/65A/59mΩ)/2 parallel X 4	
Switch, $Q_{5,6}$	None	SCT50N120 (1200V/65A/59mΩ) /2 parallel X 2
Switch, $S_{1,2}$		SCT50N120 (1200V/65A/59mΩ) X 2
Diode, $D_{1,2}$	DFE240X600NA(600V/240A/1.3V) X 2	
Output Inductor	CH740125 2 stacked 0.12mm /1200 strands / 2 Parallel / 5.5 turns	
Transformer	EE8075C 2 stacked / PL7 8T : 2T : 2T N_p : 0.12mm / 1150 strands N_s : 0.12mm / 825 strands / 2parallel L_m : 1.138mH L_{lkg} : 4.283μH	EE8075C 2 stacked / PL7 8T : 8T : 2T : 2T N_p : 0.12mm / 1000 strands N_s : 0.12mm / 825 strands / 2 parallel L_m : 891.23μH L_{lkg} : 8.78μH
Output capacitor	22201C106M4Z2A / 10μF / 100V / 5 parallel	
Snubber	R : 10kΩ / 10W / 8 parallel C : MKP 630V / 10nF / 2 parallel D : S3L60 600V / 2.2A	None

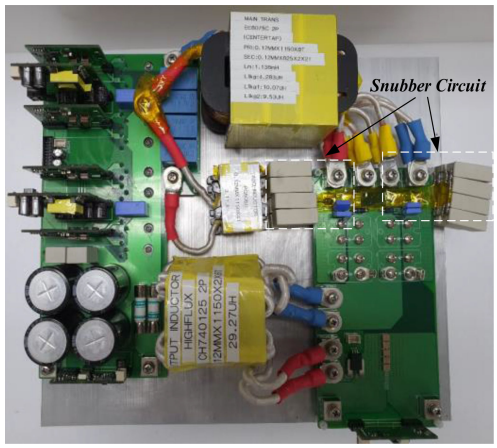

Fig. 13. Conventional topology.

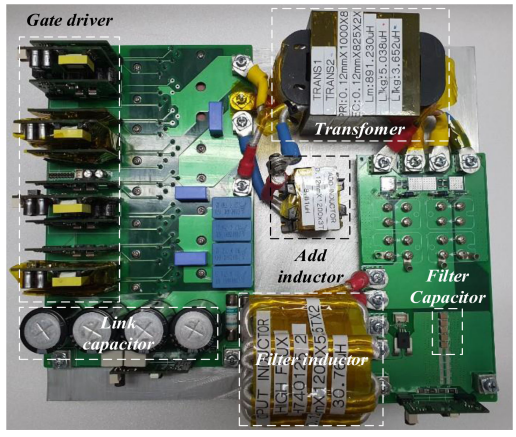

Fig. 14. Proposed topology.

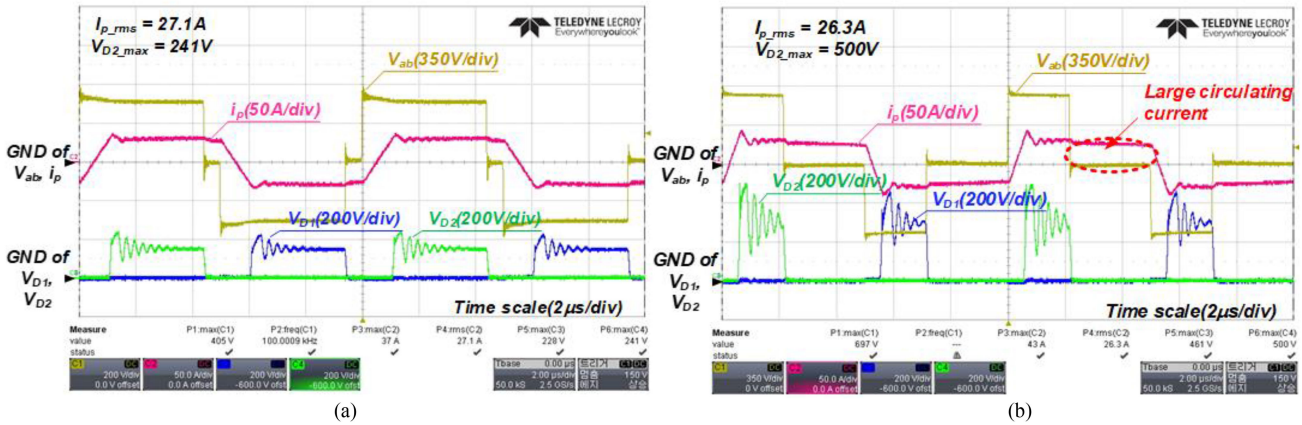

Fig. 15. Key waveforms of the conventional topology (a) at $V_{\rm in} = 311$ V and (b) at $V_{\rm in} = 622$ V.

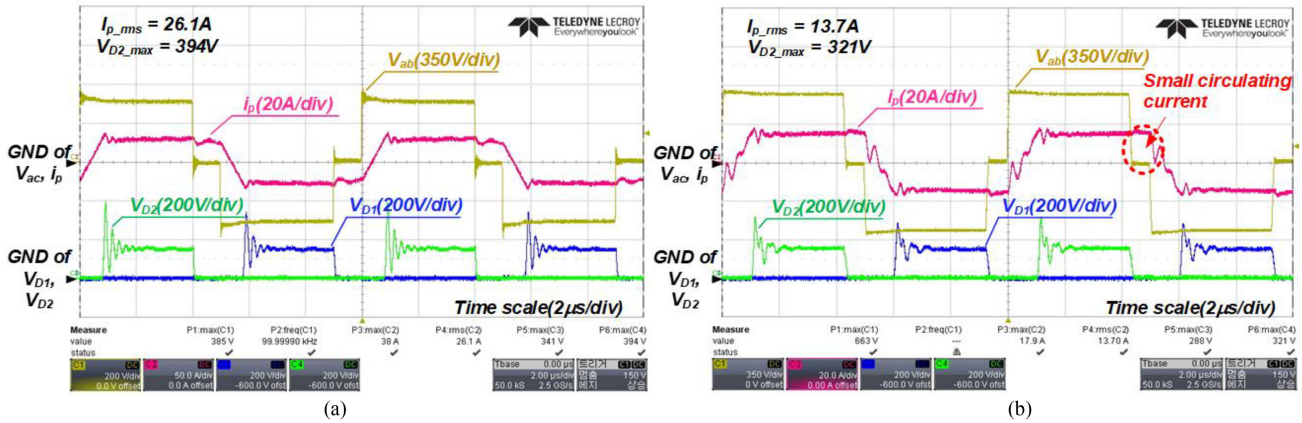

Fig. 16. Key waveforms of the proposed topology (a) at $V_{\rm in} = 311$ V and (b) at $V_{\rm in} = 622$ V.

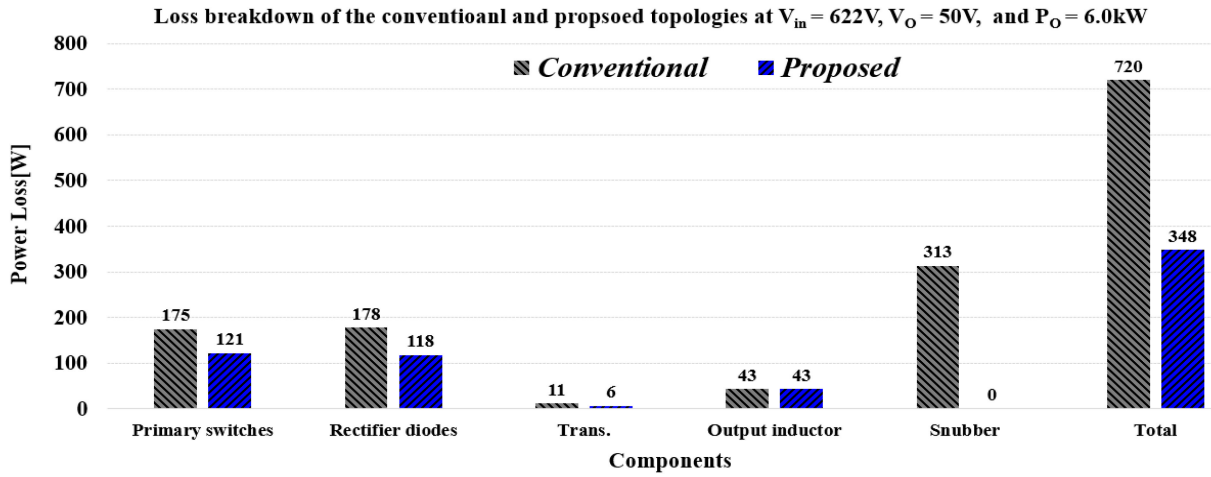

Fig. 17. Loss breakdown of prototypes at $V_{\rm in} = 622$-V, $V_O = 50$ V, and $P_O = 6.0$ kW.

16, the conventional topology is designed to have the maximum duty-ratio at the minimum input voltage, showing that it has the minimum duty-ratio at the high input voltage. As a result, the circulating current increases, and as shown in Fig. 15(b), it has an rms current stress of 26.3 A on the primary side, and the voltage stress of the secondary-side rectifier exceeds 500 V. On the other hand, the proposed topology operates at the maximum duty-ratio in both all input voltage, as shown in Fig. 16. In addition, from Fig. 16(b), the rms current stress on the primary side at 622 V input voltage is 13.7 A, half that of the conventional topology, because the turn-ratio is two-fold higher. The voltage stress at

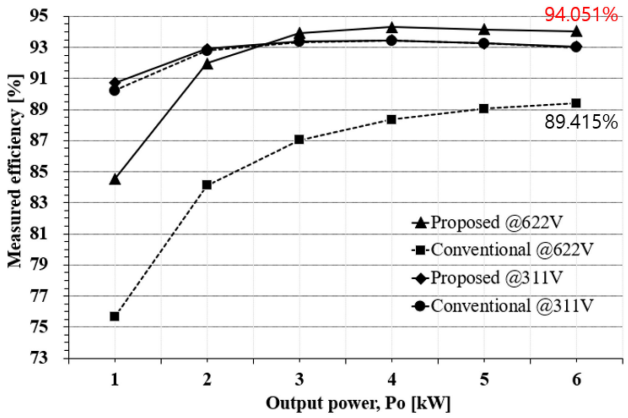

Fig. 18. Measured efficiency.

the secondary rectifying stage is also reduced by 1/2, and, as shown in Figs. 15(b) and 16(b), there is no snubber circuit on the secondary side.

Fig. 17 shows the loss breakdown of the two prototypes at 6.0 kW and 622 V input conditions and Fig. 18 shows the measured efficiency of the prototypes according to load conditions. As can be seen in Fig. 18, the proposed topology does not have a snubber circuit, so it shows the same or slightly higher efficiency performance compared to the conventional topology at the input voltage of 311 V. However, the proposed topology achieves 94.051% efficiency at 6.0 kW and 622 V conditions and on the other hand, the conventional topology shows the efficiency of 89.415% at the same load condition. And for the entire load conditions at the input voltage of 622 V, the proposed topology shows the performance improved by more than 5% compared to the conventional topology. Fig. 17 verifies that the improvement at the high input volage conditions in Fig. 18 comes from the reduction in current stress and snubber circuit loss.

V. Conclusion

In welding power supply applications, it is technically challenging to achieve high efficiency and high-power density due to the low switching frequency and wide input voltage range. Therefore, in this article, a topology suitable for this type of welding power supply applications is proposed. The proposed topology always achieves high efficiency due to a wider input voltage range compared to the conventional topology with the help of the three-leg inverter and additional transformer configuration, a reduction in circulating current due to the altered turn-ratio, and a reduction in primary and secondary rectifier voltage stress. In order to verify the validity of the proposed topology, this article designed and manufactured 6.0 kW class prototypes and presented the experimental results. The experimental results verify the aforementioned advantages and show that the proposed topology has better performance in terms of efficiency and power density than the existing topology. As a result, it is concluded that the proposed topology is well-suited to welding power supply applications with a wide input voltage range.

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