Steady-State Modeling of a Dual-Active Bridge AC–DC Converter Considering Circuit Nonidealities and Intracycle Transient Effects

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***Abstract*—Steady-state operation of dual active bridge (DAB) ac–dc converters can show a high dependence on the circuit nonidealities and on the transient nature of the consistently changing phase-shifts necessary to achieve ac–dc operation. These aspects are not fully captured using traditional modeling approaches derived from dc–dc DAB converter analyses. To address these issues, this article presents a unified modeling approach comprising of hybrid frequency and time-domain analyses that encompass the transient nature of the ac–dc converter while providing the advantages of steady-state frequency-domain analysis. The limitations of conventional modeling approaches are quantified and addressed. Additionally, a comprehensive analysis of modeling error trends with converter parameters is presented, which demonstrates the effectiveness of the proposed method over conventional methods. Finally, using the proposed modeling approach, a numerical optimization routine is proposed to find the optimal-conduction-loss modulation trajectory. The effectiveness of the method is verified by experimental testing on a 1 kW, 230–28 V fully GaN-based single-phase DAB ac–dc converter.**

***Index Terms*—AC–DC converter, circuit parasitics, dual active bridge (DAB), frequency domain, optimization, single stage, steady-state modeling.**

I. Introduction

SINGLE-STAGE isolated ac–dc converters provide an attractive solution for applications requiring high power density and high reliability, as they eliminate the bulky dc-link capacitors [1]–[3]. Single-stage converters are desirable in many applications, such as electric vehicles [4]–[5], telecommunications [6], and more-electric aircrafts [7]. Specifically, the dual active bridge (DAB)-based ac–dc converter is an excellent candidate among single-stage isolated ac–dc converters due to its high power density [8], established control [9], and soft-switched operation [10]–[11].

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The operation of a DAB ac–dc converter involves multiple modulation variables (up to four, for a two-level DAB) and meeting numerous constraints and objectives. Thus, a steady-state analytical model is necessary for the development of closed-form equations [12] and/or numerical methods [10] to find optimal solutions. The steady-state analytical modeling approaches can be further divided into time- and frequency-domain-based modeling. The time-domain approaches involve deriving closed-form expressions of relevant functions in different operating modes. Such analyses present a significant hurdle to the designer as the modes and corresponding equations are dependent on operating conditions such as port voltage ratios, phase-shift directions, and modulation strategy [13], and must be recomputed for any changes in above. To circumvent these limitations, [14]–[15] introduce harmonic-superposition-based frequency-domain approaches for modeling of DAB converters. The frequency-domain analysis removes the need for mode definitions and constraints on input/output voltage ratios, thus unifying the analysis for all modulation strategies and operation modes.

The conventional frequency-domain steady-state modeling approach extends the modeling of the DAB ac–dc converter as a generalized case of the DAB dc–dc converter. Thus, the formulation of conventional modeling (both time and frequency domain) is based on the following two assumptions:

1) *Assumption 1:* The terminal voltages are constant within a switching cycle, and phase-shifts are constant before/after the switching cycle under consideration. That is, the converter stays in steady-state for every switching cycle, which allows the analysis of every switching cycle in a decoupled manner.
2) *Assumption 2:* The circuit does not possess nonidealities and parasitics, such as magnetizing inductance, equivalent series resistances (ESR), switch capacitances, and dead times.

For a DAB ac–dc converter, the modulation variables change the value in every switching cycle to achieve power factor correction (PFC) action. Additionally, the ac input voltage changes continuously over a switching cycle. As the converter changes its state in every switching period, *Assumption 1* gets violated. To accurately model these transient effects, continuous-time state-space average modeling techniques have been deployed in dc–dc DAB converters. A lossless average-value model for

a dc–dc DAB is presented in [16]. In [17], [18], small- and large-signal average reduced-order modeling approaches are presented that also incorporate lossy components. However, by consolidating the entire switching circuit as a single element for the average modeling, these methods are not flexible with modulation strategies. In [19], a generalized average modeling is introduced, with correction factors for accurate large-signal modeling applied through algebraic equations, thus allowing its application irrespective of the switching scheme. The work in [20] utilizes time-domain modeling to develop a generic phase-shift control method to mitigate the impacts of transient phase-shift for all switching schemes. However, the implementation of [20] requires complex pulse generation logic and may not fully eliminate the dc currents due to transient phase-shifts. Another important point to note is that while the approaches in [17]–[20] effectively model the transient performance (part of *Assumption 1*) and accurately model certain parasitics/lossy components (part of *Assumption 2*), a key limitation is the difficulty in integrating these approaches with the modeling of switching transitions and dead-time effects. Especially, the dead-time effects can significantly impact the steady-state operating point in high-frequency DAB converters [21].

To incorporate dead-time modeling (*Assumption 2*), [22] presents the time-domain modeling of dead-time transitions for a DAB converter; however, the analysis is limited to single phase-shift (SPS) modulation, and the effect of switch output capacitances is not discussed. The modeling of switch output capacitances for DAB applications was introduced in [21]. In [23]–[26], detailed charge-based and energy-based calculations for nonlinear capacitors are combined with time-domain piecewise linear analysis of a DAB to find conditions to achieve zero-voltage switching (ZVS). The time-domain model in [25] considers different switching states for the full-bridge instead of the conventional half-bridge model, which yields accurate ZVS equations. Furthermore, there are several possible scenarios for switching transitions based on the dead-time duration, such as voltage polarity reversal (recharging of capacitances) [26]. The work in [26] also discusses securing full ZVS range and closed-loop control for dc–dc DAB converters. However, a crucial challenge is to consolidate these dead-time modeling methods with the large-signal modeling of the DAB ac–dc converter. In [3], the nonlinear capacitor modeling is combined with optimal modulation trajectory generation for a dc–ac DAB converter, while also considering the impact of the dead-time period. Finally, in high-frequency applications, it is also crucial to model the impact of the nonideal switching voltages as perturbations on transformer currents, and vice-versa. While circuit-based transient solvers (simulations) can typically achieve this, an iterative frequency-domain analytical approach [27] is preferable, as it allows for fast analytical solutions that can be used in numerical optimizations. A summary of the correction factors provided in existing works is provided in Table I.

To summarize, while the transient behavior and circuit parasitics have been separately analyzed for DAB converters, a unified modeling method that combines these effects into a single framework is required to accurately model the DAB ac–dc converter operation over the ac line cycle. Thus, this article presents the following key contributions.

TABLE I
SUMMARY OF DIFFERENT MODELING METHODS FOR DAB

Reference	Type of analysis	Type	Key modeling aspects
[3], [10]	Time-domain	DC-AC, AC-DC	Dead-time with switch capacitances, lossy elements
[14], [15]	Frequency-domain	AC-DC	Switch capacitances, lossy elements
[17]-[19]	Generalized state-space	DC-DC	Lossy elements, transient phase-shifts
[20]	Time-domain	DC-DC	Transient phase-shift correction method
[21]	Time-domain	DC-DC	Dead-time modeling
[25], [26]	Time-domain	DC-DC	Dead-time modeling with switch capacitances, closed-loop control methods
[27]	Frequency-domain	DC-DC	Iterative dead-time modeling with switch capacitances
Proposed Method	Frequency-domain (+time-domain corrections)	AC-DC	Lossy components, transient phase-shifts and voltages, iterative dead-time with equivalent switch capacitances

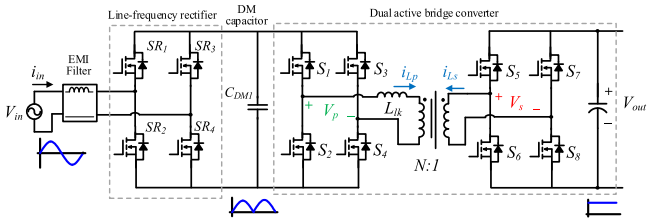


Fig. 1. Circuit diagram of the DAB ac–dc converter.

1) The generalized Fourier-series-based frequency-domain modeling approach for DAB converters is extended to ac–dc operation along with lossy and lossless parasitics.
2) A method is presented to model the ac bus voltage variations within a switching period, and phase-shift variations between switching periods using Fourier-series-based correction terms in the frequency domain.
3) The impact of dead-time switching transitions and nonlinear switch output capacitances is modeled in a hybrid time- and frequency-domain approach, yielding Fourier-series representations for switching transitions.
4) An optimal modulation trajectory generation algorithm using the proposed modeling method is applied to minimize conduction losses and maximize efficiency.

The frequency-domain correction factors substantially improve the accuracy in the modeling of DAB ac–dc transformer currents and power transfer. A key advantage of the proposed method is its flexibility for any modulation strategy and direct applicability to variations of DAB converters. The additive nature of the applied correction factors gives the flexibility to use any of the correction terms in isolation, based on the modeling requirements and converter design parameters.

II. Operation Principle and Analysis

The circuit topology of the indirect-matrix DAB ac–dc converter is shown in Fig. 1 [8]. The input ac voltage is passed through a line-frequency synchronous rectifier bridge (SR_1–SR_4) to obtain a rectified ac voltage at the capacitor C_{DM1}.

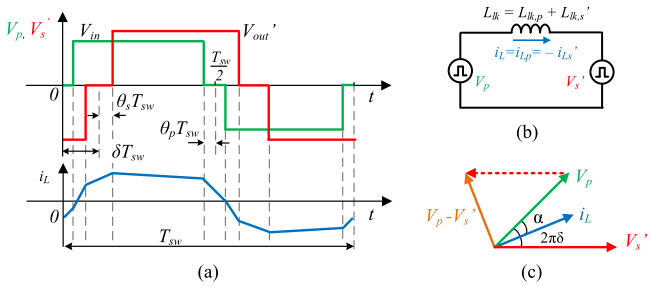


Fig. 2. (a) Characteristic DAB waveforms over one switching period with the modulation variables labeled. (b) Simplified equivalent DAB circuit for steady-state analysis. (c) Phasor diagram for the *k*th harmonic component in frequency-domain analysis.

This rectified ac voltage is then fed to a converter structure identical to a dc–dc DAB converter. A detailed operation analysis of this converter is covered in [13]. It should be noted while the analyses are presented with reference to an indirect-matrix DAB ac–dc converter, the same analyses can be applied for a direct-matrix DAB ac–dc converter [7] due to the identical operation of the high-frequency ac link (high-frequency bridges and the transformer).

In this article, the power transfer inductance is realized with the leakage inductance of the transformer, and henceforth, these two terms will be used interchangeably. The switches S_1–S_4 represent the ac-side high-frequency full-bridge (also referred to as the primary-side bridge), while the switches S_5–S_8 represent the dc-side high-frequency full bridge (also referred to as the secondary-side bridge). i_{Lp} and i_{Ls} are the transformer currents on the primary and secondary sides, respectively. In analyses where the specificity of sides is not required, i_L is used to represent the current through the leakage inductor. The secondary side quantities referred to the primary side are expressed with a "prime" symbol (for example, the output voltage V_{out} is referred to the primary side as V_{out}').

Similar to the classical dc–dc DAB, the converter in Fig. 1 can be operated with various advanced modulation strategies, as defined by the number of variables employed. The modulation variables comprise of three fractional phase-shifts (δ, θ_p, and θ_s) and the switching period T_{sw}, as noted in Fig. 2(a). In this article, the triple phase-shift (TPS) modulation (which regulates δ, θ_p, and θ_s) has been used due to its effectiveness in achieving low conduction losses for ac–dc DAB ([5], [28]).

The conventional frequency-domain analysis involves the superposition of the steady-state solutions of the DAB circuit at multiple harmonics. The conventional DAB equivalent circuit and phasor diagram for the *k*th harmonic are shown in Fig. 2(b) and (c), respectively. For a given switching cycle, a Fourier series decomposition of the primary and secondary voltages [Fig. 2(a)] gives the *k*th harmonic coefficients:

$$\langle V_p \rangle_k = -j\frac{4V_{\text{in}}\,(m)}{k\pi}\cos\left(2\pi k\theta_p\right),$$
$$\langle V_s' \rangle_k = -j\frac{4NV_{\text{out}}}{k\pi}\cos\left(2\pi k\theta_s\right) \tag{1}$$

where N is the transformer turns ratio, V_{out} is the dc output voltage, and V_p and V_s' are the transformer primary and secondary voltages, respectively. As the ac half line cycle represents the basic unit of symmetry (due to the synchronous rectification action of the input bridge SR_1–SR_4), it is used as the base period for all subsequent analyses. Thus, $V_{\text{in}}(m)$ is the zeroth-order approximation of the ac voltage in the *m*th integral switching cycle as given by (2), with T_L representing ac line cycle period:

$$V_{\text{in}}\ (m) = V_{\text{in},pk}\ \sin\left(2\pi m\frac{T_{\text{sw}}}{T_L}\right),\ m\ =\ \text{floor}\left(\frac{T_{\text{sw}}}{T_L}\right). \tag{2}$$

From the phasor diagram, the *k*th harmonic of primary-side active power flow is derived in (3), where the total leakage inductance L_{lk} is obtained by summing the primary leakage and the referred secondary leakage [Fig. 2(b)]:

$$\langle P \rangle_k = \langle V_p \rangle_k\ \langle {i_L}^* \rangle_k = \frac{\langle V_p \rangle_k \langle V_s' \rangle_k \sin\left(2\pi k\delta\right)}{4\pi k f_{\text{sw}} L_{\text{lk}}}. \tag{3}$$

Additionally, the *k*th harmonic amplitude of the inductor current i_L is given by (4). The time-domain waveform can be reconstructed by (5), where $\alpha_k = \tan^{-1}\left(\frac{\langle V_p \rangle_k - \langle V_s' \rangle_k \cos(2\pi k\delta)}{\langle V_s' \rangle_k \sin(2\pi k\delta)}\right)$ and represents the angle between the phasors of the i_L and V_p [Fig. 2(c)]. The value of $k_{\max}$ affects the accuracy of this approach and is discussed in Section IV-B:

$$\langle i_L \rangle_k = -j\left(\frac{\langle V_p \rangle_k - \langle V_s' \rangle_k e^{-j2\pi k\delta}}{2\pi f_{\text{sw}} L_{\text{lk}}}\right) \tag{4}$$

$$i_L(t) = \sum_{k=1}^{k_{\max}} \left|\langle i_L \rangle_k\right| \sin\left(2\pi k f_{\text{sw}} t + \alpha_k\right)$$
$$t \in \left[mT_{\text{sw}}, (m+1)\,T_{\text{sw}}\right]. \tag{5}$$

Considering PFC action, the time-varying input power is given by (6), where $V_{\text{in},pk}$ is the peak of the grid voltage, $I_{\text{in},pk}$ is the peak of the grid current, P_{av} is the average input power, and ω_L is the ac line angular frequency. To satisfy power balance, (6) is equated to the *m*th switching cycle averaged power given by (3). This power balance constraint C_p (7) forms a necessary condition for the DAB ac–dc converter operation:

$$P_{\text{in}}\,(t)\ = V_{\text{in},pk}\ \sin\left(\omega_L t\right) I_{\text{in},pk}\ \sin\left(\omega_L t\right)$$
$$= \frac{P_{\text{av}}}{2}\ \left(1 - \cos\left(2\omega_L t\right)\right) \tag{6}$$

$$C_p = \frac{P_{\text{av}}}{2}\ \left(1 - \cos\left(2\omega_L t\right)\right) = \sum_{k=1}^{k_{\max}} \langle P \rangle_k. \tag{7}$$

Thus, (1)–(7) form the conventional frequency-domain modeling approach for DAB ac–dc converters. Due to the inherent generality of the frequency-domain approach, the analysis is applicable for all DAB modulation schemes (SPS, DPS, TPS, and VF-TPS). However, as is evident, this conventional modeling approach is based on *Assumptions 1* and *2*.

III. Proposed Modeling Approach

To identify and address the violations of assumptions listed above for the DAB ac–dc operation, the conventional frequency-domain modeling approach is modified with four analytical

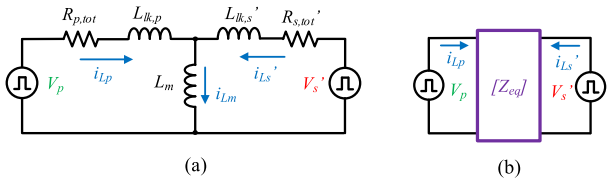


Fig. 3. (a) Detailed steady-state equivalent circuit of the DAB. (b) Equivalent representation as a two-port network with a complex $Z_{\rm eq}$.

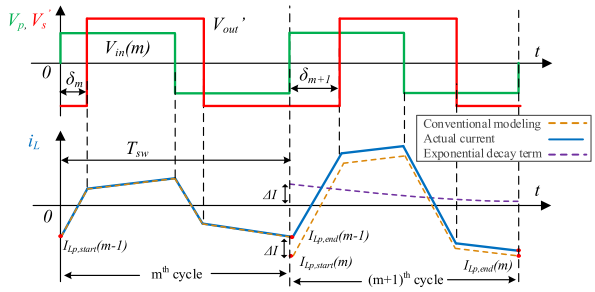


Fig. 4. Illustration of the steady-state assumption getting violated when the phase-shifts change between two switching cycles.

correction factors described in this section. While the analyses in Sections III-A and III-C are in the frequency domain, the analysis in Section III-B is carried out in the time domain. Section III-D utilizes the time domain for analyzing the switching transitions, but the final correction terms are applied in the frequency domain. Thus, the proposed modeling is based on a hybrid frequency- and time-domain analysis approach. For each subsection covering one modeling component, the limitations of the conventional modeling method are highlighted and used to formulate the corresponding improvements leading to the proposed modeling approach.

A. Generalized Complex Matrix-Based Analysis

The conventional modeling methods (both frequency and time domains) ignore the transformer magnetizing inductance and the circuit ESR for the steady-state analysis, which may lead to non-negligible modeling errors. These elements are incorporated by extending the conventional projection-based model shown in Fig. 2(b) to include ESRs and magnetizing inductances [Fig. 3(a)]. The effective circuit resistance Z_r comprises of the ESRs of the transformer and the bus (input/output) capacitors, and the $R_{\rm ds,ON}$ of the switches. As the analysis is performed in the frequency domain, the complex two-port matrix-based method is adopted for circuit analysis [Fig. 3(b)]. The computation of the equivalent impedance matrix for kth harmonic component is shown as follows:

$$Z_L(k) = jk\omega_{\rm sw}\begin{bmatrix} L_{lk,p}+L_m & L_m \\ L_m & L'_{\rm lk,s}+L_m \end{bmatrix}$$

$$Z_r = \begin{bmatrix} R_{p,\rm tot} & 0 \\ 0 & R'_{\rm s,tot} \end{bmatrix} \tag{8}$$

$$Z_{\rm eq}(k) = Z_L(k) + Z_r. \tag{9}$$

For the analysis of the dc component, Z_L is set to zero. For the kth harmonic, primary and secondary currents are computed as

$$\langle i_L\rangle_k = (Z_{\rm eq}(k))^{-1}\langle V\rangle_k \text{ where } \langle V\rangle_k = \begin{bmatrix} \langle V_p\rangle_k \\ \langle V'_s\rangle_k \end{bmatrix}. \tag{10}$$

Equation (10) will reduce to the conventional frequency-domain modeling equations (4) and (5) if the value of L_m and resistances in the matrix Z_r are set to zero. Furthermore, the complex matrix-based method can be extended to include any other circuit elements that may influence steady-state operation. Specifically, the presence of ESRs will be of key interest, as it not only alters the value of power transferred but also provides damping to dc current components arising due to the phenomena discussed in subsequent sections.

B. DC Current Component Due to Transient Phase-Shifts

To maintain PFC operation as per (7), the input voltage and power reference for the DAB must change continuously. Hence, the circuit is consistently in a transient state, with changing phase-shifts at every switching cycle. In an ideal DAB operation, the applied voltages V_p and V_s' are zero-mean over a switching cycle (this assumption itself will be addressed in Section III-D). Since the conventional modeling approach (Section II) is based on *Assumption 1*, the computed steady-state solutions of the transformer currents i_L for each switching period are individually zero-mean. However, this steady-state assumption gets violated if there is a change in phase-shift values between switching cycles, as shown in Fig. 4. If the steady-state assumption is applied, it results in a discontinuity in the computed current at the transition between switching cycles. As the current through an inductor cannot be discontinuous, the actual current at the start of the second switching period cannot be equal to $I_{Lp,\rm start}(m)$ (as predicted by the conventional model), but instead must be equal to the current at the end of the earlier switching period, $I_{Lp,\rm end}(m-1)$.

To model this phenomenon, a dc-component correction term is added to the zero-mean component of the inductor current, at the start of the second switching period. This dc component decays exponentially with the time constant of the equivalent R-L circuit, formed by the leakage inductance and the total circuit ESR. The exponential decay component for the mth switching cycle is computed in the time domain using (11), with other variables as defined in Fig. 4. Finally, the effective transformer current is computed, as shown in (12):

$$\Delta i_{Lp}(t) = \left(I_{Lp,\rm end}(m-1) - I_{Lp,\rm start}(m)\right)e^{-R_{\rm lk}t/L_{\rm lk}} \tag{11}$$

$$i_{Lp,\rm decay}(t) = i_{Lp}(t) + \Delta i_{Lp}(t),\ t\in[mT_{\rm sw},(m+1)T_{\rm sw}]. \tag{12}$$

As the correction term $\Delta i_{Lp}(t)$ is applied in the time domain, $i_{Lp}(t)$ represents such a time-domain reconstruction of the currents computed from the frequency-domain analysis.

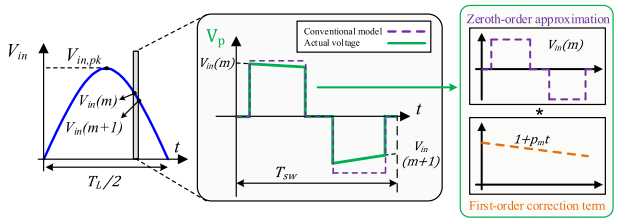


Fig. 5. Changing ac voltage over the switching cycle, which is modeled with a first-order approximation over the switching period.

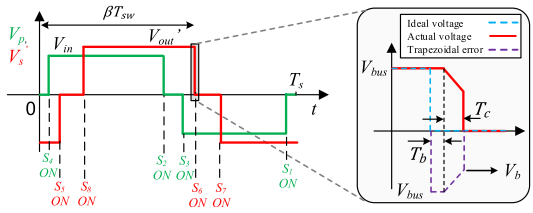


Fig. 6. Switching sequence for the TPS scheme, along with the trapezoidal waveform construction in time domain for nonideal switching transitions.

C. Transient AC Input Voltage Component

In a DAB ac–dc converter, the ac input voltage changes continuously throughout a switching period, thus violating *Assumption 1*. Traditionally, the zeroth-order approximation on the ac input voltage is used when analyzing the circuit behavior within a switching period. However, this approximation loses accuracy as the ratio of switching frequency to the ac line frequency decreases. To model the changing ac voltage over a switching period, a first-order Taylor-series approximation for the input voltage is employed, as defined in (13). Here, $p_m V_{in}(m)$ represents the slope of the normalized correction term applied to the $V_{\text{in}}(m)$, which is the zeroth-order approximation for the mth switching cycle:

$$V_{\text{in}}\ (t) = \ (1 + p_m t)\ V_{\text{in}}\ (m)\ \text{ for } t \in [mT_{\text{sw}}, (m+1)\,T_{\text{sw}}] \tag{13}$$

$$p_m = \frac{V_{\text{in}}\,(m+1)\ -\ V_{\text{in}}\,(m)}{T_{\text{sw}}\ \cdot\ V_{\text{in}}\,(m)}\ \text{ for } V_{\text{in}}\,(m) \neq 0. \tag{14}$$

It can be seen from (14) that the impact of the changing ac voltage is more significant near zero crossings. As shown in (13) and Fig. 5, the first-order approximation is obtained by the time-domain multiplication of $V_{\text{in}}(m)$ with a truncated ramp signal $(1 + p_m t)$ for $t \in [mT_{\text{sw}}, (m+1)T_{\text{sw}}]$. Using the property of convolution in the frequency domain, the equivalent Fourier series coefficients for the primary-side voltage are computed as

$$\langle V_{p(\text{ramp})}\rangle_k = \sum_{l=-k_{\max}}^{k_{\max}} \langle V_{\text{ramp}}\rangle_l \langle V_p\rangle_{k-l} \tag{15}$$

where $\langle V_p\rangle_k$ is as defined in (1). The Fourier series coefficients $\langle V_{\text{ramp}}\rangle_k$ for the periodic truncated ramp signal are given by

$$\langle V_{\text{ramp}}\rangle_k = \ j\frac{p_m T_{\text{sw}}}{k\pi},\ \langle V_{\text{ramp}}\rangle_0 = 1 + 0.5 p_m\ T_{\text{sw}}. \tag{16}$$

With the first-order approximation, the half-wave symmetry and zero-mean nature of V_p are no longer retained, as seen from Fig. 5. Thus, the dc component and even harmonics cannot be neglected for the harmonic superposition analysis.

D. Effects of Dead-Time Periods and Switch Capacitances

The presence of switch output capacitances and dead-time periods (neglected in conventional modeling based on *Assumption 2*) result in nonzero switching transition times. Due to these nonzero transition times, the effective V_p and V_s' are no longer ideal square or ideal quasi-square waveforms. As the nonideal voltages directly alter the transformer current shape and power transfer, it is crucial to accurately model these switching transitions in high-frequency applications.

In this article, the dead-time period is assumed to occur on the rising edge of the pulse signals. Thus, the ideal switching case is a soft-switching turn-ON transition with zero transition time, shown by the dashed cyan line in Fig. 6. For an ideal transition, the conventional modeling method is accurate. However, to model practical nonzero transition times, a linear approximation is proposed for the nonideal voltages, which is then implemented as a frequency-domain correction term.

In this article, a generalized trapezoidal error waveform is proposed to implement a first-order approximation of the voltages during the dead-time period, as illustrated in Fig. 6. This trapezoidal error waveform, when subtracted from the ideal quasi-square voltage waveform, yields the actual voltage waveform. The kth harmonic Fourier series coefficients for the trapezoidal signal are computed in (17). The variables V_b, T_b, T_c, and β are as defined in Fig. 6, and are computed for each switch transition separately. V_{bus} is equal to $V_{\text{in}}(m)$ and $V_{\text{out}}{}'$ for the primary- and secondary-side switches, respectively. The subscript *sx (x = 1 to 8)* corresponds to the switch index.

$$\begin{aligned}\langle V_{\text{trap},sx}\rangle_k = {} & e^{-j\left(2k\pi(\beta+\frac{0.5T_b}{T_{\text{sw}}})\right.}\left(-j\frac{2V_{\text{bus}}}{k\pi}\sin\left(k\pi\frac{T_b}{T_{\text{sw}}}\right)\right) \\ & + e^{-j\left(2k\pi(\beta+\frac{T_b+0.5T_c}{T_{\text{sw}}})\right.}\left(\left(\frac{V_{\text{bus}}+V_b}{k\pi}\right)\sin\left(k\pi\frac{T_c}{T_{\text{sw}}}\right)\right. \\ & -j\left(\frac{-V_{\text{bus}}+V_b}{k\pi}\right)\left(\cos\left(k\pi\frac{T_c}{T_{\text{sw}}}\right)+\left(\frac{T_{\text{sw}}}{k\pi T_c}\right)\sin\left(k\pi\frac{T_c}{T_{\text{sw}}}\right)\right)\Big)\end{aligned} \tag{17}$$

$$\langle V_{\text{trap},sx}\rangle_0 = V_{\text{bus}}\left(\frac{T_b}{T_{\text{sw}}}\right) + \frac{V_{\text{bus}}+V_b}{2}\left(\frac{T_c}{T_{\text{sw}}}\right). \tag{18}$$

Referring to Fig. 6, the switching transitions are classified as "rising" transitions (i.e., when the voltage rises for S_1, S_4, S_5, and S_8 turn-ON) and "falling" transitions (for S_2, S_3, S_6, and S_7 turn-ON). The correction term in (17) is added for a "rising" transition and subtracted for a "falling" transition. Thus, the Fourier-series coefficients for the voltages are computed in (19) and (20):

$$\begin{aligned}\langle V_{p(\text{trap})}\rangle_k = {} & \langle V_p\rangle_k\ + \langle V_{\text{trap},s1}\rangle_k - \ \langle V_{\text{trap},s2}\rangle_k \\ & - \ \langle V_{\text{trap},s3}\rangle_k + \ \langle V_{\text{trap},s4}\rangle_k\end{aligned} \tag{19}$$

$$\begin{aligned}\langle V_{s(\text{trap})}\rangle_k = {} & \langle V_s\rangle_k\ + \langle V_{\text{trap},s5}\rangle_k - \ \langle V_{\text{trap},s6}\rangle_k \\ & - \ \langle V_{\text{trap},s7}\rangle_k + \ \langle V_{\text{trap},s8}\rangle_k\ .\end{aligned} \tag{20}$$

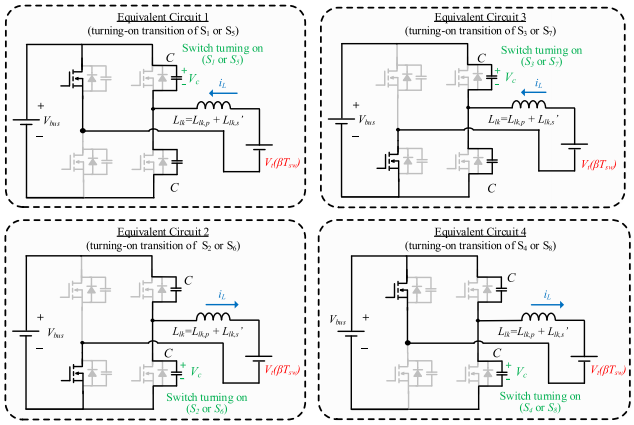


Fig. 7. Four unique equivalent circuits for resonant switching transitions that exist for different switches in the DAB, when using TPS modulation.

TABLE II
COMPUTATION OF VARIABLES USED IN (21) AND (22) FOR EACH SWITCH

Switch	β	V_{bus}	V_d	C
S1	$1 - \theta_p$	$V_{in}(m)$	$-V_s'(\beta T_{sw})$	$C_{oss,p,tr} = f(V_{in}(m))$
S2	$0.5 - \theta_p$		$-V_s'(\beta T_{sw})$	
S3	$0.5 + \theta_p$		$V_{in}(m) + V_s'(\beta T_{sw})$	
S4	θ_p		$V_{in}(m) - V_s'(\beta T_{sw})$	
S5	$\delta + 1 - \theta_s$	V_{out}'	$-V_p(\beta T_{sw})$	$C_{oss,s,tr}'$
S6	$\delta + 0.5 - \theta_s$		$-V_p(\beta T_{sw})$	
S7	$\delta + 0.5 + \theta_s$		$V_{out}' + V_p(\beta T_{sw})$	
S8	$\delta + \theta_s$		$V_{out}' - V_p(\beta T_{sw})$	

The computation of V_b, T_b, T_c, and β for each switch depends on the current at the switching instant and the switching states of other legs. For the TPS switching scheme shown in Fig. 6, the transition behavior for each switch is described by one of the four equivalent circuits shown in Fig. 7. The equivalent circuits differ in the effective dc voltage applied across the inductor during the switching transition. However, a generalized resonant circuit can be used for all the equivalent circuits. With current and voltage polarities as shown in Fig. 7, (21) and (22) describe the general resonant behavior for all four equivalent circuits:

$$V_c\ (t) = -\frac{i_{L0}}{2\omega_r C}\sin(\omega_r t) + (V_{\rm bus} - V_d)\cos(\omega_r t) + V_d \tag{21}$$

$$i_L\ (t) = -2\omega_r C\,(V_{\rm bus} - V_d)\sin(\omega_r t) + i_{L0}\cos(\omega_r t) \tag{22}$$

where $\omega_r = \sqrt{1/2L_{\rm lk}C}$ is the resonant frequency of the equivalent LC circuit, i_{L0} is the initial value of i_L, and other variables are defined in Table II for the eight switches.

For the effective switch output capacitance C, the voltage-dependent nonlinearity is incorporated by using the time-related capacitance. As seen from Fig. 7, the effective capacitance during a switching transition is the sum of the capacitances of the top and bottom switches in a half-bridge. To accurately capture the capacitor nonlinearity, the effective "per-switch" capacitance as a function of voltage is expressed as follows,

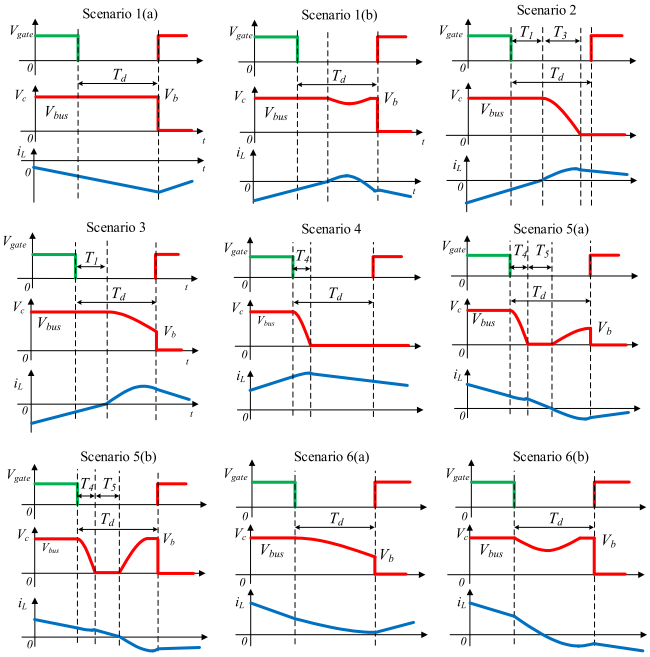


Fig. 8. Illustration of the six distinct scenarios (with subvariations) for switching transitions in the DAB circuit.

where V is the voltage across the charging switch:

$$C\ (V) = 0.5\,(C_{\rm top}\,(V) + C_{\rm bot}\,(V_{\rm bus} - V))\,. \tag{23}$$

The effective time-related capacitance can thus be expressed as $C = \int_0^{V_{\rm bus}} C(V)dV$. Since $V_{\rm bus}$ is fixed on the dc side, the effective time-related capacitance is constant; however, since primary-side $V_{\rm bus}$ changes over the line cycle, the capacitance for the primary-side switches for the mth switching cycle is computed as $C(m) = \int_0^{V_{\rm in}(m)} C(V)dV$. Last, it should be noted that the transformer intrawinding capacitance appears in parallel to the switch capacitances during switching transitions [27]. Thus, these capacitances can be lumped along with the switch capacitance C for all analyses in this section.

Based on the direction and magnitude of i_L and $V_{\rm bus}$, the switching transitions are classified into six scenarios (Fig. 8). The conditions to identify the correct scenario and the corresponding values of V_b, T_b, and T_c are derived from the solutions of (21) and (22) and are compiled in Table III. For the sake of simplicity, the dead-time period T_d is set at the same value for all switches (Table IV). However, it should be noted that the dead-time can also be optimally set for each switching transition, based on objectives such as maximizing efficiency or enforcing full ZVS. Regardless, Fig. 8 and Table III cover all possible scenarios that may exist with fixed or variable dead-time switching transitions. Additionally, the variables T_1, T_2, T_3, T_4, and T_5 used in Table III are defined as follows:

T_1: Time from the beginning of dead-time period, after which i_L crosses from negative to positive (obtained using a binary search method)

$$T_2 = \frac{1}{4}\frac{2\pi}{\omega_r},\ T_3 = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_d}{|V_{\rm bus} - V_d|} + \frac{\pi}{2}\right) \tag{24}$$

TABLE III
SCENARIOWISE EXPRESSIONS FOR TRAPEZOIDAL WAVEFORM VARIABLES

Scenario	Condition to exist	T_b	T_c	V_b
1(a), 1(b)	$i_{L0} < 0$ and $i_L(T_d) < 0$	0	T_d	V_{bus}
2	$i_{L0} < 0$, $i_L(T_d) > 0$ and $(T_1+T_2) < T_d$	T_1	T_3	0
3	$i_{L0} < 0$, $i_L(T_d) > 0$ and $(T_1+T_2) > T_d$	T_1	$T_d - T_b$	$\min(V_{bus}, (V_{bus} - V_d) * cos(\omega_r(T_d - T_b)) + V_d)$
4	$i_{L0} > 0$, $real(T_4) < T_d$ and $imag(T_4) = 0$	0	T_4	0
5(a)*, 5(b)*	$i_{L0} > 0$, $real(T_4) < T_d$, $imag(T_4) = 0$ and $i_L(T_d) < 0$	0, T_4+T_5	T_4, $T_d - T_b$	0, $\min(V_{bus}, (V_{bus} - V_d) * cos(\omega_r(T_d - T_b)) + V_d)$
6(a), 6(b)	$i_{L0} > 0$, $real(T_4) > T_d$ and/or $imag(T_4) \neq 0$	0	T_d	$\min(V_{bus}, -\frac{i_{L0}}{2\omega_r C}\sin(\omega_r t) + (V_{bus} - V_d)\cos(\omega_r T_d) + V_d)$

*Scenario 5 comprises two superposed trapezoidal correction terms in one dead-time period.

TABLE IV
KEY CONVERTER SPECIFICATIONS

Converter Parameter	Value
AC input voltage and frequency ($V_{in,rms}, f_L$)	230 V, 400 Hz
DC output voltage (V_{out})	28 V
Nominal power and input current ($P_{av,nom}, I_{in,nom}$)	1 kW, 4.35 A
Transformer turns ratio (N:1)	9:1
Switching frequency (f_{sw})	160 kHz
Total leakage inductance (L_{lk})	6.4 µH
Magnetizing inductance (L_m)	600 µH
Dead-time period (T_d)	60 ns
Nominal switch capacitances ($C_{oss,p,tr}, C_{oss,s,tr}$)*	413 pF, 5010 pF
Primary/Secondary total ESR ($R_{p,tot}, R_{s,tot}$)	160 mΩ, 2.83 mΩ
Number of harmonics considered (k_{max})	51

*Primary capacitance value mentioned here is at peak of the ac line voltage. In code, this is computed based on the ac voltage value $V_{\rm in}(\rm m)$ for a given switching period.

$$T_4 = \frac{1}{\omega_r}\sin^{-1}\frac{V_d}{\sqrt{\left(\frac{-i_{L0}}{2\omega_r C}\right)^2 + (V_{\rm bus} - V_d)^2}} - \frac{1}{\omega_r}\tan^{-1}\frac{V_{\rm bus} - V_d}{\left(\frac{-i_{L0}}{2\omega_r C}\right)}. \quad (25)$$

T_5: Time from when full ZVS is achieved, to the instant when the current polarity reverses (obtained using a binary search method).

The first Scenario 1(a) represents the condition when the direction of i_L is negative throughout the dead-time period (i.e., fully hard-switching transition). As an alternative Scenario 1(b), the direction i_L reverses during dead-time, but due to insufficient energy and short resonant time-period, the voltage gets clamped to its original value by the end of the dead-time period—thus also resulting in a fully hard switched transition. Scenario 2 represents the case when i_L is negative at the start of the dead-time period, crosses zero during the dead-time period, and then fully discharges the capacitors to realize ZVS turn-ON.

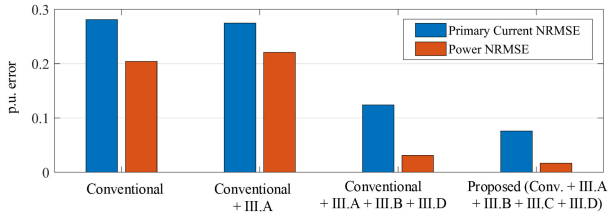


Fig. 9. Current and power NRMSEs for each step of the proposed modeling process, starting from the conventional modeling approach.

In Scenario 3, i_L similarly crosses from negative to positive during the dead-time period but does not have sufficient energy to fully discharge the switch capacitances, resulting in a partial hard-switching transition. Scenario 4 considers the case when i_L is positive at the start of the dead-time period, and there is sufficient energy to realize ZVS turn-ON. Scenarios 5(a) and (b) represent the case when i_L is positive at the start of the dead-time period, fully realizes ZVS, but then changes polarity during the remainder of the dead-time period. This phenomenon can happen when large dead-time periods are used and results in recharging of the switch capacitances, also known as voltage polarity reversal during dead-time ([22], [25]). Finally, Scenario 6(a) assumes that i_L is positive at the start of the dead-time period, but there is not sufficient energy to complete the resonant transition. In an alternative Scenario 6(b), the current becomes negative during the dead-time period, thus resulting in a partially or fully hard-switched transition.

Following the computation of the V_b, T_b, and T_c values for each switching transition, (19) and (20) are used to compute the Fourier series coefficients of the nonideal voltages, and the updated transformer current is computed using (10). It should be noted that at every iteration for computing V_b, T_b, and T_c, each switching transition is analyzed independently of the others. However, the perturbation in voltages created by one switching transition impacts the current values for subsequent switching transitions. To ensure convergence, this steady-state numerical model is iterated the exit condition for is met. The exit condition for convergence uses the mean square error of the time-reconstructed transformer currents between successive iterations, where g refers to the index of the present iteration. The threshold $K_{\rm exit}$ is selected to provide a good tradeoff between accuracy and time, and is discussed in Section IV-B.

$$C_{\rm exit}: \left(\frac{1}{T_{\rm sw}}\int_0^{T_{sw}} (i_{L,g} - i_{L,g-1})\,dt\right)^2 < K_{\rm exit} \quad (26)$$

Thus, by implementing the modeling steps described in this section, the proposed modeling approach addresses the issues arising from the two assumptions used for conventional modeling. The components in Sections III-B and III-C tackle *Assumption 1*, while the components in Sections III-A and III-D tackle *Assumption 2*. The full implementation of the proposed modeling process is shown in the flowchart in Fig. 13. As the final voltage and current expressions of the proposed modeling approach are obtained in the frequency domain, (3) and (7) are directly used for computing total power over a switching cycle.

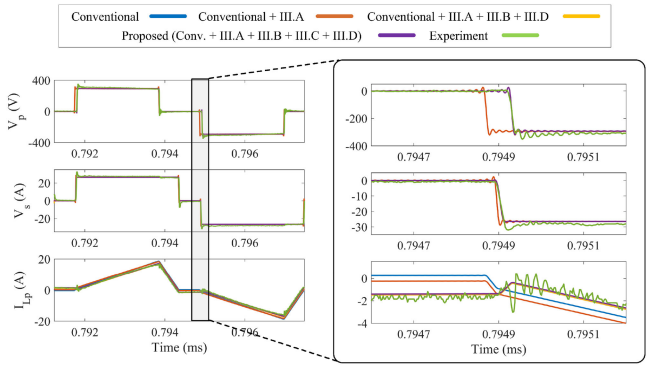


Fig. 10. Transformer voltages and current for each step of the proposed modeling process, starting from the conventional modeling approach.

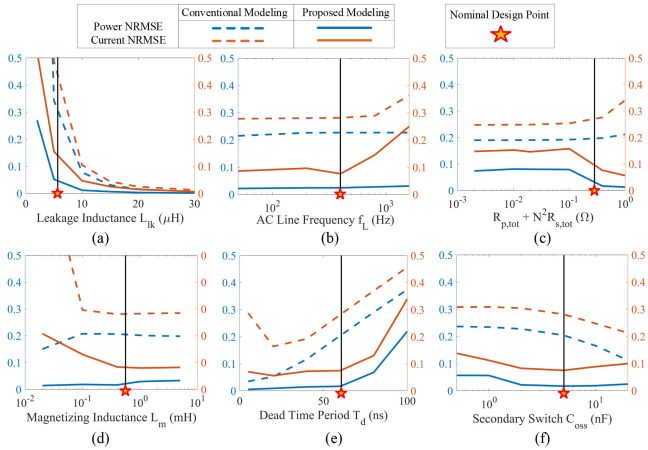


Fig. 11. (a)–(f) Trends in modeling errors for proposed and conventional methods over sweeps of key converter parameters.

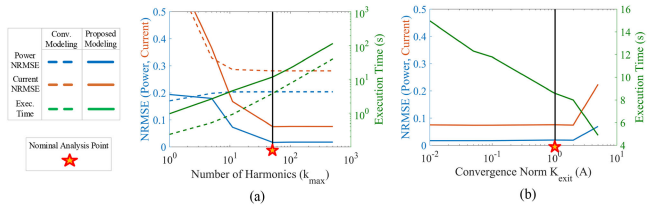


Fig. 12. Analysis of offline computation times and modeling errors for half ac line cycle (200 switching cycles) as a function of (a) $k_{\max}$ and (b) K_{exit}.

Another key advantage of the proposed modeling approach is that it is generic irrespective of the phase-shift direction (i.e., positive/negative) by virtue of the frequency-domain representations of all voltages and currents at all key steps.

IV. Quantitative Assessments of the Proposed Modeling Approach

To assess the effectiveness and accuracy of the proposed modeling method, two metrics are defined for quantifying the modeling errors: 1) the normalized root-mean-square error (NRMSE) of the power transferred over the ac half line cycle, and 2) the NRMSE of the transformer primary winding current over the ac half line cycle. The power NRMSE is formulated in (27),

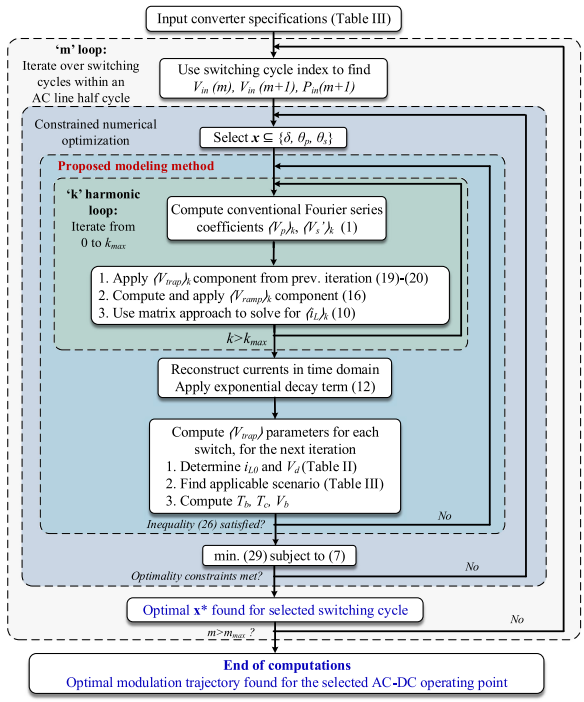


Fig. 13. Flowchart of the optimal modulation trajectory generation process, with the proposed modeling approach at its core.

quantifies the disparity between the power transfer computed using analytical modeling and the power delivered in the actual converter:

$$P_{\text{NRMSE}} = \frac{1}{P_{\text{av,nom}}} \times \sqrt{\frac{1}{m_{\max}} \sum_{m=1}^{m=\frac{T_L}{2T_{\text{sw}}}} \left(\frac{1}{T_{\text{sw}}} \int_0^{T_{sw}} \left(\widehat{V_p} \widehat{i_{Lp}} - V_p i_{Lp} \right) dt \right)^2} \tag{27}$$

where $\widehat{V_p}$ and $\widehat{i_{Lp}}$ refer to the modeled primary voltage and current, respectively, in the time domain, and V_p and i_{Lp} are the corresponding values in the actual converter. A high value of the power NRMSE corresponds to a discrepancy in power transfer and high input current THD. The transformer primary current NRMSE [in (28)] represents the errors in modeling of the current waveform when reconstructed in the time domain.

The current NRMSE relates to the accuracy of predicting current magnitude at switching instants (turn-ON and turn-OFF):

$$i_{\text{NRMSE}} = \frac{1}{I_{\text{in,nom}}} \times \sqrt{\frac{1}{m_{\max}} \sum_{m=1}^{m=\frac{T_L}{2T_{\text{sw}}}} \left(\frac{1}{T_{\text{sw}}} \int_0^{T_{sw}} \left(\widehat{i_{Lp}} - i_{Lp} \right) dt \right)^2}. \tag{28}$$

The combination of power NRMSE and current NRMSE affirms the overall modeling performance. For the analyses in this section, the converter specifications are specified in Table IV, and the trajectories of modulation variables (δ, θ_p, and θ_s)

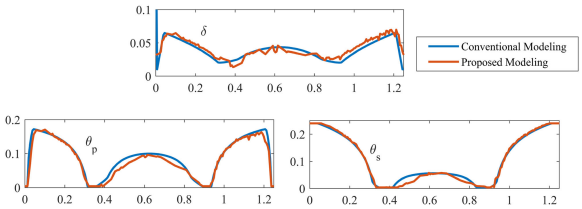
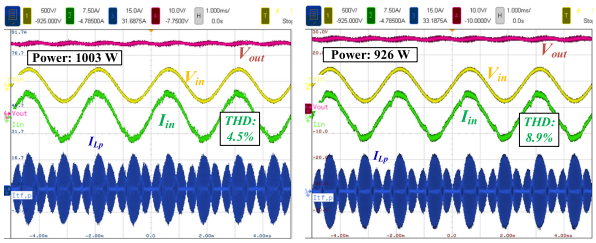


Fig. 14. Conduction-loss-optimal modulation trajectories over half ac line cycle, generated using the conventional and proposed approaches. *x*-axis for each plot corresponds to time (in ms).



(a) (b)

Fig. 15. Steady-state experimental results at 1 kW for the modulation trajectories using (a) proposed modeling and (b) conventional modeling.

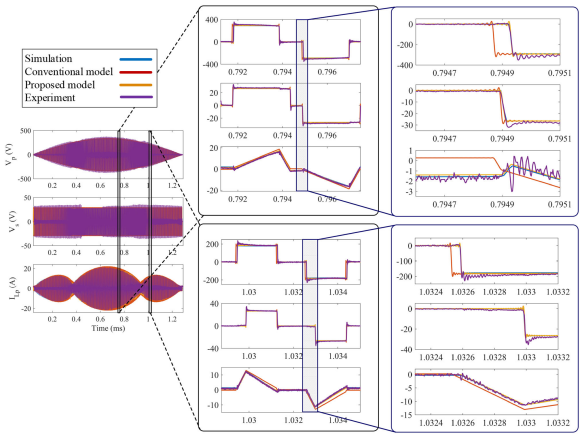


Fig. 16. Comparisons of the time-reconstructed waveforms from the conventional and proposed modeling approaches against experimental results and the high-fidelity simulation model at different time scales.

are fixed to the "conventional modeling" curves in Fig. 14. Additionally, the benchmark for actual converter operation is a high-fidelity simulation model incorporating all nonidealities and parasitics. It is validated in Fig. 16 that the simulation model shows good agreement with experimental results, thus allowing its use as a proxy for actual converter operation.

A. Stagewise Modeling Error Analysis

This analysis quantifies the improvements achieved with each component of the proposed modeling approach described in Section III and comparisons with the conventional modeling approach. The effectiveness of each modeling component is confirmed from Fig. 9, which shows the power NRMSE the primary current NRMSE for each step of the modeling process. The proposed approach yields current and power NRMSEs of 7.6% and 1.7%, respectively, as opposed to 28% and 20%, respectively, for the conventional modeling approach.

Corresponding to the NRMSE metric results presented in Fig. 9, the reconstructed time-domain transformer currents and voltages are compared later in Fig. 16. Over the ac half line cycle, two distinct switching cycles are selected with varying degrees of hard- and soft-switching transitions for each switch. From the switching cycle-level plots, the discrepancies in the current modeled using the conventional approach are visible, due to the violations of *Assumptions 1* and *2*. To visually illustrate the contribution of each correction term in the proposed modeling method, Fig. 10 considers one particular switching cycle from Fig. 16. Subsequently, the voltages and currents are plotted while considering various correction factors. By closely looking at zoomed-in switching transitions in the rightmost plots in Figs. 10 and 16, the impact of different correction factors can be appreciated, which together result in substantial changes in the transformer current. It should be noted that since Fig. 10 only shows one switching cycle, and the contribution of each correction factor will differ based on the switching cycle, the ac cycle-wide NRMSE results (Fig. 9) should be referred to for a complete assessment of the respective NRMSE contributions. The superior accuracy of the proposed approach is essential to precisely determine the modulation trajectories, power transfer, ZVS boundaries, and current stresses in the converter.

B. Modeling Error Trends With Key Converter Parameters

The analyses in Section IV-A has been performed for a specific set of converter parameters and a specific operating point as defined in Table IV. To quantify and compare the effectiveness of the proposed method versus the conventional method, this section presents the trends of modeling error with 1-D sweeps of key converter parameters. Aside from the parameter being swept in the subsequent analyses, the remaining parameters are set to the nominal values in Table IV. It should be noted that the 1-D parameter sweeps do not account for the coupling between various converter parameters. However, the error trends presented in this section seek to form the guidance on the limits of the conventional modeling method, and correspondingly, the accuracy improvements offered by the proposed method.

First, the impact of leakage inductance on the modeling errors is analyzed in Fig. 11(a). For a DAB ac–dc converter, the upper bound on the leakage inductance value is given by $L_{\mathrm{lk,max}} \leq NV_{\mathrm{out}}V_{\mathrm{in,pk}}/16P_{\mathrm{av,max}}f_{\mathrm{sw}}$, where $P_{\mathrm{av,max}}$ represents the maximum average power transferred. As seen in Fig. 11(a), a lower value of L_{lk} results in higher errors due to the nonidealities discussed in Section III. Conversely, a higher value of L_{lk} results in lower modeling errors. Thus, the proposed modeling approach provides greater accuracy benefit when inductance values are further away from the upper bound.

Regarding ac line frequency, it is clear from Section III that the impact of transient modeling errors increases with conventional modeling as the ratio f_{sw}:f_L decreases due to the violation of *Assumption 1*. This is illustrated in Fig. 11(b), where ac line frequencies ranging from 50 Hz to 3.2 kHz are considered.

However, the proposed modeling approach does not lead to an increase in errors with increasing f_L.

The impact of ESR (for the entire circuit, referred to the primary side) is shown in Fig. 11(c). The circuit ESR is varied from 2 mΩ to 1 Ω. For lower ESRs, the modeling errors do not change significantly; however, the proposed model offers substantially lower errors for cases with higher ESRs, which is consistent with expectations laid out in Section III.

The impact of the magnetizing inductance value on the modeling errors is shown in Fig. 11(d). As the conventional modeling approach does not consider the current flowing into the magnetizing inductance branch, the modeling errors increase drastically with lower values of L_m. For applications targeting a lower L_m, the proposed modeling approach offers considerable improvement in accuracy.

The error in the modeling due to dead time varies depending on several factors—the prevalence of hard switching and soft switching, and the inductive energies at each switching instant. As seen from Fig. 11(e), the conventional modeling approach offers low errors in a scenario with minimal T_d. However, the modeling errors increase as T_d increases, with the proposed method offering significantly better performance.

In Fig. 11(f), the modeling errors due to switch output capacitances ($C_{\rm oss}$) are shown. While the results are shown for secondary-side $C_{\rm oss}$, similar results are obtained with primary-side $C_{\rm oss}$. With higher $C_{\rm oss}$, the discharging during dead-time intervals is slower, resulting in increased hard-switching. A fully hard-switched converter with near-instantaneous transitions resembles an ideal converter. Hence, the conventional modeling errors decrease with higher capacitance. However, with accurate dead-time modeling, the proposed modeling method maintains consistently low errors throughout.

An analysis of the impact of computation complexity and modeling accuracy is presented in the results in Fig. 12. Fig. 12(a) shows the impact of the number of harmonics ($k_{\rm max}$) on the modeling accuracy and code execution time for one half ac line cycle (200 switching cycles). The averaged execution times are measured on MATLAB R2019b running on a computer with Intel Core i7-8700 CPU and 16 GB of RAM. While the execution time increases proportionately with $k_{\rm max}$, the accuracy improvements are incremental beyond $k_{\rm max} = 50$. For lower $k_{\rm max}$ values, the errors for the conventional and proposed modeling approaches are comparable, as the correction factors described in Section III cannot be captured with truncation of higher order harmonics. While the proposed modeling method has higher offline computation times (nearly 2x of conventional), significant improvements in accuracy are also achieved. For all modeling results in this article, $k_{\rm max} = 51$ is used.

Fig. 12(b) shows the variation of modeling accuracy and offline computation times with varying values of the convergence exit parameter $K_{\rm exit}$ [defined in (26)]. The excellent convergence rate of the model is illustrated with virtually no change in modeling accuracy for $K_{\rm exit} < 2$ A^2. However, the computation time reduces exponentially (the computation time is on a semi-log plot) with an increase in the value of $K_{\rm exit}$. For all modeling results shown in this article, the value of the norm $K_{\rm exit}$ is chosen as 1 A^2, which offers a good trade-off between computation time and accuracy.

V. Optimal Modulation and Experimental Verification

A key motivation for developing the proposed modeling approach is to find accurate optimal modulation trajectories for the operation of the DAB ac–dc converter. Using the analytical formulations from Section III, a numerical constrained optimization routine is developed to minimize the conduction losses at rated power in the transformer and switches, as shown in (29). Since the designed DAB converter has conduction losses as the most dominant loss mechanism, this is a suitable choice for the objective function. However, a more complex objective function can be designed that considers weighted losses at other power levels, other loss mechanisms, and/or differential-mode EMI considerations.

$$F\ (x) = \ i^2_{Lp,\rm rms} R_{p,\rm tot} + i^2_{Ls,\rm rms} R_{s,\rm tot}. \tag{29}$$

The complete process for finding the optimal modulation trajectory, including the description of the proposed modeling approach is shown in Fig. 13. For the nominal power of 1 kW, the optimal-conduction-loss modulation trajectories are shown in Fig. 14, computed using the conventional and proposed modeling approaches, respectively. To meet the power equality constraint (7) after accounting for all nonidealities, the modulation trajectory shape from the proposed approach is nonsmooth. The modulation trajectories are implemented on a TMS320F-28379D DSP microcontroller using 2-D look-up tables (LUTs) with bilinear interpolation. As the trajectories are generated offline, the implementation is fast and efficient, with a total execution time of 2.92 μs and total memory usage of 7.2 kB for storing the LUTs. To best demonstrate the operational differences between conventional and proposed modeling approaches, an open-loop implementation has been deployed.

To test the accuracy of the conventional and proposed modeling methods, the respective modulation trajectories (Fig. 14) are tested on a single-phase DAB ac–dc converter prototype, with key specifications as mentioned in Table IV. The prototype utilizes GaN Systems GS66516T switches on the primary side and EPC2020 switches on the secondary side. The steady-state operation results at the nominal 230–28 V operating point at 1 kW power are shown in Fig. 15(a) and (b), using the modulation trajectories derived from the proposed and conventional modeling methods, respectively. As the assumptions of the respective modeling approaches are built into the derived optimal modulation trajectories, this test case provides an example of the real-world implications of modeling inaccuracies in the conventional approach. The input current THDs for the proposed and conventional modeling-derived trajectories are 4.5% and 8.9%, respectively. Crucially, the modulation trajectory using conventional modeling has a 7.4% error for the average power transferred (different from NRMSE), whereas the error is 0.3% for the trajectory derived using the proposed modeling approach. While some of these limitations are addressable with closed-loop control, the optimal point operation may not be achieved. Thus,

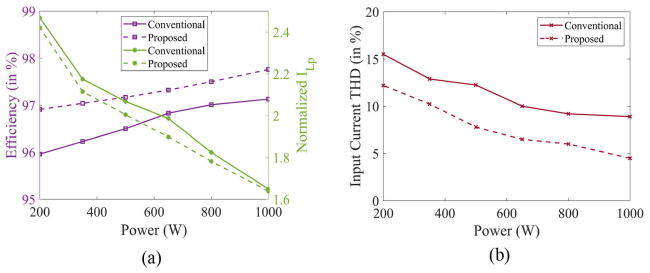


Fig. 17. Evaluation of trajectories generated using conventional/proposed modeling approaches. (a) Efficiency and transformer primary rms currents. (b) Input current THD. Transformer currents are normalized to the corresponding input currents at each power level.

by fundamentally improving the accuracy of the steady-state operating point, the proposed modeling approach seeks to substantially reduce the required controller effort.

In Fig. 16, the accuracy of modeling is compared through a time-domain comparison of the transformer voltages and currents, which are plotted for two distinct switching cycles with differing degrees of soft- and hard-switching transitions. Additionally, the impact of the switch transition modeling is also visible from the zoomed-in switching voltage waveforms. While there are significant discrepancies in the currents and voltages predicted by conventional modeling, the proposed modeling approach and the high-fidelity simulation model show excellent agreement with the experimental results. An interesting aspect to note is that by virtue of ac–dc operation, the DAB ac–dc converter is inherently a wide-voltage-range and wide-load-range converter. This is seen from Fig. 16, where one of the switching periods shows the operation in buck mode, whereas the other switching period shows the operation in boost mode. Thus, these results also verify the effectiveness of the modeling method for a very wide range of voltage conversion ratios and power levels. It should also be noted that parasitic inductances (and corresponding overshoots/oscillations) comprise higher order effects with little impact on large-signal operation, and hence are not considered in this model. The small impact of ringing oscillations can be clearly seen from the zoomed-in waveforms in Fig. 16. Comparing the extracted experimental data to predictions from the proposed modeling approach yields current and power NRMSEs of 11.2% and 2.7%, respectively, which are close to the predicted NRMSEs in Section IV-A (7.6% and 1.7%, respectively). These are substantially lower than the current and power NRMSEs of 34.2% and 18.6%, respectively, for conventional modeling.

Fig. 17(a) and (b) shows the comparison of converter efficiency and input current THD, respectively, when operated with modulation trajectories generated using the proposed and conventional methods. It should be noted that high THD at low load is typical in converters with line-frequency bridges, due to the leading power factor and interactions with the EMI filter. Furthermore, the converter prototype is compliant with the harmonics requirements specified in the DO-160 standard for all power levels. With conduction losses as the most dominant loss mechanism (accounting for over 70% of the total loss budget), a decrease in normalized transformer rms currents results in higher efficiency. Thus, with a better tracking of the optimal operating point and lower distortions in switching-cycle-average power, the trajectories generated using the proposed modeling method also provide a direct advantage of higher efficiency and lower input current THD. However, it must be noted that maximizing converter efficiency is a much more involved topic and is not the focus of this article. In fact, a potential future application of the proposed modeling method involves the integration of accurate loss models (switching, conduction, and core losses) and advanced modulation techniques (variable switching frequency and variable dead-time) with this proposed modeling method to perform a highly accurate efficiency optimization of the DAB ac–dc converter.

VI. Conclusion

This article discusses the key modeling gaps for DAB ac–dc converters and proposes a unified, systematic approach to address the various nonidealities that exist in actual circuit operation. The modeling gaps are categorized as arising from two fundamental assumptions—steady-state operation in each switching cycle and the absence of circuit parasitics considerations. The proposed modeling approach is formulated using a hybrid frequency- and time-domain analysis, which captures the transient effects inherent to ac–dc operation. The proposed modeling approach is generic in nature and can be applied to any modulation strategy. For the nominal converter parameters used in this article, the proposed approach reduces modeling errors by over 15%, as defined by the NRMSE metrics. The improvement in modeling accuracy is demonstrated by converter operation closer to the desired operating points—resulting in lower losses, lower THD, and accurate prediction of soft-/hard- switching, as verified from the experimental results. The proposed modeling is compatible with existing nonlinear optimization routines, which can be used to develop accurate modulation trajectories for a wide range of objective functions. Additionally, the proposed modeling approach can be directly used for parametric design optimizations for the DAB ac–dc converter.

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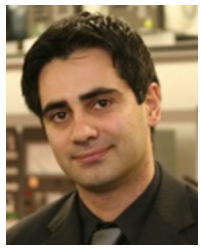

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