Single-Phase Three-Level PWM Rectifier Predictive Control With Fixed Switching Frequency Based on Current Convex Optimization

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***Abstract*—This article proposes a fixed switching frequency predictive control method for neutral point clamped (NPC) single-phase PWM rectifier to achieve global optimization of the current during the entire switching cycle. Through the optimization of the switching sequence, a three-stage switching sequence that can control the midpoint potential balance is obtained. The extreme point, the initial point, and the end point of the current error within the switching period are employed to establish an error matrix, and the error matrix ℓ_2-norm minimality is considered as the optimization objective. This optimization problem is a convex optimization problem, and the optimal duty cycle of the switching sequence can be obtained by solving the convex problem. The optimal duty cycle of each feasible switching sequence is obtained, and then the switching sequence that minimizes the error matrix ℓ_2-norm is selected as the system output among all feasible switching sequences. Finally, the experimental results show that the proposed control scheme has good performance.**

***Index Terms*—Convex optimization, model predictive control (MPC), single-phase PWM rectifier.**

I. Introduction

SINGLE-PHASE three-level PWM rectifiers are widely used as key equipment in high-power fields such as rail transit [1]. They enable bidirectional flow of electrical energy, maintaining high power factor and low total harmonic distortion (THD) of the grid side current [2],[3]. For the control of single-phase PWM rectifiers, current control schemes such as *dq*-axis current control [3] and direct power control (DPC) [4] based on proportional integral (PI) controllers are widely used in rail transit. In recent years, due to the rapid development of digital signal processors, control algorithms with complicated calculation, such as model predictive control [5], can be implemented, though the computational burden is often higher than the strategies based on PI controllers. For conventional model predictive control, the input is continuous, and the control target is the output error minimization problem in a limited time range. [6]–[8]. However, in the field of power electronics, the reference voltage needs to obtain the drive signal of the power electronic switches through the modulator [9]. In [10], a finite control set model predictive control (FCS-MPC) scheme is proposed. By using each feasible switching state, the tracking errors are predicted according to the predictive model of the system, and the switching state minimizing the cost function is selected as the optimal input of the FCS-MPC. FCS-MPC has the abilities of fast dynamic response, multiobjective optimization control with constraints, and nonlinear control, but there are still some common problems. As an example, it is not conducive to design the power supply filters owing to the switching frequency of FCS-MPC is not fixed [11].

Several predictive control methods for maintaining a fixed switching frequency or a switching frequency fluctuating within a small range have been proposed in [12]–[25]. For example, the modulator is obtained by using a low-pass filter on the basis of the FCS-MPC algorithm in [12]. In [13], the current error signal in the cost function is digitally filtered, and the current error is passed through a band-stop filter so that a specific frequency current error is allowed to exist, thereby obtaining a desired current spectrum characteristic. However, the use of filters adversely affects the dynamic performance of the FCS-MPC system. In [14], the deadbeat predictive control method is used to calculate the modulated voltage reference value, and then the driving signal of the power electronic switches is generated by the modulation portion. In the deadbeat predictive control, the modulation part adopts the principle of volt-second balance, and its error is large at low switching frequency [15]. The works in [16]–[18] studied modulated model predictive control (M^2PC) to achieve a fixed switching frequency to improve the steady-state performance, but it is difficult to achieve multiobjective optimization. The works in [19] proposed an improved modulated model predictive control (M^3PC), which can achieve multiobjective optimization. However, the M^2PC and M^3PC are approximate optimization of the current error at high switching frequency, which will lead to degraded performance at low switching frequency. The authors in [20]–[22] use the virtual space vector to fix the switching

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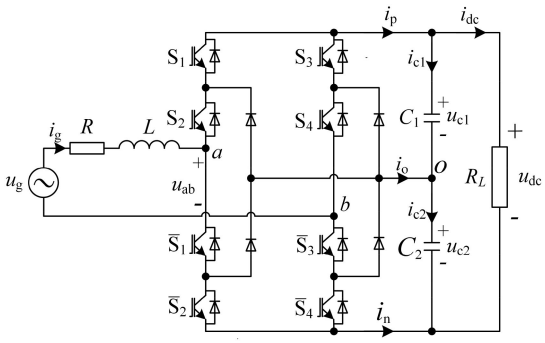

Fig. 1. Single-phase three-level NPC converter.

frequency to improve the steady-state performance, but increase the switching frequency. The works in [23] first proposed the optimal switching sequence, focusing on the current behavior during the switching cycle. It aims at minimizing the current error after the end of a fixed switching cycle, calculates the action time of each voltage vector, and reduces the effect of discrete errors on current tracking. The works in [24] applied the optimal switching sequence method to neutral point clamped (NPC) single-phase three-level converter. The authors in [25] implemented midpoint voltage balance control on the basis of [24]. Although a weighting factor is introduced, the weighting factor does not affect the steady-state performance of the system. It is worth noting that although the optimal switching sequence method predicts the current behavior within a switching cycle, it only focuses on the current error at the end of a fixed switching cycle, and does not restrict the current behavior of the current during the switching process during the fixed switching cycle. The evaluation of current control target has certain limitations.

In this article, NPC single-phase three-level PWM rectifier is taken as the research object, a three-stage switching sequence with only twice ON–OFF state switches in one switching cycle is studied, and the selection of redundant switching state is used to control the midpoint potential balance. The FCS-MPC is used to calculate the extreme points and end points of the current error, and the current error matrix is composed of the initial point, the extreme point, and the end point of the current error to evaluate the dynamic behavior of the current in one switching cycle. The current error matrix ℓ_2-norm is taken as the current quality evaluation standard, which can obtain a better current quality than the current error ℓ_1-norm minimality standard [26]. Simulation and experimental results show the correctness and superiority of the proposed algorithm.

II. Single-Phase NPC Three-Level Converter

The single-phase NPC three-level converter topology is shown in Fig. 1. The converter consists of two bridge arms, each with four switching devices and two diodes. Each bridge arm has three switch states $S_k \in \{-10, 1\}$, $k \in \{\mathrm{A}, \mathrm{B}\}$. Assuming each capacitor voltage is half the dc bus voltage, these three switch states represent the three bridge arm phase voltages $u_{xo} \in \{-u_{\mathrm{dc}}/20, u_{\mathrm{dc}}/2\}$, where $x \in \{a, b\}$.

TABLE I
Switching State

S_1	S_2	S_3	S_4	S_A	S_B	u_{ab}	states
1	1	0	0		-1	u_{dc}	V_1
1	1	0	1	1	0	$u_{dc}/2$	V_2
0	1	0	0	0	-1	$u_{dc}/2$	V_3
0	1	0	1	0	0	0	V_4
1	1	1	1	1	1	0	V_5
0	0	0	0	-1	-1	0	V_6
0	1	1	1	0	1	$-u_{dc}/2$	V_7
0	0	0	1	-1	0	$-u_{dc}/2$	V_8
0	0	1	1	-1	1	$-u_{dc}$	V_9

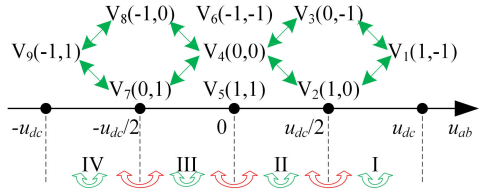

Fig. 2. Voltage regions and switch state switching rules.

Considering that the effective switching state of the single-phase NPC three-level converter is generated by two bridge arms, the entire converter generates 9 (3^2) switching states. Table I summarizes the switching state correspondence of single-phase NPC three-level converters. According to the value of the voltage u_{ab}, it is divided into four regions of I, II, III, and IV, as shown in Fig. 2, where each region has at least two effective switching states $\{V_{1j}, V_{2j}\}$, $j \in \{\mathrm{I,II,III,IV}\}$.

A three-segment symmetric switching sequence that considers only two valid states in each switching cycle is defined as

$$\mathbf{V}_j = \{\underbrace{V_{1j}}_{\frac{d_{1j}}{2}}, \underbrace{V_{2j}}_{d_{2j}}, \underbrace{V_{1j}}_{\frac{d_{1j}}{2}}\} \tag{1}$$

where d_{ij} is the duty ratio corresponding to the ith switching state V_{ij} in the j-region, $i \in \{1, 2\}$.

III. Establishment and Solution of Convex Function Model With Optimal Duty Cycle

In the standard FCS-MPC, the tracking error generated when each switching state of the system acts on the entire switching cycle is predicted according to the system model, and the switch state that minimizes the error is selected. The control strategy proposed in this article introduces another modulation stage in the standard FCS-MPC. Since the switching period Tc is relatively small, when using the standard FCS-MPC control, the variation of the controlled variable in one switching period can be approximated as linear. In the j-region, the increment of the grid-current i_g after the ith switch state functioning an entire switching cycle is defined as

$$\Delta y_{ij} = i_{gij}^{k+1} - i_g^k \tag{2}$$

where i_{gij}^{k+1} denotes the predicted value of the grid-current i_g at the time $k+1$ applying the ith switch state for an entire switching cycle in the j-region.

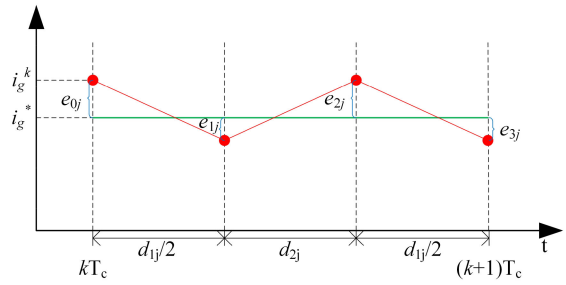

Fig. 3. Diagram of controlled variable when switching state is switched.

Considering the tracking effect of the controlled variable throughout the switching period, the switching position is the extreme point of the tracking error, and the current error ℓ_2-norm minimization has a better control performance than the ℓ_1-norm minimization [25]. In this article, the tracking error ℓ_2-norm minimization at the switching position throughout the switching period is taken as the control target.

The tracking error matrix $\boldsymbol{E}_j$ under the control of j-region switch state is defined as

$$\mathbf{E}_j = \left[e_{0j}\ e_{1j}\ e_{2j}\ e_{3j} \right]. \tag{3}$$

Then, the tracking error ℓ_2-norm ERR_j under the control of j-region switch state is expressed as

$$\mathrm{ERR}_j = \|\mathbf{E}_j\|_2 = \sum_{k=0}^{3} e_{kj}^2. \tag{4}$$

When the switching sequence of (1) acts on the controlled system, the curve of the controlled variable i_g from time k to time $k+1$ is as shown in Fig. 3, where e_{0j}, e_{1j}, e_{2j}, and e_{3j} are the errors between the controlled variable and the reference value i^*g at each switch state switching moment after determining the selected switch state in the j-region, respectively, which can be expressed as

$$\begin{cases} e_{0j} = i_g^k - i_g^* \\ e_{1j} = e_{0j} + \Delta y_{1j} \frac{d_{1j}}{2} \\ e_{2j} = e_{1j} + \Delta y_{2j} d_{2j} = e_{0j} + \Delta y_{1j} \frac{d_{1j}}{2} + \Delta y_{2j} d_{2j} \\ e_{3j} = e_{2j} + \Delta y_{1j} \frac{d_{1j}}{2} = e_{0j} + \Delta y_{1j} d_{1j} + \Delta y_{2j} d_{2j}. \end{cases} \tag{5}$$

Bring (5) into (4)

$$\begin{aligned} \mathrm{ERR}_j = 1/2(&3\Delta y_{1j}^2 d_{1j}^2 + 4\Delta y_{2j}^2 d_{2j}^2 + 8e_{0j}\Delta y_{1j} d_{1j} \\ &+ 8e_{0j}\Delta y_{2j} d_{2j} + 3\Delta y_{1j}\Delta y_{2j} d_{1j} d_{2j} + 8e_{0j}^2). \end{aligned} \tag{6}$$

Define $G_j = 3\Delta y_{1j}^2 d_{1j}^2 + 4\Delta y_{2j}^2 d_{2j}^2 + 8e_{0j}\,\Delta y_{1j} d_{1j} + 8e_{0j}\,\Delta y_{2j} d_{2j} + 3\Delta y_{1j}\Delta y_{2j}\ \times d_{1j} d_{2j} + 8e_{0j}^2$, $\boldsymbol{x}T\,j\ =\ [d_{1j},\ d_{2j}]$, $\boldsymbol{q}T\,j = 8e_{0j}[\Delta y_{1j},\ \Delta y_{2j}]$, $r_j = 8e_{0j}^2$,

$$\mathbf{P} = \begin{bmatrix} 6\Delta y_{1j}^2 & 3\Delta y_{1j}\Delta y_{2j} \\ 3\Delta y_{1j}\Delta y_{2j} & 8\Delta y_{2j}^2 \end{bmatrix}.$$

Then, under the control of j-region switch state, the tracking error ℓ_2-norm ERR_j minimization problem is equivalently described as

$$\begin{aligned} \text{minimize} \quad & G_j(\mathbf{x}_j) = \frac{1}{2}\mathbf{x}_j^T \mathbf{P} \mathbf{x}_j + \mathbf{q}_j^T \mathbf{x}_j + r_j \\ \text{subject to} \quad & 0 \preceq \mathbf{x}_j \preceq 1 \\ & \mathbf{1}^T \mathbf{x}_j = 1. \end{aligned} \tag{7}$$

In the optimization problem (7), the matrix $\boldsymbol{P}$ is obviously a real symmetric matrix, $\boldsymbol{1}$ denotes the vector with all entries one, and then the each-order sequential principal minor determinant of the matrix $\boldsymbol{P}$ is verified as $P_1 = |6\Delta y_{1j}^2| = 6\Delta y_{1j}^2 \geq 0$, $P_2 = |\boldsymbol{P}| = 39\Delta y_{1j}^2 \Delta y_{2j}^2 \geq 0$.

The each-order sequential principal minor of the matrix $\boldsymbol{P}$ is greater than or equal to zero; then the matrix $\boldsymbol{P}$ is a semipositive definite matrix, and the constrained function is affine obviously, so the optimization problem (7) is a convex quadratic programming problem [27]. In the quadratic programming problem, we minimize a convex quadratic function over a polyhedron, which is written in standard form as

$$\text{minimize } G_j(\mathbf{x}_j) = \frac{1}{2}\mathbf{x}_j^T \mathbf{P} \mathbf{x}_j + \mathbf{q}^T \mathbf{x}_j + r_j \tag{8-a}$$

$$\text{subject to } f_1(\mathbf{x}_j) = \left[-1\ 0 \right] \mathbf{x}_j \leq 0 \tag{8-b}$$

$$f_2(\mathbf{x}_j) = \left[0\ -1 \right] \mathbf{x}_j \leq 0 \tag{8-c}$$

$$f_3(\mathbf{x}_j) = \left[1\ 0 \right] \mathbf{x}_j - 1 \leq 0 \tag{8-d}$$

$$f_4(\mathbf{x}_j) = \left[0\ 1 \right] \mathbf{x}_j - 1 \leq 0 \tag{8-e}$$

$$h(\mathbf{x}_j) = \left[1\ 1 \right] \mathbf{x}_j - 1 = 0. \tag{8-f}$$

The optimal solution to problem (7) satisfies the Karush–Kuhn–Tucker (KKT) conditions. Let $\boldsymbol{x}_j^*$, $\boldsymbol{\lambda}_j^*$, and μ_j^* be any points that satisfy the KKT condition, and then

$$f_i(\mathbf{x}_j^*) \leq 0, i \in \{1,2,3,4\} \tag{9-a}$$

$$h(\mathbf{x}_j^*) = 0 \tag{9-b}$$

$$\lambda_{ij}^* \geq 0, i \in \{1,2,3,4\} \tag{9-c}$$

$$\lambda_{ij}^* f_i(\mathbf{x}_j^*) = 0, i \in \{1,2,3,4\} \tag{9-d}$$

$$\nabla G_j(\mathbf{x}_j^*) + \sum_{i=1}^{4} \lambda_{ij}^* \nabla f_i(\mathbf{x}_j^*) + \mu_j^* \nabla h(\mathbf{x}_j^*) = 0. \tag{9-e}$$

When the primal problem is convex problem, points satisfying the KKT conditions are also optimal solutions of primal and dual problems. In other words, if f_i is convex and h are affine, then $\boldsymbol{x}_j^*$, $\boldsymbol{\lambda}_j^*$, μ_j^* are any points that satisfy the KKT conditions. In that way, $\boldsymbol{x}_j^*$ and $(\boldsymbol{\lambda}_j^*,\ \mu_j^*)$ are respectively the optimal solution of the primal problem and Lagrange dual problem of (8), with zero duality gap [27].

Next, it is divided into the following two cases.

1) When $\boldsymbol{x}_j{}^*$ does satisfy the inequality constraint $0 \prec \boldsymbol{x}_j^* \prec 1$, that is

$$f_i(\mathbf{x}_j^*) < 0, i \in \{1,2,3,4\}. \tag{10-a}$$

From (9-d) and (10-a), we can get

$$\lambda_{ij}^* = 0, i \in \{1,2,3,4\}. \tag{10-b}$$

At this time, (9-a)–(9-d) are all established; (9-b) and (9-d) can be written as

$$\begin{cases} \mathbf{1}^T\mathbf{x}_j^* = 1 \\ \mathbf{P}\mathbf{x}_j^* + \mathbf{q}_j + \mathbf{1}^T\mu_j^* = 0 \end{cases} \tag{10-c}$$

which equals

$$\begin{bmatrix} \mathbf{P} & \mathbf{1}^T \\ \mathbf{1} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}_j^* \\ \mu_j^* \end{bmatrix} = \begin{bmatrix} -\mathbf{q}_j \\ 1 \end{bmatrix}. \tag{10-d}$$

Bringing the matrix parameters into (10-d) can obtain the analytical expression of the problem

$$\mathbf{x}_j^* = \begin{bmatrix} d_{1j}^* & d_{2j}^* \end{bmatrix}^T \tag{11}$$

where $d*1j = (8\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j} + 8e_{0j}\Delta y_{2j})/(3\Delta y_{1j}^2 + 4\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j})$, $d*2j = (3\Delta y_{1j}^2 - 4\Delta y_{2j}^2 - 8e_{0j}\Delta y_{2j})/(3\Delta y_{1j}^2 + 4\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j})$.

2) When $\boldsymbol{x}_j{}^*$ does not satisfy the inequality constraint $0 \prec \boldsymbol{x}_j^* \prec 1$, that is

$$\exists i \in \{1,2,3,4\}, f_i\left(\mathbf{x}_j^*\right) \geq 0. \tag{12-a}$$

From (9-a) (9-b) and (12-a), we can get

$$f_i\left(\mathbf{x}_j^*\right) = 0, i \in \{1,2,3,4\}. \tag{12-b}$$

According to (9-b) and (12-b)

$$\mathbf{x}_j^* \in \left\{ \begin{bmatrix} 0 & 1 \end{bmatrix}^T, \begin{bmatrix} 1 & 0 \end{bmatrix}^T \right\} \tag{12-c}$$

which is

$$\mathbf{x}_j^* = \begin{cases} \begin{bmatrix} 0 & 1 \end{bmatrix}^T, G_j\left(\begin{bmatrix} 0 & 1 \end{bmatrix}^T\right) < G_j\left(\begin{bmatrix} 1 & 0 \end{bmatrix}^T\right) \\ \begin{bmatrix} 1 & 0 \end{bmatrix}^T, \text{else}. \end{cases} \tag{12-d}$$

From the definition of G_j and the equation constraint (9-b), we can see

$$\mathbf{x}_j^* = \begin{cases} \begin{bmatrix} 0 & 1 \end{bmatrix}^T, d_{1j}^* \leq 0 \\ \begin{bmatrix} 1 & 0 \end{bmatrix}^T, d_{1j}^* \geq 1. \end{cases} \tag{13}$$

Then, according to (11) and (13), the analytical expression of the convex optimization problem (7) can be expressedas follows:

$$\mathbf{x}_j^* = \begin{cases} \begin{bmatrix} 0 & 1 \end{bmatrix}^T, d_{1j}^* \leq 0 \\ \begin{bmatrix} d_{1j}^* & d_{2j}^* \end{bmatrix}, 0 < d_{1j}^* < 1 \\ \begin{bmatrix} 1 & 0 \end{bmatrix}^T, d_{1j}^* \geq 1 \end{cases} \tag{14}$$

where $d_{1j}^* = (8\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j} + 8e_{0j}\Delta y_{2j})/(3\Delta y_{1j}^2 + 4\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j})$, $d_{2j}^* = (3\Delta y_{1j}^2 - 4\Delta y_{2j}^2 - 8e_{0j}\Delta y_{2j})/(3\Delta y_{1j}^2 + 4\Delta y_{2j}^2 - 3\Delta y_{1j}\Delta y_{2j})$.

IV. Selection of Switching Sequence

A. Judge the Feasible Region

For the single-phase three-level PWM rectifier NPC topology studied in this article, the bridge arm phase voltage (u_{ao}, u_{bo}) and the voltage between the two bridges (u_{ab}) when every time the system switches cannot generate voltage jumps exceeding $u_{\mathrm{dc}}/2$. The former is unfavorable to the rectifier circuit, causing damage to the switching device, and the latter is unfavorable to the power grid and causes excessive impact on the grid.

TABLE II
Effect of Switching State on Midpoint Potential.

states		V_2	V_3	V_7	V_8
u_o	i_g>0	↘	↗	↗	↘
	i_g<0	↗	↘	↘	↗

Therefore, the region switching rule does not allow compartment switching. The region division is as shown in Fig. 2. As an example, if the region of the *k*-1th switching period is **I**, that is, $j^{k\text{-}1} = \mathbf{I}$, then at the time k, the region can only select one of **I**, **II**, that is, $j^k \in \{\mathbf{I}, \mathbf{II}\}$.

B. Select Switch States

The circuit topology is shown in Fig. 1, where the continuous domain dynamic dc side capacitor voltage is

$$\begin{cases} \frac{du_{C1}}{dt} = \frac{1}{C}i_{C1} = \frac{1}{C}(i_p - i_{\mathrm{dc}}) \\ \frac{du_{C2}}{dt} = \frac{1}{C}i_{C2} = \frac{1}{C}(-i_n - i_{\mathrm{dc}}) \end{cases} \tag{15}$$

where u_{C1} and u_{C2} are the upper and lower busbar capacitor voltages, respectively, i_{C1} and i_{C2} are the capacitor currents in the system, *C* is the upper and lower busbar capacitance value, i_p and i_n are the internal currents of the NPC rectifier, and i_{dc} is the dc-side current. When the switching period T_c is small, i_{p}, i_n, and i_{dc} can be considered to remain unchanged. According to formula (15), the dc upper and lower bus capacitor voltage values (*uk*+1 *C*1 and *uk*+1 *C*2) at time *k*+1 can be calculated as

$$\begin{cases} u_{C1}^{k+1} = u_{C1}^k + \frac{1}{C}\int_{kT_c}^{(k+1)T_c}\left(i_p^k - i_{dc}^k\right)dt \\ u_{C2}^{k+1} = u_{C2}^k - \frac{1}{C}\int_{kT_c}^{(k+1)T_c}\left(i_n^k + i_{dc}^k\right)dt. \end{cases} \tag{16}$$

In order to avoid the measurement of i_p and i_n, it is convenient to define the direct relationship between the switching state of the NPC rectifier and the current i_g

$$\begin{cases} i_p^k = \frac{\mathrm{S_A}(\mathrm{S_A}+1) - \mathrm{S_B}(\mathrm{S_B}+1)}{2} i_g^k \\ i_n^k = \frac{\mathrm{S_A}(\mathrm{S_A}-1) - \mathrm{S_B}(\mathrm{S_B}-1)}{2} i_g^k. \end{cases} \tag{17}$$

Therefore, the dc side midpoint voltage u_{o} can be expressed as

$$u_o^{k+1} = u_{C1}^{k+1} - u_{C2}^{k+1} = u_o^k + \frac{1}{C}\int_{kT_c}^{(k+1)T_c}\left(i_p^k + i_n^k\right)dt. \tag{18}$$

Analysis of (17) and (18), Table I shows that the change in the midpoint potential u_o occurs only when the u_{ab} voltage is $\pm u_{\mathrm{dc}}/2$. The analysis and summary of the working state and the qualitative analysis results of the grid side current to the midpoint potential are shown in Table II, where "↘" means that the midpoint potential drops, and "↗" means that the midpoint potential rises.

After determining the region, the switch state combination is selected according to the midpoint potential u_{o} and the grid side current i_g. As an example, when the first region is selected, if $u_{\mathrm{o}} \times i_g <= 0$, then V_3 and V_7 are selected, if $u_o \times i_g > 0$, then V_2 and V_8 are selected.

C. Determination of the Sequence of Switches Within the Feasible Region

For the single-phase three-level NPC topology, not all of the nine switch states can be switched directly during each switching action, which needs to be properly constrained. The specific switching law of switch state is shown in Fig. 2. In order to keep the same region switching (whether the selected switch states are consistent or not), the head-to-tail switch state (V_{1j}) are the same. If $j^k = j^{k-1} = \mathrm{I}$, the head-to-tail switch state is $V_{11} = V_1$; if $j^k = j^{k-1} = \mathrm{II}$, the state of the head-to-tail switches is $V_{12} = V_4$; if $j^k = j^{k-1} = \mathrm{III}$, the state of the head-to-tail switches is $V_{13} = V_4$; if $j^k = j^{k-1} = \mathrm{IV}$, the state of the head-to-tail switches is $V_{14} = V_9$;

In the switching of different region switching states, in order to reduce the number of switching device operations as much as possible, the switching sequence is determined according to the current direction of the grid side and the direction of the midpoint potential.

For example, when $j^k = \mathrm{I}$, $j^{k-1} = \mathrm{II}$, if $u_o \times i_g <= 0$, then $V_{11} = V_2$; if $u_o \times i_g > 0$, then $V_{11} = V_3$. All switch sequence rules are as shown in Fig. 4.

D. Determination of the Optimal Switching Sequence

1) Judge the feasible region at time k according to IV-A

$$j^k \in \begin{cases} \{\mathrm{I}, \mathrm{II}\}, j^{k-1} = \mathrm{I} \\ \{\mathrm{I}, \mathrm{II}, \mathrm{III}\}, j^{k-1} = \mathrm{II} \\ \{\mathrm{II}, \mathrm{III}, \mathrm{IV}\}, j^{k-1} = \mathrm{III} \\ \{\mathrm{III}, \mathrm{IV}\}, j^{k-1} = \mathrm{IV}. \end{cases} \tag{19}$$

2) For each feasible region, switch states V_{1j} and V_{2j} are selected according to IV-B.
3) For each feasible *j*-region and based on the selected switching state, the switching sequence is determined according to IV-C.
4) Calculate the increments Δy_{1j} and Δy_{2j} of the controlled variable if each switch state in 2) operates the entire switching cycle T_c.

In circuit topology Fig. 1, the continuous domain dynamic grid side current i_g expression is

$$\frac{di_{\mathrm{g}}}{dt} = \frac{1}{L}(u_{\mathrm{g}} - Ri_{\mathrm{g}} - u_{\mathrm{ab}}) \tag{20}$$

where u_g represents the grid side voltage, u_{ab} represents the voltage between the two bridge arms a and b, L is the grid-side filter inductor, and R is the parasitic resistance on the filter inductor.

Equation (20) can be converted to a discrete time domain by the classical forward Euler method to ensure that the controller can predict the grid side current value at time $k+1$ and calculate the increment of the controlled variable

$$\Delta y_{ij} = i_{gij}^{k+1} - i_g^k = -\frac{T_s R}{L} i_g^k + \frac{T_c}{L}(u_g^k - u_{abij}) \tag{21}$$

where T_c represents the switching period; according to the rectifier switching state (seen in Table I), it can be concluded that the voltage u_{ab} in the rectifier corresponding to the switching state V_{ij} is u_{abij}.

1) Calculate the corresponding optimal duty ratio $\boldsymbol{x}_j{}^*$ by using the increments Δy_{1j} and Δy_{2j} of controlled variables in each *j*-region obtained in 4). According to the system state $i_g{}^k$ at time *k*, and system given value i_g^*, $e_0^j = i_g^k - i_g^*$ can be calculated. Calculate the optimal duty cycle $\boldsymbol{x}_j{}^*$ of the corresponding switch sequence according to (14).
2) Bring each set of duty cycles in 5) into $G_j(\boldsymbol{x}_j) = 1/2\boldsymbol{x}_j^T \boldsymbol{P}\boldsymbol{x}j + \boldsymbol{q}_j^T \boldsymbol{x}_j + r_j$ to find the G_j corresponding to the feasible *j*-region, compare the G_j value of different *j*-regions, select the sequence corresponding to the *j*-region that minimizes the G_j value, and optimal duty cycle $\boldsymbol{x}_j{}^*$ to output and act on the converter.

V. Calculation of the Reference Current

In Fig. 5 , ω_0 stands for the angular frequency of grid voltage, u_{g} is the single-phase input signal, the proportional gain k is the constant, which has influence on system bandwidth, and u_α and u_β are the two orthogonal signals generated by second-order generalized integrator (SOGI).

Therefore, the transfer functions between u_α and u_{g} and u_β and u_{g} are shown as follows:

$$H_\alpha = \frac{u_\alpha}{u_g} = \frac{k\omega_0 s}{s^2 + k\omega_0 s + \omega_0^2} \tag{22}$$

$$H_\beta = \frac{u_\beta}{u_g} = \frac{k\omega_0^2}{s^2 + k\omega_0 s + \omega_0^2} \tag{23}$$

Since the proportional gain k is related to the system bandwidth, considering the filtering effect, we set $k = 1$. In Fig. 5, the orthogonal signals generated by SOGI are u_α ($u_\alpha = u_m\cos(\omega_0 t)$), u_β ($u_\beta = u_m\sin(\omega_0 t)$), and ($i_\alpha = i_m\cos(\omega_0 t + \varphi)$), i_β ($i_\beta = i_m\sin(\omega_0 t + \varphi)$) for the case of the input signal is u_g ($u_g = u_m\cos(\omega_0 t)$) and ($i_g = i_m\cos(\omega_0 t + \varphi)$), respectively.

Hence, according to the instantaneous power theory, the instantaneous active power p_g and reactive power q_g are defined as follows:

$$\begin{cases} p_g = \frac{1}{2}(u_d i_d + u_q i_q) \\ q_g = \frac{1}{2}(u_q i_d - u_d i_q) \end{cases} \tag{24}$$

where u_d and u_q, i_d, i_q are *d*-axis and *q*-axis components of voltage and current in the two-phase rotating coordinate system, respectively. It is assumed that the grid-voltage u_m, is fixed to *d*-axis, namely, $u_d = u_m$ and $u_q = 0$. Consequently, the values of active and reactive powers are deduced as in the following equations:

$$p_g = \frac{1}{2} u_d i_d \tag{25}$$

$$q_g = -\frac{1}{2} u_d i_q. \tag{26}$$

The relation of i_g, i_d,and i_q can be expressed as

$$i_g = i_d \cos\theta - i_q \sin\theta. \tag{27}$$

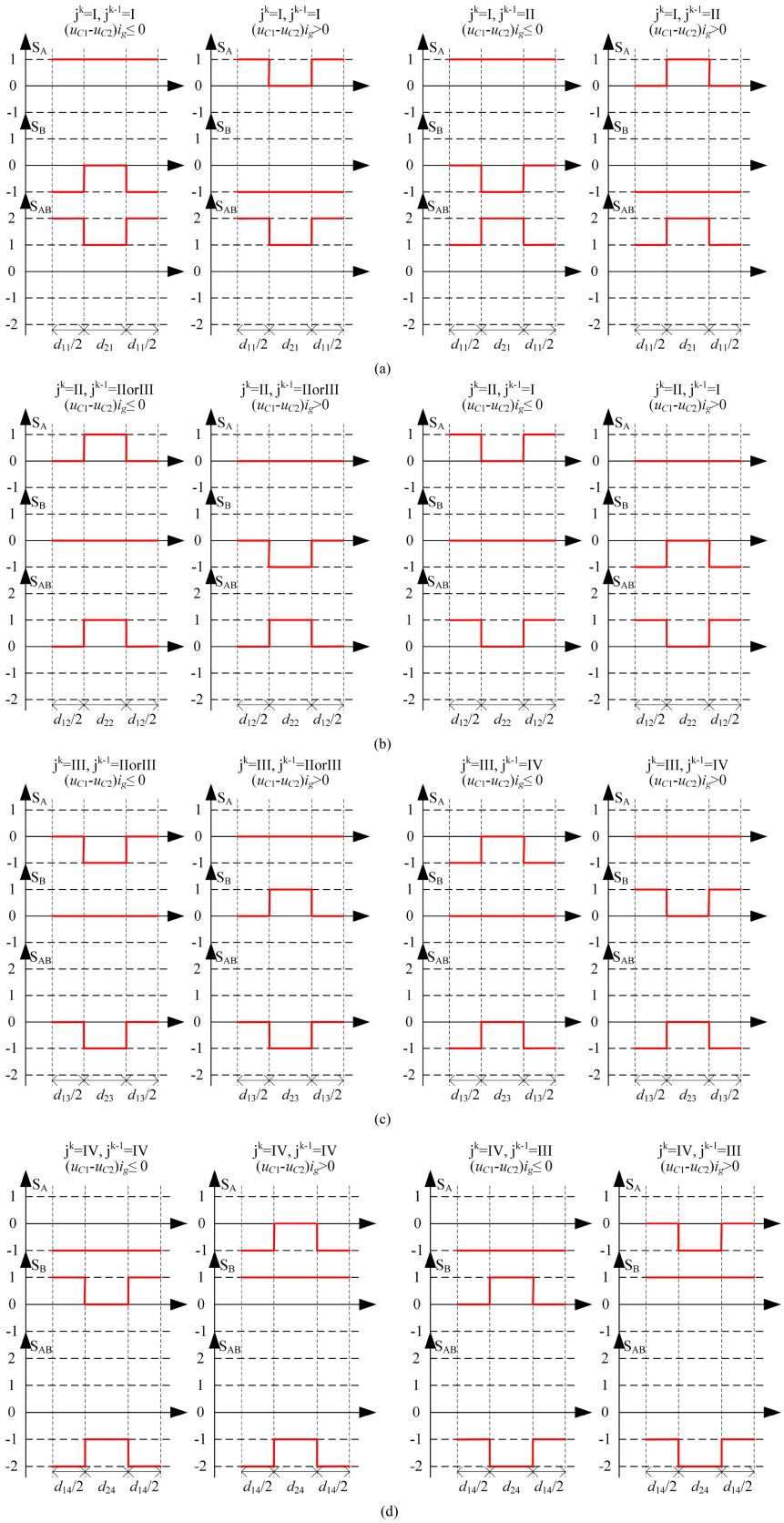

Fig. 4. Switching rules of switch sequence. (a) I region. (b) II region. (c) III region. (d) IV region.

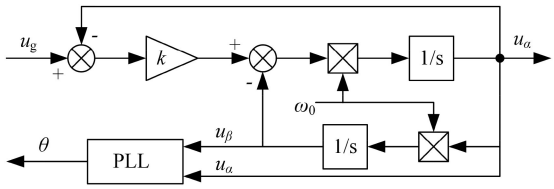

Fig. 5. Second-order generalized integrator schematic.

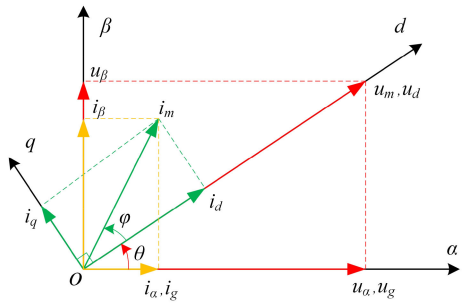

Fig. 6. Vector diagram.

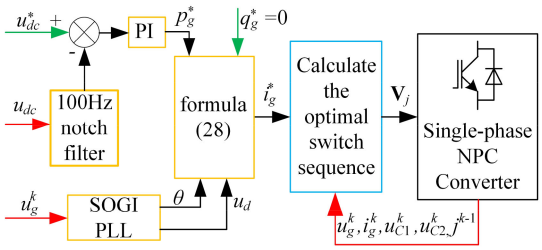

Fig. 7 System control block diagram.

Substituting (25) and (26) into (27), the reference grid-current i_g^* can be expressed as

$$i_g^* = \frac{2p_g^*}{u_d}\cos\theta + \frac{2q_g^*}{u_d}\sin\theta \tag{28}$$

where p_g^* and q_g^* represent the reference values of active power and reactive power, respectively.

Therefore, the active and reactive power injected to or absorbed from the grid can be controlled by regulating the grid-side current.

The system control block diagram of the proposed method is shown in Fig. 7. The active power reference value p_g^* is obtained by the PI controller from the difference between the dc bus voltage reference value $u_{\rm dc}^*$ and the actual value $u_{\rm dc}$. Since the dc bus has twice the grid power frequency (100 Hz), and in order to reduce the power reference value of two times the power frequency signal interference, the dc bus voltage signal is filtered by a 100-Hz notching filter. In order to maintain the grid-side unit power factor, the reactive power reference value q_g^* is set to zero.

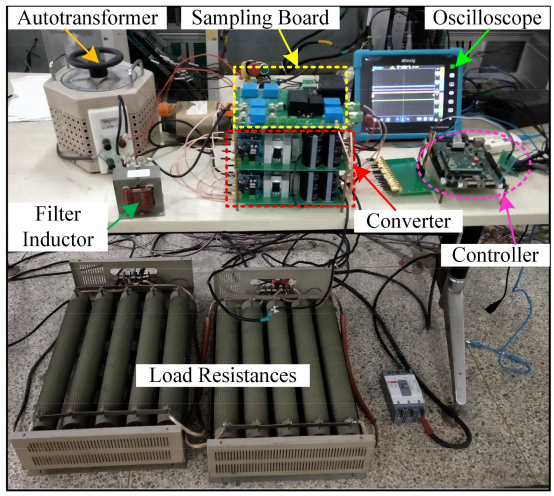

Fig. 8 Experimental platform.

VI. Validation and Analysis of Experimental Results

In order to verify the effectiveness and superiority of the proposed fixed-frequency control method for single-phase three-level PWM rectifier based on convex optimization, an experimental platform of NPC single-phase three-level PWM rectifier with 400 V dc voltage is established as shown in Fig. 8. The effective value of the grid voltage is 230 V, the grid power frequency is 50 Hz, the upper and lower busbar capacitances on the dc side are 2200 μF, the dc load is 25 Ω, the reactive power is zero, the ac side filter inductor is 5 mH, and the parasitic resistance is 0.1 Ω. Then, a 300-MIPS 32-bit TMS320C28346 digital signal processing (DSP) board and FGY75N60SMD IGBT is employed, and programming is realized in CCS6.0 environment.

A. Steady State

The fixed switching frequency predictive control method of single-phase three-level PWM rectifier based on convex optimization proposed in this article is compared with the optimal switching sequence scheme in [25] and three-stage vector modulation employed in deadbeat predictive current control (DBPCC).

To ensure that the three control schemes have a consistent switching frequency, the T_c of OSS-MPC, DBPCC, and proposed-MPC methods are 500 μs. Then, the average switching frequency of the three schemes are 500 Hz. At full load (load resistance is 25 Ω), the steady-state test results of the two schemes are shown in Figs. 9 –11.

The analysis of Figs. 9–11 shows that the switching frequency of the three schemes are close to 500 Hz. Comparing Figs. 9, 10, and 11, it shows that the current THD of proposed-MPC is lower than OSS-MPC under the same switching frequency and DBPCC.

In order to study the influence of different loads on the current THD of the three control schemes, the current THD is counted under the measured of 500 Hz of average switching frequency

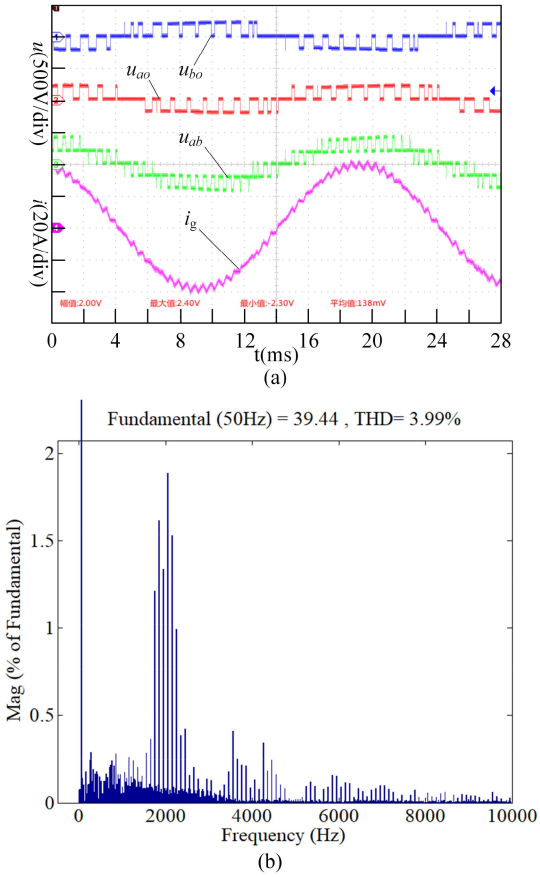

Fig. 9. Experimental results of proposed-MPC. (a) Voltage and current waveforms of the converter. (b) Current spectrum analysis.

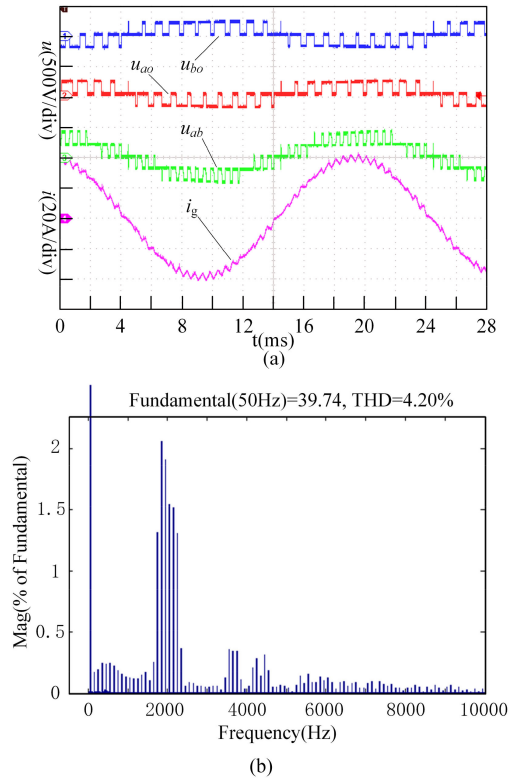

Fig. 10. Experimental results of OSS-MPC. (a) Voltage and current waveforms of the converter. (b) Current spectrum analysis.

and different load conditions. The results are shown in Fig. 12. It can be seen that the current THDs of the three control schemes all decrease as the load increases. The results show that under the same load condition, the current THD of proposed-MPC is lower than that of OSS-MPC and DBPCC, which proves the superiority of the proposed-MPC.

In order to further study the influence of the switching frequency on the current THD of the three control schemes, the current THD analysis was performed at full load on the two control schemes at 250, 500, 625, 833, and 1250 Hz switching frequencies, respectively. As a result, as shown in Fig. 13, it can be seen that the current THDs of the three control schemes all decrease with the increase of the switching frequency. The results show that the current THD of proposed-MPC is lower than that of OSS-MPC and DBPCC at the same switching frequency, which proves the superiority of the proposed-MPC.

B. Dynamic Response

In order to verify the dynamic performance of the proposed-MPC and OSS-MPC, the dynamic response test is conducted. Figs. 14 and 15 show the dynamic experiment of proposed-MPC and OSS-MPC, with half load at 0–40 ms and full load at 40–140 ms.

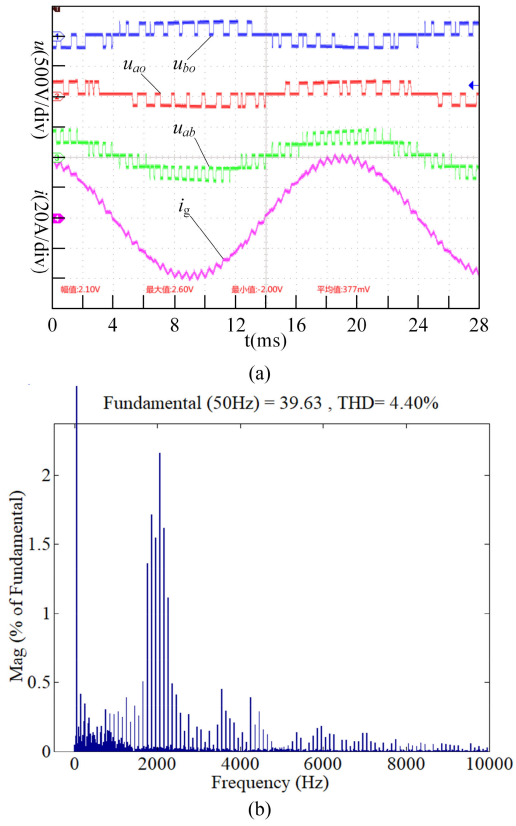

Fig. 11. Experimental results of DBPCC. (a) Voltage and current waveforms of the converter. (b) Current spectrum analysis.

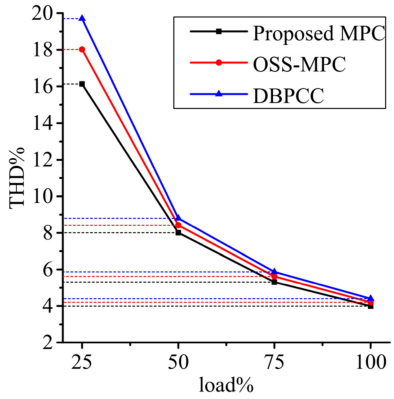

Fig. 12. Current THD curve with respect to load for constant load control methods.

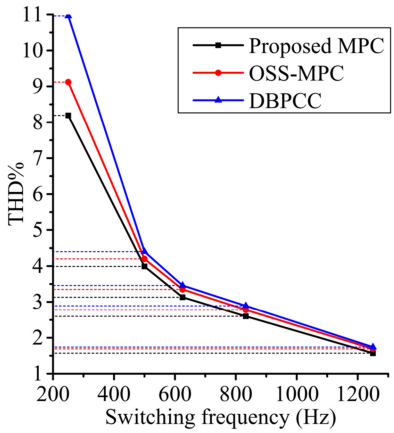

Fig. 13. Current THD curve with respect to switching frequency for constant switching frequency control methods.

Figs. 14(a) and 15(a) show the voltage and current waveforms of the converter, respectively, including the bridge arm phase voltages u_{ao}, u_{bo}, line-to-line voltage u_{ab}, and the grid side current i_g. It can be seen that there is no cross-level voltage jump in the u_{ao}, u_{bo}, u_{ab} when the load is abrupt, which proves the reliability of the proposed-MPC and OSS-MPC.

Figs. 14(b) and 15(b) show the dc-side dynamic response waveform of the system, including the dc bus voltage waveform, the dc side upper and lower bus capacitor voltage waveforms, and the midpoint potential waveform. It can be seen that the dc bus voltage can effectively track the reference value when the load is changed, and the upper and lower bus capacitor voltages and the midpoint potential can be effectively controlled, which proves the effectiveness of proposed-MPC and OSS-MPC for the midpoint potential control. The dynamic performance of the proposed-MPC is basically consistent with OSS-MPC.

C. *Experimental Tests With* C1 ≠ C2

In order to verify the impact on the system when the dc bus capacitance is not equal, we replaced the capacitor C_2 with 1470 μF (a 1000-μF capacitor and a 470-μF capacitor in parallel), and the capacitor C_1 is still 2200 μF. The proposed-MPC

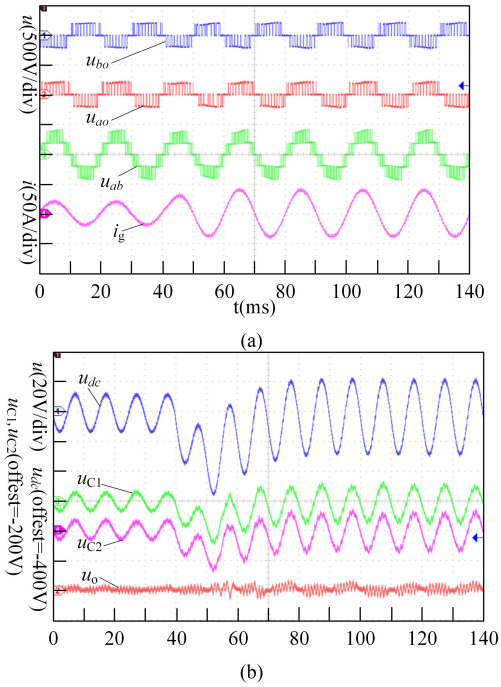

Fig. 14. Dynamic experiment results of proposed-MPC. (a) AC-side voltage and grid-side current. (b) DC-side voltage.

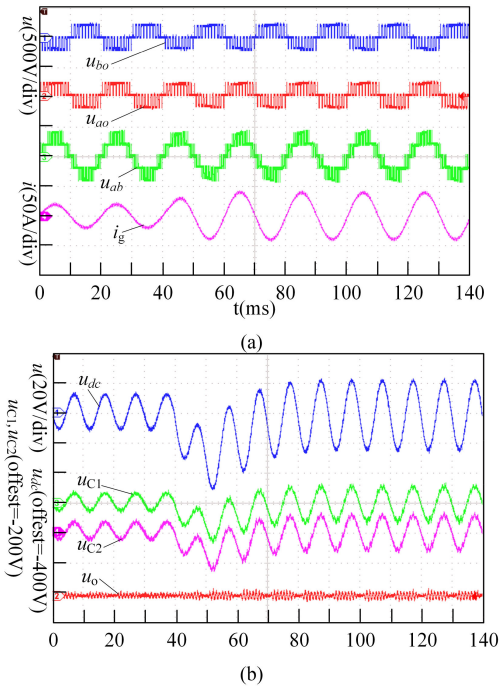

Fig. 15. Dynamic experiment results of OSS-MPC. (a) AC-side voltage and grid-side current. (b) DC-side voltage.

grid-side current i_g and midpoint potential u_o are shown in Fig. 16. The THD of grid-side current is 4.15%, which is a slight increase compared to when $C_1 = C_2 = 2200$ μF (Fig. 9). The grid-side current i_g and midpoint potential u_o when the OSS-MPC method is different from λ are shown in Fig. 17, where λ is the midpoint potential weighting factor [25]. As can be seen from Fig. 17, since the midpoint voltage control scheme

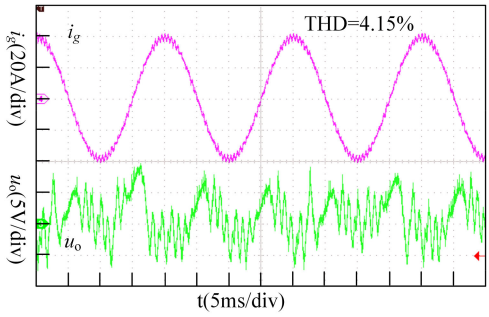

Fig. 16 Experiment results of proposed-MPC with $C_1 \neq C_2$.

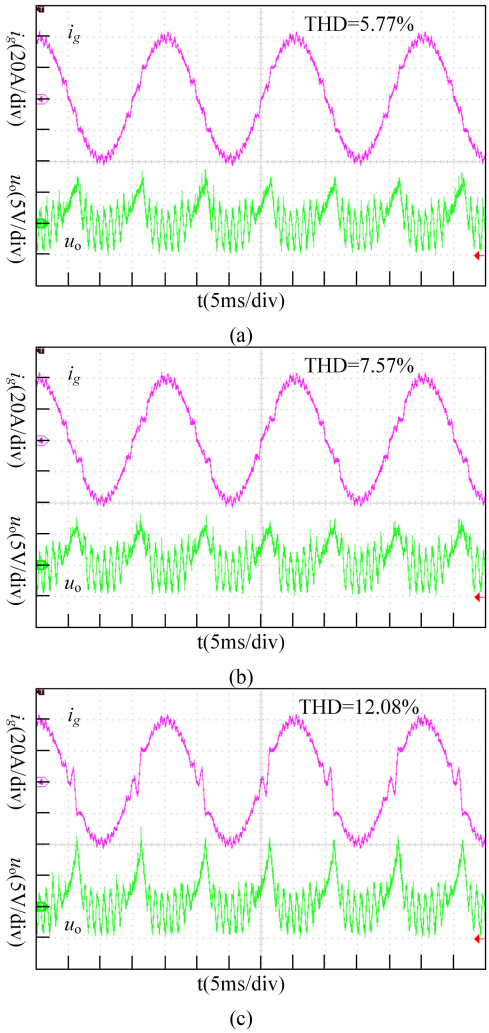

Fig. 17 Experiment results of OSS-MPC with $C_1 \neq C_2$. (a) $\lambda = 1$. (b) $\lambda = 10$. (c) $\lambda = 100$.

of the OSS-MPC depends on the dc-side capacitance value, λ affects its steady-state performance when the capacitances are not equal. The larger the λ, the larger the THD of grid-side current, and the midpoint potential does not decrease as λ increases. In comparison, proposed-MPC is more robust to dc-side capacitance parameters.

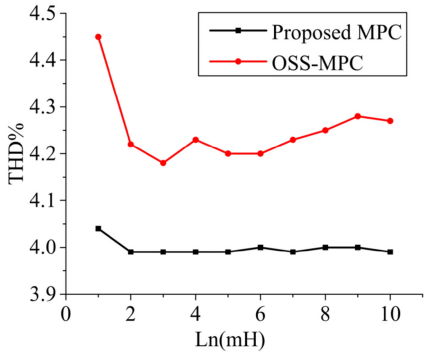

Fig. 18 Experimental results in inductance mismatch.

D. Inductance Parameter Mismatch

The experimental results of the proposed MPC and OSS-MPC method under the inductance mismatch condition at switching frequency 500 Hz and full load are shown in Fig. 18, where L_n is set in programming. The vertical axis is the grid-side current THD. From this figure, it is clear that both of proposed MPC and OSS-MPC have good inductance parameter robustness, and the current THD of the proposed MPC grid side is less affected by the inductance parameter mismatch.

VII. Conclusion

In this article, a fixed-frequency predictive control method for single-phase three-level PWM rectifier based on convex optimization is proposed. Through the switch optimization, a three-stage switching sequence that can control the midpoint potential balance is obtained. Based on above, a convex function which can evaluate the global performance of the controlled variable in one switching cycle, that is, the ℓ_2-norm index of the error matrix composed of the initial points, the extreme points and the end points, is established. When the error matrix of each feasible switch sequence obtain the minimum value, the corresponding duty ratio is calculated, and then the switch sequence that minimizes the error matrix ℓ_2-norm is selected as the system output among all feasible switch sequences. The experiment is compared with OSS-MPC and DBPCC, and the results show that the control scheme has good performance. The convex optimization-MPC and three-stage modulation methods proposed in this article can also be applied to single-phase NPC three-level new energy grid-connected, UPS converters, and other application.

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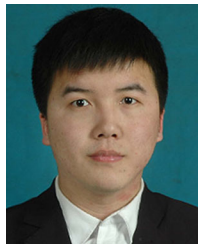

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