SiC-Based 5-kV Universal Modular Soft-Switching Solid-State Transformer (M-S4T) for Medium-Voltage DC Microgrids and Distribution Grids

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Abstract*—Medium-voltage dc (MVdc) grids are attractive for electric aircraft and ship power systems, battery energy storage system (BESS), fast charging electric vehicle (EV), etc. Such EV or BESS applications need isolated bidirectional MVdc to low-voltage dc (LVdc) or LVac converters. However, the existing Si-based solutions cannot fulfill the requirements of a high-efficiency and robust converter for MVdc grids. This article presents a 5-kV SiC-based universal modular solid-state transformer (SST). This universal current-source SST can interface either an LVac or LVdc grid with an MVdc grid in single-stage power conversion, while the conventional dual-active bridge (DAB) converter needs an additional inverter. The proposed SST module using 3.3-kV SiC MOSFETs and diodes is bidirectional and can serve as a building block in series or parallel for higher voltage higher power systems. The topology of each module is based on the soft-switching solid-state transformer (S4T) with reduced conduction loss, which features reduced electromagnetic interference electromagnetic interference (EMI) through controlled dv/dt, and high efficiency with full-range zero-voltage switching for main devices and zero-current switching for auxiliary devices. Operation principle of the modular S4T (M-S4T), capacitor voltage balancing control between the cascaded modules, design of components including a medium-voltage (MV) medium-frequency transformer (MFT) to realize a 50-kVA, 5-kV dc to 600 V dc or 480 V ac M-S4T are presented. Importantly, the MV MFT prototype achieves very low leakage inductance (0.13%) and 15-kV insulation with coaxial cables and nanocrystalline cores. The proposed universal modular SST is compared against the DAB solution and verified with dc–dc and dc–ac simulation and 4-kV experimental results. Significantly, the MV experimental results of a modular dc transformer with each module at MVdc are rarely covered in the literature and reported for the first time.

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***Index Terms*—Current-source converter (CSC), dc transformer (DCT), high-frequency link (HFL), input-series output-parallel (ISOP), isolated bidirectional dc–dc converter (IBdc), medium-voltage direct-current network, power electronic transformer (PET), zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

THE need for resiliency and islanded operation from the utility has created a distinct move towards implementing microgrids, where local generation, sustainable resources including PV, EV, and wind, and energy storage are integrated with loads to realize significant benefits for both the end-users and the utility [1]–[3]. Since renewable energy resources and most loads have a power electronic interface with a dc-link, dc microgrids through corresponding dc–dc converters present an attractive option because of enhanced efficiency from reduction in conversion stages, power quality independence from the utility, and simplified control due to absence of reactive and harmonic power flows or problems with synchronization [3]–[5]. In recent years, there has been an increasing interest in the concept of a 5-kV dc grid fed from the 13/22-kV ac system for loads in the 100 kW–5 MW range [6]–[8].

A critical requirement for such a dc subsystem is the availability of power conversion modules that can serve as a building block to implement a variety of end-use applications. The basic need is to convert 5-kV dc to 480-V ac or $<$1000-V dc with isolated high-frequency link (HFL), high efficiency, bidirectional power flow, and robust and reliable operation.

For implementing medium-voltage dc (MVdc) converters, one challenge is the relative high voltage for traditional Si power semiconductors. With low-voltage Si devices, either a large number of series-connected devices or multiple stacked modules are needed [9]. Alternatively, the use of high-voltage Si IGBTs (3.3 kV or higher) limits the switching frequency to below 500 Hz, which dramatically impacts size and performance of the converter system [10]–[12]. The performance limitation and high solution cost have limited the commercial viability of such MVdc subsystems. Availability of MV SiC devices has

reignited the interest in MV converters because of the superior performance compared to Si devices. Although currently the cost of SiC devices is higher than their Si counterparts, it is continuously dropping and the SiC devices have already shown system-level cost savings from increased switching frequency, smaller passives, reduced cooling requirement, and improved efficiency in some applications [13]–[15]. However, simply replacing the Si devices with the SiC devices can result in issues such as electromagnetic interference (EMI) from large dv/dt as high as 100 kV/μs [16], [17].

From circuit topology point of view, the isolated bidirectional dc–dc converter (IBdc) topologies based on the dual-active bridge (DAB) in [18], [19] have been proposed to implement 5 kV dc to LV dc conversion in [20] and applied to some MVdc applications [21]–[26]. The soft switching, bidirectional power flow capability, and high-frequency isolation features of the DAB converter provide a significant advantage in dc–dc applications [18], [19]. Especially, the zero-voltage switching (ZVS) can reduce the dv/dt to mitigate the EMI issue [27]–[29] and hence is suitable for converters based on SiC devices. However, the ZVS is lost and efficiency can decrease when input to output voltage ratio and load power vary [18], [19]. Moreover, in MVdc–LVac (low-voltage ac) applications, an additional dc–ac converter is needed, which is normally hard switched and can cause EMI issue with SiC devices. Furthermore, the need for multiple power conversion stages can lead to high complexity and losses [11], [30]. Another IBdc topology is the resonant converter, which is known for wide-load-range soft switching [31]–[33]. However, the resonant converter in [31], [32], and [34] operates at a specific frequency in an open-loop mode for high efficiency, which does not have as much controllability for voltage regulation as the DAB and requires an additional stage for regulation [31]–[32]. Moreover, the short-circuit overload protection of the resonant tank can be of concern [33]. Alternatively, the LLC converter can operate with variable switching frequency for better controllability but the switching-frequency variation would be large and efficiency is impaired compared to fixed frequency [31], [35]. Phase shift plus variable frequency control is recommended to mitigate this issue [8], [35]. In addition, similar to the DAB converter, an additional dc–ac converter is required to interface an LVac load.

In this article, a new modular soft-switching solid-state transformer (M-S4T) topology is proposed to achieve efficient and robust power conversion for MVdc applications. The S4T circuit in [36] is used here due to ~20% conduction loss improvement compared to the prior S4T in [11]. The existing literature of the S4T focuses on single-cell LV prototype [11], [37]–[39]. However, the solid-state transformer (SST) or power electronic transformer (PET) is an MV application, and input-series output-parallel (ISOP) (or series-connected device) is needed with device voltage lower than the MV grids. This article reports an MV S4T prototype and demonstrates ISOP modular S4T (M-S4T) at MV for the first time. The existing literature investigates MV experimental validations of single-cell (with series-connected devices or $\geq$10 kV SiC devices) bidirectional dc–dc transformers in [6], [8], [17], [33], and [40]. Significantly, MV experimental results of a modular bidirectional dc–dc transformer with each cell achieving MVdc and connected ISOP for MVdc–LVdc conversion are rarely covered in the literature and reported in detail for the first time, to the authors' best knowledge. The modularity is important from the perspective of scalability, reliability, and redundancy [9], [41]–[43].

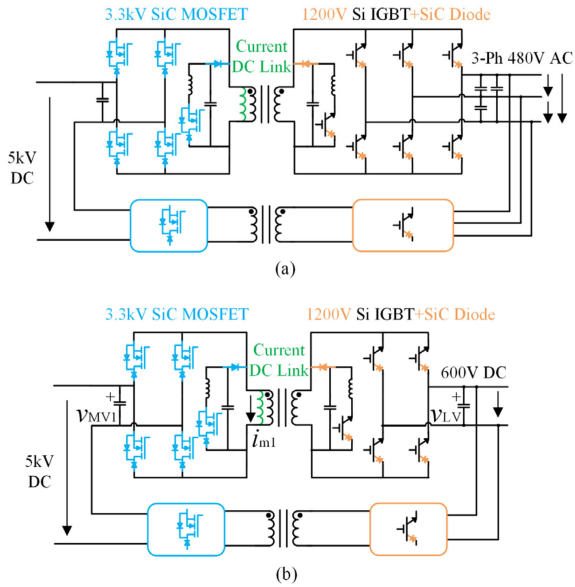


Fig. 1. (a) Schematic of the current-source modular soft-switching solid-state transformer (M-S4T) for MVdc to three-phase LVac application. (b) Schematic of the M-S4T for MVdc to LVdc application. The devices shown correspond to the experimental prototype in this article and do not imply any preference of IGBT or MOSFET for this topology.

This article presents the design and implementation of a 5-kV universal MVdc M-S4T that can interface either three-phase LVac or LVdc in a single stage. The converter modules are based on customized 3.3-kV SiC reverse-blocking modules. The converter has reduced EMI through controlled dv/dt, ZVS, and high efficiency over the full operating range. Therefore, the proposed converter does not have the limited ZVS range and the EMI issue when the ZVS is lost in the DAB. Moreover, no additional conversion stage is needed for LVac. The topology, operation principle, control of voltage sharing between modules on the MV side are presented in Section II. The proposed converter is verified through MVdc to LVdc and LVac simulation results in Section III. Section IV discusses design considerations to realize a 50-kVA, 5-kV dc to 600-V dc/480 V ac prototype. Experimental results at 20 kW, 4 kV are presented to verify the effectiveness of the proposed converter in Section V. Section VI is devoted to comparison between the proposed M-S4T and the conventional solution. Finally, Section VII concludes this article.

II. The Proposed Universal Modular MVdc Solid-State Transformer (SST)

A. Circuits and Topologies

The schematic of the universal modular MVdc SST or PET to interface LVac and LVdc loads or sources is shown in Fig. 1(a)

and (b), respectively. The converter module is based on the soft-switching solid-state transformer (S4T) topology with reduced conduction loss [36]. The converter is composed of a medium-frequency transformer to provide galvanic isolation and a current-source dc-link inductor (magnetizing inductance of the transformer), two reverse-blocking semiconductor bridges, and auxiliary resonant circuits to provide ZVS conditions for all the main devices. The auxiliary resonant switches are switched under zero-current switching (ZCS) conditions. The MV bridge has two legs to interface the MVdc grid, while the LV bridge has two legs for LVdc application or three legs for LVac application. A modular approach is required for MV applications, where the voltage level can be significantly higher than a single commercially available device. Like any modular converter, the converter modules are connected in series on the MV side and in parallel on the LV side. In this article, 3.3-kV SiC reverse-blocking MOSFET modules are used on the MV side, which is why two modules are stacked in series to handle 5 kV in Fig. 1.

The proposed converter can be considered a universal MVdc SST because it can provide bidirectional power flow, interface the LVdc grid or the LVac grid with a small configuration change (two-leg versus three-leg), and achieve higher voltages and power by ISOP configuration. In addition, the converter modules feature a single-stage HFL power conversion architecture, reduced dv/dt, full-range ZVS, and robustness with benign fault modes.

B. Operation Principle

The basic operation principle and conceptual operation waveforms of the M-S4T converter are shown in Figs. 2 and 3. The M-S4T has two cycles including a forward cycle (mode 1), where energy is transferred from the sending terminal and stored in the magnetizing inductance ($L_{\rm m}$) of the transformer which serves as a dc-link inductor to buffer the input and the output power difference, and a regen cycle (mode 3) where energy is transferred from the inductance to the receiving terminal. The two active states are interposed with ZVS transition state (mode 0) and/or resonant state (mode 4), which aid in achieving the ZVS. During the resonant state, the auxiliary devices Sri and Sro switch under ZCS conditions as illustrated in $i_{\rm LrMV}$ and $i_{\rm LrLV}$ traces of Fig. 3 to flip the polarity of the resonant-capacitor voltages ($v_{\rm CrMV}$ and $v_{\rm CrLV}$). Suppose the converter is at the end of mode 2, where the switches corresponding to mode 2 are turned OFF. Then, in mode 0, the resonant capacitors on both sides of the transformer are discharged until the resonant capacitor voltages reach the voltage level of the next state, i.e., mode 3. At that instant, the voltages across the switches for the regen state should be the voltage difference between the resonant capacitors and the filter capacitor voltages ($V_{\rm bao}$) and close to zero. Hence, the switches for mode 3 can be turned ON at zero voltage and the ZVS is achieved. The sequence of the states and the time spent in each state are derived according to the control scheme described below.

C. Control Scheme

Any modular series-stacked converter needs a fast and robust stacked-side capacitor voltage balancing method [43]. In the case of the M-S4T, the dynamic voltage balancing is even more challenging because of the reduced dc-link (where $L_{\rm m}$ is the current-source dc-link in the S4T and is normally designed for 40%–60% peak-to-peak ripple unless specific use cases require larger $L_{\rm m}$) compared to other modular converters. A detailed discussion on the control method for such a stacked reduced dc-link converter is in [43]. Here, for the sake of clarity, the control method under the MV to LV power flow for MVdc to LVdc conversion in the later simulation is introduced, while other cases are similar, e.g., LV to MV power flow or MVdc to three-phase LVac conversion where two LV vectors are used instead of one in the LVdc case.

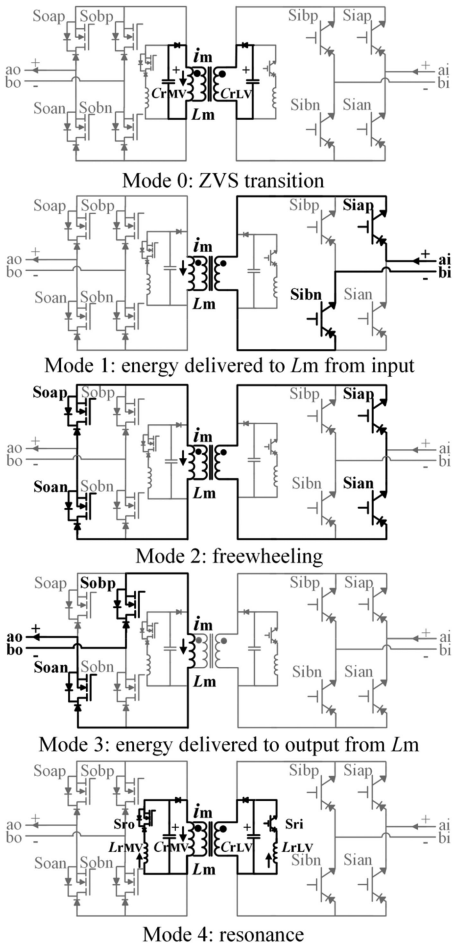


Fig. 2. Switching states of the proposed M-S4T under the LV-to-MV power flow direction.

The control objectives of the proposed stacked converter include regulating the magnetizing current, balancing the stacked-side capacitor voltage on the MV side, and controlling the LV-side voltage or current. With a constant switching frequency, there are only two independent control freedoms for each module, i.e., the MV-bridge duty cycle and the LV-bridge duty cycle, to achieve the three abovementioned objectives during transients or steady state. Therefore, a trade-off among the three tasks in terms of control efforts should be made. To achieve that, a novel model-predictive priority-shifting (MPPS) control is proposed in Figs. 4 and 5. In Fig. 4, the converter has two priority modes

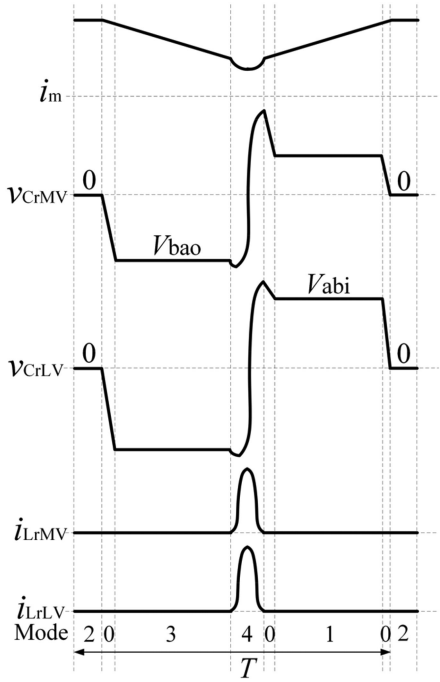


Fig. 3. Conceptual operating waveforms of the proposed M-S4T under the LV-to-MV power flow.

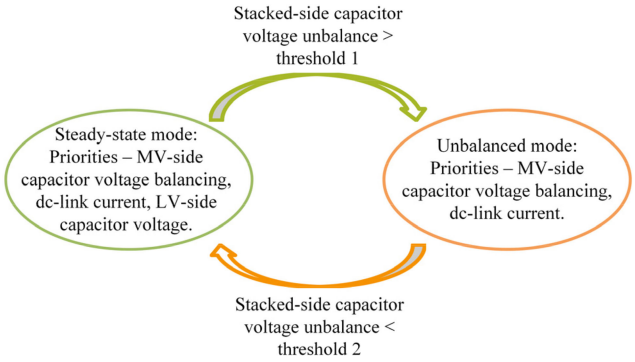


Fig. 4. Priority-shifting control block of the proposed model predictive priority-shifting (MPPS) control.

including the steady-state mode and the unbalanced mode. The system is in the unbalanced mode when the voltage unbalance between the two stacked capacitors is out of threshold 1. In this mode, all the control efforts are assigned to the stacked-side capacitor voltage balancing and the dc-link current regulation to ensure that the voltage balance is restored as fast as possible, because avoiding overvoltage is important for safe and reliable operation of the devices and the converter [43]. The system enters the steady-state mode if the stacked-side capacitors are balanced within threshold 2. In the steady-state mode, all the three control objectives are realized.

The calculation of the MV-bridge dwelling time (T_{MV1}), the LV-bridge dwelling time (T_{LV1}), and the freewheeling or zero-vector dwelling time (T_{z1}) for module 1 of the two modules in the steady-state mode under MV to LV power flow direction

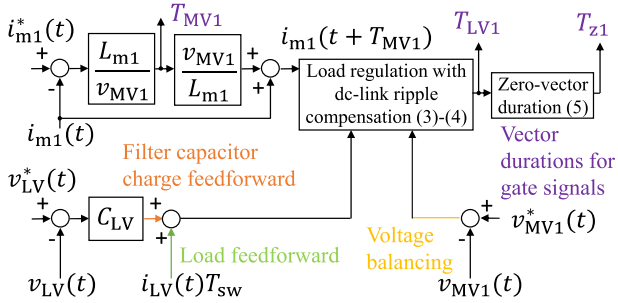


Fig. 5. Model-prediction control block in the steady-state mode of the proposed model predictive priority-shifting (MPPS) control.

are given in (1)–(7) and illustrated in Fig. 5. The fundamental idea behind (1)–(7) is similar to deadbeat control or predictive control. In other words, the equivalent circuit models of the system are derived during each state and the state variables can be steered according to predictive control laws. Equation (1) calculates the MV-bridge vector timing (T_{MV1}) to ramp up the dc-link current ($i_{\mathrm{m1}}(t)$), similar to mode 1 in Fig. 3, to the desired reference ($i^*_{\mathrm{m1\_peak}}(t)$) with the measured MV-side filter capacitor voltage ($v_{\mathrm{MV1}}(t)$)

$$T_{\mathrm{MV1}} = \left(i^*_{\mathrm{m1\_peak}}(t) - i_{\mathrm{m1}}(t)\right) \cdot L_{\mathrm{m1}}/v_{\mathrm{MV1}}(t) \quad (1)$$

where t is the instant when the next switching cycle starts. Equation (2) updates the dc-link current after the MV-bridge vector, while (3) computes the LV-bridge vector timing (T'_{LV1}) required to make the LV-side filter capacitor voltage ($v_{\mathrm{LV1}}(t)$) track the reference ($v^*_{\mathrm{LV1}}(t)$)

$$i_{\mathrm{m1}}(t+T_{\mathrm{MV1}}) = i_{\mathrm{m}}(t) + v_{\mathrm{MV1}}(t)/L_{\mathrm{m1}} \cdot T_{\mathrm{MV1}}. \quad (2)$$

The term $(v^*_{\mathrm{LV1}}(t) - v_{\mathrm{LV1}}(t))C_{\mathrm{LV1}}$ in (3) is the required charge feedforward for the LV-side filter-capacitor-voltage reference tracking. The term $i_{\mathrm{LV}}(t)T_{\mathrm{sw}}$ in (3) is the charge corresponding to the LV-side load current ($i_{\mathrm{LV}}(t)$) feedforward. The physical meaning of the term $v_{\mathrm{LV1}}(t)T'^2_{\mathrm{LV1\_last}}/(2L_{\mathrm{m1}})$ is additional charge from the high dc-link current ripple due to the reduced dc-link of the M-S4T [43]. The term $[1/2 + k_{\mathrm{p}}(v_{\mathrm{MV1}}(t) - v^*_{\mathrm{MV1}}(t))]$ adjusts the LV-bridge vector timing for the MV-side capacitor voltage balancing, where 1/2 is the current sharing between the two balanced modules, and k_{p} is a translation factor for the MV-side balancing

$$T'_{\mathrm{LV1}} = [1/2 + k_{\mathrm{p}}(v_{\mathrm{MV1}}(t) - v^*_{\mathrm{MV1}}(t))] \frac{(v^*_{\mathrm{LV1}}(t) - v_{\mathrm{LV1}}(t))C_{\mathrm{LV1}} + i_{\mathrm{LV}}(t)T_{\mathrm{sw}}}{i_{\mathrm{m1}}(t+T_{\mathrm{MV1}})} \quad (3)$$

$$T_{\mathrm{LV1}} = T'_{\mathrm{LV1}} + \frac{v_{\mathrm{LV1}}(t)T'^2_{\mathrm{LV1\_last}}/(2L_{\mathrm{m1}})}{i_{\mathrm{m1}}(t+T_{\mathrm{MV1}})}. \quad (4)$$

The following equation computes the dc-link current after the LV-bridge vector

$$i_{\mathrm{m1}}(t+T_{\mathrm{sw}}) = i_{\mathrm{m}}(t+T_{\mathrm{MV1}}) - \frac{v_{\mathrm{LV1}}(t)}{L_{\mathrm{m1}}} \cdot T_{\mathrm{LV1}}. \quad (5)$$

Note that after the computation of (2) and (5), the constraint in (6), essentially a saturation limit for the LV-bridge and the

TABLE I
SIMULATION PARAMETERS OF THE MODULAR SOFT-SWITCHING SOLID-STATE TRANSFORMER (M-S4T)

Parameter	Symbol	Value
Magnetizing inductance	$L_{\text{m\_LV}}$	262.5 μH
Leakage inductance	$L_{\text{leakage\_LV}}$	500 nH
MV-side resonant inductor	$L_{\text{r\_MV}}$	80 μH
MV-side resonant capacitor	$C_{\text{r\_MV}}$	6.25 nF
LV-side resonant inductor	$L_{\text{r\_LV}}$	5 μH
LV-side resonant capacitor	$C_{\text{r\_LV}}$	100 nF
MV-side filter capacitor	$C_{\text{f\_MV}}$	4.9 μF
LV-side filter capacitor	$C_{\text{f\_LV}}$	60.0 μF

MV-bridge vector timings, should be enforced to ensure no large overshoot or undershoot on the reduced dc-link for safe and reliable operation.

$$I_{\text{m1\_lower}} < i_{\text{m1}} < I_{\text{m1\_upper}}. \tag{6}$$

The freewheeling duration (T_{z1}) is shown in (7) to ensure a constant switching frequency (f_{sw}).

$$T_{\text{z1}} = T_{\text{sw}} - T_{\text{MV1}} - T_{\text{LV1}} - T_{\text{ZVS}} - T_{\text{r}} \tag{7}$$

where T_{ZVS} is the lost time during mode 0 and T_{r} is the lost time during mode 4 in Fig. 3.

III. SIMULATION RESULTS OF THE MODULAR SOFT-SWITCHING SOLID-STATE TRANSFORMER (M-S4T)

A. Voltage-Balancing Control

In order to verify the operation and the control, a 16-kHz M-S4T converter in Fig. 1(b) with parameters in Table I similar to experiments is simulated. Furthermore, a 10% parameter mismatch is added between the two modules in terms of the magnetizing inductance and the MV-side filter capacitor. k_{p} is selected to be 0.002, which means that 250 V voltage difference is translated to 50% current sharing difference for balancing [43]. In the first case, a step change from 100% load current to 10% and back to 100% is simulated. As shown in Fig. 6, the MVdc filter capacitor voltages are balanced even under the load step-change and the magnetizing current is regulated about its reference value. Only minor load voltage transient can be observed, thanks to the fast MPPS control method.

In the second case, a large unbalance is intentionally introduced on the stacked-side MVdc filter capacitor voltages in Fig. 7. The controller enters unbalanced mode and prioritizes capacitor voltage and magnetizing current to bring the stacked-side voltage back in a timely manner, when the stacked-side voltage exceeds threshold 1 of 6% in Fig. 4 in this simulation. During this period, a voltage drop can be observed on the load side, because the LV-side voltage regulation is temporarily given up in the unbalanced mode and all the control efforts are devoted to the balancing and the dc-link control to restore the balance as soon as possible for safe and reliable operation [43]. When the stacked-side voltage unbalance goes back into the steady-state range, i.e., threshold 2 of 3.5% in Fig. 4, the load voltage is regulated back to the normal value. Note that the settling time for MVdc voltage balancing is as fast as ~500 μs, which is mainly limited by the physical power processing capability (power rating) of the converter modules and the capacitive filter values. The simulation results verify the MPPS control method and demonstrate the ability to balance the stacked-side capacitor voltages even under large transients.

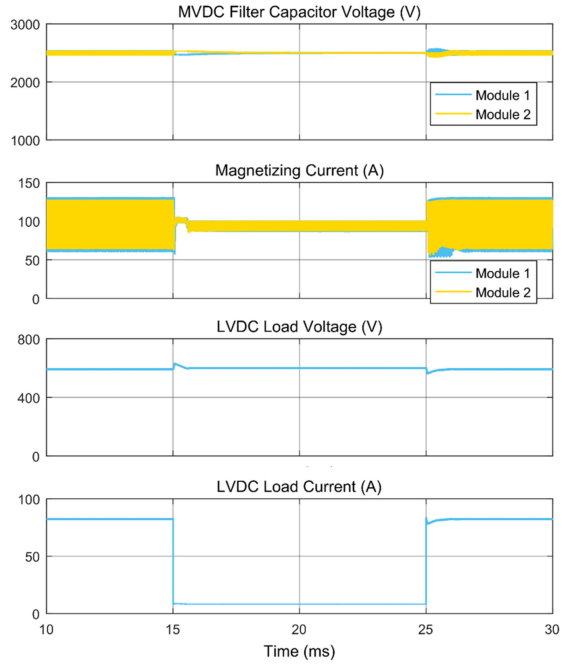


Fig. 6. Simulation waveforms of the MVdc SST to interface an LVdc grid under a load step change. The magnetizing current is referred to the LV side of the 4:1 transformer of the converter.

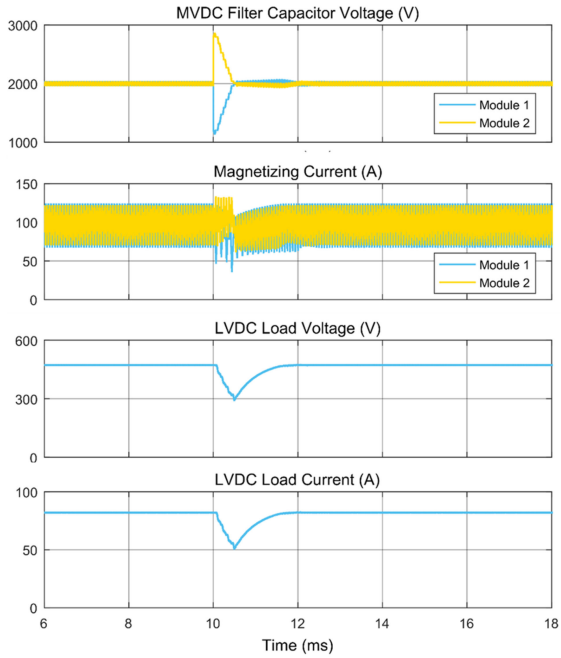


Fig. 7. Simulation waveforms of the MVdc SST to interface an LVdc grid under a large disturbance of the stacked-side unbalance.

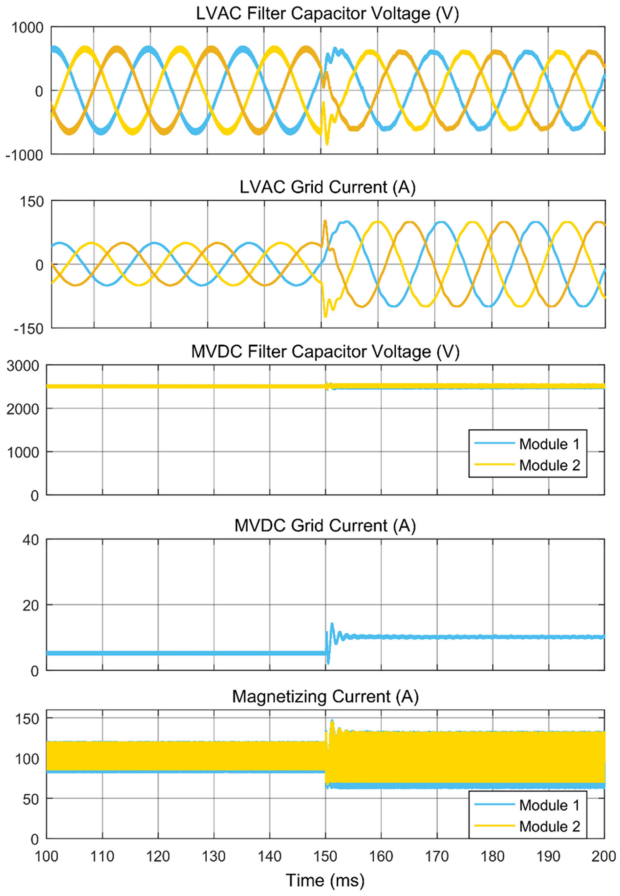


Fig. 8. Simulation waveforms of the 5-kV MVdc SST to interface a three-phase 480-V LVac grid. The magnetizing current is referred to the LV side of the 4:1 transformer of the converter.

B. MVDC-LVAC Conversion

The MVdc–LVdc conversion in Fig. 1(b) has been verified in the simulation and will be demonstrated in the experimental section. For the sake of proof of concept and to show that the proposed converter is universal and can interface the three-phase LVac grid in Fig. 1(a), the MVdc–LVac conversion is verified in this simulation. The parameters are the same as the MVdc–LVdc simulation case above, except three 8.5-μF capacitors connected in delta configuration as the LV-side filter capacitors for each module. Moreover, three 1.5-mH filter inductors are connected between the LV side of the converter and the three-phase LVac grid. A 2-mH filter inductor is connected between the MV side of the converter and the MVdc grid. A 10% parameter mismatch is added between the two modules in terms of the magnetizing inductance and the MV-side filter capacitor. The simulation results in Fig. 8 show sinusoidal line currents drawn from the LVac grids with THD $< 1.5\%$ during steady state. A load-current step change from 50% to 100% occurs at 150 ms. During the step change, the MVdc filter capacitor voltages remain balanced and the magnetizing current is controlled at its reference. Fig. 8 verifies the operation of the proposed configuration in Fig. 1(a) to interface LVac grids during dynamic and steady-state conditions and highlights the proposed M-S4T is a universal converter for MVdc grids.

Fig. 9. (a) Customized Cree reverse-blocking module based on 3.3-kV SiC MOSFET dies and 3.3-kV SiC diode dies. (b) Customized Cree 3.3-kV discrete SiC diodes.

IV. Design of the Modular Soft-Switching Solid-State Transformer (M-S4T)

The objective is to design a 50-kVA, 5-kV dc to 480 V ac/600 V dc M-S4T converter based on two 25-kVA, 2.5-kV dc to 480 V ac/600 V dc modules. The selection and the design of devices, snubbers, resonant tanks, medium-frequency transformer, and high-isolation gate-driver power supply are discussed.

A. Device and Snubber Design

A customized MV reverse-blocking module from Cree based on 3.3 kV SiC MOSFET dies and 3.3 kV SiC diode dies including the main switches, and the auxiliary resonant switch is developed as shown in Fig. 9. This module has been characterized using a double-pulse test to show that the switching losses are reduced by over 90% with the ZVS [44]. On the LV side, discrete devices with low conduction drop are selected for main switches and auxiliary resonant switch, including 1.2-kV discrete Si IGBTs Infineon IGW60T120 (two in parallel in each reverse-blocking switch) and 1.2-kV discrete SiC diodes GlobalPower GP2D050A120B (two in parallel in each reverse-blocking switch). Here, 1.2-kV Si IGBTs are applied on the LV side because of reasonably low conduction-voltage drop and low cost. 1.2-kV SiC MOSFETs can replace the 1.2-kV Si IGBTs if achieving higher efficiency is the target. Ideally, 1.2-kV high-current-rating SiC reverse-blocking modules should be used on the LV side for very small conduction loss. Unfortunately, such device modules have limited availability on the market, which ultimately compromises the efficiency of the prototype.

At the end of the resonant state, i.e., mode 4 in Fig. 2, the resonant-inductor current reaches zero and the diodes in Sri and Sro snap OFF. Then, the oscillations between the resonant inductors and the diode capacitances begin as the diodes start to block voltage. The equivalent circuit of the oscillations is illustrated in Fig. 10(c) using the LV side as an example. Once this oscillation is damped out, the diodes in Sri and Sro block the positive voltages across the resonant capacitors, while the IGBT or the MOSFET in Sri and Sro is forward biased.

Ideally, without the oscillations, diodes of the same voltage rating as the main devices can be used for the diodes in Sri and Sro. However, the LC parasitic oscillations can result in 200% voltage stress and are hard to damp [45]. These oscillations are

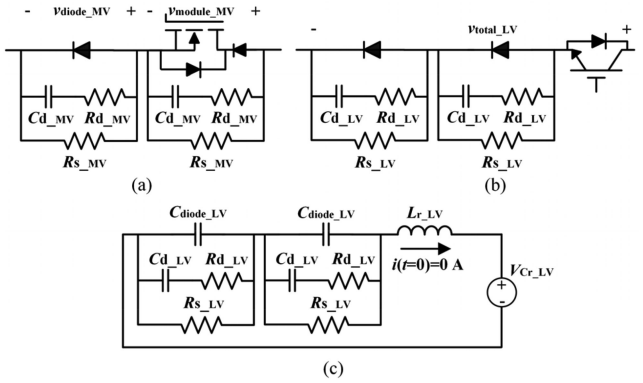


Fig. 10. (a) MV resonant switch and snubbers. (b) LV resonant switch and snubbers. (c) Equivalent circuit of the parasitic oscillation at the end of the resonant state with the LV resonant switch and snubbers. During the time scale of the oscillation, the resonant-capacitor voltage can be assumed fixed. The IGBT is forward-biased. The discrete diode and the diode inside the module block voltages have equivalent parasitic capacitances.

similar to the oscillations between the auxiliary inductor and the device capacitance at the end of the resonant state in the auxiliary resonant commutated pole (ARCP) converter [45]. Normally, RC snubbers are designed for damping of device-commutation-loop-induced oscillation with small inductance, e.g., ∼100 nH in [46] or smaller, including device module inductance, PCB parasitic inductance, etc. However, the involved inductances here are more than an order of magnitude larger, i.e., the resonant inductances of 80 μH on the MV side and 5 μH on the LV side. According to [47] and [48], oscillations with larger inductance and higher inductive energy need larger snubber capacitance and thus higher snubber loss.

In fact, the snubber power loss can be too high to be acceptable here. For example, on the MV side, the installed snubber capacitance is roughly seven times the diode capacitance at the voltage of interest and dissipates more than 20 W, while the voltage stress remains as high as 170%–200% in experimental waveforms. To reduce the voltage stress to an acceptable level like 120%, the snubber capacitance and thus the snubber capacitive power loss, will be significantly increased [47] and [48]. A similar damping problem between a 12-μH auxiliary inductor and SiC diode capacitances is discussed in an ARCP-DAB converter [45]. Snubber capacitance of 50 nF, which is more than 100 times the SiC diode capacitance, still results in 115%–130% voltage stress [45]. The "100 times" snubber capacitance further supports the prior finding of excessive snubber requirement. Note that compared to the M-S4T, the large snubber capacitance in [45] does not induce an unacceptably high percentage of loss in the ARCP-DAB due to lower switching frequency of 1 kHz, much larger main circuit rating of 5 MW, and other differences in the nature of topologies.

Because the snubber loss can be too large to reduce the voltage stress to 120% from both SST efficiency and through-hole resistor rating point of view, two diodes are connected in series on both the MV side and the LV side for robustness and safe operation in Fig. 10. The 2-pu voltage rating only applies to the diode in Sri and Sro but not to the IGBT or MOSFET or any other diode. Note that this issue has not been studied in prior LV S4T prototype [37], where 1.2-kV devices are used in 208 V application, providing a large enough margin.

On the LV side, two sets of 1.2-kV SiC diodes GP2D050A120B are used as the resonant switch diode. In each set, two diodes are connected in parallel. Since an equivalent 2-pu diode is used, the oscillation-induced voltage-stress-mitigation requirement is relaxed and voltage balancing between the diodes is the dominant constraint for snubber design. According to the design method in [49], for the worst case, one set of diodes is considered to have nominal reverse charge $Q_{\mathrm{c\_LV}}$, i.e., 220 nC, while the other set has zero reverse charge. The snubber capacitor should be large enough so that resultant voltage stress for each set is within the voltage margin in (8), i.e., 1.2 kV $V_{\mathrm{rating\_LV}}$ and 600 V $V_{\mathrm{d\_pk\_LV}}$ considering the transient voltage stress

$$C_{\mathrm{d\_LV}} > Q_{\mathrm{c\_LV}} / \left(V_{\mathrm{rating\_LV}} - V_{\mathrm{d\_pk\_LV}}\right). \tag{8}$$

The snubber resistor should be small enough to allow the snubber capacitance to be sufficiently discharged even during the shortest forward-bias duration of the diodes $T_{\mathrm{ON\_min}}$; that is, the shortest duration when the resonant capacitors have negative voltages, e.g., 3 μs. This requirement is given as [49]

$$R_{\mathrm{d\_LV}} < \frac{T_{\mathrm{ON\_min}}}{3C_{\mathrm{d\_LV}}}. \tag{9}$$

Furthermore, the equivalent snubber resistor $R_{\mathrm{d\_LV(eq)}}$, i.e., two $R_{\mathrm{d\_LV}}$ in series, should be higher than the approximate critical-damping value as given in (10). $C_{\mathrm{d\_LV(eq)}}$ and $C_{\mathrm{diode\_LV(eq)}}$ are two $C_{\mathrm{d\_LV}}$ and $C_{\mathrm{diode\_LV}}$ in series. $L_{\mathrm{r\_LV}}$ is 5 μH and $C_{\mathrm{diode\_LV(eq)}}$ is 0.25 nF for two sets of diodes in series

$$R_{\mathrm{d\_LV(eq)}} > 2\sqrt{\frac{L_{\mathrm{r\_LV}}}{C_{\mathrm{d\_LV(eq)}} + C_{\mathrm{diode\_LV(eq)}}}}. \tag{10}$$

Finally, static voltage sharing with 10% tolerance needs to be ensured considering possible leakage current deviation as given by (11), according to the methodology in [49]. $V_{\mathrm{s\_pk\_LV}}$ is 300 V considering the static voltage stress and the worst-case $I_{\mathrm{diode\_lkg\_LV}}$ is 8 μA at 300 V for each set of diodes

$$R_{\mathrm{s\_LV}} < \frac{0.1V_{\mathrm{s\_pk\_LV}}}{I_{\mathrm{diode\_lkg\_LV}}}. \tag{11}$$

Using (8)–(11), $C_{\mathrm{d\_LV}}$, $R_{\mathrm{d\_LV}}$, and $R_{\mathrm{s\_LV}}$ are sized to be 390 pF, 100 Ohm, and 1 MOhm, respectively. For this design, $C_{\mathrm{d\_LV}}$ is of the similar value as $C_{\mathrm{diode\_LV}}$ and hence the snubber power loss is small and less than 2 W. Note that when $C_{\mathrm{d\_LV(eq)}}$ is less than four times $C_{\mathrm{diode\_LV(eq)}}$, overdamped response is not achieved with (10) and in fact cannot be achieved regardless of $R_{\mathrm{d\_LV}}$. The above statement can be verified in Fig. 8 of [50], where even the minimal quality factor is above one when the snubber capacitance is relatively small. However, as discussed, with series connection of diodes and the snubber design for voltage sharing [49] resolving the voltage stress issue, the undamped oscillations are acceptable from basic functionality point of view.

On the MV side, another 3.3-kV SiC discrete diode Cree CPW3-3300-Z045B in Fig. 9(b) is series-connected to the

TABLE II
SPECIFICATION OF MEDIUM-FREQUENCY TRANSFORMER FOR THE MODULAR SOFT-SWITCHING SOLID-STATE TRANSFORMER (M-S4T)

Parameter	Value
Operating frequency (f_{sw})	16 kHz
DC component of magnetizing current	25 A (MV) / 100 A (LV)
Magnetizing inductance (L_{m_LV})	200-400 μH
Inter-winding capacitance (C_{ps})	< 2.0 nF
Leakage inductance ($L_{leakage\_LV}$)	< 1.0 % of L_{m_LV}
Loss	< 1.0 %
Isolation level	15 kV
Turns ratio	4:1

resonant-switch position of the customized module in Fig. 9(a) to realize the 2-pu diode in Fig. 10. Different from the LV side, the authors found through experiments that the diode die in the discrete package and the diode die in the module are different with different external characteristics, which is challenging. After experimental trials, larger snubber capacitance is needed for better voltage balancing and the snubber capacitance $C_{\mathrm{d\_MV}}$ is ultimately limited by the allowed snubber capacitive loss dissipation (∼26 W for 2-kV operation) on the snubber resistor with limited power rating. Design of other parameters still follow (9)–(11) [49], assuming the die in the module has the same capacitance and leakage current as CPW3-3300-Z045B (the capacitance and leakage current of the diode die in the module are not available to the authors from Cree). The final parameter selections are 820 pF, 390 Ω, and 3 MΩ for $C_{\mathrm{d\_MV}}$, $R_{\mathrm{d\_MV}}$, and $R_{\mathrm{s\_MV}}$, respectively.

B. Transformer Design

The specifications of the transformer are provided in Table II. One challenge of the design is to achieve high isolation level and low leakage inductance at the same time. It should be noted that the transformer magnetizing inductance serves as the dc-link inductor for the M-S4T. The transformer turns ratio is designed to be 4:1 to match the nominal voltage conversion ratio. The operating frequency is selected to be 16 kHz so that the transformer is free from audible noise emission. The peak transformer current is a function of transformer magnetizing inductance and average magnetizing current, i.e., dc component of the magnetizing current. The average magnetizing current is chosen to be 2.5 pu of the nominal load current. The additional 0.5-pu current is to address the duty cycle lost during the resonant state and the ZVS transition state as well as provide some margins for robustness. The value of the magnetizing inductance is a free variable to be determined through optimization. Higher magnetizing inductance results in lower current ripple but larger transformer, while smaller magnetizing inductance leads to higher current ripple and increased conduction losses. The impacts of the leakage inductance are explained in detail in [38], where the major conclusion is briefly presented as follows. A larger leakage inductance translates to larger resonant capacitors to limit the voltage stress due to larger leakage energy. Larger resonant capacitors mean more lost duty cycle and lower efficiency, which is why a smaller leakage inductance, e.g., $L_{\mathrm{leakage}}/L_{\mathrm{m}} < 0.5\%$, is preferred for this converter [38]. Such level of leakage inductance is achievable with the traditional foil-based transformer design for LV prototype, e.g., ∼0.5% in [37]–[39], but for MV prototype, the feasibility needs further investigation due to the required insulation and the associated complexity for termination, etc. The target values of the parasitics for this design are also presented in Table II. Moreover, the transformer is designed to meet 15-kV isolation.

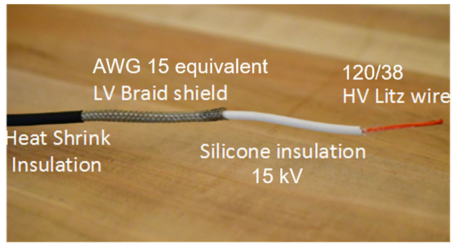


Fig. 11. Structure of the coaxial cable to achieve both low leakage inductance and high isolation capability.

In this design, a customized coaxial cable is used to achieve both low leakage and high isolation. Compared to the foil-based design, the advantage is the simplified MV insulation design and termination, lower lost duty cycle, larger effective duty cycle, and higher efficiency. The coaxial winding consists of an inner Litz wire and an outer tinned-copper braid separated by Silicone insulation to achieve 15-kV isolation, as shown in Fig. 11. In addition, the coaxial cable is provided with an outer LV insulation. The inner Litz wire acts as the MV winding while the outer braid acts as LV winding.

Three core materials, namely ferrite, nanocrystalline, and amorphous, are considered for this design. The core losses are calculated using the following equation, based on the Steinmetz equation [51]:

$$\Delta B = B_{\max} \cdot \frac{0.5\, I_{\mathrm{pp}}}{I_{\mathrm{m\_dc}} + 0.5\, I_{\mathrm{pp}}} \tag{12}$$

$$I_{\mathrm{pp}} = \frac{V_{\mathrm{in\_pk}} \cdot D_{\mathrm{in\_pk}}}{L_{\mathrm{m}} \cdot f_{\mathrm{sw}}} \tag{13}$$

$$P_{\mathrm{amorphous}}\left(\frac{W}{m^3}\right) = 7290 \cdot 6.5 \cdot (f_{\mathrm{sw}})^{1.51} \cdot (\Delta B)^{1.74} \tag{14}$$

$$P_{\mathrm{nanocrystalline}}\left(\frac{W}{m^3}\right) = 7180 \cdot 1.09 \cdot (f_{\mathrm{sw}})^{1.62} \cdot (\Delta B)^{1.98} \tag{15}$$

$$P_{\mathrm{ferrite}}\left(\frac{W}{m^3}\right) = 4850 \cdot 32.9 \cdot (f_{\mathrm{sw}})^{1.36} \cdot (\Delta B)^{2.86} \tag{16}$$

where ΔB is the peak–peak variation in flux density, $B_{\max}$ is the peak flux density of the material, I_{pp} is the peak-to-peak current ripple, $I_{\mathrm{m\_dc}}$ is the dc component of the transformer magnetizing current, $V_{\mathrm{in\_pk}}$ is the peak input voltage, $D_{\mathrm{in\_pk}}$ is the duty cycle for peak input voltage, L_{m} is the transformer magnetizing inductance, and f_{sw} is the switching frequency.

According to [52], the ac resistance factor ($F_{\mathrm{R,MV}}$) to calculate the copper loss in the Litz winding (MV winding) is shown

as

$$F_{\mathrm{R,MV}} = 1 + \frac{(\pi n N_{\mathrm{MV}})^2 d_{\mathrm{s}}^6}{192\delta^4 b^2} \tag{17}$$

where n is the number of strands in the Litz wire, d_{s} is the diameter of each strand, N_{MV} is the number of MV turns, δ is the skin depth, and b is the height of the winding.

The copper braid (LV winding) of thickness t_{LV} and diameter d_{LV} is treated as foils of thickness t_{LV} and length $d_{\mathrm{LV}} \cdot N_{\mathrm{LV}}$, where N_{LV} is the number of turns in a single layer. With this assumption, the ac resistance factor ($F_{\mathrm{R,LV}}$) can be calculated using the following equations with the Dowell equation [53]:

$$F_{\mathrm{R,LV}} = G_1 + \frac{2}{3}\left(N^2 - 1\right) \cdot G_2 \tag{18}$$

$$G_1 = \Delta \frac{\sinh 2\Delta + \sin 2\Delta}{\cosh 2\Delta - \cos 2\Delta} \tag{19}$$

$$G_2 = \Delta \frac{\sinh \Delta - \sin \Delta}{\cosh \Delta + \cos \Delta} \tag{20}$$

$$\Delta = \frac{t_{\mathrm{LV}}}{\delta} \tag{21}$$

where *N* is the number of layers. Once the ac resistance factor is calculated, the ac loss is calculated using

$$P_{\mathrm{ac\_loss\_cond}} = \left(\frac{I_{\mathrm{pp}}}{2} * 0.577\right)^2 \cdot F_{\mathrm{R}} \cdot R_{\mathrm{dc}} \cdot D_{\mathrm{eff}} \tag{22}$$

where D_{eff} is the effective duty cycle, i.e., the sum of duty cycles for modes 1 and 3. The leakage inductance and the parasitic capacitance are calculated using the following equations:

$$L_{\mathrm{lkg}} = l_{\mathrm{coil}} \cdot \left(0.5 + 2 \cdot \log\left(\frac{OD_{\mathrm{MV}} + 2 \cdot t_{\mathrm{ins}}}{OD_{\mathrm{MV}}}\right)\right) \tag{23}$$

$$C_{ps} = 8.84 \cdot 10^{-12} \cdot \epsilon \cdot l_{\mathrm{coil}} \frac{\pi \cdot \left(OD_{\mathrm{MV}} + \frac{t_{\mathrm{ins}}}{2}\right)}{t_{\mathrm{ins}}} \tag{24}$$

where l_{coil} is the length of the winding, OD_{MV} is the outer diameter of the MV winding, t_{ins} is the thickness of insulation, and ϵ is the permittivity of the insulation material.

The results of the design with the nanocrystalline core are shown in Fig. 12. As expected, the loss tends to reduce with increased L_{m}, but the cost and the weight increase as the core size increases. With a fixed L_{m}, the loss is higher at a lower number of turns, because the core loss dominates there and increases with reduced turns. The leakage inductance and the parasitic capacitance increase with the number of turns and core size.

An analysis has been performed to compare nanocrystalline, ferrite, and amorphous cores across various parameters, including core size (core area A_{c} multiplied by window area A_{w}), cost, leakage inductance, parasitic capacitance, and magnetizing inductance. The loss of 200 W is kept the same across all the designs. The cost is calculated based on quotes received from manufacturers and the derived per unit weight or volume price of each core material. The results of the comparison are shown in Fig. 13. The design with amorphous cores is not able to achieve loss <200 watts even with a large core ($L_{\mathrm{m}} = 1000\ \mu$H) and a large number of turns like 24. An even larger core can be chosen, but it tends to increase copper loss and negate any decrease in core loss from a larger core. Cables or foils with larger cross section area can be used. However, the same foil or cable is used for different cores in this design for a fair comparison. The resultant design with the amorphous core has higher leakage inductance and parasitic capacitance than the cores with the

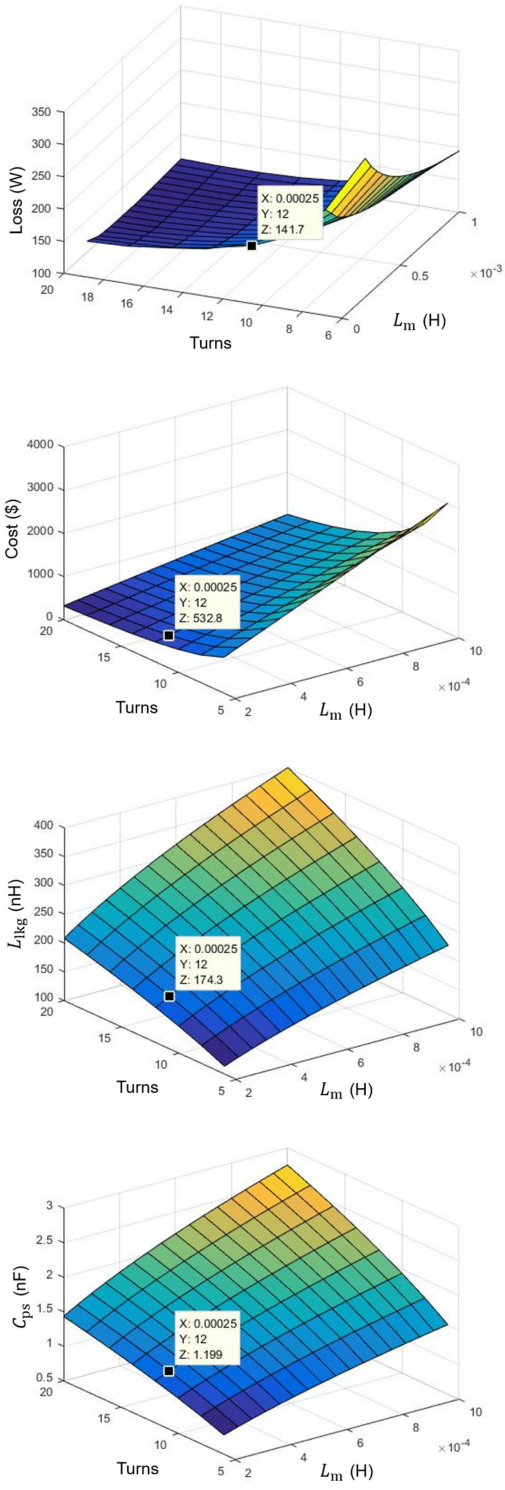


Fig. 12. Transformer design with the nanocrystalline core under different number of turns and different magnetizing inductance.

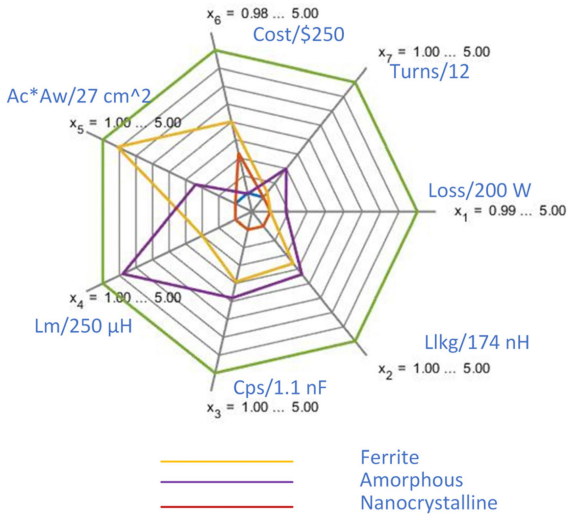


Fig. 13. Comparison of transformer design with different core materials.

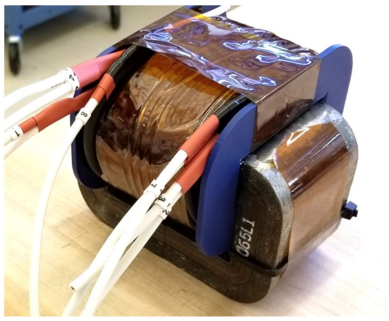


Fig. 14. A 25-kVA 16-kHz medium-frequency transformer prototype.

ferrite and the nanocrystalline. The nanocrystalline-based design is better than the ferrite-based design across all parameters.

As shown in Fig. 12, for a nanocrystalline design with 12/48 LV/MV turns, $L_{\rm m} = 250\ \mu$H is selected to be the optimal design. Accordingly, the SC2065M1 core has been selected to meet the design requirements. The image of the built 25–kVA, 16-kHz transformer is shown in Fig. 14. The winding consists of four layers with 12-MV turns in each layer. The co-axial winding has a natural turns ratio of 1:1. To achieve a turns ratio of 4:1, the outer insulation and the braid are split at the ends of each layer and are connected in parallel. It is important to note that at no point, MV insulation is disturbed. This approach simplifies MV termination issues and allows attaining basic impulse levels in a much simpler way. The transformer is tested to verify the design. The theoretical values and the measured values are shown in Table III.

C. Resonant Circuit Design

The objective of the resonant circuit design is to achieve the ZVS with appropriate controlled dv/dt and small lost duty cycle during the ZVS transition state and the resonant state. There are two resonant branches across both sides of the transformer.

TABLE III
VERIFICATION OF TRANSFORMER DESIGN BASED ON THE NANOCRYSTALLINE CORE

Parameter	Theoretical	Measured
Magnetizing inductance ($L_{\rm m\_LV}$)	250 µH	270 µH
Leakage inductance ($L_{\rm leakage\_LV}$)	270 nH	343 nH
Saturation current	130 A	110 A

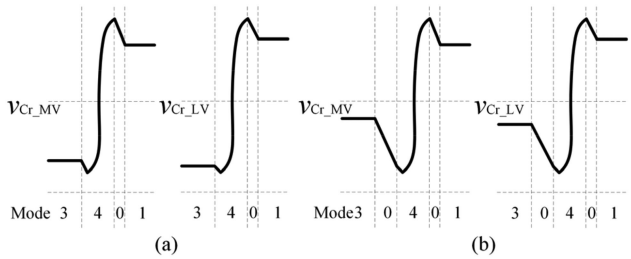


Fig. 15. Resonant-capacitor-voltage discharge control for the full-range ZVS under the LV-to-MV power flow direction. (a) Mode 3 voltage (absolute value) is larger than mode 1. (b) Mode 3 voltage is smaller than mode 1 and additional mode 0 is needed. A ZVS transition state (mode 0) can be inserted in (b) before the resonant state (mode 4) to ensure that the resonant capacitor voltage at the end of the resonant state is higher than the voltage level in mode 1.

Each resonant branch consists of a resonant capacitor, a resonant inductor, and a resonant switch.

The resonant capacitors are among the key components to ensure the ZVS. During a switching cycle, the resonant-capacitor voltages are controlled to traverse from the space vectors corresponding to the most positive voltage level to that corresponding to the most negative voltage level. At the end of the switching cycle, the resonant state is initiated. Before the resonant state, the resonant capacitor voltages should be replenished to a proper negative voltage level in Fig. 15, if the absolute value of the voltages in mode 3 is not larger than mode 1's voltages. In other words, as shown in Fig. 15(b), during the additional mode 0, the resonant capacitor can be further discharged, if needed, to achieve the full-range ZVS. Then, after the resonant state, the resonant capacitor is always reset to a positive enough voltage which is higher than the incoming space vector's voltage for the ZVS.

The circuit schematic and the sign convention under the resonant state are illustrated as mode 4 in Fig. 2, which essentially involves the resonances between the MV-side resonant capacitor $C_{\rm r\_MV}$ and the MV-side resonant inductor $L_{\rm r\_MV}$, and between the LV-side resonant capacitor $C_{\rm r\_LV}$ and the LV-side resonant inductor $L_{\rm r\_LV}$. The MV and the LV resonant capacitors and inductors are sized to conform to the transformer turns ratio, which means that the converter structure is symmetrical in per-unit sense. Therefore, for simplicity, half of the circuit works, i.e., either the MV-side resonance or the LV-side resonance, are analyzed. In other words, in the differential equations of the resonant state in (25) and (26), the state variables $v_{\rm Cr}$ and $i_{\rm Lr}$ would yield their MV-side values if the parameters $L_{\rm r}$ and $C_{\rm r}$ and the initial value $V_{\rm Cr}$ are referred to the MV-side of the

transformer and plugged into the following:

$$\begin{cases} v_{\mathrm{Cr}} = -L_{\mathrm{r}} \frac{di_{\mathrm{Lr}}}{dt} \\ i_{\mathrm{Lr}} - I_{\mathrm{m}}/2 = C_{\mathrm{r}} \frac{dv_{\mathrm{Cr}}}{dt} \end{cases} \tag{25}$$

$$\begin{cases} i_{\mathrm{Lr}(t=0)} = 0 \\ v_{\mathrm{Cr}(t=0)} = V_{\mathrm{Cr}} \end{cases} \tag{26}$$

Subsequently, the resonant time, the peak voltage of the resonant capacitor, and the peak current of the resonant inductor can be calculated by

$$T_{\mathrm{r}} = \sqrt{L_{\mathrm{r}} C_r} \left(2\pi - \arcsin \left(\frac{\sqrt{{I_{\mathrm{m}}}^2 {V_{\mathrm{pk}}}^2 C_{\mathrm{r}}/L_{\mathrm{r}}}}{{I_{\mathrm{m}}}^2/4 + {V_{\mathrm{pk}}}^2 C_{\mathrm{r}}/L_{\mathrm{r}}} \right) \right) \tag{27}$$

$$V_{\mathrm{Cr,pk}} = \sqrt{{V_{\mathrm{Cr}}}^2 + (I_{\mathrm{m}}/2)^2 L_{\mathrm{r}}/C_{\mathrm{r}}} \tag{28}$$

$$I_{\mathrm{Lr,pk}} = I_{\mathrm{m}}/2 + \sqrt{(I_{\mathrm{m}}/2)^2 + {V_{\mathrm{Cr}}}^2 C_{\mathrm{r}}/L_{\mathrm{r}}} \tag{29}$$

where I_{m} is the magnetizing current, C_{r} is the resonant capacitance, L_{r} is the resonant inductance, V_{pk} is the peak voltage of the input and output, and V_{Cr} is the resonant capacitor voltage at the beginning of the resonance.

With the above adaptive resonant-capacitor-voltage control and the analytical results of the resonant state, selection of the resonant capacitor is determined by the following criteria. First, dv/dt should be appropriate to reduce switching loss and mitigate the EMI issue from the SiC devices. Second, the time lost in the resonant state in (27) and the ZVS transition state in (30) should be small and the effective duty cycle in (31) should be large enough. Third, the resonant-capacitor peak voltage stress in (28) should be within main devices' voltage rating. Selection of the resonant inductor is mainly determined by the small resonant time in (30) for large effective duty cycle because the resonant state is only activated once per switching cycle and the peak current stress on the resonant switch in (29) is generally not a concern

$$T_{\mathrm{ZVS}} = \frac{2V_{\mathrm{pk}}}{dv/dt} = \frac{2V_{\mathrm{pk}}}{I_{\mathrm{m}}/2C_{\mathrm{r}}} \tag{30}$$

$$D_{\mathrm{eff}} = 1 - (T_{\mathrm{r}} + T_{\mathrm{ZVS}})/T_{\mathrm{s}}. \tag{31}$$

The leakage inductance of the transformer can play a significant role in the voltage stress of the resonant capacitor, which should be verified through simulation or worst-case calculation in [38]. Considering all the trade-offs involved, the parameters selected are shown in Table IV, where the MV-side and the LV-side quantities conform to the 4:1 transformer turns ratio.

D. Power Supply for MV-Device Gate Drivers

The MV-bridge devices and the associated driver circuits need to be isolated from each other and from the ground. The control signal sent to the gate driver and the power supply energizing the drivers have to be isolated, both between the controller and drivers and between the drivers. The control signal is sent to the gate drivers via fiber optic cables for the required isolation. The power supply isolation is provided by the high-frequency power supply shown in Fig. 16. Power is transferred to individual gate drivers through a 50-kHz current loop driven by a half-bridge inverter. The current loop passes through pick-up current transformers coupled to each of the gate drivers. The high-frequency power is then rectified on the gate driver side to generate appropriate dc voltages for driving the MV device modules. The insulation of the single-turn primary-side cable of the transformers in Fig. 17 is selected to be 15 kV.

TABLE IV
DESIGNED RESONANT CIRCUIT PARAMETERS OF THE 25 KVA, 2.5 KV DC M-S4T CONVERTER MODULE

Parameter	MV side	LV side
Resonant capacitor (C_{r})	6.25 nF	100 nF
Resonant inductor (L_{r})	80 μH	5 μH
Dv/dt	2 kV/μs	500 V/μs
Resonant time (T_{r})	3.5 μs	
ZVS transition time (T_{ZVS})	2.8 μs	
Effective duty cycle (D_{eff})	90%	

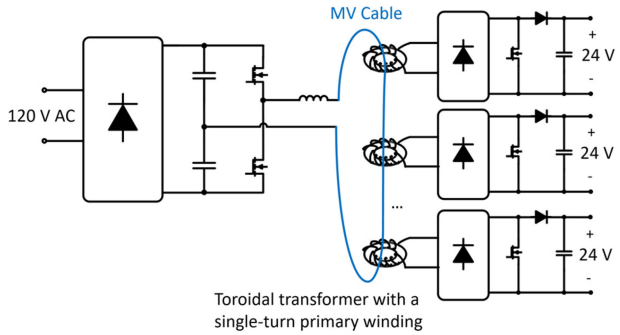
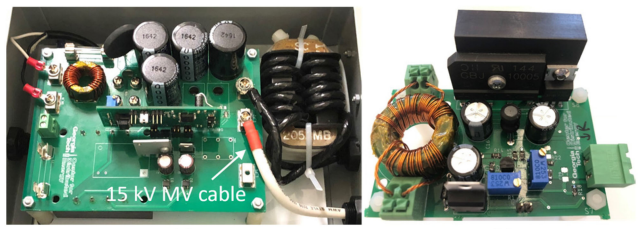


Fig. 16. High-isolation power supply for MV-device gate drivers.



(a) (b)

Fig. 17. High-isolation power supply prototype. (a) Conversion stage on the primary side. (b) Conversion stage on the secondary side with the toroidal core.

E. 25-kVA Converter Modules

The image of two 25 kVA M-S4T modules is shown in Fig. 18. For this article, a control board based on FPGA (Cyclone IV EP4CE75F23C7) and DSP (TMS320C6713B) is used to control the two modules simultaneously. Note that inside the control board, the control codes of the two controllers for the two modules are separate and one do not need to communicate with the other for the other's duty cycle information. Moreover, the control method can be implemented in a distributed fashion with each modules having its own controller as demonstrated in [12].

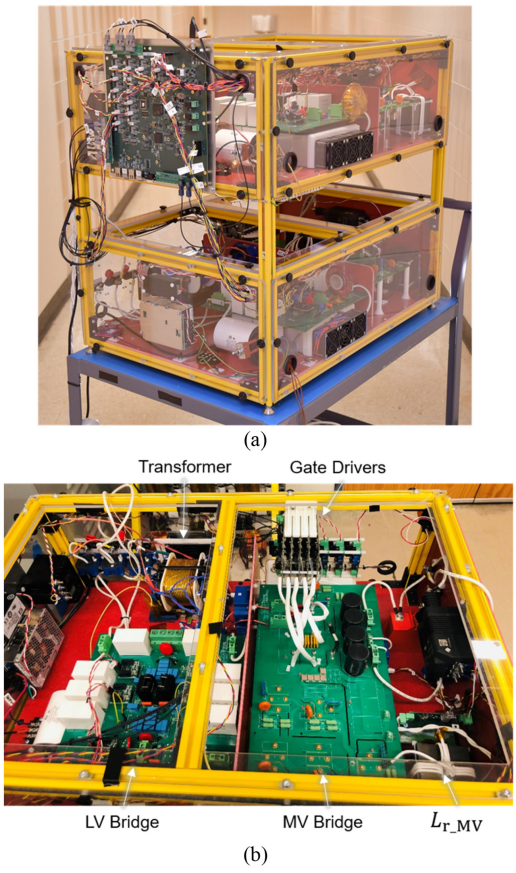


Fig. 18. (a) Two 25-kVA 2.5-kV dc modular soft-switching solid-state transformer (M-S4T) modules. (b) Zoomed single-module photo.

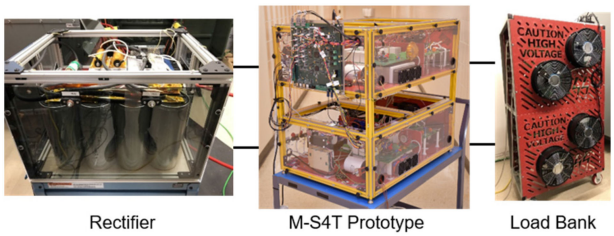


Fig. 19. Experimental setup for the soft-switching solid-state transformer (M-S4T) modules.

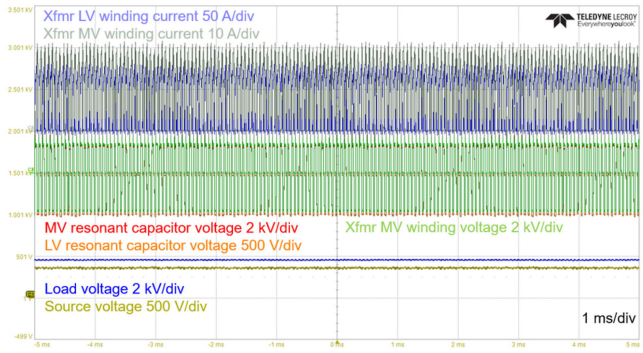


Fig. 20. Single-module experimental waveforms at about 2 kV, 10 kW of the modular soft-switching solid-state transformer (M-S4T) prototype.

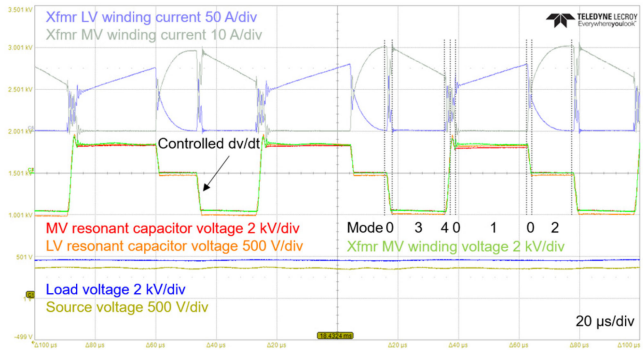


Fig. 21. Switching-cycle single-module waveforms at about 2 kV, 10 kW.

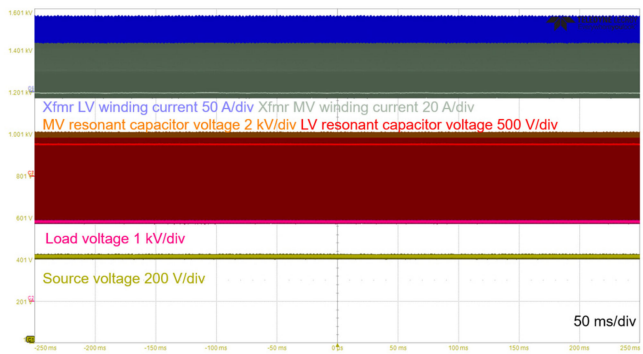


Fig. 22. Single-module experimental waveforms at about 2 kV, 14 kW of the modular soft-switching solid-state transformer (M-S4T) prototype.

V. Experimental Results

A 50–kW, 5-kV dc to 600 V dc setup has been built to test the prototype. The image of the test setup is shown in Fig. 19. An LVdc rectifier feeds the LV-side of the converter, while the MV-side is connected to a resistor load bank. With this setup, power flow from LVdc to MVdc is tested. In other words, load voltage is the MV output voltage, i.e., v_{MV1} in Fig. 1(b) for module 1, and source voltage is the LV input voltage, i.e., v_{LV} in Fig. 1(b).

The single-module test results at about 2 kV 10 kW and 2 kV 14 kW are shown in Figs. 20–23, respectively. From Figs. 20 and 22, it can be observed that the load voltage is smooth and steady. The dc-link current, i.e., the magnetizing current, whose envelope is indicated by the LV and the MV transformer winding currents, is regulated about its reference value. In Fig. 21, the operating modes of the converter within a switching cycle are labeled with the same nomenclature as the conceptual waveforms in Fig. 3. Agreeing with the conceptual waveforms, the magnetizing current, which is the sum of the LV and MV winding currents, is increased in mode 1 to store energy and is decreased in mode 3 to deliver energy to the output in Fig. 21. Also, the magnetizing current is almost constant in mode 2 during the freewheeling state. The resonant capacitors are discharged with falling voltages in mode 0 and charged in the

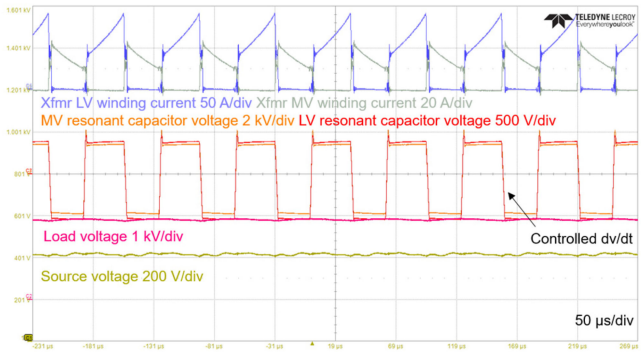


Fig. 23. Switching-cycle single-module waveforms at about 2 kV, 14 kW.

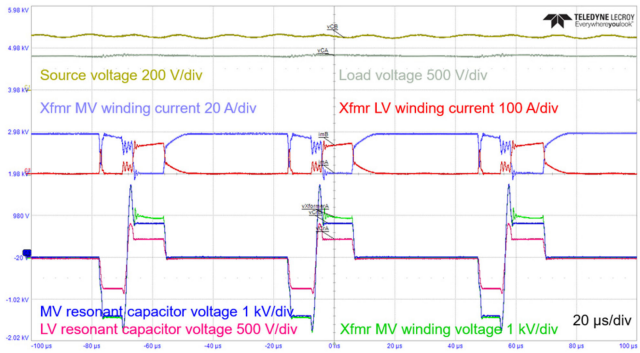


Fig. 25. Switching-cycle single-module waveforms at about 1.5 kV, 2 kW.

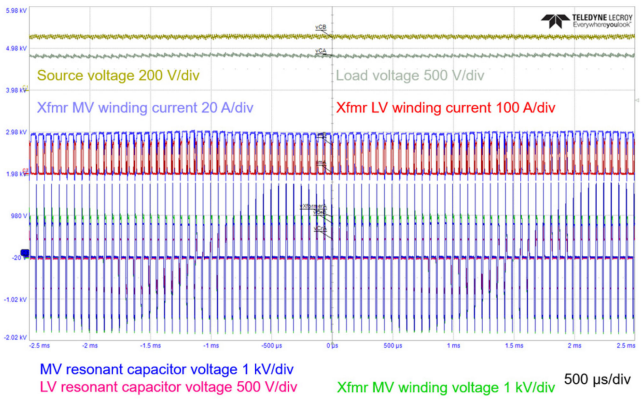


Fig. 24. Single-module experimental waveforms at about 1.5 kV, 2 kW of the modular soft-switching solid-state transformer (M-S4T) prototype.

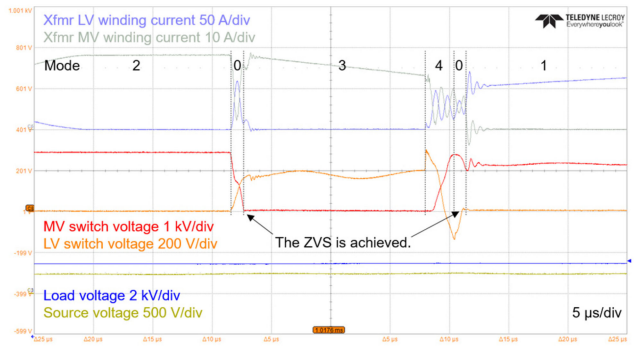


Fig. 26. Switch voltage measurements to verify the ZVS and the controlled dv/dt across the reverse-blocking switches.

resonant state, mode 4. The dv/dt across the resonant capacitors in Figs. 21 and 23 is controlled to be less than the designed value in Table IV. In the test, the MV switches corresponding to the MV vector when the magnetizing inductance delivers energy to the MV load are kept ON during the resonant state. It can reduce the voltage stress from $L_{\rm r}$ and $C_{\rm r}$ resonance in mode 4 of Fig. 2. Therefore, the peak stresses on the resonant capacitors in Figs. 21 and 23 are roughly equal to the peak input and output voltages. It should be noted that in Fig. 23, the dwelling time of the freewheeling state, i.e., the zero vector, is reduced to almost zero to minimize the dc-link current for high efficiency. Therefore, the duration when the resonant capacitor voltages are zero is very small in Fig. 23. The single-module test results at about 1.5 kV 2 kW in Figs. 24 and 25 further verify the performance of the proposed SST under a light load condition, where the operation principles and the controlled dv/dt can be similarly validated.

Fig. 26 verifies the ZVS and the controlled dv/dt across the switches. In Fig. 26, the MV switch refers to Sobp while the LV switch refers to Siap in Fig. 2. In mode 1, the LV source energizes magnetizing inductance and increases the magnetizing current, when the LV switch Siap conducts and has a voltage close to zero in Fig. 26. As illustrated in Fig. 2, the freewheeling switches are Soap, Soan, Siap, and Sian, which is why the LV switch Siap conducts and the MV switch Sobp blocks during mode 2 in Fig. 26. During mode 3 in Fig. 26, the MV switch Sobp conducts so that energy can be delivered from the magnetizing inductance to the MV output. In Fig. 26, if the switch is not turned ON under zero voltage, there will be a sharp glitch on the voltages across the switches at turn ON due to much larger dv/dt under hard switching than the dv/dt controlled by the resonant capacitors, i.e., $<$ 2 kV/μs for the MV switch and $<$500 V/μs for the LV switch. The waveforms in Fig. 26 are clean and the dv/dt across the device is always controlled at turn ON, verifying that the ZVS is achieved. Switch current is not measured due to the difficulty to install the current probe with existing layout for low parasitic inductance. To summarize, the single-module test verifies the ZVS and the controlled dv/dt of the M-S4T and the control method for single-module operation.

The LV resonant switch voltage $v_{\rm total\_LV}$ in Fig. 10 is measured in Fig. 27. Although the undamped oscillations lead to additional stress at the end of the resonant state, this stress is resolved with the 2-pu series-connected diodes inside the resonant switch and the snubber design. Fig. 28 illustrates the reverse-blocking module voltage $v_{\rm module\_MV}$ and the additional discrete diode voltage $v_{\rm diode\_MV}$ in the MV resonant switch whose sign convention follows Fig. 10. When the resonant-capacitor voltage is negative, the MOSFET in the module blocks and hence $v_{\rm module\_MV}$ and $v_{\rm diode\_MV}$ have a positive voltage and a zero voltage, respectively. When the resonant-capacitor voltage is positive, the diode in the module and the discrete diode block and hence $v_{\rm module\_MV}$ and $v_{\rm diode\_MV}$ are sharing the voltage. As discussed, because the diode dies in the module

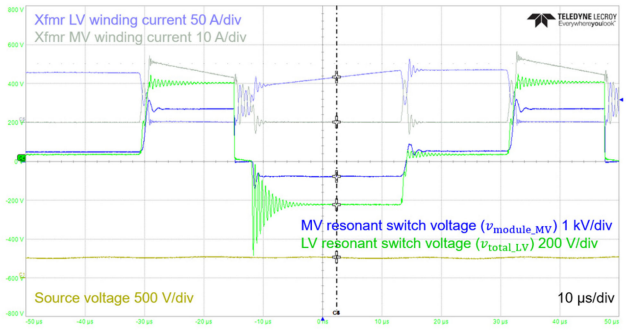


Fig. 27. Switch voltage measurements of the LV resonant switch and the MV resonant switch.

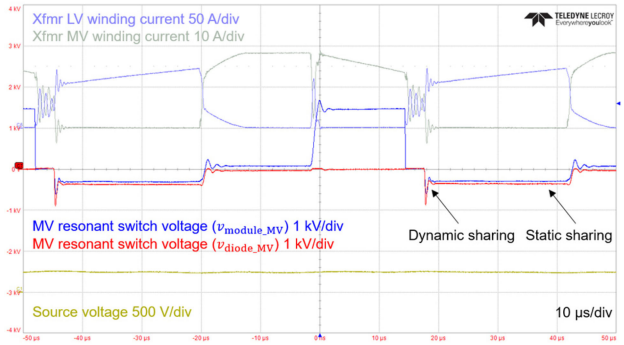


Fig. 28. Switch voltage measurements of the MV resonant switch at about 1.5 kV.

and in the discrete package are different, there is a ∼10% static sharing mismatch which is acceptable considering that the equivalently 2-pu diodes are used. In terms of dynamic sharing and voltage stress, first, the oscillations are damped out quickly with the appropriate snubber resistor selection and the snubber capacitance which is roughly seven times diode capacitance. Second, there are some dynamic voltage mismatches because of the different dies. Third, the voltage overshoot is more than 170% because the snubber capacitance limited by the snubber loss is still not large enough [45]. However, while the snubber capacitance is limited by power dissipation and cannot be further increased, the 2-pu diodes have been used to stand and address the above voltage stress.

A two-module steady-state stacking operation can be observed in Fig. 29 at 4 kV 20 kW. In Fig. 29, the output voltages of modules 1 and 2 are steady and balanced. Moreover, the magnetizing currents of both of the modules are controlled about the reference. In Fig. 30, the switching-cycle waveforms under the stacking test show that the two modules are interleaved with each other by half of a switching cycle. Dynamic balancing capability of the M-S4T is verified in Fig. 31. In the beginning, the voltage-balancing function is disabled and the two stacking capacitor voltages are different, i.e., approximately 900 V for module 2 and 1 kV for module 1. Then, the balancing function is enabled. It can be observed that the module 1's voltage and the module 2's voltage quickly become balanced without any overvoltage. To summarize, the stacking-module test verifies

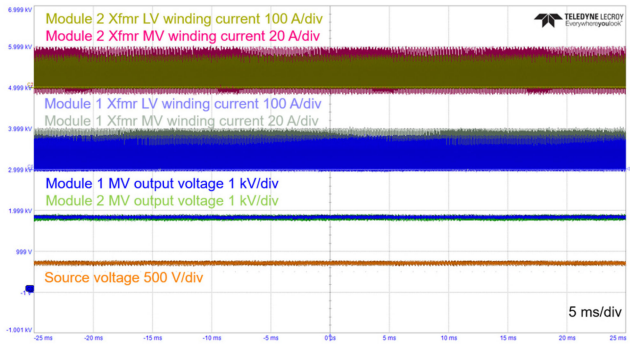


Fig. 29. Interleaved two-module stacking test at 4 kV, 20 kW of the modular soft-switching solid-state transformer (M-S4T) prototype.

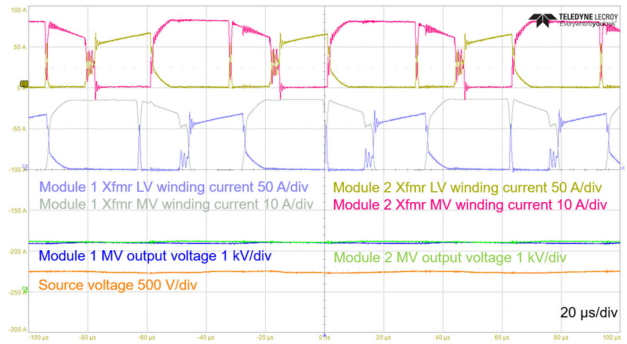


Fig. 30. Switching-cycle interleaved two-module waveforms.

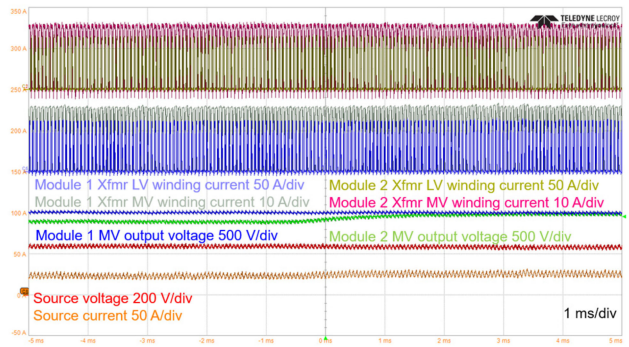


Fig. 31. Stacked-side voltage balancing test. The voltage balancing function is enabled approximately in the middle of the waveforms.

the steady-state interleaved operation and the dynamic balancing function of the MPPS control, which is critical for reliable and safe operation of the M-S4T.

The measured efficiency from Yokogawa WT 1806E power analyzer and the estimated efficiency at different operating points are shown in Fig. 32. The estimated peak efficiency in Fig. 32 is 97.5% at 20 kW, 600 V to 2.5-kV conversion. The estimated power loss breakdown at 13 kW 420 V to 2-kV conversion is illustrated in Fig. 33. The LV-device conduction loss accounts for more than 50% of the total loss. In fact, the major obstacle to further improve the efficiency is the lack of

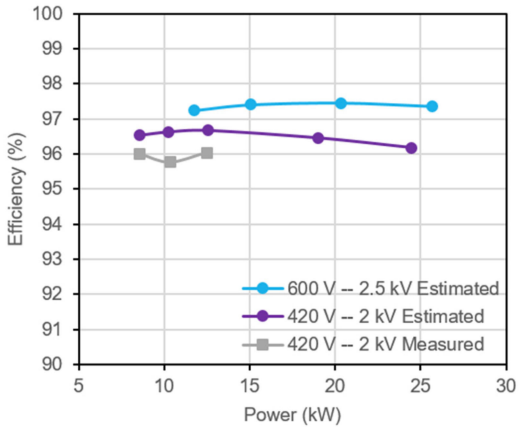


Fig. 32. Efficiency measurement and estimation of the modular soft-switching solid-state transformer (M-S4T) prototype.

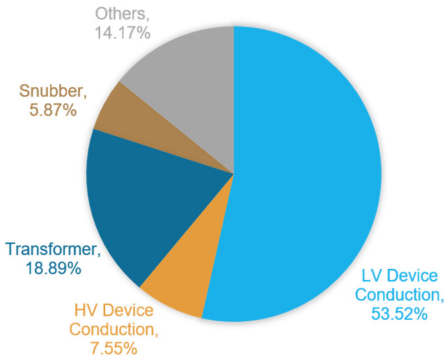


Fig. 33. Estimated loss breakdown at 13 kW, 420 V to 2 kV conversion. Other losses include resonant inductor loss, device switching loss, resonant capacitor loss, filter capacitor loss, etc.

commercially available 1.2-kV high-current-rating SiC reverse-blocking modules to decrease the conduction loss.

VI. Comparison

The proposed MV dc transformer (DCT) is compared in Table V against the conventional DCT solution, i.e., the DAB for MVdc–LVdc conversion followed by a hard-switching voltage-source inverter for additional LVac–LVdc conversion. The proposed topology can achieve a single-stage conversion for LVdc output or LVac output, while the conventional solution needs an additional inverter for the LVac output. The additional inverter also means a large dc-link capacitor and three-phase output filters are needed. By avoiding the bulky dc-link capacitors which are normally electrolytic capacitors, the power density, the operating temperature range, and the reliability of the converter can be improved.

For soft-switching capability, the proposed converter can achieve full-range ZVS by adaptively controlling the resonant capacitor voltage before the resonant state as shown in Fig. 13. The DAB in the conventional solution has limited-range ZVS [18]–[19] and the inverter is normally hard-switched. The dv/dt in the proposed converter is controlled by the resonant capacitor,

TABLE V
Comparison Between the Proposed Modular S4T and Other Solutions

	Proposed Modular S4T	DAB + Inverter for MVDC-LVAC
Number of Conversion Stages	DC-DC: 1. DC-AC: 1.	DC-DC: 1. DC-AC: 2.
Large DC-Link Capacitor	No.	DC-DC: No. DC-AC: Yes.
Soft Switching	Full-range ZVS.	DAB: Limited-range ZVS. Inverter: Hard switching.
Dv/dt	Low, ~2 kV/μs, controlled by *Cr*.	DAB: Low, if within the ZVS range. Inverter: High, > 50 kV/μs, uncontrolled.
Dead Time	No.	Yes. Shoot-through protection is needed.
Short-Circuit Current Limiting	Inherent.	No. Very fast desaturation protection is needed.
Modularity	Yes.	Yes.

while the DAB only has controlled dv/dt within its ZVS range and the inverter's dv/dt is uncontrolled. The uncontrolled dv/dt of MV SiC devices can be as high as 100 kV/μs [16], [17]. The reduced dv/dt in the proposed converter can reduce the EMI [27]–[29].

From robustness point of view, the proposed S4T is a current-source converter (CSC), which has better fault tolerant capability than the voltage-source converter [54]–[55]. For example, dead time needs to be added to the switches in a half bridge for the conventional voltage-source solution to prevent shoot-through. For a CSC, the dead time is not needed. Moreover, the CSC has inherent short-circuit current limiting from the dc-link inductor [55]. In the conventional solution, if a short-circuit happens, the dc-link capacitor voltage can cause fast current rise through the switches and timely desaturation protection is needed in the gate driver. The device turn-OFF speed in the desaturation process needs to be carefully controlled to avoid parasitic-inductance-induced voltage spikes, which is especially more challenging for MV SiC devices [16]. Also, in the conventional solution, the dc-link capacitor's inrush current needs to be managed during start-up and fault conditions [56]. Furthermore, the soft-switching technique in the S4T with reduced dv/dt and EMI can help to mitigate the operation noise injected into the gate driver, controller, peripherals, etc., and decrease the gate-source voltage oscillation during device switching [44].

Finally, both the proposed S4T and the conventional solution can scale to higher voltage and higher power and improve reliability by adopting a modular structure with optional redundant modules.

VII. Conclusion

This article presents the design and the implementation of a 5-kV bidirectional universal modular soft-switching solid-state transformer (M-S4T) for MVdc grids. This single-stage topology for MVdc–LVdc and MVdc–LVac conversion and the operation principle are described. The M-S4T has potentially reduced EMI from controlled dv/dt and full-range ZVS capability. With a novel MPPS control method, voltage balancing between the stacked converter modules under the steady-state and the dynamic conditions is achieved. A coaxial-cable-based MV MFT prototype has been built to achieve very low leakage inductance (0.13%) and 15-kV insulation at the same time. The experimental results at 4 kV verify the abovementioned concepts. Significantly, MV experimental results of a modular bidirectional dc–dc transformer with each cell achieving MVdc and connected ISOP for MVdc–LVdc conversion are rarely covered in the literature and reported in detail, in this study, for the first time, to the authors' best knowledge.

Acknowledgment

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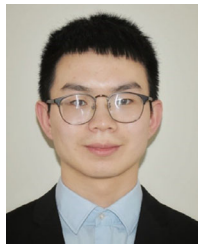

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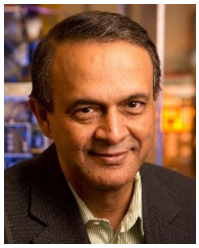

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