Resilient Operation of an MMC With Communication Interruption in a Distributed Control Architecture

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***Abstract*—Modular multilevel converters (MMCs) in high-voltage dc applications usually adopt a distributed control architecture to manage a large number of submodules (SMs) through a communication network. The communication congestion and network disconnection might lead to communication interruption (CI) and eventually cause the system to malfunction. In this article, a resilient operation strategy is proposed and studied to ride-through the CI fault, in order to prevent frequent fault SM bypassing, replacement, or even system shutdown. The analysis of the MMC distributed control system with the presence of CI indicates that the insertion index of the faulted SM might become constant, which distorts the output current and results in overvoltage of the communication interrupted SM (CI-SM). The CI-SM capacitor voltage prediction can be used to determine the MMC safe operation period after CI occurs. During the safe operation period, the CI-SM power balance is sustained by utilizing prestored phase signals to generate a sinusoidal insertion index according to its capacitor voltage tracking error. Two operation modes are proposed and analyzed to ensure the MMC stable operation under various conditions. The system protection is sensibly used only if the CI duration exceeds a safe operation period, which avoids frequent SM cut-off. Good agreement of the CI-SM capacitor voltage is achieved between the theoretical and simulation results. The effectiveness and robustness of the proposed MMC resilient operation are experimentally confirmed.**

***Index Terms*—Communication interruption (CI), distributed control, modular multilevel converters (MMCs), resilient operation.**

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I. Introduction

MODULAR multilevel converter (MMC) is one of the most promising topologies in recent years for medium- or high-voltage industrial applications, such as high-voltage dc transmission (HVdc), medium-voltage microgrids, and medium-voltage motor drives [1]–[6]. The wide adoption of MMCs in industry is mainly due to their modularity, flexible expandability, common dc bus, etc. In HVdc applications, hundreds of submodules (SMs) are typically required for the MMCs to handle a high-voltage level (hundreds of kilovolts) with relatively low-voltage power devices. In favor of properly manipulating such large numbers of SMs, distributed controls for MMCs are proposed in [7], [8], in order to distribute the heavy computational burden into different digital controllers. In the distributed structures, control messages are exchanged between the central and local controllers through the communication network [7]–[12]. However, communication failure during the data transmission [e.g., network congestion and communication interruption (CI)] is an inherent problem along with the distributed control structures for MMCs. The communication failure obstructs the data transmission between the central and local controllers, invalidating the central controller command, and might eventually cause the overall MMC system to malfunction.

In recent years, communication technologies for multilevel converters with distributed control systems have been investigated [12]–[15], while the communication reliability is a pending issue coming with the distributed network for the MMC system due to its massive communication links. The basic characteristics of the MMC communication network, which include the transmission media, synchronization accuracy, and network topology, are investigated in [15]. It indicates that the network topology has a strong impact on the network delay and the tolerance to failures. In [16], an additional leakage thyristor valve is applied in the LCC–MMC hybrid HVdc system in order to avoid the high-voltage stress of the short-fault SMs in the communication failure condition. A fail-safe operation scheme is designed for the MMCs in [17], where the failure of slave controllers or SMs can be recognized in the communication break scenario by continuously checking the incoming data of the master controller. A fault-tolerant control architecture based on MMC distributed systems is presented in [18], in which a set of controllers are endowed with the capabilities to be the master controller and each controller in the control array is linked to

the nearby controllers to improve the communication network redundancy. According to the previous research, the CI fault in an MMC system would terminate the data exchange among controllers and might cause system failure. To the best of our knowledge, existing solutions for MMC CI fault mostly focus on the postfault operation. The network timeout method is mentioned in [18] to detect the failure in the controller modules. However, it is quite tricky to affirm a timeout in a real-time control system for the sake of an equilibrium between the effective protection and avoiding frequently triggering the fault alarm. Although redundant SMs are conventionally equipped in MMC system and can be simply switched-in during communication failure, the MMC resilient operation should be designed to ride-through the temporary CI faults avoiding frequently precharging, inserting/bypassing redundant SMs [19], and replace the SMs having possibly permanent faults with redundant ones.

In this article, a resilient operation scheme, which ensures the safe and stable operation of the system after CI appears, is proposed according to theoretical analysis of the distributed controlled MMC performance with an SM CI fault. The analysis reveals that the interaction between the constant communication interrupted SM (CI-SM) insertion index and the additional dc component in the output current result in the CI-SM capacitor voltage ascent. The steepest CI-SM voltage ascent and the capacitor voltage safe margin are employed to determine the maximum allowable system operation period after CI occurs, which is used as the criterion to wisely classify the temporary and permanent communication network faults. During the allowable system operation period, the proposed resilient operation scheme utilizes prestored reference phase angle to implement the sinusoidal CI-SM insertion index, which stabilizes the SM capacitor voltage. The system would recover as long as the temporary CI fault is cleared. The resilient operation applying either stored output voltage or output current phase angles is discussed and compared in terms of the capacitor voltage deviation and the voltage balancing capability. The proposed resilient operation with MMC output reference amplitude and phase variation during the CI is investigated to reveal the restraints for a critical reference step change. Moreover, if the CI duration exceeds the maximum allowable operation period, a permanent network fault will be affirmed by the system and protecting actions are implemented to decently cut the CI-SM off from the MMC main circuit. Simulation and experimental results are presented to verify the analytical findings. The effectiveness of the proposed resilient operation under both voltage and current phase conditions is verified on an MMC prototype.

II. MMC Distributed Control Architecture

The basic structure and operation principles of an MMC with distributed control have been extensively explained in the literature [7], [20] and will not be discussed in this article. The schematic diagram of a three-phase MMC is shown in Fig. 1. N half-bridge SMs are connected in series in one arm. Each arm is equipped with an arm inductor $L_{\rm arm}$ and an equivalent resistor $R_{\rm arm}$. The three-phase output voltages and currents of the MMC

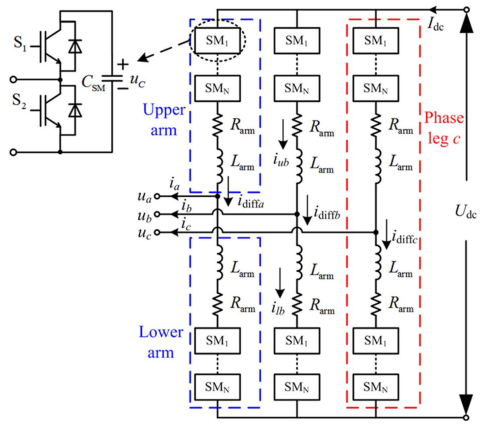

Fig. 1. Structure of a three-phase MMC.

are expressed as

$$\begin{cases} u_{ox} = U_o \cos(\omega_o t + \varphi_{ox}) \\ i_{ox} = I_o \cos(\omega_o t + \varphi_{ox} + \varphi_L) \end{cases} \tag{1}$$

where $x \in (a, b, c)$, U_o and I_o are the amplitudes of u_{ox} and i_{ox}, respectively, ω_o refers to the fundamental angular frequency, φ_{ox} denotes the phase angle, and φ_L stands for the phase displacement between the output voltage and current. The differential current in phase leg x is defined as

$$i_{{\rm diff}x} = I_{\rm dc} + i_{{\rm cir}x} \tag{2}$$

where $I_{\rm dc}$ is a dc current that maintains the power balance between the dc and ac sides of the MMC [3], [21], and $i_{\rm cirx}$ is the circulating current ripple, which is dominated by the second-order harmonic [20]. The arm currents can be written as

$$\begin{cases} i_{ux} = i_{{\rm diff}x} + 0.5 i_{ox} \\ i_{lx} = i_{{\rm diff}x} - 0.5 i_{ox}. \end{cases} \tag{3}$$

Assuming the SM capacitor voltages are well-balanced, the normalized insertion index of the kth SM in the upper and lower arms can be obtained as

$$\begin{cases} n_{ukx} = 0.5\,(1 - u_{ox}{}^*) \\ n_{lkx} = 0.5\,(1 + u_{ox}{}^*) \end{cases} \tag{4}$$

where $u_{ox}{}^* = 2u_{ox}/U_{\rm dc}$.

The structure of the distributed control architecture for the MMC is illustrated in Fig. 2, where the control tasks are assigned to different controllers, i.e., a central controller and local controllers in SMs [7]. The central controller mainly coordinates and manages the overall operation of the MMC. The output current control is implemented in the central controller with measured arm currents within each control cycle. The reference of the SM capacitor voltage $u_C{}^*$ is calculated by the central controller according to the dc bus voltage and operation requirements of the MMC, e.g., in normal operation, in start-up process [7], or in fault-tolerant operation [22]. The local controller deals with the internal dynamics, PWM generation, and immediate protections [22] of the SM. It measures the capacitor voltage of the corresponding SM for voltage control and regulates the differential

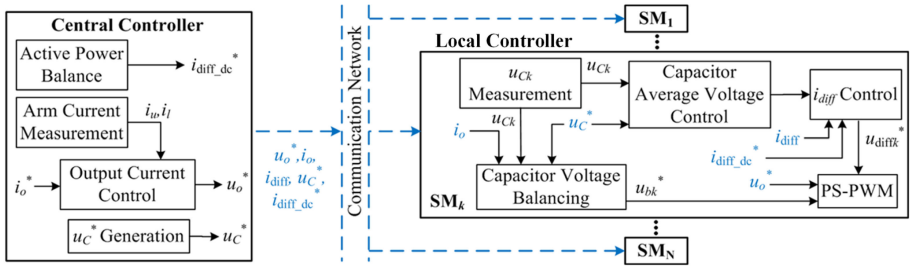

Fig. 2. Distributed control structure of the MMC.

current of the MMC. The phase-shifted PWM scheme [23], [24] is adopted in the distributed control architecture. A phase-shifted triangular carrier is generated in each local controller. Necessary information is exchanged between the central and local controllers through a communication network. One message containing $u_{ox}{}^*$, $i_{\mathrm{diff\_dc}}{}^*$, i_{ox} and $i_{\mathrm{diff}x}$, which conveys adequate information for the real-time control in local controllers, is broadcasted by the central controller through the communication network in each control cycle. After receiving the message, an interrupt will be generated to enable the closed-loop control of each local controller in the same control period.

If CI happened, the corresponding local controller detects the fault once it cannot receive the message from the central controller on time. It should be noted that CI might be introduced by the network congestion lasting only for a few control cycles or by permanent network disconnection. Therefore, it is not practical to shut down the MMC system as soon as the occurrence of CI. Resilient protection and operation schemes under these circumstances have to be elaborately designed to prevent severe malfunctions or catastrophic damages of an MMC system without frequent operation interruptions.

III. Analysis of MMC Performance With Communication Interruption

In the case of CI, the local controller of CI-SM is not able to receive the real-time control information from the master controller, which invalidates the local closed-loop control of CI-SM. The gating signals of CI-SM would be generated according to the insertion index calculated right before the occurrence of CI. Attention should be paid that the gating signals of the CI-SM become constant-duty-cycle square waves instead of SPWM waveforms, which greatly deteriorate the MMC performance. In this section, a single-phase MMC inverter is adopted to investigate the MMC performance with square-wave gating signals for one SM located in the lower arm, corresponding to a CI occurring at t_{CI}. The analytical results can be utilized to determine the action instant of the proposed MMC CI protection.

A. Arm Voltage After CI

According to [25], [26], the output voltage of the ith SM in the lower arm, i.e., u_{li} is obtained as

$$u_{li} = \frac{U_{\mathrm{dc}}}{2N} + \frac{MU_{\mathrm{dc}}}{2N}\cos(\omega_o t + \varphi_o) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2U_{\mathrm{dc}}}{m\pi N}\times\sin\left[\frac{(m+n)\,\pi}{2}\right]\times J_n\left(\frac{Mm\pi}{2}\right) \times\cos\left\{m\left[\omega_c t + (i-1)\,\frac{2\pi}{N}\right] + n\,(\omega_o t+\varphi_o)\right\} \tag{5}$$

where $M = 2U_o/U_{\mathrm{dc}}$, ω_c denotes the angular frequency of the triangular carriers, m is the harmonic order of the carrier wave ($m = 1, \ldots, \infty$), n is the harmonic order of the reference ($n = -\infty$, $\ldots$, ∞), and $J_n(x)$ refers to the Bessel coefficient of order n [25].

The output voltage of the CI-SM (e.g., the kth SM in the lower arm, $k \in [1, N]$) around CI instant can be expressed as

$$u_{lk} = \frac{U_{\mathrm{dc}}}{N}n_{\mathrm{CISM}} + \frac{U_{\mathrm{dc}}}{N\pi}\sum_{n=1}^{\infty}\frac{1}{n} \times\left\{\sin(n\pi n_{\mathrm{CISM}}) - \sin\left[2n\pi\left(1-\frac{n_{\mathrm{CISM}}}{2}\right)\right]\right\}\cos(n\omega_c t) \tag{6}$$

where $n_{\mathrm{CISM}} = 0.5 + 0.5M_{\mathrm{CISM}}\cos(\omega_o t_{\mathrm{CI}} + \varphi_o)$ is the insertion index of the CI-SM, t_{CI} is the time instant when CI appears [27]. The voltage of the lower arm near $t = t_{\mathrm{CI}}$ can be derived accordingly

$$u_l = \sum_{i=1}^{N, i\neq k} u_{li} + u_{lk} = Q_1 + Q_2 + Q_3 + Q_4 \tag{7}$$

where Q_1 represents the dc component, Q_2 is the fundamental-frequency component, Q_3 refers to the carrier-frequency components introduced by the CI-SM constant-duty-cycle output square waves, and Q_4 stands for the carrier-frequency components introduced by the remaining healthy SMs as in (8) shown at bottom of this page.

$$\begin{aligned} &Q_1 = \tfrac{(N-1)U_{\mathrm{dc}}}{2N} + \tfrac{U_{\mathrm{dc}}}{N}n_{\mathrm{CISM}},\ Q_2 = \tfrac{(N-1)MU_{\mathrm{dc}}}{2N}\cos(\omega_o t+\varphi_o),\ Q_3 = \tfrac{U_{\mathrm{dc}}}{N\pi}\sum_{n=1}^{\infty}\tfrac{1}{n}\left\{\sin(n\pi n_{\mathrm{CISM}}) - \sin\left[2n\pi\left(1-\tfrac{n_{\mathrm{CISM}}}{2}\right)\right]\right\}\cos(n\omega_c t),\\ &Q_4 = \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\tfrac{2U_{\mathrm{dc}}}{m\pi N}\times\sin\left[\tfrac{(Nm+n)\pi}{2}\right]\times J_n\left(\tfrac{MNm\pi}{2}\right)\times\cos\left\{Nm\left[\omega_c t + (i-1)\,\tfrac{2\pi}{N}\right] + n\,(\omega_o t+\varphi_o)\right\}\\ &\quad - \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\tfrac{2U_{\mathrm{dc}}}{m\pi N}\times\sin\left[\tfrac{(m+n)\pi}{2}\right]\times J_n\left(\tfrac{Mm\pi}{2}\right)\times\cos\left\{m\left[\omega_c t + (k-1)\,\tfrac{2\pi}{N}\right] + n\,(\omega_o t+\varphi_o)\right\} \end{aligned} \tag{8}$$

A. B. Capacitor Voltage of CI-SM

The CI-SM without any control or protection operates in a critical condition, which makes it vital to investigate the operating condition of the CI-SM. Meanwhile, in order to obtain the CI-protection acting time, i.e., the safe operation period after the occurrence of CI at $t_{\rm CI}$, a relatively precise mathematical expression of the CI-SM capacitor voltage is crucial. The scenario that CI fault simultaneously occurs in multiple SMs is investigated in this subsection for the sake of generality.

The capacitor voltages of CI-SMs are assumed the same in a relatively short period after CI. Considering the voltage of any CI-SM at $t_{\rm CI}$ is $U_{\rm dc}/N$, the CI-SM capacitor voltage is yielded as

$$u_{\rm CISM} = \frac{U_{\rm dc}}{N} + \frac{1}{C}\int n_{\rm CISM} \times i_l dt \tag{9}$$

where i_l is the lower arm current.

If the low-frequency harmonics in the differential current have been completely suppressed as in [28], the lower arm current can be written as

$$i_l = I_{\rm dc} - \frac{i_o}{2}. \tag{10}$$

The output power is scarcely influenced in the steady state by CI thanks to the high-bandwidth MMC output control, while it is assumed that a large number of SMs are used and the MMC is not overmodulated. According to the power balance of the single-phase MMC, the active power can be expressed as

$$I_{\rm dc}U_{\rm dc} = U_o I_o \cos\varphi_L = P_o. \tag{11}$$

Combining (1), (10), and (11) with (9), the capacitor voltage of the CI-SM can be derived as

$$u_{\rm CISM} = \frac{U_{\rm dc}}{N} + \frac{1}{C}\int n_{\rm CISM}\left(\frac{P_o}{U_{\rm dc}} - \frac{i_o}{2}\right)dt. \tag{12}$$

According to (12), once CI occurs, the average dc component in the CI-SM capacitor current, which has a major contribution to the deviation of the CI-SM capacitor voltage, is randomly determined by the insertion index calculated in the last control cycle. However, on the account of the capacitor voltage control in normal SMs, the sum of the dc components of all the SM output voltages in one phase is forced to $U_{\rm dc}$:

$$U_{\rm dc} = 0.5\left(N - N_{\rm CI}\right)U_{Cli} + n_{\rm CISM}N_{\rm CI}U_{\rm CISM} + 0.5NU_{Cui} \tag{13}$$

where U_{Cui}, U_{Cli}, and $U_{\rm CISM}$ stand for the dc capacitor voltages of the normal SMs in the upper and lower arms, and the CI-SM, respectively, after the occurrence of CI, and $N_{\rm CI}$ refers to the number of CI-SMs.

At $t = t_{\rm CI}$ instant, the sum of the dc components of all the SM output voltages in one phase differs from the dc-bus voltage due to the CI-SMs. The voltage difference force $I_{\rm dc}$ to change. The changing $I_{\rm dc}$ causes almost the same capacitor voltage deviation, i.e., $f(t)$, of all normal SMs in this phase in a short period after CI. The capacitor voltages of the upper and lower arm normal SMs can be expressed as

$$\begin{cases} U_{Cui} = \frac{U_{\rm dc}}{N} + f\left(t\right) \\ U_{Cli} = \frac{U_{\rm dc}}{N} + f\left(t\right). \end{cases} \tag{14}$$

By combining (13) and (14), $f(t)$ can be derived as

$$f\left(t\right) = \frac{U_{\rm dc} - N_{\rm CI}n_{\rm CISM}U_{\rm CISM}}{N - 0.5N_{\rm CI}} - \frac{U_{\rm dc}}{N}. \tag{15}$$

Given that $n_{\rm CISM}$ becomes a constant value during CI, only the dc components in the lower arm current contribute to the CI-SM capacitor voltage deviation according to (12). And, the constant $n_{\rm CISM}$ introduces also extra dc components in the lower arm current. Based on (11), $I_{\rm dc}$ is almost the same before and after CI. Hence, the dc components introduced into i_o during CI should be investigated, which can be derived as

$$\begin{aligned} i_{o\_\rm dc} &= \frac{u_{o\_\rm dc}}{R} = \frac{\left(u_l - u_u\right)_{\rm dc}}{2R} \\ &= \frac{\left[0.5(N - N_{\rm CI})U_{\rm Cli} + N_{\rm CI}n_{\rm CISM}U_{\rm CISM}\right] - \left[0.5NU_{\rm Cui}\right]}{2R} \\ &= \frac{N_{\rm CI}}{N - 0.5N_{\rm CI}} \times \frac{Nn_{\rm CISM}U_{\rm CISM} - 0.5U_{\rm dc}}{2R} \end{aligned} \tag{16}$$

where u_l and u_u indicate the upper and lower arm output voltage, respectively, and R is the load resistance. Equation (16) indicates that the occurrence of CI induce an extra dc component in the output current, and such a dc current varies with $n_{\rm CISM}$.

Substituting (16) into (12) and the average voltage of the CI-SM capacitors can be solved as

$$\begin{aligned} U_{\rm CISM} = &\left[\left(\frac{N}{N_{\rm CI}} - 0.5\right)\frac{4RP_o}{n_{\rm CISM}NU_{dc}} + \frac{U_{\rm dc}}{2n_{\rm CISM}N}\right] \\ &+ \left[\frac{U_{\rm dc}}{N} - \left(\frac{N}{N_{\rm CI}} - 0.5\right)\frac{4RP_o}{n_{\rm CISM}NU_{dc}} - \frac{U_{\rm dc}}{2n_{\rm CISM}N}\right] \\ &e^{-\frac{N_{\rm CI}}{N - 0.5N_{\rm CI}}\frac{n_{\rm CISM}^2 N}{4RC}t}. \end{aligned} \tag{17}$$

The capacitor voltage variation of the CI-SMs can be described by (17). When $n_{\rm CISM} = 0$, the CI-SM is bypassed, the capacitor voltages would stay at the initial voltage as described by (12). When $n_{\rm CISM} \neq 0$, the first part of (17) determine the steady-state value of $U_{\rm CISM}$, which is inversely proportional to $n_{\rm CISM}$, while the second part indicates the rising rate of the capacitor voltage.

When CI happens, $U_{\rm CISM}$ would exceed the predefined safe-operation voltage range in a short period of time, i.e., t_p. If the dc bus voltage, the rated power, the SM capacitance, the maximum modulation index, the number of CI-SMs, and the allowed capacitor voltage range of the MMC system are fixed, t_p can be calculated according to (17). Moreover, as can be calculated based on (17), the deviation of $U_{\rm CISM}$ decreases with the increase of the number of CI-SMs, as long as the assumptions made in this subsection hold. Therefore, $N_{\rm CI} = 1$ is mostly considered for the analysis in this article. Note that the CI occurring instant is not predictable, which makes it impossible to acquire the exact value of $n_{\rm CISM}$. Thus, t_p should be selected according to the minimum value calculated by (17). In summary, t_p is related with the MMC dc bus voltage, the SM number, the output power, the SM capacitance, the maximum modulation index, and the allowed capacitor voltage deviation. It should be noted that the capacitor voltage ripple due to the ac components of the arm current, whose amplitude is normally

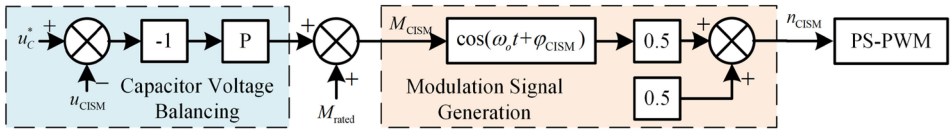

Fig. 3. Block diagram of the capacitor voltage balancing loop in CI-SM.

less than 10% of the capacitor operating dc voltage, would also affect the CI-SM capacitor voltage value. Thus, adequate margin should be reserved in t_p selection.

IV. Proposed Resilient Operation of an MMC With Communication Interruption

In this MMC distributed control system, the safe operation period t_p calculated in the previous section can be utilized to make a distinction between the network congestion and network disconnection. Based on the MMC distributed control scheme, the central controller sends messages to SMs in each control cycle and the SMs update their status to the central controller by request for system monitoring [7]. On the one hand, if a local controller does not receive the central controller's message for a few control cycles and the request from the central controller is not acknowledged but the communication is recovered within t_p, no critical protection is required and the MMC operation is scarcely affected. On the other hand, if CI between the central and local controllers lasts for a period of t_p, network disconnection is present by both the central and local controllers and necessary protecting actions are required before any device damages or malfunctions of the system.

This section presents a resilient operation scheme for the MMC systems to ride-through the CI problem. The resilient operation scheme can be divided into two stages: sustention stage and protection stage. At the sustention stage, the capacitor voltage of the CI-SM is stabilized and the system operates normally. At the protection stage, the CI-SM intentionally and gradually drifts its capacitor voltage down to zero and then cut itself off from the system automatically. Meanwhile, the central controller operates the MMC system with remaining SMs [22].

A. Sustention Stage

According to the analysis in Section III, depending on the direction of the average CI-SM capacitor current, the $U_{\rm CISM}$ might increase or decrease dramatically if the MMC operates at its rated power and the insertion index happens to be close to unity. In this case, the capacitor voltage likely reaches the safe-operation boundary when the period of CI is close to t_p. The high capacitor voltage might cause overvoltage damage for the CI-SM capacitor and switching devices, and lead to the CI-SM malfunction. Moreover, the MMC performance might be deteriorated by the significantly increased CI-SM capacitor voltage.

The essential reason for the CI-SM capacitor voltage ascent is that $n_{\rm CISM}$ becomes a constant value without the fundamental component for power balance [20]. To avoid the constant insertion index for the CI-SM, the discrete phase angles of the output voltage in the last fundamental period are stored in the memory of the local controllers. The stored phase angles are utilized to generate a sinusoidal signal with the fundamental frequency. The amplitude of the sinusoidal signal is generated by a local control loop, as shown in Fig. 3, where $n_{\rm CISM} = 0.5\,[1 + M_{\rm CISM} \times \cos(\omega_o t + \varphi_{\rm CISM})]$. The values of $\cos(\omega_o t + \varphi_{\rm CISM})$ in the last fundamental period are recorded. $M_{\rm rated}$ is the modulation index of the rated operation point and $u_c{}^*$ is the SM capacitor voltage reference. In order to eliminate the impact of voltage ripple on the control loop, the measured CI-SM capacitor voltage is low-pass filtered to obtain $u_{\rm CISM}$. The capacitor voltage error is fed into a proportional (P) controller to change the amplitude of the sinusoidal signal, i.e., $M_{\rm CISM}$, for capacitor voltage balance. The output of the P controller in Fig. 3 is normalized by $u_c{}^*$.

Note that the stored sinusoidal signal can either be in phase with the output voltage or with the output current. For simplicity, the two conditions are named as the voltage phase condition (VPC) and the current phase condition (CPC), respectively.

It is assumed that all SMs operate in the rated operation point before CI appears. Considering that the output control for normal SMs functions effectively during CI, the fundamental frequency component in the MMC output switching function can be regarded as unchanged as given in the following:

$$\begin{aligned} NM_{\rm rated}\cos(\omega_o t+\varphi_o) &= \frac{1}{2}M_{\rm CISM}\cos(\omega_o t+\varphi_{\rm CISM}) \\ &\quad + (N-1)n_{li(\rm ac)} - Nn_{ui(\rm ac)} \end{aligned} \tag{18}$$

where $n_{li(\rm ac)}$ and $n_{ui(\rm ac)}$ stand for the fundamental components in the SM insertion indices for the lower and upper arms, respectively. The modulation indices of the normal SMs should have almost the same value during CI. Therefore $n_{li(\rm ac)}$ and $n_{ui(\rm ac)}$ can be expressed as

$$\begin{aligned} n_{ui\_(\rm ac)} &= -0.5 \times M' \times \cos(\omega_o t + \varphi_o{}') \\ n_{li\_(\rm ac)} &= 0.5 \times M' \times \cos(\omega_o t + \varphi_o{}') \end{aligned} \tag{19}$$

where M' and $\varphi_o{}'$ represent the amplitude and the phase angle of $n_{li(\rm ac)}$ and $n_{ui(\rm ac)}$, respectively, during CI. Substitute (19) into (18), the fundamental frequency components in $n_{li(\rm ac)}$ and $n_{ui(\rm ac)}$ yields as

$$\begin{aligned} &M'\cos(\omega_o t + \varphi_o{}') \\ &= \frac{2NM_{\rm rated}\cos(\omega_o t+\varphi_o) - M_{\rm CISM}\cos(\omega_o t+\varphi_{\rm CISM})}{2N-1}. \end{aligned} \tag{20}$$

The circulating current is directly generated by the difference between the dc-link voltage and the sum of the inserted voltages in the arms. Ignoring the impact of parasitic arm resistance $R_{\rm arm}$,

$i_{\rm cir}$ can be derived as

$$i_{\rm cir} = \frac{1}{2L_{\rm arm}} \int [U_{\rm dc} - (u_u + u_l)]dt. \tag{21}$$

The sum of the dc capacitor voltages in each arm remains constant, which equals $U_{\rm dc}$. Based on the effect of the voltage controllers, the capacitor voltages of normal SMs in one arm have an average distribution, and the output voltage of upper and lower arms can be derived accordingly:

$$\begin{aligned} u_u &= U_{\rm dc}\left[0.5 - 0.5M'\cos(\omega_o t + \varphi_o')\right] \\ u_l &= \left(U_{\rm dc} - U_{\rm CISM}\right)\left[0.5 + 0.5M'\cos(\omega_o t + \varphi_o')\right] \\ &\quad + U_{\rm CISM}\left[0.5 + 0.5M_{\rm CISM}\cos(\omega_o t + \varphi_{\rm CISM})\right]. \end{aligned} \tag{22}$$

Substituting (20) and (22) into (21), $i_{\rm cir}$ is yielded as

$$\begin{aligned} i_{\rm cir} = &\frac{NU_{\rm CISM}}{2\left(2N-1\right)\omega_o L_{\rm arm}} \\ &\times \left[M_{\rm rated}\sin(\omega_o t + \varphi_o) - M_{\rm CISM}\sin\left(\omega_o t + \varphi_{\rm CISM}\right)\right]. \end{aligned} \tag{23}$$

According to (3), the lower arm current is $i_l = -0.5i_o + I_{\rm dc} + i_{\rm cir}$. The current flowing through the capacitor in the CI-SM can be obtained as the product of the switching function and the lower arm current. However, only the dc component in CI-SM capacitor current contributes to the capacitor voltage shifting, thus the dc capacitor current is derived as

$$\begin{aligned} \left(n_{\rm CISM} i_l\right)_{\rm dc} = &\frac{1}{2}I_{\rm dc} - \frac{1}{8}M_{\rm CISM}I_o\cos(\varphi_o + \varphi_L - \varphi_{\rm CISM}) \\ &+ \frac{M_{\rm CISM}M_{\rm rated}NU_{CISM}}{8\left(2N-1\right)\omega_o L_{\rm arm}}\sin(\varphi_o - \varphi_{\rm CISM}). \end{aligned} \tag{24}$$

Note that $I_{\rm dc}$ can be substituted by $M_{\rm rated}I_o\cos(\varphi_L)/4$ according to the MMC active power balance [20], (24) is rewritten as

$$\begin{aligned} \left(n_{\rm CISM} i_l\right)_{\rm dc} = &\frac{M_{\rm rated}I_o}{8}\cos\varphi_L - \frac{M_{\rm CISM}I_o}{8} \\ &\cos(\varphi_o + \varphi_L - \varphi_{\rm CISM}) \\ &+ \frac{M_{\rm CISM}M_{\rm rated}NU_{\rm CISM}}{8\left(2N-1\right)\omega_o L_{\rm arm}}\sin(\varphi_o - \varphi_{\rm CISM}). \end{aligned} \tag{25}$$

Based on the aforementioned principle of resilient operation, the CI-SM would operate in either VPC or CPC during the sustention stage. The stability of the CI-SM under these two conditions should both be investigated.

When the CI-SM operates in VPC, the phase angle $\varphi_{\rm CISM}$ is equal to $\varphi_{\rm o}$. The dc component in the CI-SM capacitor current is derived as

$$\left(n_{\rm CISM} i_l\right)_{\rm dc} = \frac{1}{8}M_{\rm rated}I_o\cos\varphi_L - \frac{1}{8}M_{\rm CISM}I_o\cos\varphi_L. \tag{26}$$

According to Fig. 3, $M_{\rm CISM}$ should be equal to the rated modulation index $M_{\rm rated}$ when CI occurs. Thus, the two terms in (26) spontaneously cancel each other out in VPC, which means no disturbance is introduced into the CI-SM capacitor current by CI fault in VPC. Hence, the value of $U_{\rm CISM}$ remains unchanged and (26) always equals zero during the sustention stage.

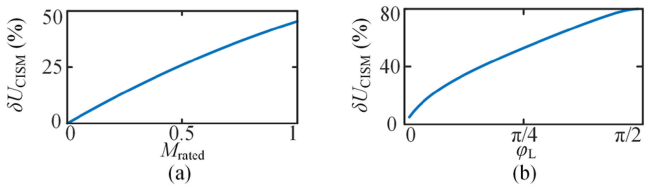

Fig. 4. Theoretical value of CI-SM capacitor voltage deviation rate $\delta U_{\rm CISM} = |NU_{\rm CISM}/U_{\rm dc} - 1|$ with varied. (a) $M_{\rm rated}$. (b) φ_L.

When the CI-SM operates in CPC, the phase angle $\varphi_{\rm CISM}$ equals $\varphi_{\rm o} + \varphi_{\rm L}$. The dc component in the CI-SM capacitor current can be expressed as

$$\begin{aligned} \left(n_{\rm CISM} i_l\right)_{\rm dc} = &\frac{1}{8}M_{\rm rated}I_o\cos\varphi_L - \frac{1}{8}M_{\rm CISM}I_o \\ &- \frac{M_{\rm CISM}M_{\rm rated}NU_{\rm CISM}}{8\left(2N-1\right)\omega_o L_{\rm arm}}\sin\varphi_{\rm L}. \end{aligned} \tag{27}$$

Given that a P-controller is applied in the CI-SM voltage balance control, $M_{\rm CISM}$ can be expressed as

$$M_{\rm CISM} = M_{\rm rated} + K_{\rm P\_bal}\left(\frac{NU_{\rm CISM}}{U_{\rm dc}} - 1\right) \tag{28}$$

where $K_{\rm p\_bal}$ is the gain of the P-controller. Evaluating (27) in s-domain, the current disturbance in (27) is a zero-order element, which can be restrained by a first-order controller, i.e., the P-controller. Therefore, the capacitor voltage of the CI-SM can be stabilized based on the control structure in Fig. 3. Equation (27) would be equal to zero in steady state, and the CI-SM capacitor voltage in CPC can accordingly be derived as

$$\begin{aligned} U_{\rm CISM} = &-\frac{\left(2N-1\right)\omega_o L_{\rm arm}I_o}{2NM_{\rm rated}\sin\varphi_L} - \frac{U_{\rm dc}\left(M_{\rm rated} - K_{\rm P\_bal}\right)}{2K_{P\_bal}N} \\ &+ \sqrt{\left[\frac{\left(2N-1\right)I_o\omega_o L_{\rm arm}}{2NM_{\rm rated}\sin\varphi_L} + \frac{U_{dc}\left(M_{\rm rated} - K_{\rm P\_bal}\right)}{2K_{P\_bal}N}\right]^2} \\ &+ \left(\frac{U_{\rm dc}I_o\left(2N-1\right)\omega_o L_{\rm arm}}{K_{P\_bal}N^2M_{\rm rated}\sin\varphi_L}\right)\left(M_{\rm rated}\cos\varphi_L\right. \\ &\left.-M_{\rm rated} + K_{P\_bal}\right). \end{aligned} \tag{29}$$

However, a steady-state error might be introduced into $U_{\rm CISM}$ while using P-controller, which is evaluated as

$$\left[U_{\rm CISM}\right]_{ss} = \left|U_{\rm CISM} - \frac{U_{\rm dc}}{N}\right|. \tag{30}$$

According to (29), the deviation of $U_{\rm CISM}$ is positively related to $M_{\rm rated}$ and φ_L, while the correlations can be more intuitively observed from Fig. 4. It should be noted that the proportional-integral controller can be used to eliminate the steady-state error in (30).

The control abilities of the capacitor voltage balancing controller during CI with different phase conditions are also investigated. Based on the control structure depicted in Fig. 3 and the capacitor balancing control introduced in Fig. 15 in [7], the

TABLE I
SIMULATION PARAMETERS AND EXPERIMENTAL SETUP

Parameters	Simulation	Experiments
Number of SMs: N	20 per arm	4 per arm
DC-link voltage: $U_{\rm dc}$	2000 V	160 V
Modulation index: m	0.7	0.85
Arm inductance: $L_{\rm arm}$	20 mH	5 mH
SM capacitance: $C_{\rm SM}$	3300 μF	940 μF
Carrier frequency: f_c	500 Hz	2 kHz
Load resistance: R_l	50 Ω	12 Ω
Load inductor: L_l	10 mH	0 / 20 mH
Allowable $U_{\rm C}$ deviation rate	50%	50%

closed-loop transfer function of the voltage balance control loop is derived as follows, when the CI-SM operates in VPC:

$$\phi(s)=\frac{I_o\omega_x N\left(K_{P\_\rm bal}\cos\varphi_L\right)}{8sC_{\rm SM}\left(s+\omega_x\right)U_{\rm dc}+I_o\omega_x N\left(K_{P\_\rm bal}\cos\varphi_L\right)} \tag{31}$$

where $\omega_{\rm x}$ stands for the cut-off frequency of the low-pass filter.

When the CI-SM operates in CPC, the closed-loop transfer function of the balancing controller is derived as

$$\phi(s)=\frac{I_o\omega_x NK_{P\_\rm bal}}{8sC_{\rm SM}\left(s+\omega_x\right)U_{\rm dc}+I_o\omega_x NK_{P\_\rm bal}}. \tag{32}$$

It can be concluded from (31) and (32) that the balancing control ability is attenuated in VPC when compared with that in CPC. The control ability in VPC would be further deteriorated with the ascending of φ_L.

B. Reference Variation During Sustention Stage

When CI happens, the local controller of the CI-SM could not receive the command from the central controller, which is critical if the output reference varies during this period. The MMC system performance with the proposed resilient operation during the output reference change is vital to be investigated.

Assuming the MMC output current amplitude $I_{\rm o}$ is increased, the value of M for normal SMs would be simultaneously raised while $M_{\rm CISM}$ remains unaltered. It can be deduced from (26) and (27) that the dc capacitor current in CI-SM augments in both phase conditions, leading to an ascending $U_{\rm CISM}$. According to Fig. 3, $M_{\rm CISM}$ would then rise up and $U_{\rm CISM}$ will eventually be stabilized at a value higher than the capacitor voltage reference $u_c{}^*$, to retrieve the balance in (26) and (27). The increased $U_{\rm CISM}$ contributes to the MMC output variation as well. Therefore, the proposed operation method ensures the MMC output reference tracking while its amplitude varies.

Assuming that the phase of output reference is shifted during the sustention stage, an additional phase change $\varphi_{\rm ch}$ would be introduced into the output voltage and current:

$$\begin{cases} u_o=U_o\cos(\omega_o t+\varphi_o+\varphi_{\rm ch}) \\ i_o=I_o\cos(\omega_o t+\varphi_o+\varphi_L+\varphi_{\rm ch}). \end{cases} \tag{33}$$

However, the phase angle of CI-SM remains $(\omega_o t+\varphi_{\rm CISM})$ after the reference phase change. The upper and lower arm voltages are derived as

$$\begin{aligned} u_u=&\,N\left(\frac{1}{2}-\frac{1}{2}M_{\rm rated}\cos(\omega_o t+\varphi_o+\varphi_{ch})\right)U_{Cui} \\ u_l=&\,(N-1)\left(\frac{1}{2}+\frac{1}{2}M_{\rm rated}\cos(\omega_o t+\varphi_o+\varphi_{ch})\right)U_{Cli} \\ &+\left(\frac{1}{2}+\frac{1}{2}M_{\rm CISM}\cos(\omega_o t+\varphi_{\rm CISM})\right)U_{\rm CISM}. \end{aligned} \tag{34}$$

For that the output current control is still efficient in sustention stage, the fundamental component in the normal SM insertion index can be derived similar to (20)

$$\begin{aligned} &M'\times\cos(\omega_o t+\varphi_o{}'+\varphi_{\rm ch}) \\ &=\frac{2NM_{\rm rated}\cos(\omega_o t+\varphi_o+\varphi_{ch})-M_{\rm CISM}\cos(\omega_o t+\varphi_{\rm CISM})}{2N-1}. \end{aligned} \tag{35}$$

Taking CPC as an example, the additional ac component in $i_{\rm cir}$ is obtained as

$$\begin{aligned} i_{\rm cir\_ac}=&-\frac{M_{\rm rated}}{4\omega_o L_{\rm arm}}\left\{(N-1)\left[\sin(\omega_o t+\varphi_{\rm ch})\left(U_{Cli}-U_{Cui}\right)\right]\right. \\ &\left.+\left[\sin(\omega_o t+\varphi_L)U_{\rm CISM}-\sin(\omega_o t+\varphi_{\rm ch})U_{Cui}\right]\right\}. \end{aligned} \tag{36}$$

According to (3), the upper arm current is derived as

$$i_u=0.5\left[I_o\cos(\omega_o t+\varphi_{\rm ch}+\varphi_{\rm L})+I_{\rm o\_dc}\right]+I_{\rm dc}+i_{\rm cir\_ac}. \tag{37}$$

The insertion index for the upper arm SMs considering reference phase change is

$$n_u=\frac{1}{2}-\frac{1}{2}M_{\rm rated}\cos(\omega_o t+\varphi_o+\varphi_{\rm ch}). \tag{38}$$

During the steady-state operation, the circulating current control would properly adjust the dc components in the circulating current to ensure that the dc capacitor current in the normal SMs, i.e., $(n_u i_u)_{\rm dc}$, approximately equals zero for the sake of system stable operation [11].

According to (37) and (38), $(n_u i_u)_{\rm dc}$ can be expressed as

$$\begin{aligned} (n_u i_u)_{\rm dc}=&\,\frac{I_{\rm dc}}{2}-\frac{M_{\rm rated}I_o\cos\varphi_L}{8}+\frac{I_{\rm o\_dc}}{4} \\ &-\left[\frac{M_{\rm rated}}{2}\cos(\omega_o t+\varphi_o+\varphi_{ch})\times i_{\rm cir\_ac}\right]_{\rm dc} \\ =&\,\frac{I_{\rm o\_dc}}{4}-\left[\frac{M_{\rm rated}}{2}\cos(\omega_o t+\varphi_o+\varphi_{ch})\times i_{\rm cir\_ac}\right]_{\rm dc}=0. \end{aligned} \tag{39}$$

Therefore, $I_{\rm o\_dc}$ can be obtained by substituting (36) into (39):

$$I_{\rm o\_dc}=\frac{M_{\rm rated}^2U_{\rm CISM}}{4\omega_o L_{\rm arm}}\sin(\varphi_{\rm ch}-\varphi_L). \tag{40}$$

According to (36) and (40), the reference phase change during the sustention stage would bring an extra dc component in $i_{\rm o}$ and a fundamental frequency component in $i_{\rm cir}$. Based on (36) and (40), the direct component in the CI-SM capacitor current can

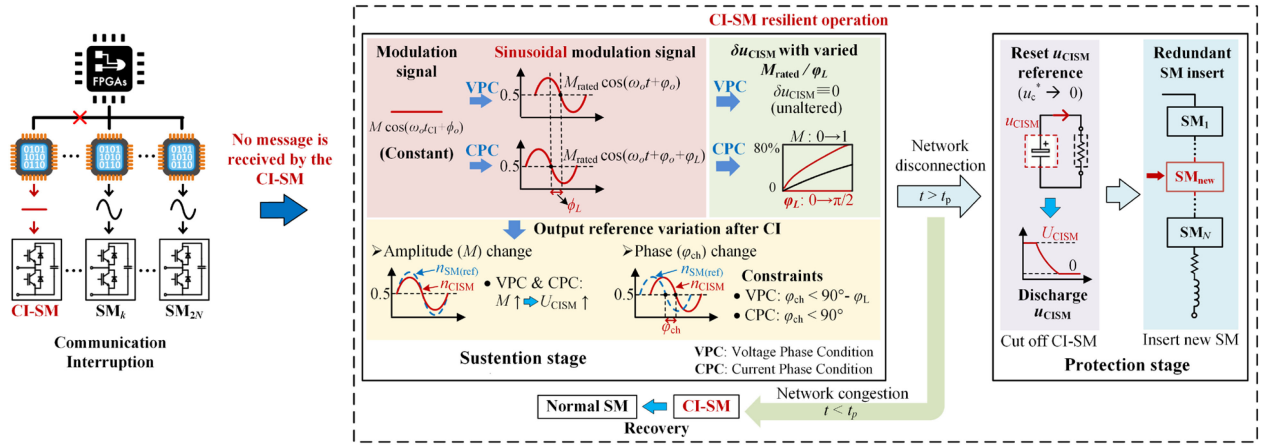

Fig. 5. Block diagram of the CI-SM resilient operation after CI occurs.

be expressed as

$$(n_{\mathrm{CISM}} i_l)_{\mathrm{dc}} = \frac{1}{8} M_{\mathrm{rated}} I_o \cos\varphi_L - \frac{M_{\mathrm{rated}}^2 U_{\mathrm{CISM}}}{16\omega_o L_{\mathrm{arm}}} \sin(\varphi_{\mathrm{ch}} - \varphi_L) - \frac{1}{8} M_{\mathrm{CISM}} I_o \cos\varphi_{\mathrm{ch}} - \frac{M_{\mathrm{rated}} M_{\mathrm{CISM}}}{16\omega_o L_{\mathrm{arm}}} [(N-1)(U_{Cli} - U_{Cui}) - U_{Cui}] \sin(\varphi_{\mathrm{ch}} - \varphi_{\mathrm{L}}). \quad (41)$$

When φ_{ch} changes, (41) can still be zero by properly adjusting M_{CISM}. The adjustment is accomplished by the capacitor voltage balance controller for CI-SM. Thus, the dc disturbance in CI-SM capacitor current would eventually be canceled out in steady-state when the output reference phase is changed. However, $i_{\mathrm{diff\_ac}}$ and $I_{\mathrm{o\_dc}}$ would increase when φ_{ch} augments, which subsequently causes the saturation of the voltage balance and circulating current controllers. Thus, a large reference phase shift during CI might induce the MMC distributed control system instability. Similar results can also be obtained in VPC. Note that φ_{ch} should not be more than 90° in CPC and $(90^\circ - \varphi_L)$ in VPC, since the voltage control in CI-SM may have a reverse effect according to the capacitor voltage balance diagram in Fig. 15 in [7].

Based on the aforementioned investigation, it is found that VPC is superior to CPC in terms of the capacitor voltage steady-state error while utilizing a P controller to regulate the CI-SM capacitor voltage. However, CPC possesses a better capacitor voltage balancing ability than that of VPC when φ_L is not zero. The preferred reference phase change range is dependent of φ_L. Hence, the operation mode should be selected considering all the above aspects.

C. Protection Stage

If CI lasts continuously for a period of t_p, the network disconnection is confirmed by both the central and local controllers and the protection for the CI-SM is activated. During the protection stage, the CI-SM capacitor voltage reference would be set to zero and U_{CISM} would drop to zero accordingly. The central controller would cut the CI-SM off and operate with the remaining SMs as discussed in [4], [22].

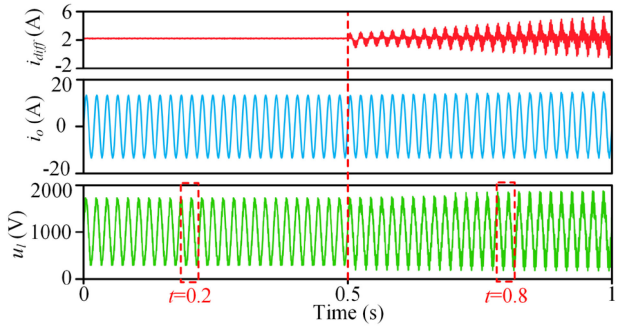

Fig. 6. Simulated waveforms of the MMC when CI happens at $t = 0.5$ s with $n_{\mathrm{CISM}} = 0.6$.

The overall procedure of the proposed resilient operation of the MMC encountering CI is illustrated in Fig. 5. The MMC with single SM communication failure is investigated in this section. It is possible that more than one SM in MMC occur CI problem. The proposed resilient operation method can be extended to the MMC with more than one CI-SM.

V. Simulation and Experimental Verification

The theoretical analysis was validated by both simulation and experimental results. The specifications of the simulated system and the experimental setup are shown in Table I.

A. Simulation Results

The simulation system with 20 SMs per arm was built to verify the proposed model with CI in Section III. Fig. 6 shows the waveforms of the MMC when CI occurs at 0.5 s with $n_{\mathrm{CISM}} = 0.6$. No resilient operation is applied to the CI-SM. It can be observed that the differential current is drastically deteriorated due to the CI, while the fundamental frequency component in the output current is not severely affected. Also, the output voltage of the lower arm containing the CI-SM is

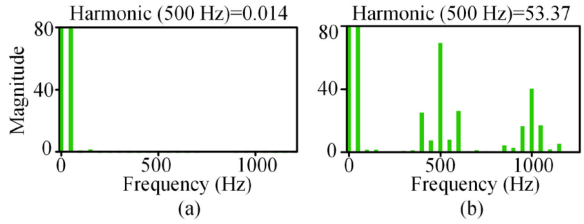

Fig. 7. Harmonic spectra of lower arm voltage u_l with $n_{\mathrm{CISM}} = 0.6$ at (a) $t = 0.2$ s and (b) $t = 0.8$ s.

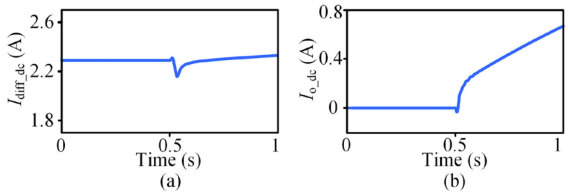

Fig. 8. Current during CI fault. (a) DC component in i_{diff}. (b) DC component in i_o.

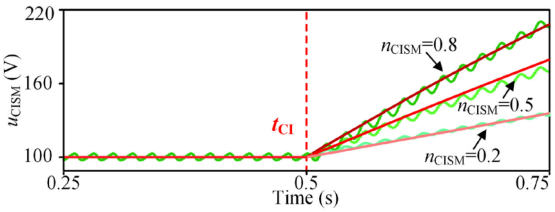

Fig. 9. Simulated CI-SM capacitor voltage when CI happens at $t = 0.5$ s with different duty ratios.

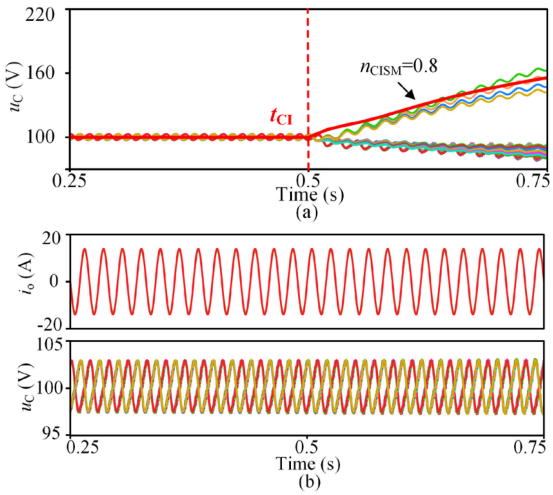

Fig. 10. Simulated waveforms of MMC when CI happens at $t = 1$ s: (a) without resilient operation method; (b) with proposed resilient operation method.

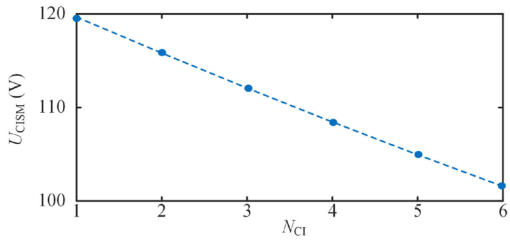

Fig. 11. Capacitor voltage of CI-SM at $t = 0.58$ s with different N_{CI}.

distorted after CI ($t_{\mathrm{CI}} = 0.5$ s). The harmonic spectrums of the lower arm voltage at $t = 0.2$ and 0.8 s are depicted in Fig. 7(a) and (b), respectively. The harmonics around the carrier frequency (500 Hz) are largely introduced into the lower arm voltage, which coincides with the study of u_l in (7) and (8).

In Fig. 8, the dc current in i_{diff} almost remains the same before and after CI. However, the dc component in i_{o} keeps rising since t_{CI}, which induces a non-negligible dc disturbance in the CI-SM capacitor current as given in (16). U_{CISM} would be increased by the CI-SM dc current and eventually exceed the critical capacitor voltage. The CI-SM capacitor voltages with different n_{CISM} are shown in Fig. 9. It can be observed that U_{CISM} quickly ascends after CI. To verify the accuracy of the mathematical model, U_{CISM} was calculated based on (17). The calculated U_{CISM} was depicted as the red curves in Fig. 9. The figures show that the simulation results of U_{CISM} have sufficient accordance with the calculated values under different conditions.

The U_{CISM} calculation and the proposed resilient operation for a 20 SM MMC with 4 CI-SMs in the lower arm are investigated by simulation as well. Fig. 10 shows that the capacitor voltage and output current are scarcely impacted by the multiple CI faults with the help of the proposed resilient operation method. Comparing U_{CISM} in Fig. 9 with that in Fig. 10, it can be found that the capacitor voltage deviation is decreased. The diagram showing U_{CISM}, which is calculated based on (17) and parameters in Table I, with different N_{CI} at $t = 0.58$ s is depicted in Fig. 11. The insertion index of the CI-SMs, i.e., n_{CISM}, is selected as 0.8 during the calculation. It can be seen that U_{CISM} deviation is mitigated with the increase of N_{CI}, and a larger t_p is sufficient to ensure the MMC safe operation in this case.

B. Experimental Results

In order to verify the validity of the proposed resilient operation method of the MMC, a single-phase MMC prototype with four SMs per arm was configured as shown in Fig. 12. Detailed parameters are specified in Table I.

1) Sustention Stage of Resilient Operation: The effectiveness of utilizing the stored sinusoid signal and local voltage balance controller to maintain the capacitor voltages was verified in both current and VPCs by adopting different power factors (PFs) (1 and 0.874). The MMC system with a unity PF was first investigated. Figs. 13 and 14 present the output waveforms of the MMC operating in VPCs and CPCs, respectively. It can be seen that the MMC output current operated normally and the individual capacitor voltages remained stable after the CI occurred. As depicted in Figs. 13 and 14, the CI-SM capacitor voltage deviation is negligible, which agrees well with the analysis in (26) and (27).

Figs. 15 and 16 represent the current and voltage waveforms of the MMC when PF was 0.874. The MMC output was connected

Fig. 12. Downscaled laboratory prototype of MMC.

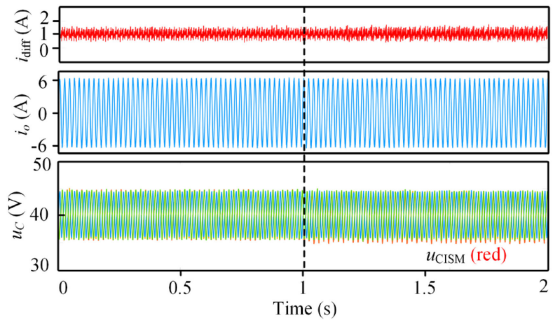

Fig. 13. Measured waveforms in sustention stage of the MMC in VPC when $\cos(\varphi_L) = 1$.

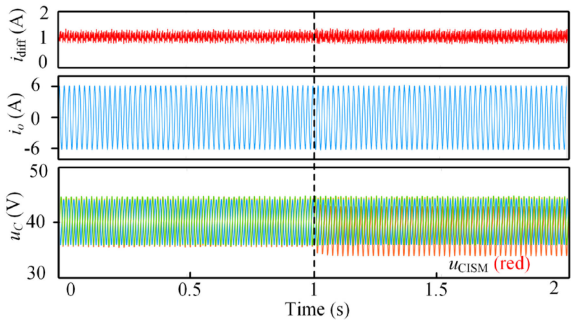

Fig. 14. Measured waveforms in sustention stage of the MMC in CPC when $\cos(\varphi_L) = 1$.

to an *R-L* load in this set of experiments. No capacitor voltages diverging was found in VPC because (26) is satisfied regardless of the PF. In CPC, the output of the MMC remained stable, but the U_{CISM} in CPC showed an apparently steady-state error compared with that in Fig. 14. This is explained by that the deviation of U_{CISM} is positively related to the PF angle in CPC according to (30). With the help of the capacitor voltage control, the sum of the capacitor voltages in one arm remains approximately the same before and after CI [11]. Thus, in Fig. 16, the capacitor

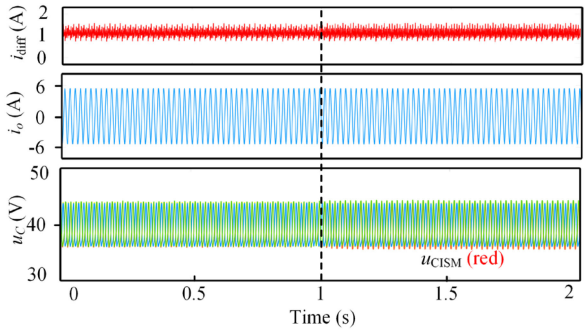

Fig. 15. Measured waveforms in sustention stage of the MMC in VPC when $\cos(\varphi_L) = 0.874$.

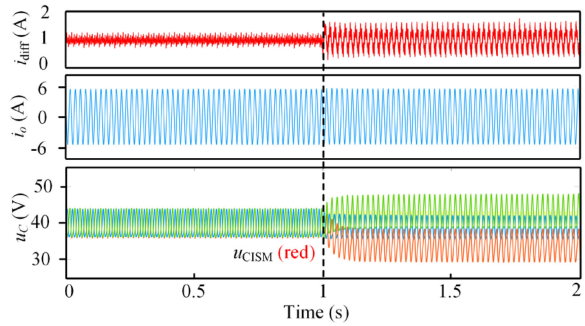

Fig. 16. Measured waveforms in sustention stage of the MMC in CPC when $\cos(\varphi_L) = 0.874$.

voltages of normal SMs in the lower arm increased while the U_{CISM} decreased after CI, so that the arm voltage is almost unaltered.

2) Reference Change During Sustention Stage: In the following set of experiments, the output reference variation during the sustention stage was studied. A resistor and inductor serial load is utilized for the sake of a 0.874 PF. Both amplitude change and phase change scenarios were discussed to evaluate the MMC system performance.

Fig. 17 shows the capacitor voltages and the output current of the MMC when the modulation index changed from 0.6 to 0.85. According to the waveforms, U_{CISM} in both phase conditions climbed to a value higher than the reference value (U_{dc}/N). The positive capacitor voltage deviation introduced a positive output in the voltage balance controller [7], [29]. Therefore, M_{CISM} is accordingly increased and the output active power of the CI-SM is improved to fulfill the MMC output ascent.

Fig. 18(a) presents the circulating current and the output current in VPC, while Fig. 18(b) presents the individual capacitor voltages in both VPC and CPC. The reference phase change φ_{ch} was zero from 0 to 2 s. When $t = 2$ s, φ_{ch} was step-changed to 60° while at $t = 4$ s it was subsequently changed to 90°. According to the analysis in Section IV, phase change during the sustention stage would introduce an additional ac component in i_{cir} and a dc component in i_o, which was clearly verified as shown in Fig. 18(a). It can be seen in Fig. 18(b) that the capacitor voltages remained stable when $\varphi_{\mathrm{ch}} = 60°$. However, when φ_{ch} stepped

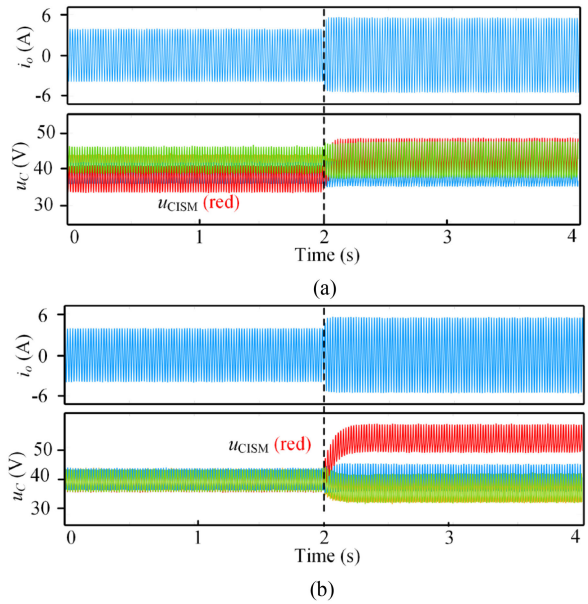

Fig. 17. Measured waveforms of the MMC when the output current amplitude has a step change: (a) CPC; (b) VPC.

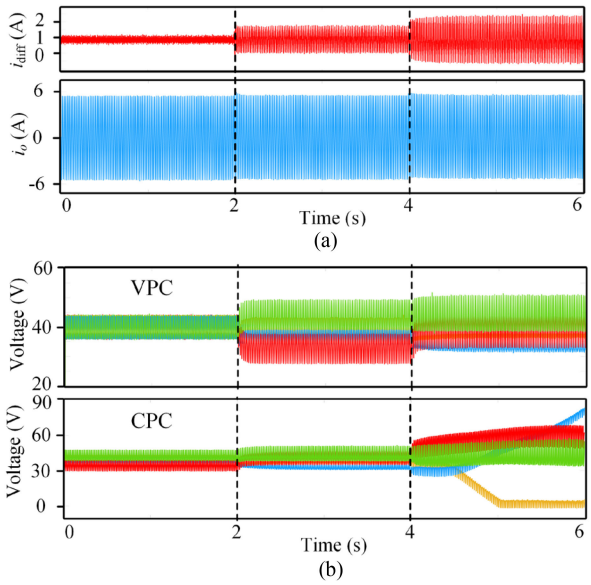

Fig. 18. Measured waveforms of the MMC when $\varphi_{\rm ch}$ changes from 0° to 60° and then to 90°. (a) Circulating current and output current in VPC. (b) Capacitor voltages in VPC and CPC operation.

to 90°, the MMC system in CPC quickly became unstable. This is because the voltage balancing capability for CI-SM in CPC is deprived when $\varphi_{\rm ch} = 90°$. The capacitor voltages in VPC remain stable since the critical $\varphi_{\rm ch}$ in VPC is $(90^{\circ} - \varphi_L)$ as in Section IV-B, where $\varphi_L \leq 0$.

3) Protection Stage of the Resilient Operation: After the period of t_p, the network disconnection was confirmed by the CI-SM local controller. The CI-SM capacitor voltage reference was then set to zero and $U_{\rm CISM}$ gradually drops to zero as given

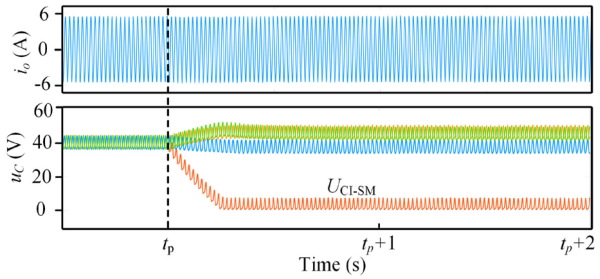

Fig. 19. Measured waveforms while controlling the CI-SM capacitor voltage to zero in the protection stage when $t > t_p$.

in Fig. 19. Afterward, the CI-SM could be cut-off and the MMC was able to operate normally with the remaining SMs [22].

VI. Conclusion

In this article, the influence of CI to the MMC distributed control system is analyzed. It shows that a CI might lead to a high increase of the CI-SM capacitor voltage and give instability of the system. According to the protection period t_p associated with the voltage increase rate and the capacitor voltage safe margin, the CI faults are classified as temporary and permanent ones in the fault analysis. A resilient operation strategy having sustention and protection stages that correspond to the temporary and permanent CI faults, respectively, is proposed to ride-through a CI fault. In the sustention stage, prestored phase angles are utilized to generate the sinusoidal modulation signal for the CI-SM in order to maintain the capacitor voltage of the CI-SM. If the network cannot recover within the predefined time period t_p, the protection stage will be triggered to discharge the capacitor and then bypass the CI-SM. The MMC operates with remaining SMs. The effectiveness of the proposed resilient operation strategy is experimentally verified on a prototype in the laboratory. The results show that, with the resilient operation strategy, the MMC distributed control system is immune to CI faults and can operate with higher reliability not only in the steady-state but also during the transient process. The MMC can operate normally during the CI fault without frequently triggering the protection actions and bypassing or replacing the faulty SMs.

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