Quantitative Analysis of Asymmetric Multilevel Inverters With Reduced Device Count From Reliability and Cost Function Perspective—A Review

Daki Krishnachaitanya and Chitra A.

***Abstract*—To more efficiently harness the renewable energy sources, advanced power converters have become an indispensable part in real time implementation. Multilevel inverters (MLI) appear to be a promising alternative to the classical inverters in medium power applications. This article attempts to present a quantitative review of recent reduced switch multilevel inverter topologies. The topology selection plays a vital role in utility applications. The figure of merits that have been considered for the quantitative analysis are switching losses, cost function, and reliability. The analysis has been carried out for eight asymmetric topologies, which involve reduced device count. To have a common platform for comparison, all the eight topologies are selected with 15-level output. The exhaustive analysis has been compiled in a pictorial fashion and solid conclusions have been derived for future utility. A new 15-level asymmetric MLI has been proposed in this article. The proposed inverter is validated through MATLAB/Simulink, and the results are presented. The proposed topology has been compared with existing inverter. The proposed topology has been exhaustively analyzed to figure out the impact of switching frequency and duration on time from reliability perspective. Also, the implementation level cost has been provided in detail including the various factors. The results reveal that the proposed topology provides superior performance in terms of total harmonic distortion (THD), losses, cost, and reliability.**

***Index Terms*—Cost function, multilevel inverter with reduced device count (MLI with RDC), reliability, switching losses, total harmonic distortion (THD).**

I. Introduction

THE dc to ac conversion systems (inverters) have been employed more often in solar systems. Generally, based on the nature of the output waveform, inverters are classified as square wave inverters, quasi-square wave inverters, two-level pulse width modulation (PWM) inverters, and multilevel inverters (MLIs) [1]–[5]. MLI topologies are introduced as an alternative in medium-voltage and high power situations. Mainly MLIs are classified into neutral point clamped, flying capacitor, and cascaded H-Bridge (CHB) MLIs [6]–[10]. Among these classical topologies, the CHB is widely used in renewable energy applications due to its multiple dc source requirements [11]. When the number of levels increase in output voltage, it requires a large number of power electronic switches, dc sources, driver circuits, heat sink, and protection circuits, thereby leading to cost increment, control complexity, and reduction in reliability of the inverter[12], [13]. Consequently, for the past few years efforts are directed to reduce power electronic switch count in MLIs and a large number of topologies appear in the literature. In the application point of view, these circuits have their own merits and demerits [14].

In order to evaluate the performance of an inverter or any converter, it is very important to consider the switching losses, cost function, and reliability. The switching loss can be reduced when there exists an equal stress sharing among all switches in the topology [15]. The tangible implementation cost of the selected topology is mainly influenced by the number of power switches. The assessment of the inverter reliability must be done during its design phase [16].

This article aims at presenting an exclusive review on few asymmetrical reduced device count MLI topologies. The review has been focused toward the major performance indices of MLI like switching losses, cost function, and reliability. An exhaustive quantitative analysis has been presented for the all the eight topologies.

The article has been organized as follows. Section II discusses the various reliability estimation methods for power converters. In Section III, the cost function evaluation is presented in detail. The topological review of MLI with reduced device count (MLI with RDC) has been detailed in Section IV. Performance investigation of MLI with reduced device count topologies is quantitatively tabulated in Section V. The proposed topology with detailed analysis is presented in Section VI. Finally, Section VII concludes this article.

II. Reliabilty Estimation Methods for Power Converters

This section explains about the assessment of the reviewed topologies based on the performance of the MLIs [17]. Mainly, the performance of the product depends on the quality, constructional, operational, time duration, and environmental conditions. If any one of the condition fails, performance of the product will reduce to a particular time period known as product failure. The

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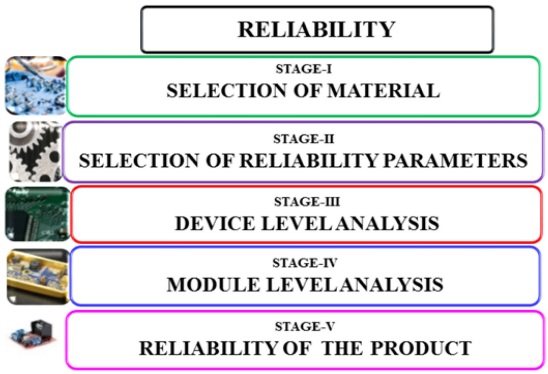

Fig. 1. Stages for the evaluation of the reliability for the electronic module.

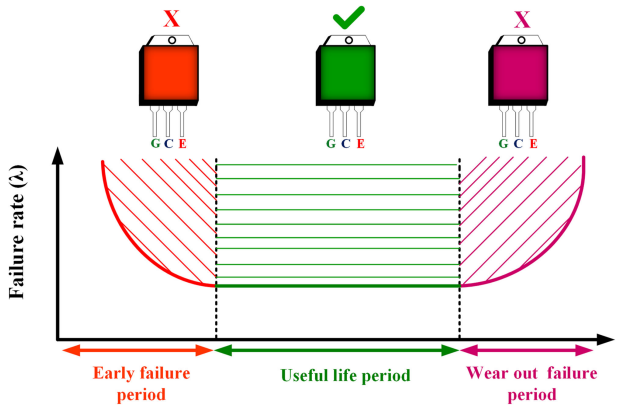

Fig. 2. Model graph of the bathtub curve for the electronic devices.

improvement of the product performance can be achieved by the prediction of reliability. Reliability is defined as the prediction of performance of the product for a specified time duration [18]. It refers to use the mathematical models and data to estimate the circuit reliability before the empirical data is obtained, so as to estimate the failure rate of the product over the life of the product. Reliability is divided into five stages for the electronic modules as shown in Fig. 1.

Selection of material is the first step for the reliability assessment. The constants and the standards are dependent on the power semiconductor material used in MLI. Joint Army-Navy Technical Exchange Verified (JANTXV), Joint Army-Navy Technical Exchange (JANTX), Joint Army-Navy (JAN), and Joint Army-Navy Space (JANS) are high quality and reliable materials designated by the MIL-S-19500 standard. Sensitivities of the materials are different from each other.

The second step of the reliability is the parameter selection based on the operation and application. Common parameters of the electronic devices are losses, failure rate, voltage stress, etc. These parameters' effect depends on the device characteristics and sensitive factors involved in the manufacturing [19].

In the third stage, the device level analysis can be obtained by calculating the component level failure rate for individual devices. The testing process of subjecting the device to rated voltage and current and examining the dynamic characteristics of the device refers to module level analysis. The above four steps decide the reliability of the circuit in the way of designing and fabrication. The fifth step of the reliability is the evaluation process of life of the product and mean time failure rate of the entire system providing the product bath tub curve as shown in Fig. 2.

These phases are the major considerations in the process of designing and manufacturing of a reliable product. Estimation and assessment of the reliability has been calculated with different types of approaches [20]. Each approach has a special characterization for the reliability assessment. In this work, an exhaustive review of various methods of evaluation of reliability has been explored.

In [21], the authors have explained the different approaches for reliability of the power semiconductor devices. The temperature cycle has been calculated for a 600V/300A insulated-gate bipolar transistor (IGBT) module and failure rate estimation is used to calculate the product life cycle. The evaluation process

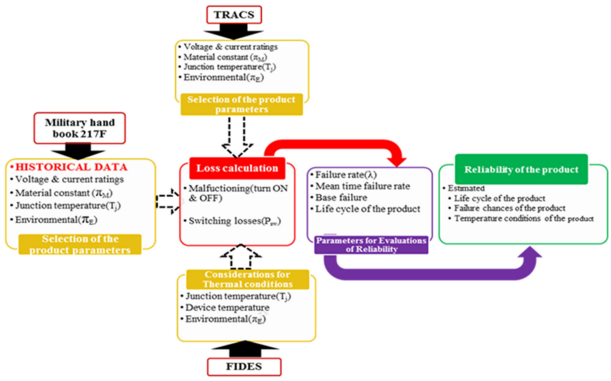

Fig. 3. Evaluation process for the reliability for different methods.

of the reliability has been calculated by using the standard of Military handbook 217F. This process of evaluation depends on the power semiconductor device malfunctioning, component temperature, switching losses, and the life profile of the product as shown in Fig. 3.

Military handbook 217F is a widely used standard for the reliability determination. The development of this model is based on the historical failure data of the component. The component failure rate is multiplied with the base failure rate with the specific application factor (π). Failure rate of the component depends on the switch voltage and current. In switch transition period, the voltage and current will overlap and will be finite. Voltage and current stress during switching is dependent on the power factor of the inverter. These switching stresses have an impact on the energy losses, efficiency, and failure rate of the device. The main disadvantage in this method is the limitation of static historical data set involved. This method is called as bottom-up statistical method. To overcome this problem, researchers employ the actual reliability method of the system. Actual reliability means the mathematical analysis of the reliability before the system is fielded and this method is known as top-down similarity analysis method.

In [22], the authors have explained the top-down method for reliability of the power semiconductor devices. The selection and quality of the product plays a vital role for the assessment of reliability. The evaluation process of the reliability has been calculated by using the standard of FIDES handbook. The selection of the product depends on the voltage, current, application,

TABLE I
FORMULATION OF THE GENERALIZED RELIABILITY METHODS

Literature	Methods & Standards	Material used	Parameters π_T	π_E	T_d	T_j	π_s	π_M	π_R	Failure rates	Required data	Collection of data	Method success rate
[21]	Bottom-up statistical Mil-Hdbk-217F	JANTX	✓	✓	✓	✓	-	-	-	$\lambda = \sum_{i=1}^{n} N_i \lambda_i$	Historical data	Moderate	Good
[22]	Top-down similarity analysis FIDES, TRACS	JANTX	-	✓	-	✓	✓	✓	✓	$\lambda = \lambda_{phys} \pi_{PM} \pi_{Process}$	Field data	Difficult	Best
[23]	Bottom-up-physics of failure FIDES	JANTX	-	✓	-	✓	✓	✓	✓	$\lambda = \lambda_{base} \pi_{PM} \pi_{Process}$	Experimental data	Easy	Good

environment, temperature, quality, and material constant factors as shown in Fig. 3.

This method will provide the system reliability for selected components in real time implementation. The main disadvantage in this method is the requirement of filed stress and acceleration models for estimation. This method does not provide any operational reliability of the product. To overcome this problem, researchers are looking into the reliability prediction methods. The reliability prediction of power semiconductor devices have been evaluated by the method called bottom-up physics of failure.

In [23], the authors have explained the bottom-up physics of failure method for the reliability assessment of the power semiconductor device. The switching losses and failure rate have been considered for the assessment of reliability to calculate the end life of the product. This method will provide the reliability prediction for the specific failure mechanisms of the group model or system. The limitations of this method are that it is not applicable for field reliability due to its high complex and expensive nature. Also, it has a drawback that it fails to project the entire reliability of the system. The reliability prediction depends on the failure rate, application factor, mean time failure rate, on mission failure rate, and life cycle of the product as shown in Fig. 3.

In [24], the authors calculate the failure rate for the different types of power electronic devices using several methods. They found that each method gave different type of failure rate for the components with wide range of variations in failure rate. Reliability predictions obtained by these methods for particular components or systems cannot be compared, because of the sensitivity of the parameter are different for each method and each method has its own assumption and data [25]–[30]. Apart from the aforementioned methods, recently fuzzy logic, artificial neural network (ANN), chain rule, probability, and fault tree have been used for the reliability prediction of the power semiconductor devices. The formulation of the generalized reliability methods are shown in Table I.

In [31], the authors explained the reliability assessment for power semiconductor devices by using the artificial intelligence method. This method establishes the functional relationship between design and reliability parameters. The required data for the implementation is either simulation or experimental data. For predicting the reliability of the converter, the authors have considered the ambient temperature, thermal stress, and switching frequency associated with the power converter. In traditional methods, any one the data (thermal stress, switching frequency, and temperature conditions) is normally taken for reliability estimation. But in this ANNs based method, two or more parameters can be used for the reliability assessment. The authors have employed two ANNs for optimizing the assessment complexity of the reliability prediction. ANN1 is trained with the converter design parameters that can map the operating conditions and junction temperature of power semiconductor devices. ANN2 is trained with ANN1, ambient temperature, thermal stress, and switching frequency. The output of the ANN2 is the life time calculation.

The malfunctioning of the power semiconductor device is also one of the influencing factors for reliability evaluation. Malfunctioning of the power semiconductor leads to increased switching losses. This may result in higher energy losses, higher temperature, and more failure chances in the system. The following equations have been for the loss calculations:

$$\text{Losses} = T_{\text{conduction}} * \text{no.of levels on} - \text{condition} * \lambda_p \quad (1)$$

$$T_{\text{conduction}} = T_{\text{total}} - (T_{\text{on}} - T_{\text{off}}). \quad (2)$$

In this article, reliability deals with the failure rate of the power electronic switches by using the bottom-up physics of failure (BP) and bottom-up statistical methods (BS) [32]–[35]. BP method provides the specific failure mechanisms and is valuable for prediction of end of life for known failure mechanism. BS method provides the actual failure rate and defects densities and is suitable for field reliability [36]. It also provides the procedure to be adapted to calculate the failure rate of power electronic component. The objectives for the reliability prediction are to provide safety instructions, achieve a reliable and quality product, and assess potential warranty risk.

Failure rate is defined as the number of components failing per unit time. Every product has the failure rate and this failure rate changes throughout the life of the product [37]–[39]. The process of the reliability evaluation of the power semiconductor device is as shown in Fig. 4.

In this article, the reliability process has been oriented toward the failure rate of the power semiconductor devices as shown in Fig. 4. The procurement of the product always depends on the parameters under consideration like temperature factor, environmental factor, etc. Parameter consideration will decide the material selection for the system implementation. According to the

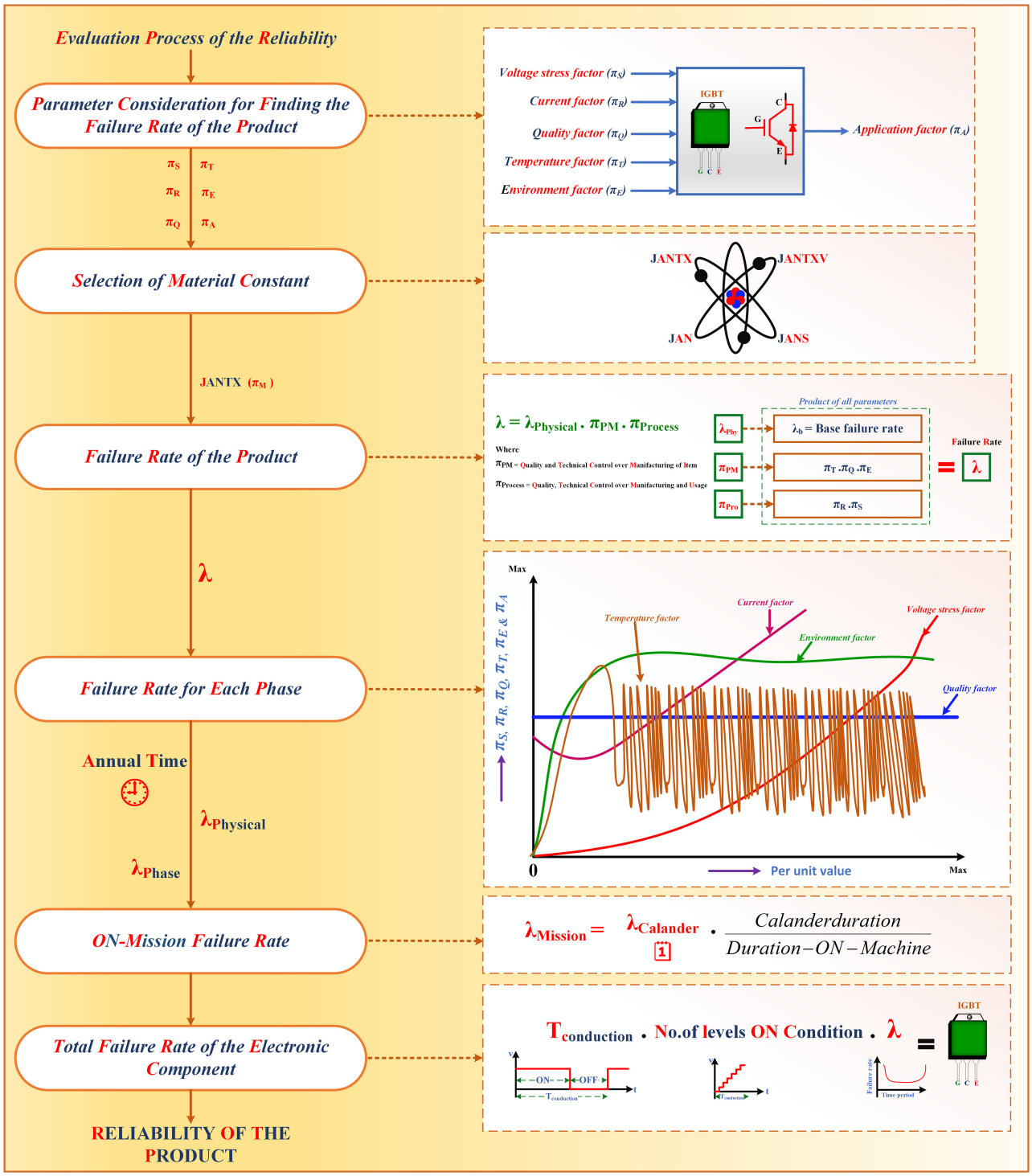

Fig. 4. Followed procedure for the reliability evaluation of power semiconductor device.

system operating conditions, losses may be developed in the system, which will decide the life time of the product. For arriving at the on mission failure rate, 24 h operation has been considered in this article as a worst case scenario. The above detailed procedure is used for finding the reliability of the reviewed topologies as shown in Fig. 4. This reliability assessment will provide the valuable sensitivities as well as good quality outcome of the product. Quality of the product will increase the life and reduce the maintenance expenses of the product. The expenses of the product implementation have been controlled by the cost prediction in selection level. The cost function is discussed in the next section.

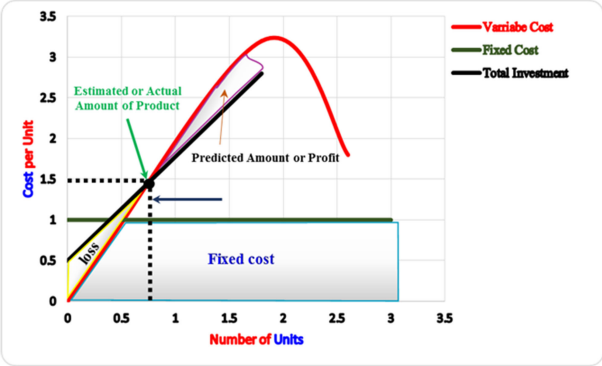

Fig. 5. Characteristics of the cost, loss, and prediction of the amount.

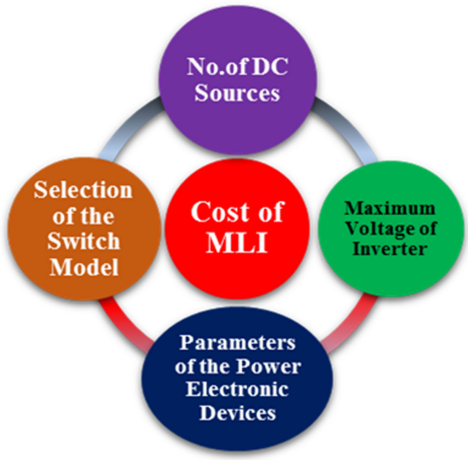

Fig. 6. Cost effecting factors of the MLI.

III. Evaluation of Cost Function for Power Converters

The quality of the product is directly proportional to the tangible cost. There are three types of costs: variable, fixed, and mixed cost; the type of the cost depends on the product. In this article, an exhaustive review of cost evaluation for the MLI topologies has been explored. In [40], the authors have explained about characteristics of variable cost and their effects on the product. Variable cost is one of the most effected cost on any product, because of this cost variation depends on the place and availability of the product [41]. Variable cost of the product is directly proportional to the number of units, but variable cost per unit is constant. It leads to the price difference on the product; this type of cost is called as tangible cost. In [42], the authors have discussed about the fixed cost characteristics for the equipment. This cost used for the price estimation of the equipment but fixed cost per unit changes with the system so that the product selection with fixed cost may lead to the economic loss. This is suitable for the less quantity of products. The relation between fixed and variable costs is shown in Fig. 5.

The intersection of the variable cost and investment of the product is called as the estimation price of the product as shown in Fig. 5. MLI cost analysis has been estimated by using the standards of cost estimation function [43]–[45]. Cost function of the MLI depends on the number of device count and the number of dc voltage sources. Mainly, the electronics cost depends on several ratings of the product, which is voltage, current, and power rating of the system. So, these are the factors considered for the cost estimation of the product [46]. Selection of the components is dependent on the finalized ratings of the MLI [47]–[49]. The considered factors for the cost evaluation of MLI are as shown in Fig. 6.

The steps to be followed for arriving at the cost function are as shown in Fig. 7

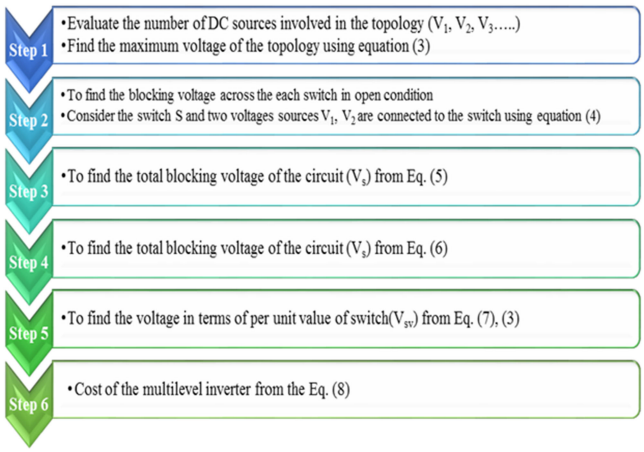

Fig. 7. Evaluation procedure of the cost function.

$$V_{\max} = \sum_{n=1}^{k} V_n \quad \text{where } n = 1, 2, 3, \ldots. \tag{3}$$

Blocking voltage across each switch (V_{block})

$$V_{\text{block}} = \text{sum of the connected voltage sources } (V_1 + V_2). \tag{4}$$

$$\text{Total blocking voltage of each switch } (\text{T}.V_{\text{block}}) \tag{5}$$

$$V_{\text{s}} = \sum_{i=1}^{j} V_{\text{si}} \text{ where } i = 1, 2, 3, \ldots. \tag{6}$$

$$V_{\text{sv}} = \frac{V_{\text{s}}}{V_{\max}}. \tag{7}$$

$$\text{Cost function of multilevel inverter } = N_{\text{IGBT}} + \text{current} \times V_{\text{sv}}$$

$$N_{\text{IGBT}} = \text{number of IGBT}. \tag{8}$$

The above following steps are used for the calculation cost function of multilevel inverter as shown in Fig. 7. It provides the cost function in per unit value. In Section V, the performance analysis of the reviewed MLI topologies has been evaluated based on the above selected reliability and cost function prediction methods.

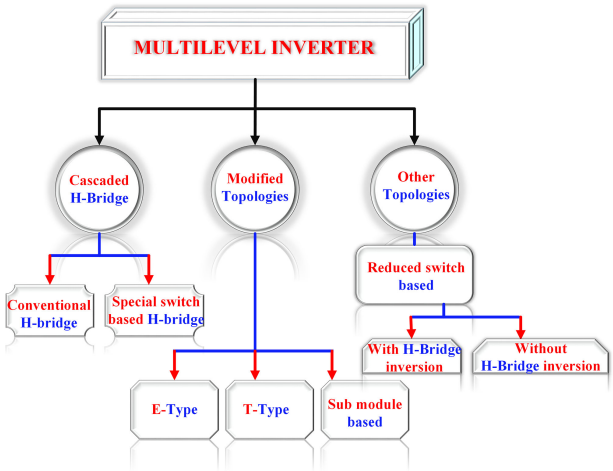

Fig. 8. Constructional classification of multilevel inverters.

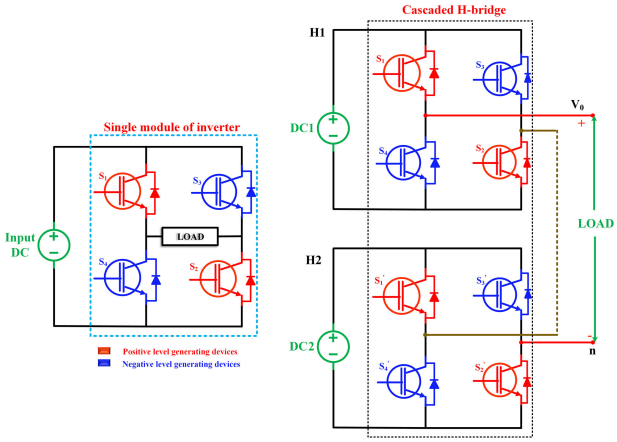

Fig. 9. Constructional view of traditional inverters.

In the next section, the constructional review of the reduced switch multilevel inverter topologies and the comparison of the topologies have been explored.

IV. Review of MLI Topologies With Reduced Device Count

The MLI can be classified as shown in Fig. 8.

Research and industry community has wide interest in the MLIs for viable technology. The first patent of the converter describing a conventional topology capable of producing multilevel voltage from various dc voltage sources has been published by Baker and Bannister [50]–[52]. The first invited topology is capable of producing the two-level output in Fig. 9. The topology is called as CHB inverter, it consists of series connection of single phase inverter as shown in Fig. 9. In CHB, increment of output voltage levels leads to the maximum number of power semiconductors devices as well as number of sources [53]–[56]. This in turn increases the constructional layout and cost of the inverter, but these topologies are considered as the standard dc-ac converters in power electronic societies as shown in Fig. 9.

In order to reduce the number of power semiconductor devices and sources, researchers are developing new multilevel inverter topologies to reach the advantages of multilevel inverter [57], [58]. In reduced switch multilevel inverters (RSMLI) inversion of front end output is possible by using the conventional construction of inverter as shown in Fig. 10. This construction is modified into special switch based configuration as shown in Fig. 10. Primarily, this configuration is focused on reducing the stress on power semiconductor devices and to eliminate the complimentary possibilities in the topology [59]–[66]. Level generating switch combinations are connected to any one side of the H-bridge circuit. Some other topologies employ special module based functional units to achieve higher output levels with reduced part count [67]–[76].

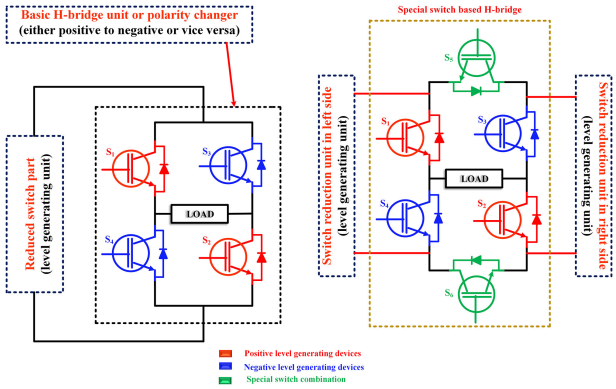

Fig. 10. Constructional view of polarity conversion used in MLI topologies.

Researchers are modifying the topologies by replacing the different switch, module, and bidirectional combinations [77]–[81]. In this section, the recent RSMLI topologies are to be reviewed based on the structure, combinations, and configuration of power semiconductor devices. In this article, RDC-MLI topologies, as proposed in [81]–[100], are evaluated. These topologies are enlisted as follows:

1) E-Type (Envelope type) inverter;
2) T-Type inverter;
3) submodule-based inverter;
4) RSMLI with and without H-Bridge inversion.

A. E-Type Inverter Topology

The primary introduction about the E-type topology has been described with the help of few classical topologies. In [82]–[85], a new constructional MLI topology, herewith referred to as the E-type MLI, have been reported. These topologies have less number of power device count compared to the conventional inverter topologies. A single-phase structure of the topology with two, three, and four sources are shown in Fig. 11.

E-type topologies can be easily modularized. Further, it can be employed in high power applications with lesser stress on semiconductor devices, involving optimal number of devices. Most of the E-type MLIs have the ability to generate both positive and negative output voltage levels without any H-Bridge at the output side. In Fig. 11, the level increment is possible by increasing the number of series and parallel switch combination in (a), (c), and series switch combination in topology (b). Addition of number of series connections is easy in topology (b).

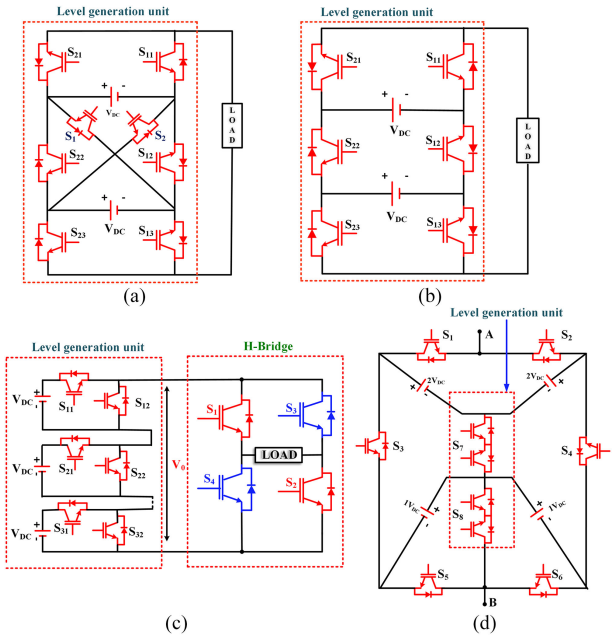

Fig. 11. (a) Topology proposed in [82]. (b) Topology proposed in [83]. (c) Topology proposed in [84]. (d) Topology proposed in [85].

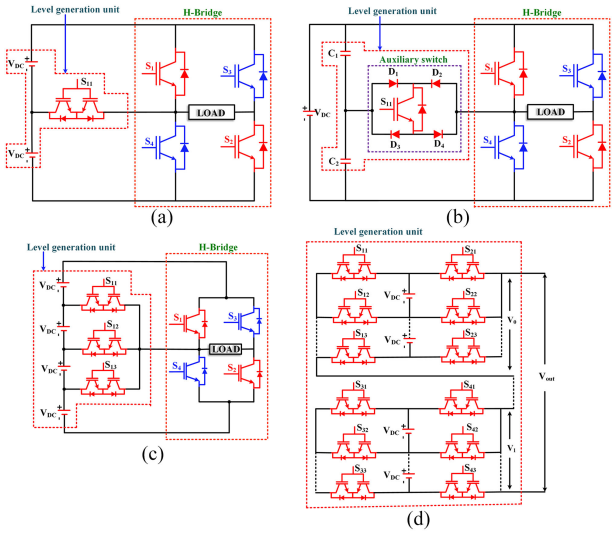

Fig. 12. (a) Topology proposed in [86]. (b) Topology proposed in [87]. (c) Topology proposed in [88]. (d) Topology proposed in [89].

Topology (a) is the basic structure of E-type MLI. This topology has been modified on the structure wise basis to yield (b), (c), and (d). (a), (b), and (c) topologies are made with unidirectional switches, whereas (d) topology is made with bidirectional switch with common emitter (CE) combination. Bidirectional switches are of two types, common collector (CC) and CE. CC type has comparatively higher switching losses and it needs two driver circuits to turn-ON the switch but in case of CE type, it requires single gate driver circuit to turn-ON the switch.

B. T-Type Inverter Topology

The primitive and expanded T-type topologies are explained with help of Fig. 12. In [86]–[89], authors have proposed new

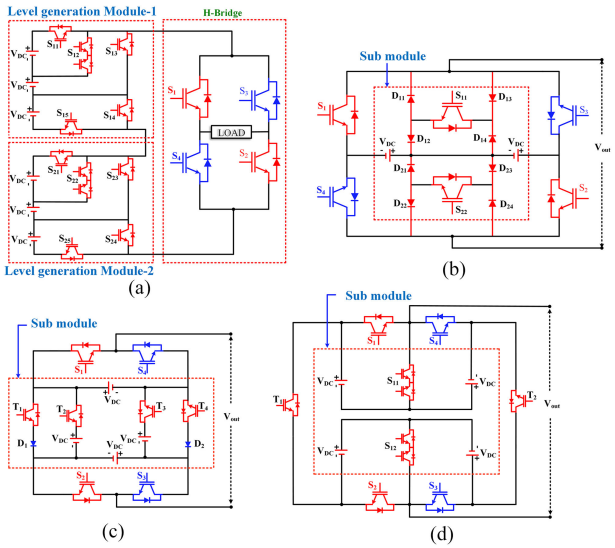

Fig. 13. (a) Topology proposed in [90]. (b) Topology proposed in [91]. (c) Topology proposed in [92]. (d) Topology proposed in [93].

multilevel inverter topologies, herewith referred to as the T-type inverter. Fig. 12, topology (a) is the basic structure of T-type MLI. It needs only one bidirectional switch in level generation structure of the MLI. Topology (b) is able to provide the five level output by using the auxiliary switch, four power switches, and only one center tap provided by the two capacitors.

This auxiliary switch performs the expected level generation, and it helps to produce the clean spectrum of the output voltage. Level increment of output voltage possibility depends on the number of parallel switches connected in T structure and number of series connected voltage sources as well as parallel capacitors. These topologies have bidirectional switch combination, because of the midpoint in topology it offers comparatively more stress on the switches. Topology (c) is basically a modified version of topology (a). Topology (d) has ability to generate both positive and negative output voltage without any H-bridge. (a), (b), and (c) have a common positive and negative output voltage generating unit H-Bridge, and level generation is achieved with bidirectional CE configuration semiconductor devices.

C. Submodule Based Topologies

In [90]–[93], different types of multilevel inverter topologies have been proposed as shown in Fig. 13. Each topology has unique consideration on the basis of the structure and configurations of power semiconductor devices. In Topology (a), the H-bridge circuit has been used in the backend of the submodule to change the polarity of the output voltage.

Each module has required voltage sources and unidirectional, bidirectional switches for the targeted output levels. Symmetrical operation of the multilevel inverter is obtained with equal dc sources. Number of levels increment in output voltage leads to increase in submodules and complementary conditions in the topology. The dc source values should be different from one submodule to another for asymmetrical operation of the MLI. In Fig. 13, topologies (b), (c), and (d) have submodules in the

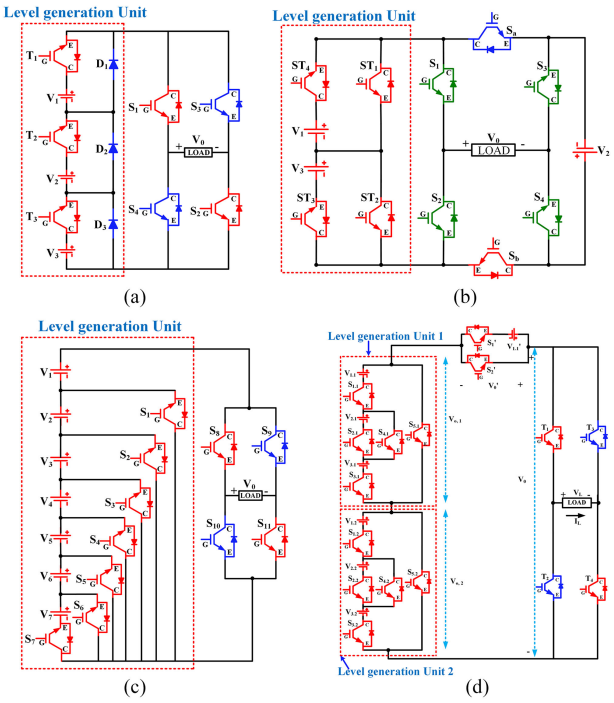

Fig. 14. (a) Topology I proposed in [94]. (b) Topology II proposed in [95]. (c) Topology III proposed in [96]. (d) Topology IV proposed in [97].

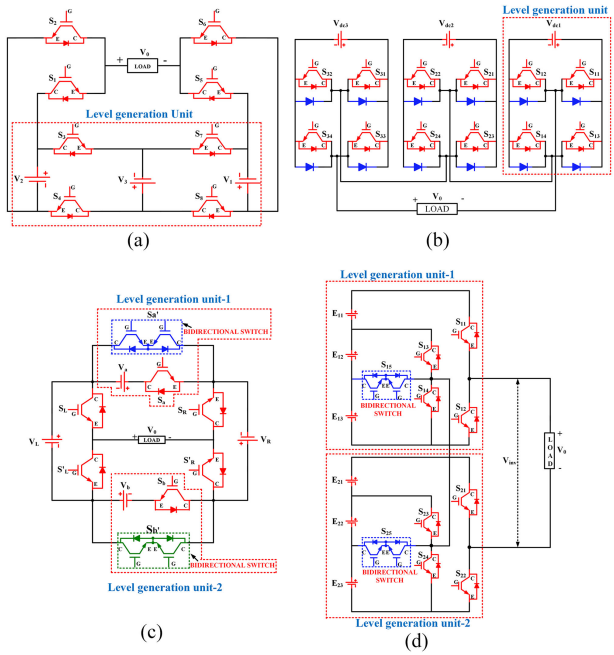

Fig. 15. (a) Topology V proposed in [98]. (b) Topology VI proposed in [99]. (c) Topology VII proposed in [100]. (d) Topology VIII proposed in [101].

middle portion of the H-bridge. Three different submodule configurations are presented, namely, power switch diode bridged, series and parallel switched, and parallel bidirectional switch based combinations. Possibility of the higher levels in output voltage can be achieved by the increment in modules. Topology (b) has the minimal sources structure with series connection to generate the output voltage. Topology (c) has several magnitude alternatives that are presented to generate levels in output voltage by employing series and parallel source combination. Topology (d) has the variety values of dc sources but only parallel combination and two bidirectional switches are used for the desired output levels.

D. RSMLI With and Without H-bridge Topologies

The primary introduction of the RSMLI topologies has been explained with the few topologies as shown in Figs. 14 and 15. Topologies, which are proposed with an exclusive claim of reducing the number of switches for the given phase voltage levels are referred to as reduced device count multilevel inverter topologies. These topologies are having more flexibility and compatibility in the view of number of power semiconductors, sources, and level extension. The RSMLI topologies are categorized by the input source configuration. MLIs with input voltage of same values are classified as symmetric topologies and input voltage of unequal values are classified as asymmetric configuration. In the asymmetric source configuration, two popular types are binary and trinary. Binary configuration voltage level values are with a geometric progression factor of 2 (i.e., V_{DC}, $2V_{\mathrm{DC}}$, $4V_{\mathrm{DC}}$, $8V_{\mathrm{DC}}$ … …). In trinary configuration, geometric progression factor is 3 (i.e., V_{DC}, $3V_{\mathrm{DC}}$, $9V_{\mathrm{DC}}$, $27V_{\mathrm{DC}}$ … …).

Asymmetric topologies are employed to synthesize more output levels with the same number of switches. According to the output conversion system, the topologies are divided into two types one is with H-bridge and without H-bridge topologies.

1) With H-Bridge: H-bridge RSMLI topologies in [94]–[97], as shown in Fig. 14, present the reviewed topologies from I to IV. The performance of the RSMLI depends on the switch positioning in the circuit. Switch positioning is one of the performance effecting factors in RSMLI topologies. So, the researchers have developed different types of switch positioning in topologies. This positioning facilitates the inverter to produce the required number of levels in output voltage.

These switch connections make a separate unit called level generation unit. These circuits are not capable to produce the +ve and –ve polarities. The generation of both +ve and –ve polarities is possible by using the H-bridge from the back end of the level generation unit. Fig. 14, topology (a) consists of seven unidirectional switches with antiparallel diode (T_1, T_2, T_3, S_1, S_2, S_3, S_4) and three dc voltage sources (V_1, V_2, and V_3). Topology (b) consists of ten unidirectional switches with three dc sources (V_1, V_2, and V_3). Topology (c) consists of eleven unidirectional switches with seven dc sources (V_1, V_2, V_3, V_4, V_5, V_6, V_7). Topology (d) consists of sixteen unidirectional switches with seven dc sources (V_1, V_2, V_3, V_4, V_5, V_6, V_7). The source magnitude of each topology (V_1: V_2: V_3 …: V_n) should be in the binary asymmetrical ratio (1:2:4 …n) to generate positive and negative levels in output voltage. Topologies (a), (b), and (c) have a fewer number of power semiconductor devices compared with topology (d). Topology (b) has fewer number of dc sources compared with other topologies (a), (c), and (d). The performance of the RSMLI depends on the power devices count in level generation unit and conversion module of the topology.

If the number of levels increases, the number level conversions are added into the operation of H-bridge, and it leads to the life time deduction of the power semiconductor device. To overcome this problem in MLIs, the researchers have introduced RSMLI without H-bridge.

2) Without H-Bridge: Here, RSMLI without H-bridge topologies are discussed, which are proposed in [98]–[101], as shown in Fig. 15. All topologies are capable of producing the +ve and –ve polarities in output voltage. This type of topologies have the special switch configuration for producing the +ve and –ve polarities of output voltage. Switch configuration of the topology polarity conversion system depends on the generation of number of levels. If the number of levels increases, the maximum turn ON period will increase for each switch or main switches. The number of dc sources and number of level generation capability of the topology will decide the switch configuration. In this type of topologies, unidirectional or bidirectional are the widely used configurations for polarity conversion. It depends on the topology voltage rating and number of levels generation. Unidirectional switches are employed in low power applications and bidirectional switches are employed in high power applications for level generation circuits.

Two types of configured topologies are shown in Fig. 15, topologies (a) and (b) are low voltage rating, and topologies (c) and (d) are high voltage rating RSMLIs. Topology (a) consists of eight unidirectional switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8). Switching combinations of this inverter (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) should not be turned ON simultaneously, because it leads to short circuit of voltage sources. Topology (b) consists of twelve unidirectional switches (S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24}, S_{31}, S_{32}, S_{33}, and S_{34}). Switching combinations of this inverter (S_{11}, S_{12}), (S_{13}, S_{14}), (S_{21}, S_{22}), (S_{23}, S_{24}), (S_{31}, S_{32}), and (S_{33}, S_{34}) should not be turned ON simultaneously because of it leads to a short circuit of voltage sources.

In topologies (a) and (b), magnitude of each voltage source (V_1 V_{dc1}: V_2 V_{dc2}: V_3 V_{dc3}) should be in asymmetrical ratio (1:2:5) to generate positive and negative levels in the output voltage. Topology (a) has fewer number of power semiconductor devices compared with topology (b). Topology (c) consists of four dc sources (V_R, V_L, Va, and V_b) and the magnitude of the dc sources are $V_L = V_{dc}$, $V_R = 2\,V_{dc}$, $V_a = V_b = 4\,V_{dc}$. There are eight switches (S_L, S'_L S_R, S'_R , S_a, S'_a , S_b, and S'_b). The switches of (S_L, S'_L), (S_R, S'_R), (S_a, S'_a), (S_b, S'_b), (S_L, S_R, S_a) and (S'_L , S'_R, S_b) acts as in complementary mode. Topology (d) consists of six dc sources (E_{11}, E_{12}, E_{13}, E_{21}, E_{22}, and E_{23}) magnitude of the dc sources $E_{11} = E_{12} = E_{13} = V_{dc}$, and $E_{21} = E_{22} = E_{23} = 2V_{dc}$. It includes ten switches (S_{11}, S_{12}, S_{21}, S_{22}, S_{13}, S_{23}, S_{14}, S_{24}, S_{15}, S_{25}).

Topologies (c) and (d) involve two bidirectional switches. The bidirectional switches consist of two IGBTs, power diodes, and driver circuit with CE structure being used. Topology (c) has fewer power semiconductor devices compared with topology (d). The constructional details of the reviewed topologies are tabulated below in Table II.

From Table II, the constructional details of the reviewed topologies are consolidated. Many RSMLI topologies are considered for the exhaustive constructional and operational analysis. The constructional comparison of the reviewed topologies from I to VIII have been presented in a pictorial fashion for better understanding in the below Fig. 16.

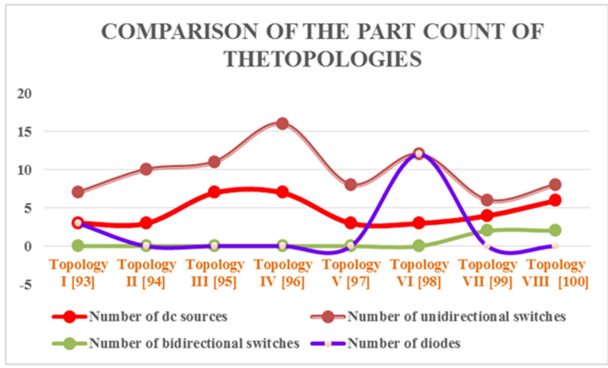

Fig. 16. Comparison of part count for the RSMLI topologies.

From the Fig. 16, it is observed that Topology IV has more number of switches and voltage sources, Topology VII has less number of switches and voltage sources compared with all other topologies. Topology I is configured with the power switch and diode, part count of the topology has been presented in the Table II. Increase in the number of power devices leads to the more conduction time and more losses involved with each switch. The next parameter to be considered is the switching losses. Switching losses depends on the turn-ON and turn-OFF times of the switch. But before presenting the switching losses it is necessary to observe the turn-ON times of the switches in each individual topology. Comparison between the turn-ON times of the switches in each individual topology is presented in Fig. 17. The total turn ON times can be logically obtained from the respective truth tables of each topology. For each switch, total turn ON time for each cycle can be manually calculated from the truth table. If the switch conducts for more number of times its performance is degraded. It may increase the switching losses.

From the Fig. 17, it is observed that the Topologies I and V provide similar active modes for all the switches. The Topology IV has more number of devices and out of the all switches five switches (S_1, S_2, S_3, S_6, and S_{10}) are being active for a longer duration. The Topology VIII half the switches are (S_5–S_8) less active in the functioning of the inverter. From the pictorial data of the active modes of switches as in Fig. 17, Topologies III and VII have been found to involve fewer active modes compared to all other topologies. In the next section the performance analysis of the reviewed RMLI topologies has been evaluated based on the assessment parameters reliability and cost function as explained in Sections II and III of this article, respectively.

V. Performance Analysis of Multilevel Inverter Topologies

In this section, performance analysis of the RMLI topologies has been assessed in terms of switching losses, cost function, and reliability. The reliability necessary calculations have been explained in Section II. The performance evaluation of the RMLI topology is mainly dependent on the switching losses. During the switching operations, the voltage and current are assumed to have a linear profile. Based on this assumption the switching

TABLE II
CONSTRUCTIONAL FORMULATION DETAILS OF THE TOPOLOGIES

Topology	Literature	Number of unidirectional switches	Number of bidirectional switches	Number of driver circuits	Minimum offered THD	Blocking voltages
Cascaded H-bridge	Proposed[49]-[80]	$6(n_{level}-1)$	-	$\frac{4n_{level}}{2}$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$6[(n_{level}-1)]$
	Proposed [81]	$2(n_{level}+1)$	$(n_{level}+1)$	$\frac{2(n_{level}+1)}{2}$		$2\sum_{j=1}^{k} V_{stage,j}.$
	Proposed [82]	$3(n_{level}+1)$	-	$3(n_{level}+1)$		$\sum_{j=1}^{k} V_{stage,j}.$
T-Type MLI	Proposed [83]	$(2n_{level}+4)$	$\frac{(2n_{level}+4)}{2}$	$(n_{level}+4)$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$2\sum_{j=1}^{k} V_{stage,j}.$
	Proposed [84]	$4n_{level}$	$\frac{2(n_{level}+1)}{\ln[n(n+1)+1]}$	$\frac{4n_{level}}{2}$		$\sum_{j=1}^{k} V_{stage,j}.$
	Proposed [85]	4(Nsource)	-	$\frac{2\ln[2(n_{level}+1)]}{\ln 2}$		
	Proposed [86]	$(n_{level}+2)$	-	$\frac{8(n_{level}-1)}{6}$		
E-Type MLI	Proposed [87]	$\frac{n_{level}-2}{2}$	-	$\frac{2\ln[2(n_{level}+1)]}{\ln 2}$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$\frac{N_{level}}{5}\times V$
	Proposed [88]	$\frac{5(n_{level}-1)}{6}$	$\frac{n_{level}}{2}$	$\frac{8(n_{level}-1)}{6}$		
	Proposed [89]	$(n_{level}+3)$	$(2n_{level}m_{source}+4)$	$\frac{(n_{level}+2)}{2n}(n_{level}-1)+4$		
Sub module MLI	Proposed [90]	$6n_{level}$	-	$(n_{level}+1)$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$\frac{V_{std}}{2nV_{dc}}$
	Proposed [91]	$8n_{level}$	-	$8n_{level}$		
	Proposed [92]	$\frac{10(n_{level}-1)}{8}$	$(n_{level}-1)$	$8n_{level}$		
	Proposed [93]	$(n_{level}+4)$	-	$\frac{2n_{level}}{4}$		
RSMLI With H-Bridge	Proposed [94]	$(n_{level}-5)$	-	$\frac{(n_{level}+5)}{2}$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$(2\ln+6)V_{dc}$
	Proposed [95]	$\frac{(n_{level}-1)}{2}$	-	$\frac{2(n_{level}-2)}{2}$		
	Proposed [96]	$(5n_{level}+6)$	-	$(5n_{level}+6)$		
	Proposed [97]	$\frac{(n_{level}+1)}{2}$	-	$\frac{2n_{level}+2}{4}$		
Without H-bridge	Proposed [98]	$(n_{level}-3)$	-	$\frac{2(n_{level}-3)}{2}$	$\sqrt{\left(\frac{V_{0rms}}{V_{01}}\right)^2-1}$	$\left(\frac{N_{level}-2}{6}+1\right)\times V_{dc}$
	Proposed [99]	$(8n_{level}+2)$	$\frac{(n_{level}-3)}{6}$	$(6n_{level}+2)$		
	Proposed [100]	$\frac{(n_{level}+5)}{2}$	$\frac{(n_{level}-3)}{6}$	$\frac{(2n_{level}+6)}{3}$		

losses can be obtained using the following:

$$E_{on} = \frac{V_{\mathrm{IGBT}}.I.t_{\mathrm{on}}}{6} \tag{9}$$

$$E_{\mathrm{off}} = \frac{V_{\mathrm{IGBT}}.I.t_{\mathrm{off}}}{6} \tag{10}$$

$$\mathrm{Thepowerswitchinglosses} = \frac{1}{\mathrm{T}}(N_{\mathrm{on}}E_{\mathrm{on}} + N_{\mathrm{off}}E_{\mathrm{off}}). \tag{11}$$

The comparison of switching losses for the reviewed RSMLI topologies has been shown in Table III.

From Table III, it is evident that the losses occurred in each topology with respect to each device keeps varying. In Topology III, the losses keep on increasing from S_1 to S_{11} and this results in the higher switching losses with respect to each switch. From the individual device point of view, Topology VII provides lesser switching losses compared with the all other topologies. The next parameter to be considered is the total switching losses and cost function of the each topology as shown in Table IV. The total switching losses for each topology is obtained by

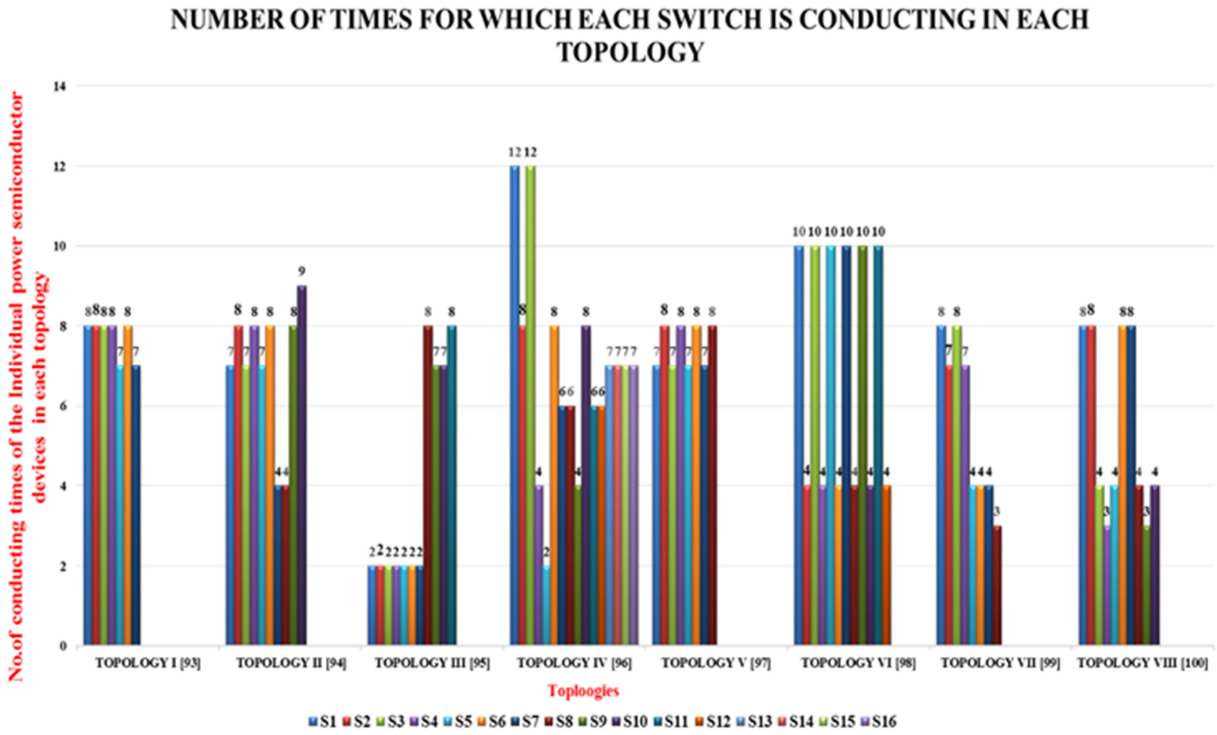

Fig. 17. Switching operations of the individual switch in each topology.

TABLE III
SWITCHING LOSSES OF EACH DEVICE IN EIGHT TOPOLOGIES

S. No	S_1 w-sec	S_2 w-sec	S_3 w-sec	S_4 w-sec	S_5 w-sec	S_6 w-sec	S_7 w-sec	S_8 w-sec	S_9 w-sec	S_{10} w-sec	S_{11} w-sec	S_{12} w-sec	S_{13} & S_{14} w-sec	S_{15} & S_{16} w-sec
Topology I [93]	0.0009	0.0587	0.368	0.0090	0.0090	0.1936	0.1936	-	-	-	-	-	-	-
Topology II [94]	0.0003	0.0003	0.0003	0.0003	0.0044	0.0044	0.0002	0.0006	0.0095	0.012	-	-	-	-
Topology III [95]	**0.0964**	**0.0273**	**0.144**	**0.379**	**0.3924**	**0.3093**	**0.5665**	**0.1086**	**1.897**	**1.897**	**1.897**	**-**	**-**	**-**
Topology IV [96]	0.0019	0.0006	0.0026	0.0005	0.0001	0.0011	0.0009	0.0019	0.0005	0.0019	0.0009	0.0015	0.0032	0.0032
Topology V [97]	0.8251	0.0045	0.0119	0.0072	0.0001	0.00015	0.0058	0.0064	-	-	-	-	-	-
Topology VI [98]	0.0035	0.0005	0.0035	0.0005	0.0081	0.0027	0.0081	0.0027	0.0162	0.0336	0.0162	0.0336	-	-
Topology VII [99]	**0.0006**	**0.0088**	**0.0093**	**0.0095**	**0.0002**	**0.00054**	**0.2429**	**0.0005**	**-**	**-**	**-**	**-**	**-**	**-**
Topology VIII [100]	0.0959	0.0959	0.0225	0.0057	0.0114	0.0959	0.0959	0.0225	0.0057	0.0114	-	-	-	-

TABLE IV
TOTAL SWITCHING LOSSES AND COST FUNCTION OF EIGHT TOPOLOGIES

S. No	Total Switching Losses W-Sec	Total Switching Losses in %	Cost Function of MLI Per Unit =1
Topology I [93]	0.832	83.28	30.815
Topology II [94]	0.323	32.3	28.15
Topology III [95]	0.91	91	32.635
Topology IV [96]	**0.935**	**93.5**	**76.5**
Topology V [97]	0.861	86.12	26.15
Topology VI [98]	0.89	89	48
Topology VII [99]	**0.270**	**27.03**	**28.075**
Topology VIII [100]	0.426	42.6	54

summing up the individual switching losses. Cost function of the MLI depends on the number of components used in a specific topology. For arriving at the numerical values of the cost function in Table 4, the equations through (3) to (8) in Section III have been employed.

Total switching losses and cost function of the each topology is presented in Table IV. Among all the topologies, Topology VII seems to provide the least percentage of switching losses, and the Topology IV has the highest percentage of switching losses. With regard to the cost function, Topology IV found to

TABLE V
SWITCH MODELS USED FOR RELIABILITY ANALYSIS FOR THE EIGHT TOPOLOGIES

S. No	Model Number(switch)	Voltage Rating (V)	Current Rating (A)	Junction Temperature(°C)	Considered Material
Topology I [93]	**MG0675S-BN4MM**	**600**	**75**	**175**	**JANTX**
Topology II [94]	FGA180N30D	300	30	150	JANTX
Topology III [95]	FGA180N30D	300	30	150	JANTX
Topology IV [96]	**MG0675S-BN4MM**	**600**	**75**	**175**	**JANTX**
Topology V [97]	FGA180N30D	300	30	150	JANTX
Topology VI [98]	FGA180N30D	300	30	150	JANTX
Topology VII [99]	FGA180N30D	300	30	150	JANTX
Topology VIII [100]	FGA180N30D	300	30	150	JANTX

TABLE VI
FAILURE RATE OF EACH DEVICE IN EIGHT TOPOLOGIES

S.NO	S_1 $\lambda_b/10^6$ hours	S_2 $\lambda_b/10^6$ hours	S_3 $\lambda_b/10^6$ hours	S_4 $\lambda_b/10^6$ hours	S_5 $\lambda_b/10^6$ hours	S_6 $\lambda_b/10^6$ hours	S_7 $\lambda_b/10^6$ hours	S_8 $\lambda_b/10^6$ hours	S_9 $\lambda_b/10^6$ hours	S_{10} $\lambda_b/10^6$ hours	S_{11} $\lambda_b/10^6$ hours	S_{12} $\lambda_b/10^6$ hours	S_{13} & S_{14} $\lambda_b/10^6$ hours	S_{15} & S_{16} $\lambda_b/10^6$ hours
Topology I [93]	**12**	**12**	**12**	**6**	**6**	**6**	**6**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
Topology II [94]	0.081	0.081	0.0162	0.0162	0.0141	0.0141	0.0141	0.0141	0.0141	0.0283	-	-	-	-
Topology III [95]	0.168	0.168	0.168	0.168	0.168	0.168	0.168	0.672	0.588	0.588	0.672	-	-	-
Topology IV [96]	**0.0274**	**0.0182**	**0.0274**	**0.0914**	**0.045**	**0.0182**	**0.0137**	**0.0137**	**0.0914**	**0.0182**	**0.09**	**0.09**	**0.1**	**0.1**
Topology V [97]	0.588	0.672	0.588	0.588	0.672	0.672	0.588	0.672	-	-	-	-	-	-
Topology VI [98]	0.202	0.081	0.202	0.081	0.202	0.081	0.202	0.081	0.202	0.081	0.202	0.081	-	-
Topology VII [99]	**0.3361**	**0.3361**	**0.672**	**0.672**	**0.3361**	**0.252**	**0.588**	**0.588**	**-**	**-**	**-**	**-**	**-**	**-**
Topology VIII [100]	0.164	0.164	0.0841	0.0127	0.0841	0.164	0.164	0.0841	0.0127	0.0841	-	-	-	-

be more expensive due to its higher part count. Also it can be seen from the table that Topology V has less estimated cost represented in terms of per unit value but in terms of switching losses the performance is not satisfactory. The next parameter to be considered is the switch selection for the topologies. Selection of the switch model is one of the most important factors for the design and implementation. The switch models considered for all eight topologies are shown in Table V.

It can be observed from the table that, in Topologies I and IV, higher rating switches are used. The next parameter to be considered is the failure rate. In any system first problem is the failure rate of the product. When the failure rate is more the life of the product will be reduced. Failure rate of MLI depends on the total conduction period of the switches involved in the operation of MLI. Failure rate of the each device in the topologies is as shown in Table VI. For arriving at the numerical values of the component level failure rate in Table VI, (12), and (13) have been employed. The various factors which are considered for the failure rate calculation are listed in Table I. These calculations are based on the bottom up statistical method given in Table I

$$\text{Failure rate of the product } = \lambda = \sum_{i=1}^{n} N_i.\lambda_i \qquad (12)$$

$$\text{where } \lambda_{\text{p}} = \lambda_b.\pi_T.\pi_Q.\pi_E.\pi_R.\pi_S. \qquad (13)$$

From Table VI, it is observed that in Topology IV each switch has lesser individual failure rate but the part count involved is more. Topology I has less number of components but the individual component have a greater failure rate. It can be concluded that Topology VII employs fewer number of devices and still provides a better reliability with regard to individual switches. The next parameter to be considered is the total failure rate and reliability. Reliability is totally dependent on the device involved in the operation of MLI in a particular time interval. The total failure rate for all the eight considered topologies are compiled in Table VII. For evaluating the overall reliability of the individual topologies has been employed as follows:

$$\lambda_T = \frac{\text{sum of the failure rate}}{100} + \text{reliability constant.} \qquad (14)$$

From the compiled results of the table, it is revealed that the Topology VII has a better reliability compared to all other schemes. Also, it is clear from the results that the Topology IV has poor reliability compared to all other topologies. To consolidate the quantitative analysis in this work, a pictorial presentation of all the assessment parameters has been explored as below in Fig. 18.

Assessment parameters are explained in Section II according to that all the figure of merits such as switching losses, cost function, and reliability of various considered topologies are plotted in the form of radar chart as in Fig. 18. From the results, it is clear that Topology VII seems to outperform all the other topologies. Total harmonic distortion (THD) and blocking voltage have been considered for all the topologies and tabulated in Table VIII.

In order to have a better picture Table VIII, data have been presented pictorially in Fig. 19. From the results, it can be observed that Topology II provides the least THD, whereas from blocking voltage aspect Topology III has the maximum blocking voltage capability. The new proposed 15-level inverter has been discussed in the next section.

VI. NEW PROPOSED 15-LEVEL MLI

Among all the reviewed topologies, Topology VII found to be one of the promising solution for RSMLI. This has been proven from the various figures of merits, which are tabulated in the previous section. Now, as a contribution a new RSMLI

TABLE VII
TOTAL FAILURE RATE OF EIGHT TOPOLOGIES

S.NO	Failure Rate of the Multilevel Inverter W-Sec	Reliability in Terms of Failure Rate of the Multilevel Inverter in %
Topology I [93]	0.60	60
Topology II [94]	0.42	42
Topology III [95]	0.40	40
Topology IV [96]	**0.94**	**94**
Topology V [97]	0.504	50.4
Topology VI [98]	0.698	69.8
Topology VII [99]	**0.37**	**37.80**
Topology VIII [100]	0.52	52

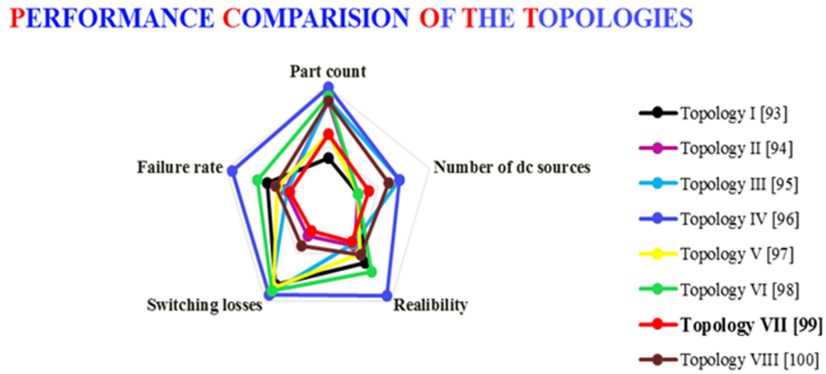

Fig. 18. Performance comparison of MLI topologies.

TABLE VIII
THD AND V_{BLOCK} OF THE REVIEWED TOPOLOGIES

S. No	THD%	V_{BLOCK} (V)
Topology I [93]	6.03%	180
Topology II [94]	4.63%	100
Topology III [95]	7.58%	400
Topology IV [96]	6. 9%	120
Topology V [97]	5.4%	120
Topology VI [98]	6.69%	150
Topology VII [99]	6.91%	165
Topology VIII [100]	7.01%	200

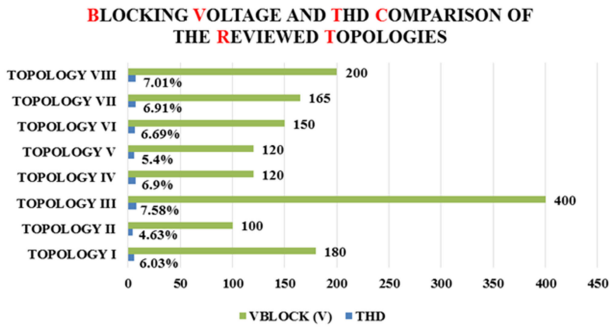

Fig. 19. Blocking voltage and THD comparison of the reviewed topologies.

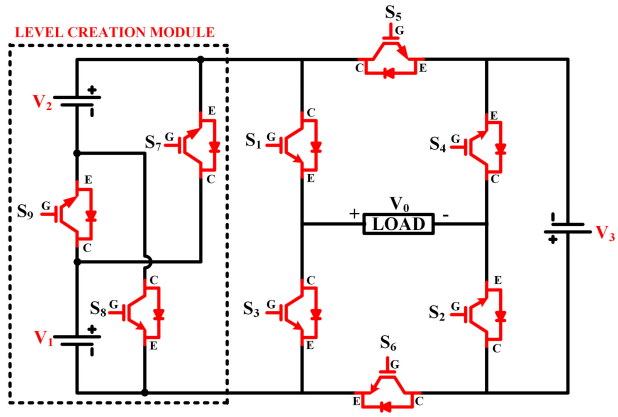

Fig. 20. Constructional view of the proposed 15-level inverter.

topology with 15-level output has been proposed and is shown in Fig. 20. The proposed topology has been validated in MATLAB/ Simulink environment and the results are presented. The proposed topology has been compared with the Topology VII in terms of various performance indices like part count, cost function, and reliability, etc. The main advantage of the proposed topology is that it eliminates the expensive bidirectional switches.

The simultaneous turn-ON of (S_1, S_3), (S_2, S_4), (S_5, S_6), (S_7, S_8), (S_7, S_9), (S_8, S_9), and (S_7, S_8, S_9) causes the voltage sources to short-circuit. Therefore the simultaneous turn-ON of the mentioned switches must be avoided. The detailed switching table for the proposed inverter is as shown in Table IX.

In Table IX, 1 and 0 indicates the ON and OFF states of the switches, respectively. The magnitude the dc voltage sources V_1: V_2: V_3 should be in the ratio of 1: 2: 4 to generate all positive and negative levels in output voltages. In this condition the maximum

TABLE IX
SWITCHING TABLE OF PROPOSED FIFTEEN-LEVEL INVERTER

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$1V_{dc}$	1	1	0	0	0	1	1	0	0
$2V_{dc}$	1	1	0	0	0	1	0	1	0
$3V_{dc}$	1	1	0	0	0	1	0	0	1
$4V_{dc}$	0	0	1	1	0	1	0	0	0
$5V_{dc}$	1	0	1	0	0	1	1	0	0
$6V_{dc}$	1	0	1	0	0	1	0	1	0
$7V_{dc}$	1	0	1	0	0	1	0	0	1
$-1V_{dc}$	0	0	1	1	1	0	1	0	0
$-2V_{dc}$	0	0	1	1	1	0	0	1	0
$-3V_{dc}$	0	0	1	1	1	0	0	0	1
$-4V_{dc}$	1	1	0	0	1	0	0	0	0
$-5V_{dc}$	0	1	0	1	1	0	1	0	0
$-6V_{dc}$	0	1	0	1	1	0	0	1	0
$-7V_{dc}$	0	1	0	1	1	0	0	0	1

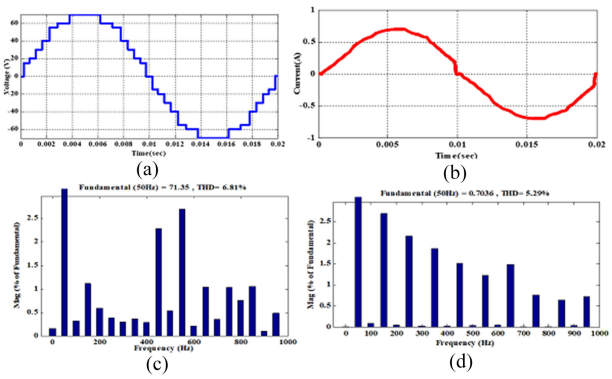

Fig. 21. (a) Output voltage. (b) Output current. (c) Voltage THD. (d) Current THD.

output voltage level is calculated as follows: $V_{0\ \max} = V_1 + V_2 + V_3 = 7V_{\rm dc}$

In general, for the proposed topology in this article, the number of dc sources ($N_{\rm sources}$), number of switches ($N_{\rm switches}$), and number of output voltage levels ($N_{\rm step}$) are given through (15) to (17). It consists of $2n$ unidirectional power switches and n number of dc voltage sources

$$N_{\rm source} = n \tag{15}$$

$$N_{\rm switch} = 2n + 3 \tag{16}$$

$$N_{\rm step} = 2^{n+1} - 1 \tag{17}$$

where n is the number of dc voltage sources used in the proposed topology. The ability of the proposed topology to generate the all positive and negative level in output voltage has been validated using simulation results. Simulations results are obtained in MATLAB environment. In The simulation studies, the proposed 15-level inverter has been operated with an inductive load, with a value of $R = 100\ \Omega$ and $L = 55$ mH. It is operated with a switching frequency 2 kHz and frequency of output voltage is 50 Hz. Simulation results of the proposed topology as shown in Fig. 21.

Output wave form of the phase voltage for proposed 15-level inverter as shown in Fig. 21(a) and it is confirmed that proposed topology can generate all positive and negative levels. Output phase current is as shown in Fig. 21(b). THD analysis for phase output voltage and phase output current is shown in Fig. 21(c) and (d). THD in output voltage is 6.81% and output current

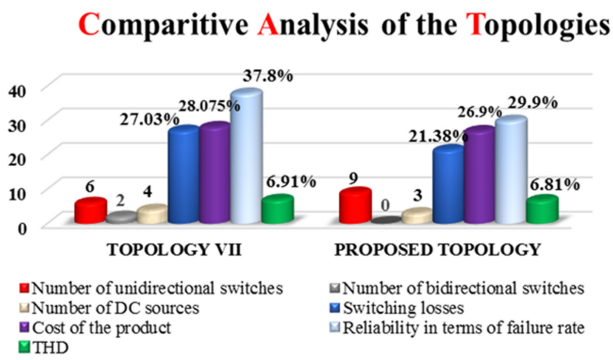

Fig. 22. Comparison of the proposed topology with Topology VII.

TABLE X
IMPACT OF $F_{\rm S}$ ON THE RELIABILITY OF THE INVERTER

S.NO	Realiability interms of failure rate of the topologies at different frequencies W-sec			
	2 kHz	10 kHz	15 kHz	20 kHz
Topology VII	0.37	0.74	4.114	41.142
Proposed Topology	**0.177**	**0.377**	**1.956**	**19.56**

is 5.29%. The constructional and observational results of the proposed topology have been compared with the Topology VII as shown in Fig. 22.

From Fig. 22, it is observed that in the constructional point of view there are two major differences between proposed topology and Topology VII. First, to generate the expected voltage levels in output with proposed topology possible by using the lesser dc voltage sources than Topology VII. Second, in the construction and operation of Topology VII, six unidirectional and two bidirectional switches are involved, but in the proposed topology, nine unidirectional switches are involved, so that the cost of the proposed topology is lesser than the Topology VII. To conclude, the proposed topology offers lesser switching losses, THD and higher reliability than Topology VII. For any inverter, cost and reliability are the two prime factors from industrial deployment perspective. Also, it is well proven that the proposed topology is having a lesser cost with better reliability, which makes it suitable for commercial applications.

A. Influence of Switching Frequency and Duration on Time on the Reliability of Inverters

The failure rate of the power semiconductor device is dependent on the switching frequecy (f_s) of the inverter. The increase in switching frequency may lead to higher failure rates in MLI. In order to analyze the impact of higher PWM frequencies on the reliability factor of the MLI, the failure rate for different switching frequencies have been tabulated in Table X.

It can be observed from the table that the proposed topology provides lesser failure rate at different frequencies compared with Topology VII, and hence ensures better reliability. Hence, it is evident from the analysis that as the switching frequency increases, the reliability decreases.

The maximum possible reliability of the MLI is decided based on the utility load and duration on time. To figure out the influence of duration on time on the reliability parameter, a

TABLE XI
IMPACT OF DURATION ON TIME ON THE ANNUAL RELIABILITY OF THE INVERTER

S.No	Reliability in terms of Failure rate per year											
No.of operating days/year	365 days			365 days			365 days			365 days		
Operating Frequency	2 kHz			10 kHz			15 kHz			20 kHz		
Operating hours/day	6h	12h	24h	6h	12h	24h	6h	12h	24h	6h	12h	24h
Topology VII	0.095	0.18	0.37	0.185	0.37	0.74	1.02	2.05	4.114	10.2	20.5	41.4
Proposed Topology	**0.0078**	**0.01**	**0.177**	**0.095**	**0.18**	**0.37**	**0.4**	**0.9**	**1.95**	**4.8**	**9.75**	**19.5**

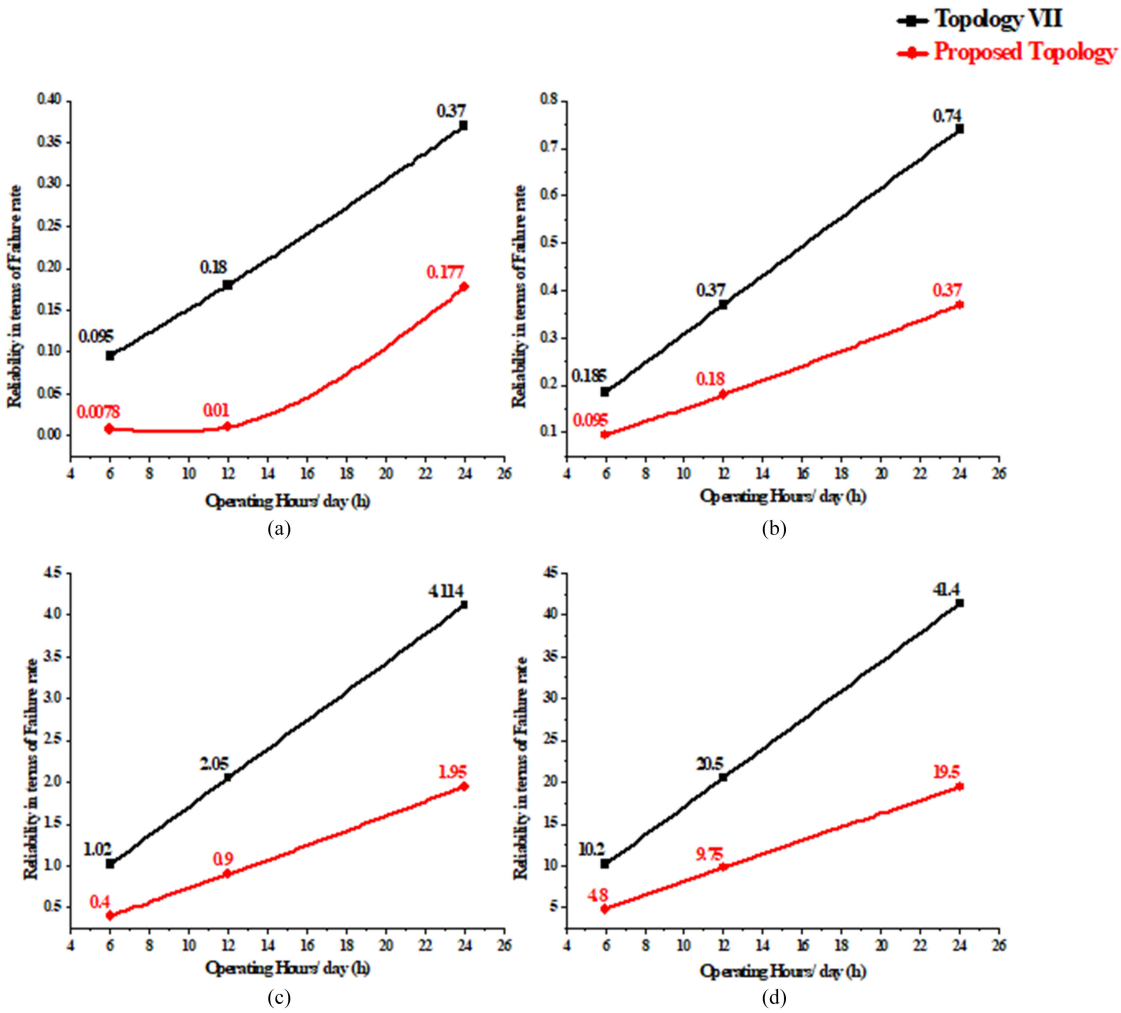

Fig. 23. Reliability comparison at different frequencies of the topologies. (a) 2 kHz. (b) 10 kHz. (c) 15 kHz. (d) 20 kHz.

detailed quantitative analysis has been carried out and presented. For this, the duration on time has been varied as 6, 12, and 24 hours and the respective annual reliability has been evaluated for varying switching frequency. For the different duration on times, the annual reliability of the Topology VII and proposed topology have been compiled in Table XI. For evaluating the duration on time of the individual topologies (18) has been employed

$$\text{Duration on time} = \sum_{i}^{\text{phase}} \frac{\text{Annual time phase}}{8760} \times \lambda_{\text{phase}}. \quad (18)$$

The considerd annual time of the MLI is 365 d (1 year) for varrious ON time (hours) and switching frequencies (kHz). The inductive load with the value of $R = 100\ \Omega$ and $L = 55$ mH has been considered for the reliability analysis. According to the Table XI compiled results, proposed topology has a better reliability compared with Topology VII. To consolidate, the quantitative analysis has been presented pictorially as shown in Fig. 23.

Based on the quantitative analysis the graphs are plotted with different duration on time for a fixed switching frequency as

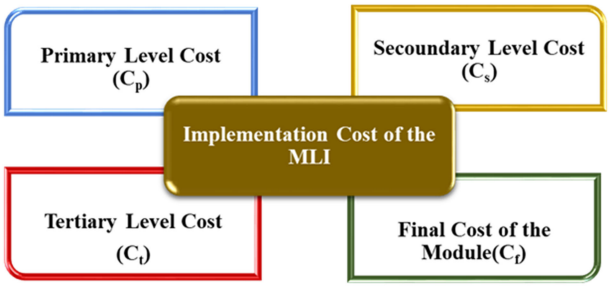

Fig. 24. Cost effecting factors of the MLI implementation.

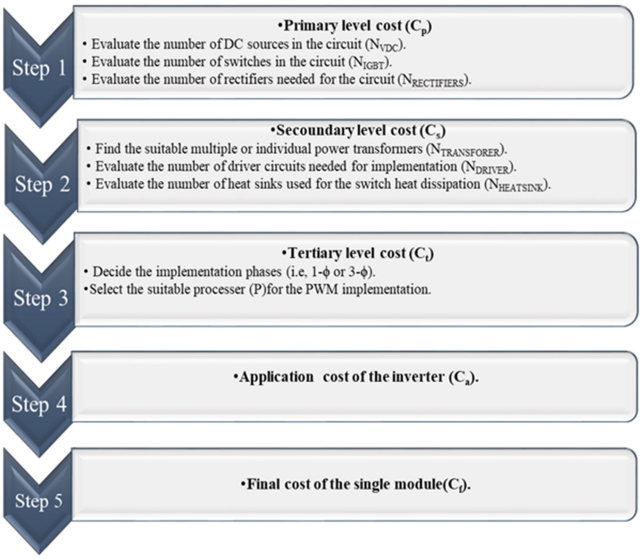

Fig. 25. Cost effecting factors of the MLI implementation.

shown in Fig. 23. From the results it is evident that the proposed topology has a lesser failure rate than the Topology VII at different frequencies. The maximum failure rate of the proposed topology at 20 kHz is ± 19.5 h. The reliability of the MLI plays a vital role in the process of procurement of the components for the implementation process. The implementation cost evaluation of the MLI has been explained in the below section.

B. Implementation Cost of the MLI

The implentation cost of the MLI depends on the number of components involved in the specific module. The number of components involved mainly influences the implementation cost of the MLI. The various factors that are to be accounted for estimating the implementation cost of the MLI are presented in the Fig. 24.

In order to have a clear picture, the implementation cost of the multilevel inverter has been divided in to four levels namely, primary level cost (C_p), secondary level cost (C_s), tertiary level cost(C_t), and final cost of the module (C_f). The sequence of steps adopted for evaluating the implementation cost of the MLI has been pictorially provided in the Fig. 25.

From Table XII, it is obseved that the estimation and implementation cost for the Topology VII is more expensive than the proposed topology due to the special switched configuration and

TABLE XII
IMPLEMENTATION COST COMPARISON OF THE PROPOSED TOPOLOGY WITH TOPOLOGY VII

S. No	Estimation Cost of MLI Per Unit = 1	Implementation cost Per Unit = 1	Implementation cost of the MLI Dollar($)
Topology VII	28.075	46	179.50$
Proposed Topology	**26.9**	**41**	**160.39$**

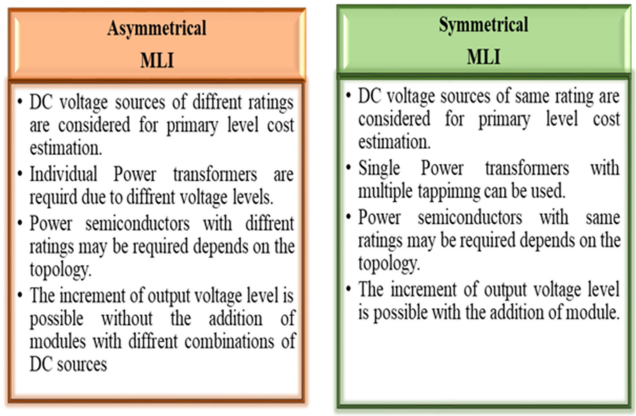

Fig. 26. Difference in cost effecting factors in asymmetric and symmetric MLI.

more number of dc sources. Table XII provides the implementation level cost has been presented in per unit as well as in dollars. The cost of the MLI depends on the configuration of the topology. Estimating the cost in the case of asymmetric MLI is different from other types of MLIs. The differences are listed in Fig. 26.

VII. CONCLUSION

In this work, eight recent reduced count asymmetric MLI topologies have been considered. To make a common platform for comparison, all the inverters are selected with 15 level output profile. Before implementing in real time, it is important to figure out which topology will be superior with regard to various performance parameters. The major assessment parameters that are projected in this work include switching losses, cost function, and reliability. The empirical means of calculating these parameters are presented in detail and the same procedure is carried out for all the eight topologies. The exhaustive quantitative review is performed and the results are presented for each topology.

According to the standards of the Military handbook 217 maximum 40% of failure rate products are eligible for the industrial applications. Maximum 46% of failure rate products are eligible for the residential applications. Maximum 44% of failure rate products are eligible for the commercial applications. From the exhaustive quantitative analysis, the following observation can be deduced. Topology I has fewer number of switches, but the conduction time is quite more with regard to each device. Though Topology V involves least number of devices, three of the switches were found to be overloaded in terms of conduction duration, which resulted in higher switching losses. It is clear that

Topology VIII involves the highest number of devices, which results in poor cost function and reliability. In addition to these draw backs, it is also subjected to higher voltage stress compared to all other topologies. It is evident from the results that Topology VII outperforms the rest seven topologies. It involves lesser part count and provides a better cost function as well as improved reliability. Also, it has an added advantage of reduced voltage stress, which in turn results in enhanced reliability.

As a contribution, a new 15-level asymmetric MLI has been proposed in this article. The results of the proposed topology are validated through MATLAB/Simulink and the results are presented. For summarizing the performance, the proposed topology has been compared with Topology VII. Impact of switching frequency and duration on time on the reliability parameter has been quantitatively tabulated. The design level and implementation level cost have been presented in detail. The implementation level cost for the proposed topology has been evaluated as 160$. From the results, it is evident that the proposed inverter provides superior performance in terms of switching losses, cost function, THD, and reliability. So, it can be concluded that the proposed topology found to be a promising candidate for commercial applications.

A. Future Scope

For the proposed new topology, the cost function can be dealt in detail by including the operational cost and other possible factors. The reliability of the proposed topology can be examined under fault conditions using reliability softwares like ISO graph. The proposed topology can be implemented in hardware and the results can be validated. The proposed new topology may also be examined with different PWM techniques.

The impact of variations in the switching frequency on the reliability estimation can be analyzed. With a promising PWM technique, a closed-loop scheme can be implemented for the proposed inverter. In the closed-loop system, the dynamic response can be elaborated for load end and source end disturbances.

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