Output Spectrum Modeling of an H-Bridge Inverter With Dead-Time Based on Switching Mode Analysis

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***Abstract*—The distortion of an H-bridge inverter can originate from many nonlinear factors, of which the most dominant one is typically the dead-time. In previous research, analytical models have been proposed to calculate the output spectrum of the H-bridge inverter. However, the existing models have not fully explored the effects of soft-switching and discontinuous conduction mode, which might severely degrade their accuracy. In this article, the characteristics and the corresponding effects of these switching modes are analyzed. Constraint functions are proposed in order to determine the time position of each switching mode. Based on this analysis, a numerical model of the output spectrum of the H-bridge inverter is then introduced. The model is shown to have a significantly improved accuracy compared to the previous analytical models especially for large inductor current ripples. The accuracy improvement is confirmed by simulation and measurements on an experimental prototype.**

***Index Terms*—Continuous conduction mode, current ripple, dead-time, discontinuous conduction mode, harmonics, soft-switching, voltage error.**

I. Introduction

THE sine-pulse-width-modulation (SPWM) H-bridge inverter is widely used in industry. Some applications, such as lithography and magnetic resonance imaging (MRI), demand high precision and high linearity [1]. Taking lithography for example, the position error of the moving stage is determined by the nonlinear error of the inverter, requiring less than -100-dB current distortion [2]. The high-linearity requirement is also desired in many other applications, and it raises the research question of what the origin is and what determines the magnitude of the inverter distortion.

Previous literature has demonstrated that the nonlinear distortion of the H-bridge inverter can originate from different sources, including the dead-time [3]–[9], nonlinear effect of the inductor [10], [11], on-resistance variation of the transistors [12], [13], SPWM [14], [15], output capacitance of the switches [7], [9], [16]–[18], device dynamics [19], [20], etc., among which the most dominant source of distortion is typically the dead-time [19], [21].

The effect of the dead-time on the output has been introduced and calculated in [5], [22]–[24] by assuming zero filter inductor current ripple during dead-time. It has been illustrated that the dead-time adds a voltage error to the switch-node voltage. The magnitude of the voltage error is proportional to the dead-time percentage and the sign is determined by the inductor current polarity [23]. Therefore, this voltage error introduces a nonlinear distortion to the output voltage. A two-level model for the voltage error approximation has been derived in these researches. The model results in a rectangular voltage error in a fundamental output period [8], [25]. Moreover, several analytical methods for calculating the output spectrum of an H-Bridge inverter are provided in [3], [26], and [27] based on this two-level approximation model. The analytical results yield monotonically decreasing odd harmonics, which are not always correct in practice. For example in [28], the third harmonic is smaller than the fifth one. This deviation mainly rises from the effect of different switching modes during the dead-time caused by the filter inductor current ripple.

When the filter inductor current ripple is large compared to the moving average value of the inductor current, the voltage error greatly deviates from the case with zero inductor current ripple, as is assumed in previous research. As presented in [29], the inductor current ripple results in three different switching modes, being soft-switching continuous conduction mode (SSCCM), discontinuous conduction mode (DCM), and hard-switching continuous conduction mode (HSCCM). Compared to the aforementioned two-level approximation models, SSCCM and DCM are added. In the SSCCM near the inductor current zero-crossing region, soft-switching is achieved, thus eliminating the switch-node voltage error. Furthermore, the DCM causes a variable switch-node voltage error contributing to the total dead-time distortion.

Several papers have investigated the different switching modes caused by the inductor current ripple [6], [8]. However, those papers assume the switch-node voltage to be the half of the dc-link voltage when the inductor current is clamped to zero in DCM. This results in a linear approximation of the voltage error while the actual voltage should be equal to the output voltage during this interval. This oversimplified linear approximation gives rise to inaccurate results. Some papers have also improved the voltage error approximation and used the approximation results for dead-time compensation, leading to better output

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linearity. Some of those approximations were obtained by simulation or measurement and modeled in lookup tables [11], [28]. Besides, some papers mainly focused on the influence of output capacitances of the switch [7], [9], [17], [30] and adjusted the modulation accordingly to reduce the output distortion but the effect of the output capacitance is typically not dominant. In addition, the models proposed in those compensation schemes were often tested for specific working conditions. In a nutshell, none of the aforementioned papers is able to accurately give a quantitative expression of either the voltage error in the DCM or the boundaries of the different conduction modes.

Numerous dead-time compensation methods, especially the feed-forward ones, have been developed based on the approximation of the switch-node voltage error as presented in [4]–[9]. The effectiveness of the dead-time compensation highly relies on the accuracy of voltage error approximation or the derived output spectrum. Therefore, an accurate model of the voltage error and the output spectrum is crucial for dead-time compensation. However, no paper or combination of papers in our literature study has fully identified or exhaustively explored the voltage error introduced by the dead-time by taking different switching modes caused by the inductor current ripple into consideration. The aim of this article is to develop an accurate computation method for calculating the voltage error. The filter inductor current waveform in each switching mode is analyzed and described mathematically. The boundaries of different switching modes are explored by a series constraint functions, based on which mathematical expressions of different switching modes are given. In addition, these constraint functions also provide a basis for the filter inductance and operating condition optimization for a lower harmonic distortion. The output voltage spectrum of the H-bridge inverter is modeled numerically based on the accurate voltage error expression. Both simulations and experiments have been carried out to validate the proposed model. The results reveal the THD pattern of the H-bridge inverter with increasing modulation depth. Compared to the traditional analytical model, the proposed model shows a significant accuracy improvement. This approach can be further used for accurate open-loop dead-time compensation and can be extended to topologies other than the H-bridge.

The structure of this article is as follows. The different switching modes, including the soft-switching continuous conduction mode, the discontinuous conduction mode, and the hard-switching continuous conduction mode and their corresponding effects are explored and modeled in Section II. Then the time position and the boundaries of the different switching modes are determined by a series of current constraint functions. The simulations and experiments are conducted to verify the method in Section III. Fianlly, Section IV conludes the article.

II. Output Voltage Spectrum Analysis

A. H-Bridge Inverter With SPWM

The basic topology of an H-bridge inverter is shown in Fig. 1. In practice, the inverter can be applied to different sorts of loads, such as inductive coils in MRI and motors in lithography applications. Generally, the load can be defined by $R + jL_{\mathrm{x}}$,

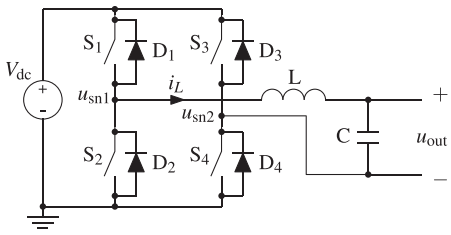

Fig. 1. Basic H-bridge inverter with output filter.

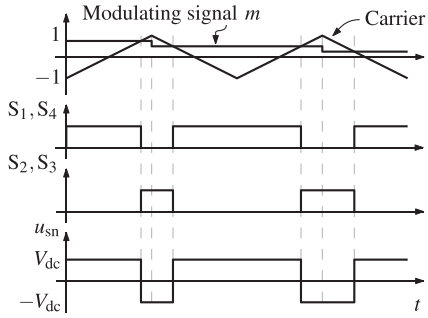

Fig. 2. Symmetrically sampled PWM waveforms without dead-time. The switch-node voltage is defined by $u_{\mathrm{sn}} = u_{\mathrm{sn1}} - u_{\mathrm{sn2}}$.

where R is the load resistance and L_{x} is the load inductance. This article focuses on the effect of dead-time on the output distortion, thus the closed-loop controller is omitted here. In this article, symmetrically sampled SPWM and bipolar modulation are used as an example. The basic operation of the switches is shown in Fig. 2. The output capacitance of the switches is neglected in order to simplify the calculation. As a result, the switches are assumed to have zero rise and fall time for current and voltage.

During a switching cycle $[nT_{\mathrm{sw}}, (n+1)T_{\mathrm{sw}}]$, with T_{sw} representing the switching period and n a nonnegative integer, the modulating signal for a symmetrically sampled SPWM is defined by

$$m(n) = M \sin\left(\frac{2\pi n}{N_{\mathrm{sw}}}\right) \tag{1}$$

where M is the modulation depth and N_{sw} is the number of switching cycles in a full fundamental period. N_{sw} here is determined by

$$N_{\mathrm{sw}} = \frac{f_{\mathrm{sw}}}{f_{\mathrm{o}}} \tag{2}$$

where f_{sw} is the switching frequency and f_{o} is the fundamental output frequency. The moving average value of the switch-node voltage is defined by

$$\langle u_{\mathrm{sn}}(n) \rangle = V_{\mathrm{dc}} m(n) \tag{3}$$

where the operator $\langle \cdot \rangle$ gives the average value over a switching cycle. An *LC* filter is used to reduce the high-frequency distortion, The cut-off frequency f_{c} is determined by

$$f_{\mathrm{c}} = \frac{1}{2\pi\sqrt{LC}} \tag{4}$$

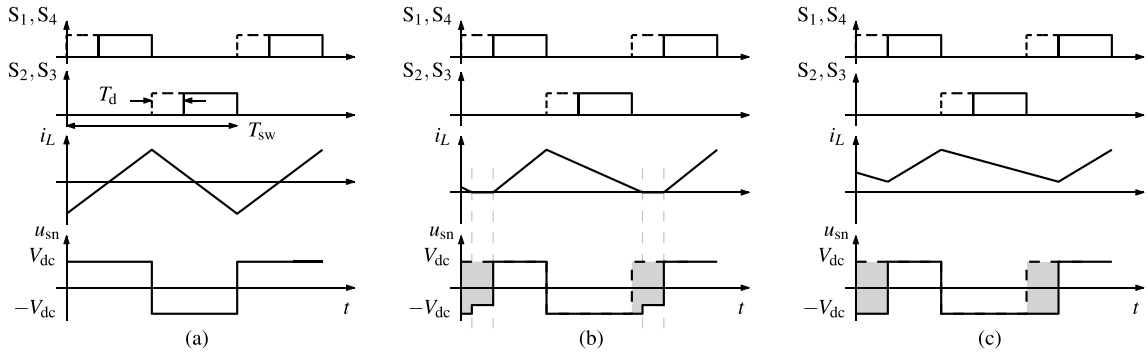

Fig. 3. Waveforms during a switching cycle. (a) Soft-switching continuous conduction mode. (b) Discontinuous conduction mode. (c) Hard-switching continuous conduction mode. The solid and dashed lines represent the case with and without dead-time, respectively. The gray area represents the volt-second error.

which is typically chosen at 1/5th of the switching frequency $f_{\rm sw}$ [31]. Therefore, the high-frequency distortion caused by SPWM is assumed to be filtered and is neglected here, such that the delivered output voltage can be considered smooth. Ideally, the output voltage should be equal to the reference voltage. However, the output filter can change the magnitude and cause phase shift to the output voltage especially around the cut-off frequency. With a properly designed output damping, the effect of the output filter is negligible within the bandwidth. As a result, the output voltage can be approximated by the reference voltage and given by

$$u_{\rm out}(t) \;\approx\; u_{\rm ref}(t) = MV_{\rm dc}\sin\left(2\pi f_{\rm o}t\right). \tag{5}$$

Consequently, the output current is then governed by

$$i_{\rm out}(t) = \frac{MV_{\rm dc}}{Z}\sin\left(2\pi f_{\rm o}t - \varphi_{\rm o}\right) \tag{6}$$

where Z and $\varphi_{\rm o}$ are the impedance and phase angle of the load, respectively.

B. Switching Mode Analysis

In practice, a certain dead-time $T_{\rm d}$ is required to prevent shoot through. During the dead-time both switches of the same leg are OFF and the switch-node voltage is dependent on the filter inductor current. The dead-time may result in a voltage error on the switch-node and output, defined by

$$u_{\rm e} = u_{\rm ref} - u_{\rm out}. \tag{7}$$

The effects of the dead-time on the switch-node voltage are shown in Fig. 3, where the switching cycle is divided into three different modes depending on the inductor current waveform. The modes comprise of SSCCM, DCM, and HSCCM.

These effects are a simplification by neglecting the output capacitance of the switches. Practically, the switch-node voltage changes with a slope due to the output capacitance of the switches. Therefore, the output capacitance causes extra voltage error in SSCCM compared to Fig. 3(a) while it mitigates the voltage error in DCM and HSCCM compared to Fig. 3(b) and (c). The quantitative analysis of the effect of the output capacitance can be found in [7], [9], [17], [30]. Whether the distortion caused by the output capacitance is dominant or not is determined by the time ratio of the rise and fall time of the switch-node voltage to the dead-time. When the dead-time is very small, such as only several nanoseconds for a gallium nitride transistor, or the output capacitance is very large by adding a snubber capacitor, the output capacitance can be the major source of the distortion [32]. However, the inductor current ripple is the dominant distortion source typically so in this article, the output capacitance is assumed to be zero in calculation. Furthermore, the measurement results in Section III also show that this assumption is reasonable in this research.

In SSCCM, the inductor current is crossing zero and changes the direction alternatively when each pair of switches is ON. As a result, despite the existence of the dead-time, the switch-node voltage $u_{\rm sn}$ remains equal to the ideal case. In DCM, the inductor current rises from negative or falls from positive to zero during the dead-time and is then clamped to zero. The switch-node voltage is equal to the output voltage during clamping. The value of the voltage error is dependent on the dead-time value and load phase angle. In HSCCM, the inductor current is strictly positive or negative, resulting in a fixed voltage error of the same polarity. Fig. 4 shows the simulated waveforms of a typical H-bridge inverter, in which the piece-wise voltage error and the corresponding inductor current reflect the effect of the dead-time in different switching modes on the output voltage and current.

Each switching mode is described analytically in this article. In order to simplify the expression, four current values, as depicted in Fig. 5, need to be primarily defined. First, during a switching cycle $[nT_{\rm sw}, (n+1)T_{\rm sw}]$, assuming zero capacitor current, the ideal moving average value of filter inductor current is equal to the output current and can be written as

$$\langle i_L(n)\rangle = i_{\rm out}(n) = \frac{MV_{\rm dc}}{Z}\sin\left(\frac{2\pi n}{N_{\rm sw}} - \varphi_o\right) \tag{8}$$

according to (6). Second, the peak-to-average inductor current ripple $\Delta i_L(n)$ during an ideal switching cycle is calculated as

$$\begin{aligned}\Delta i_L(n) &= \frac{V_{\rm dc} - m(n)V_{\rm dc}}{2\,L}\cdot\frac{\left[1+m(n)\right]T_{\rm sw}}{2}\\ &= \frac{V_{\rm dc}T_{\rm sw}}{4\,L}\left[1-m(n)^2\right].\end{aligned} \tag{9}$$

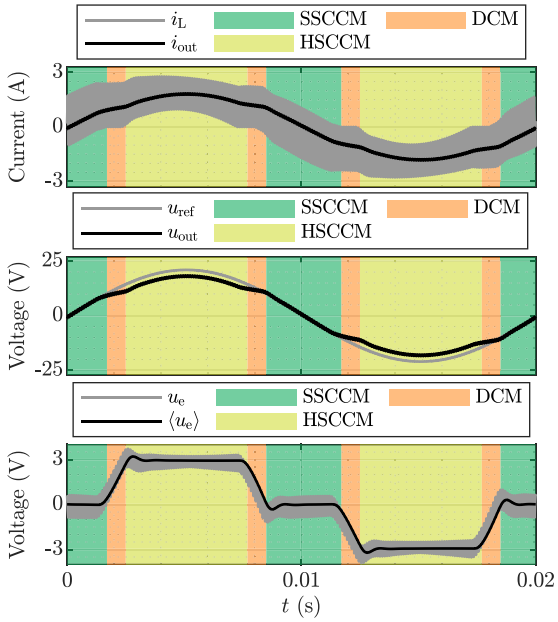

Fig. 4. Simulated waveforms with $V_{dc} = 30$ V, $M = 0.7$, $f_o = 50$ Hz, $f_{sw} = 10$ kHz, $T_d = 5$ μs, $L = 0.55$ mH, $C = 30$ μF, and a resistive load $R = 10\,\Omega$.

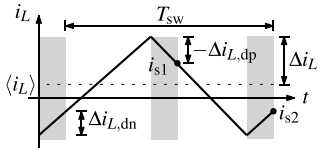

Fig. 5. Inductor current waveform for SSCCM. The gray area represents the dead-time.

Third, when the inductor current is distinctly positive during dead-time, the magnitude of the inductor current change during dead-time is expressed as

$$\Delta i_{L,\mathrm{dp}}(n) = -\frac{V_{\mathrm{dc}} T_{\mathrm{d}}}{L}\left[1 + m(n)\right]. \tag{10}$$

Fourth, the magnitude of the inductor current change during dead-time when the inductor current is distinctly negative is described as

$$\Delta i_{L,\mathrm{dn}}(n) = \frac{V_{\mathrm{dc}} T_{\mathrm{d}}}{L}\left[1 - m(n)\right]. \tag{11}$$

The four current values defined by (8)–(11) can be used to describe the inductor current in each switching mode. For example in SSCCM shown in Fig. 5, there are two dead-time intervals in each switching cycle. The inductor current at the end of each dead-time in a switching cycle is defined by i_{s1} and i_{s2}, respectively. In order to guarantee SSCCM, there are constraints for i_{s1} and i_{s2}, which can be described by

$$\begin{cases} i_{s1}(n) = \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n) \geq 0 \\ i_{s2}(n) = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n) \leq 0. \end{cases} \tag{12}$$

The voltage error is zero in these switching cycles. The inductor current waveforms for DCM are depicted in Fig. 6 [33]. For the

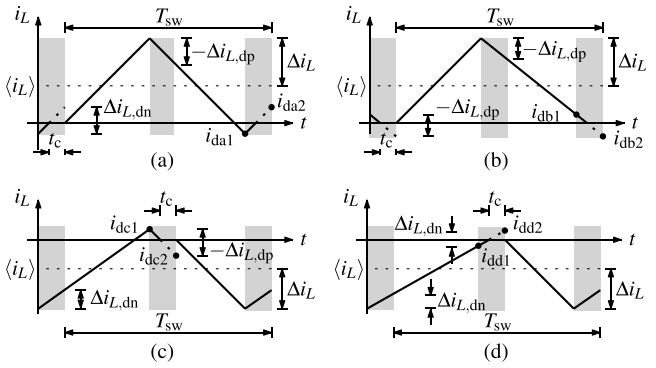

Fig. 6. Inductor current waveforms for DCM. (a) $\langle i_L \rangle > 0$ and $i_{L,\min} < 0$. (b) $\langle i_L \rangle > 0$ and $i_{L,\min} = 0$. (c) $\langle i_L \rangle < 0$ and $i_{L,\max} > 0$. (d) $\langle i_L \rangle < 0$ and $i_{L,\max} = 0$.

waveform shown in Fig. 6(a), there are constraints for i_{da1} and i_{ida2} as defined in the figure and they are given by

$$\begin{cases} i_{\mathrm{da1}} = \langle i_L(n) \rangle - \Delta i_L(n) \leq 0 \\ i_{\mathrm{da2}} = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n) > 0. \end{cases} \tag{13}$$

Moreover, the clamping time $t_c(n)$ yields

$$t_c(n) = \frac{\langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n)}{\Delta i_{L,\mathrm{dn}}(n)} T_{\mathrm{d}}. \tag{14}$$

The switch-node voltage error is found to be

$$\langle u_e(n) \rangle = \frac{\left[1 - m(n)\right] V_{\mathrm{dc}} t_c(n)}{T_{\mathrm{sw}}} \tag{15}$$

which can be rewritten as

$$\langle u_e(n) \rangle = \frac{L}{T_{\mathrm{sw}}}\left[\langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n)\right]. \tag{16}$$

In the same manner, the constraints for i_{db1} and i_{idb2} shown in Fig. 6(b) are given by

$$\begin{cases} i_{\mathrm{db1}} = \langle i_L(n) \rangle - \Delta i_L(n) > 0 \\ i_{\mathrm{db2}} = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n) < 0. \end{cases} \tag{17}$$

The voltage error is found to be the same as (16). Consequently, the two DCM modes depicted in Fig. 6(a) and (b) with an average positive inductor current can be combined. The current constraints are then expressed as

$$\begin{cases} \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n) < 0 \\ \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n) > 0. \end{cases} \tag{18}$$

Similarly, the current constraints and voltage error for the DCM with negative average inductor currents depicted in Fig. 6(c) and (d) are described by

$$\begin{cases} \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n) < 0 \\ \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n) > 0 \end{cases} \tag{19}$$

and

$$\langle u_e(n) \rangle = \frac{L}{T_{\mathrm{sw}}}\left[\langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n)\right] \tag{20}$$

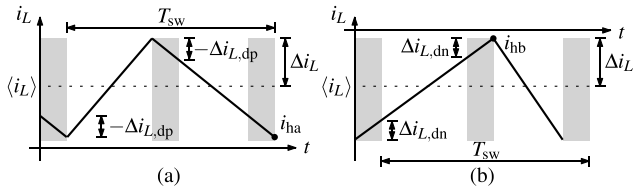

Fig. 7. Inductor current waveforms for HSCCM. (a) Distinctly positive inductor current. (b) Distinctly negative inductor current.

TABLE I
CURRENT CONSTRAINTS FOR DIFFERENT SWITCHING MODES

Switching mode	Current constraints	Switching mode	Current constraints
SSCCM	$\begin{cases} y_{sp}(n) \geq 0; \\ y_{sn}(n) \leq 0. \end{cases}$	HSCCM (a) or (b)	$y_{cn}(n) \geq 0$ or $y_{cp}(n) \leq 0$.
DCM (a) & (b)	$\begin{cases} y_{sn}(n) > 0; \\ y_{cn}(n) < 0. \end{cases}$	DCM (c) & (d)	$\begin{cases} y_{sp}(n) < 0; \\ y_{cp}(n) > 0. \end{cases}$

respectively. The inductor current waveform for HSCCM are shown in Fig. 7. It is obvious that the current constraint and the voltage error for HSCCM depicted in Fig. 7(a) and (b) are given by

$$i_{ha}(n) = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,dp}(n) \geq 0 \tag{21}$$

$$i_{hb}(n) = \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,dn}(n) \leq 0 \tag{22}$$

and

$$\langle u_e(n) \rangle = \frac{2V_{dc}T_d}{T_{sw}}, \text{ for } i_{ha}(n) \geq 0 \tag{23}$$

$$\langle u_e(n) \rangle = -\frac{2V_{dc}T_d}{T_{sw}}, \text{ for } i_{hb}(n) \leq 0 \tag{24}$$

respectively.

C. Constraint Functions

Based on the above analysis of the voltage error, a series of current constraint functions is derived to determine the boundaries of different switching modes according to (12), (18), (19), (21), and (22), which is defined by

$$y_{sp}(n) = \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,dp}(n) \tag{25}$$

$$y_{sn}(n) = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,dn}(n) \tag{26}$$

$$y_{cp}(n) = \langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,dn}(n) \tag{27}$$

and

$$y_{cn}(n) = \langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,dp}(n). \tag{28}$$

With these constraint functions, the current constraints of different switching modes are simplified in Table I.

By solving the equations $y_{sp}(n) = 0$, $y_{sn}(n) = 0$, $y_{cp}(n) = 0$, and $y_{cn}(n) = 0$, the boundaries in the time domain of different switching modes are determined. Fig. 8 shows a typical plot of the constraint functions. All functions are periodic with a period of N_{sw}. Meanwhile, $y_{sp}(n)$ and $y_{sn}(n)$, $y_{cp}(n)$ and $y_{cn}(n)$

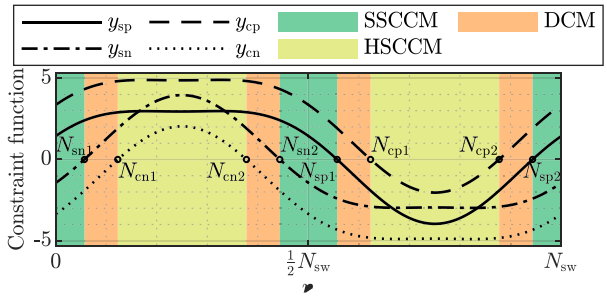

Fig. 8. Current constraint functions of the different switching modes. N_{sp1} and N_{sp2} ($N_{sp1} < N_{sp2}$), N_{sn1} and N_{sn2} ($N_{sn1} < N_{sn2}$), N_{cn1} and N_{cn2} ($N_{cn1} < N_{cn2}$), N_{sp1} and N_{sp2} ($N_{sp1} < N_{sp2}$) are the solutions of $y_{sp}(n) = 0$, $y_{sn}(n) = 0$, $y_{cp}(n) = 0$, and $y_{cn}(n) = 0$, respectively.

are both centrosymmetric about $(\frac{N_{sw}(\pi+\varphi_o)}{2\pi}, 0)$. By definition, $y_{sp}(n) > y_{cp}(n)$ and $y_{sn}(n) > y_{cn}(n)$.

Although Fig. 8 shows a typical case in which all constraint functions have two zero-crossings, it must be stressed that it is not necessarily true. For example, if $y_{sp}(n)$ and $y_{sn}(n)$ have no zero-crossing point in a fundamental period, then there is no DCM or HSCCM switching cycle, and thus soft-switching is achieved all the time. In this case, the dead-time causes no voltage error.

Similarly, if $y_{cp}(n)$ and $y_{cn}(n)$ have no zero-crossing point in a fundamental period, then there are only SSCCM and DCM but no HSCCM switching cycle. Therefore, the voltage error in a fundamental period can be written as

$$\langle u_e(n) \rangle = \begin{cases} 0, \quad n \in [N_{sp2} - N_{sw} + 1, N_{sn1}] \cup [N_{sn2}, N_{sp1}] \\ \frac{L}{T_{sw}} [\langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,dn}(n)] \\ \qquad\qquad n \in (N_{sn1}, N_{sn2}) \\ \frac{L}{T_{sw}} [\langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,dp}(n)] \\ \qquad\qquad n \in (N_{sp1}, N_{sp2}) . \end{cases} \tag{29}$$

The HSCCM cycle exists if and only if all the constraint functions have two zero-crossing points. In this case, the voltage error in a full fundamental period is described by

$$\langle u_e(n) \rangle = \begin{cases} 0, \quad n \in [N_{sp2} - N_{sw} + 1, N_{sn1}] \cup [N_{sn2}, N_{sp1}] \\ \frac{L}{T_{sw}} [\langle i_L(n) \rangle - \Delta i_L(n) + \Delta i_{L,dn}(n)] \\ \qquad n \in (N_{sn1}, N_{cn1}) \cup (N_{cn2}, N_{sn2}) \\ \frac{L}{T_{sw}} [\langle i_L(n) \rangle + \Delta i_L(n) + \Delta i_{L,dp}(n)] \\ \qquad n \in (N_{sp1}, N_{cp1}) \cup (N_{cp2}, N_{sp2}) \\ \frac{2V_{dc}T_d}{T_{sw}} \qquad n \in [N_{cn1}, N_{cn2}] \\ -\frac{2V_{dc}T_d}{T_{sw}} \qquad n \in [N_{cp1}, N_{cp2}] . \end{cases} \tag{30}$$

The boundaries of different switching modes are dependent on the operating point, including the dead-time duration, the filter inductance, the load and the modulation depth. Fig. 9 depicts the constraint functions, the simulated and calculated voltage errors for an H-bridge inverter with a resistive load working under different modulation depths. As shown in the figure, when solely changing the modulation depth, the time intervals of the switching modes in a fundamental period change accordingly.

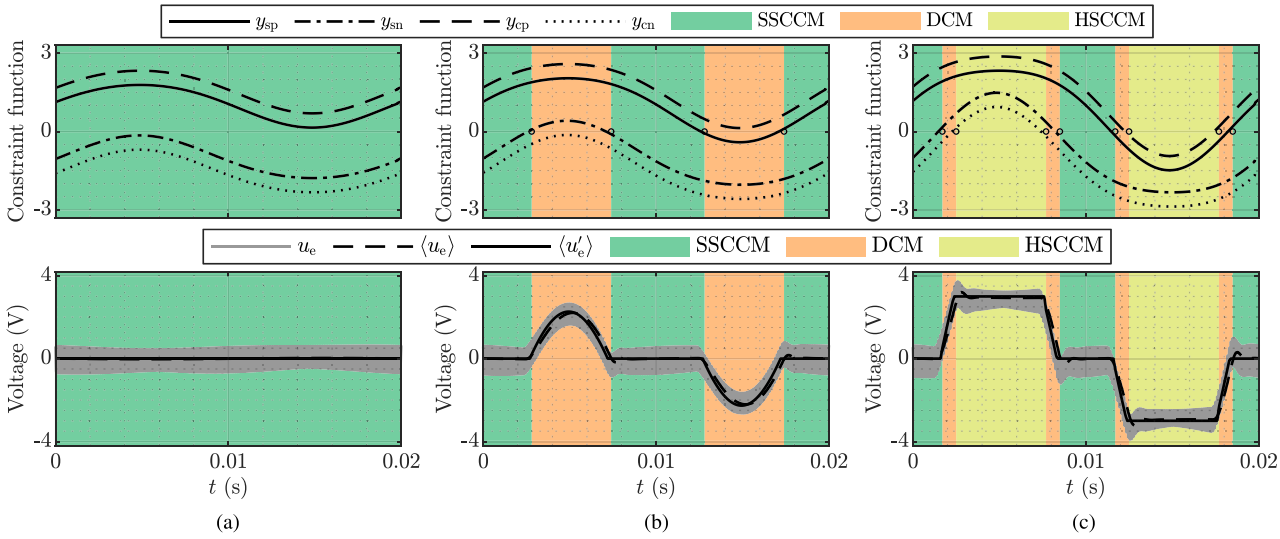

Fig. 9. Waveforms of the calculated constraint functions y_{sp}, y_{sn}, y_{cp}, and y_{cn}, the simulated voltage error u_e, the moving average value of the simulated voltage error $\langle u_e \rangle$ and the calculated voltage error $\langle u'_e \rangle$ of an H-bridge inverter working at $V_{dc} = 30$ V, $T_d = 5$ μs, $f_{sw} = 10$ kHz, $f_o = 50$ Hz, $L = 0.55$ mH, $C = 30$ μF, $R = 10$ Ω, $L_x = 0$, and (a) $M = 0.3$, (b) $M = 0.45$, (c) $M = 0.7$. The output capacitance of the switches is neglected in both simulation and calculation.

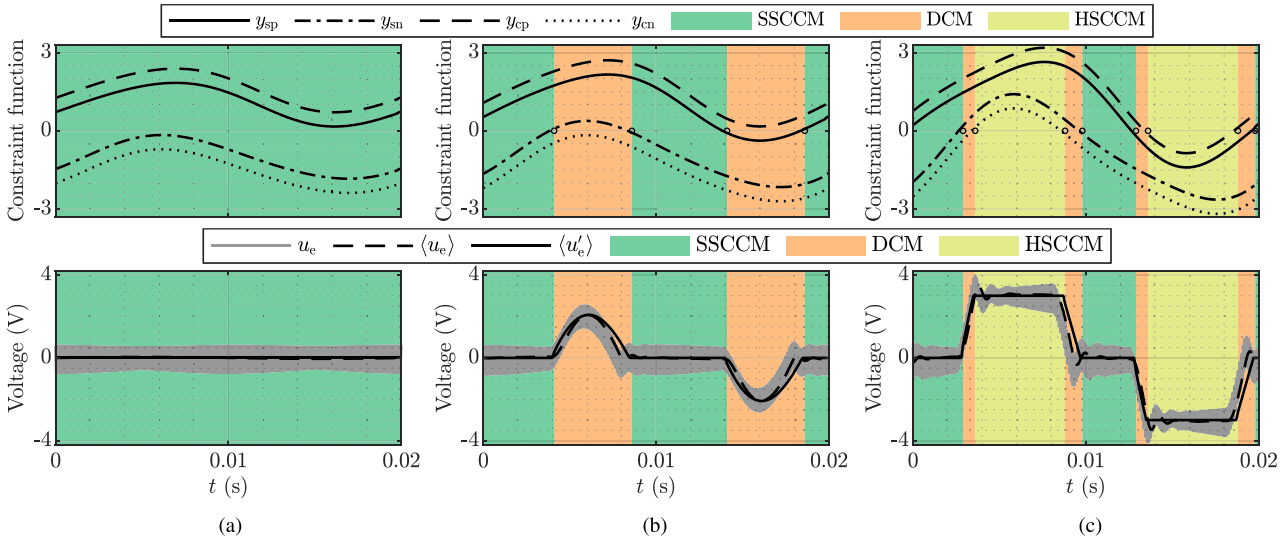

Fig. 10. Waveforms of the calculated constraint functions y_{sp}, y_{sn}, y_{cp}, and y_{cn}, the simulated voltage error u_e, the moving average value of the simulated voltage error $\langle u_e \rangle$ and the calculated voltage error $\langle u'_e \rangle$ of an H-bridge inverter working at $V_{dc} = 30$ V, $T_d = 5$ μs, $f_{sw} = 10$ kHz, $f_o = 50$ Hz, $L = 0.55$ mH, $C = 30$ μF, $R = 8.9$ Ω, $L_x = 14.4$ mH, and (a) $M = 0.3$, (b) $M = 0.45$, (c) $M = 0.7$. The output capacitance of the switches is neglected in both simulation and calculation.

When the modulation depth is low, the output current is low, making the inductor current ripple relatively high and SSCCM can be achieved all the time. When increasing the modulation depth, DCM and HSCCM appear one after another. In addition, the voltage error in DCM is variant while in HSCCM it is a fixed value. The nonlinear voltage error in DCM further illustrates the limitation of the previous models, which use the inaccurate linear approximation [6], [8]. The boundaries of the different switching modes are consistent with the zero-crossing points of the corresponding constraint functions and the calculated voltage errors fit with the simulated ones, showing the accuracy and the effectiveness of the calculation introduced in this article.

Fig. 10 depicts the inverter with an inductive load working under the same operating conditions as a comparison to the resistive load. The impedance of the inductive load in Fig. 10 is the same with that of the resistive load in Fig. 9, but it has a phase angle of 27 degrees. As can be seen in the figure, the inductive load shares the similar waveform patterns with the resistive load, while a phase shift equal to the load phase angle is introduced in both constraint functions and voltage error waveform. Moreover, both constraint functions and voltage error waveforms of the resistive load are symmetrical about $n = \frac{N_{sw}}{4}$ and $n = \frac{3N_{sw}}{4}$. However, as shown in Fig. 10, this symmetry does not stand when a inductive load is used.

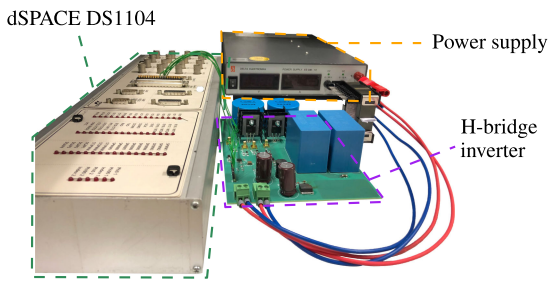

Fig. 11. Experimental setup for distortion measurement.

As presented in Figs. 9(a) and 10(a), when SSCCM is achieved in the full fundamental period, the moving average value of the switch-node voltage error caused by the dead-time is zero, which can lead to a high output linearity. This phenomenon usually happens with a small modulation depth. However, whether SSCCM is achieved in the full fundamental period or not can be used as a criterion for component selection when designing the inverters, especially for the high-precision applications. In a typical industrial design process, the load and $V_{\rm dc}$ are determined by the specifications. For a rated output current or voltage, the modulation depth is also fixed. The dead-time is determined by the performance of the selected switches. The filter inductance can be optimized according to the introduced constraint functions in order to guarantee SSCCM in a fundamental period when working at the maximum modulation depth. Due to their centrosymmetry about $(\frac{N_{\rm sw}(\pi+\varphi_o)}{2\pi}, 0)$, either $y_{\rm sp}$ or $y_{\rm sn}$ can be used to determine the minimum filter inductance, which should guarantee $y_{\rm sp}(n) \geq 0$ or $y_{\rm sn}(n) \leq 0$ for any $n \in [0, N_{\rm sw}-1]$.

D. Output Spectrum Calculation

Based on the voltage error analysis, accurate models can be built to calculate the output spectrum of the SPWM H-bridge inverter. The previous analytical models introduced in [3], [26], and [27] are based on the assumption of zero inductor current ripple. Consequently, only HSCCM cycles are considered. The voltage error in the previous analytical model is simplified as

$$u_{\rm e}(t) = \frac{2V_{\rm dc}T_{\rm d}}{T_{\rm sw}}\text{sign}\left(\sin\left(2\pi f_{\rm o}t - \varphi_{\rm o}\right)\right) \tag{31}$$

where $\text{sign}(\cdot)$ extracts the sign of the content. By using the Fourier series expansion, the voltage error is represented as

$$u_{\rm e}(t) = \sum_{k=1}^{\infty}\left[\frac{-1+(-1)^k}{2}\right]\frac{8}{k\pi}\frac{V_{\rm dc}T_{\rm d}}{T_{\rm sw}}\sin\left(2\pi f_{\rm o}t - \varphi_{\rm o}\right) \tag{32}$$

where k is the harmonic order. Therefore, the output voltage can be calculated by $u_{\rm out}(t) = u_{\rm ref} - u_{\rm e}(t)$. The amplitude of each harmonic is found to be

$$A_k = \begin{cases} \sqrt{M^2V_{\rm dc}^2 + \left(\frac{8V_{\rm dc}T_{\rm d}}{T_{\rm sw}}\right)^2 - \frac{8MV_{\rm dc}^2T_{\rm d}}{\pi T_{\rm sw}}\cos\varphi_{\rm o}}, & k=1 \\ \frac{8}{k\pi}\frac{V_{\rm dc}T_{\rm d}}{T_{\rm sw}}, & k \text{ is odd and } k\neq 1 \\ 0, & k \text{ is even.} \end{cases} \tag{33}$$

This simplification yields a result that the odd harmonics monotonically decrease with the harmonic order, which can deviate with the practice.

Specially, under the circumstances of high inductor current ripples, DCM and SSCCM also play critical roles in the output harmonics, thus notably degrading the accuracy of the analytical model. In order to improve the modeling accuracy, an accuracy-improved numerical model of the output spectrum is derived in this article.

The time positions of different switching modes can be obtained by solving the zero-crossing points of the constraint functions using numerical methods, such as Newton's method, Broyden's method, and Secant methods. Moreover, it can also be derived by searching the switching cycle which reverses the sign of the constraint function. For instance, $N_{\rm sn1}$ should hold the $y_{\rm sn}(N_{\rm sn1}) \leq 0$ and $y_{\rm sn}(N_{\rm sn1}+1) > 0$. Once the time positions of the switching modes are determined, the voltage error can be given according to (29) and (30). The voltage error is a discrete function with a period of $N_{\rm sw}$, thus discrete-time Fourier series (DTFS) can be used to analyze the harmonic components of the voltage error. As a result, the output voltage can be given by $u_{\rm out}(n) = V_{\rm dc}m(n) - \langle u_{\rm e}(n)\rangle$ and the magnitude of each harmonic of the output voltage can be computed accordingly.

It should be noted that both the analytical model and the proposed numerical model only consider the harmonics caused by the dead-time. Besides, both models give the same harmonic magnitudes regardless of the switching frequency $f_{\rm sw}$ and the output frequency $f_{\rm o}$ since SPWM harmonics are assumed to be completely filtered by the output filter. Additionally, both models give zero even harmonics, which might differ in practice. Compared to the analytical model, the presented numerical model is expected to give a more accurate result at the cost of higher computational effort. Compared to a typical electric circuit simulation, such as SPICE or PLECS, the numerical model is more straightforward, since it is able to generate a complete expression of the output voltage and inductor current, give the boundaries of of different switching modes and add more insight into the dead-time effects. The complete expression makes the numerical model easier to be implemented in the feed-forward compensation. Moreover, the computational effort of simulation highly relies on the solver, time step, and the simulated time duration. The time step of the simulation should be at most the PWM clock time, which is normally hundreds of times smaller than the switching period. Therefore, the time complexity of simulation is $O(f_{\rm clk}/f_{\rm o})$, where $f_{\rm clk}$ is the PWM clock frequency. However, for the presented numerical model, both the boundary searching and the voltage error calculation share a time complexity of $O(f_{\rm sw}/f_{\rm o})$. As a result, the numerical model significantly reduces the computation effort.

III. Simulation and Experiment Results

Both simulations and experiments were carried out to verify the presented model. The simulations were done using MATLAB/Simulink combined with the PLECS toolbox. Ideal MOSFETs without output capacitance were used in the simulation. The experiments were conducted on a setup using dSPACE with an

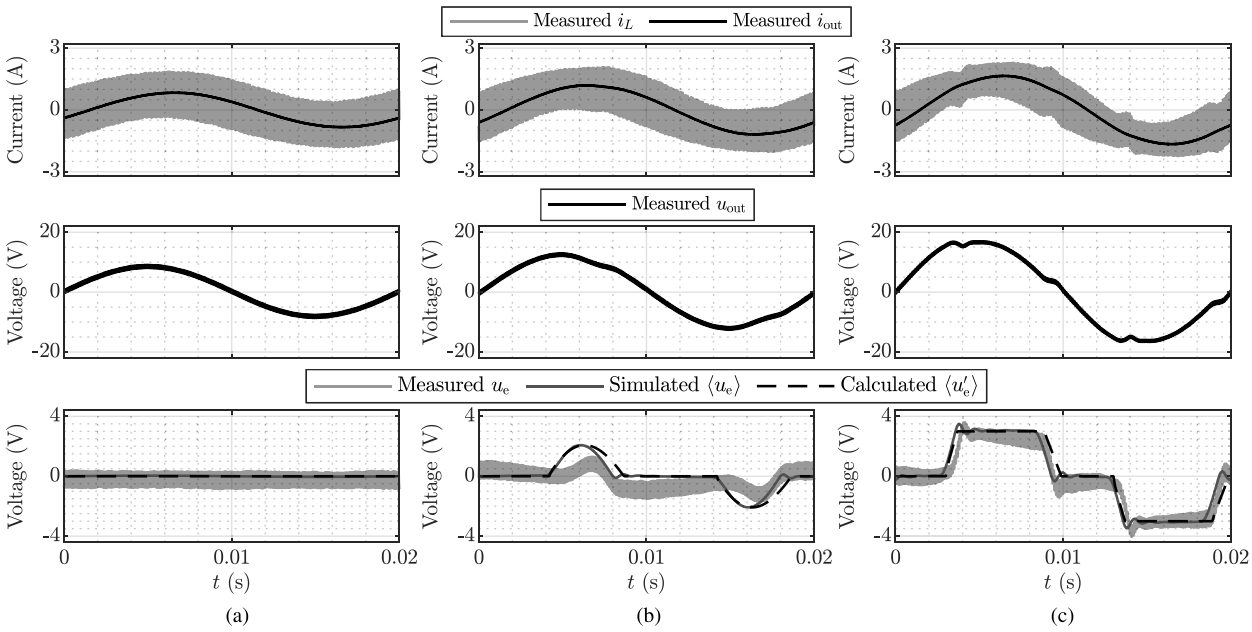

Fig. 12. Measured waveforms with the inductive load of inductor current i_L, output current i_{out}, output voltage u_{out} and voltage error u_{e} for $L = 0.55$ mH, $C = 30$ μF, $f_{\text{o}} = 50$ Hz, $f_{\text{sw}} = 10$ kHz, $T_{\text{d}} = 5$ μs and (a) $M = 0.3$, (b) $M = 0.45$, (c) $M = 0.7$. The moving average value of the simulated voltage error $\langle u_{\text{e}} \rangle$ and the calculated voltage error $\langle u'_{\text{e}} \rangle$ are shown as comparisons.

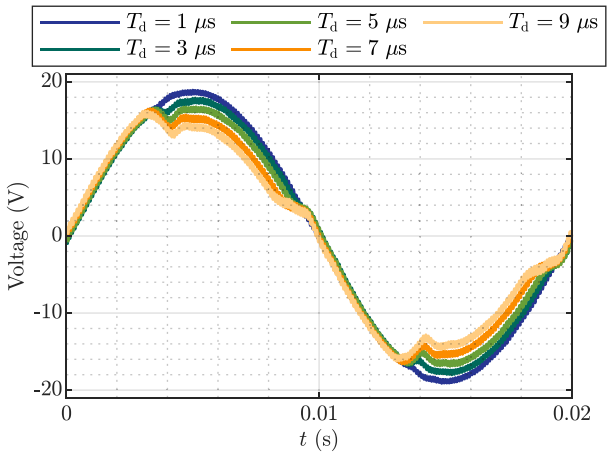

Fig. 13. Output voltage waveforms with the inductive load for $L = 0.55$ mH, $C = 30$ μF, $f_{\text{o}} = 50$ Hz, $f_{\text{sw}} = 10$ kHz, $M = 0.7$, and T_{d} ranging from 1 to 9 μs.

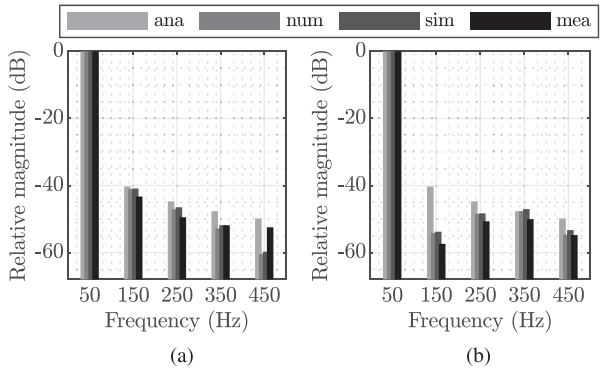

Fig. 14. Output voltage spectrum for the resistive load with $M = 0.9$, $f_{\text{o}} = 50$ Hz, and (a) $L = 2$ mH, (b) $L = 0.55$ mH, where "ana", "num", "sim", and "mea" represent the results of the analytical model, presented numerical model, simulation, and experimental measurement, respectively.

SPWM H-bridge inverter prototype, as shown in Fig. 11. The highest switching frequency limited by the dSPACE was 10 kHz. MOSFET STP80NF06 was used and operated at $V_{\text{dc}} = 30$ V. This voltage is ten times scaled-down compared to the industrial application. In order to mitigate the SPWM distortion, the fundamental frequency was set to be 50 Hz. Two different loads were used in order to visualize the effect of the load phase angle. One was a power resistor $R = 10\ \Omega$. The other was an inductive load with inductance $L_{\text{x}} = 14.4$ mH and resistance $R = 8.9\ \Omega$. Therefore, the two loads have an equal absolute impedance value while the inductive load has a phase angle of 27 degrees at 50 Hz fundamental frequency. The filter capacitor was selected to be $C = 30$ μF. Passive damping was adopted, with damping capacitance $C_{\text{d}} = 30$ μF and damping resistance $R_{\text{d}} = 10\ \Omega$. The harmonic components were measured by an SR785 signal analyzer. The relative magnitude of the output voltage harmonics was used for comparison in order to suppress the effect of the on-resistance of the MOSFETs and the series resistance of the filter inductor.

A. *Waveform Measurement*

Typical waveforms of different patterns with the inductive load of inductor current i_L, output current i_{out}, output voltage u_{out}, and voltage error u_{e} are measured and shown in Fig. 12. Both calculated and simulated moving average voltage error are plotted as comparisons. The three different switching modes and their effects on the voltage error can be seen from the waveforms, which match well with both simulated and calculated results.

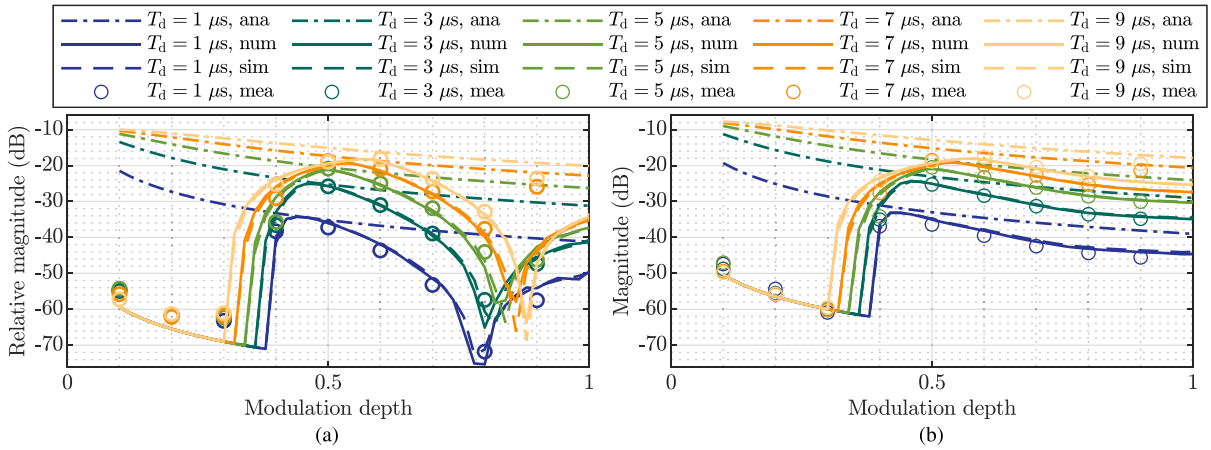

Fig. 15. (a) Relative magnitude of third harmonic and (b) magnitude of the THD for the resistive load under different dead-time and modulation depth, where "ana", "num", "sim", and "mea" represent the results of the analytical model, presented numerical model, simulation, and experimental measurement, respectively.

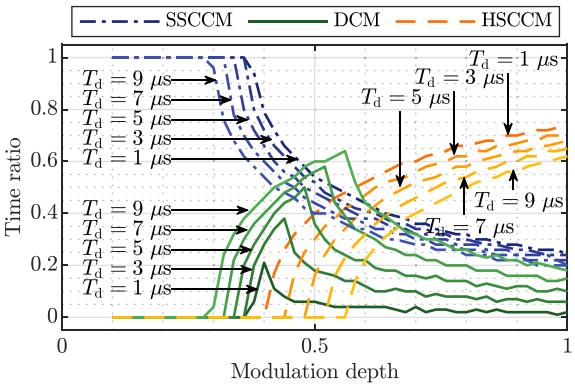

Fig. 16. Time ratio of the different switching modes under different dead-time and modulation depth.

TABLE II
HARMONIC ERRORS OF DIFFERENT METHODS COMPARED TO MEASUREMENTS FOR $L = 2$ mH AND $L = 0.55$ mH

Methods	L (mH)	Absolute errors of harmonic components (dB)			
		3rd	5th	7th	9th
Analytical	2	3.00	4.74	4.22	2.63
Numerical	2	2.22	2.39	0.95	7.95
Simulation	2	2.41	2.98	0.02	7.27
Analytical	0.55	17.10	6.12	2.39	4.96
Numerical	0.55	2.26	2.38	2.40	0.18
Simulation	0.55	3.63	2.52	3.00	1.51

In addition, output voltage waveforms with different dead-time under a typical operating condition are measured and plotted in Fig. 13. As seen in the figure, when increasing the dead-time under this working condition, the output distortion becomes more severe.

B. Output Spectrum Measurement

The existence and boundaries of SSCCM and DCM are highly dependent on the inductor current ripple, which is determined by the filter inductance. In order to see the effect of SSCCM and DCM on the output spectrum, filter inductors of 2 and 0.55 mH were used for comparison. The switching frequency is 10 kHz and the dead-time is 1 μs. The output spectrum up to ninth order are depicted in Fig. 14(a) and (b), respectively. The absolute errors of different methods compared to the measurements are listed in Table II. The even harmonics from the measurement are skipped in the plots.

With $L = 2$ mH, the maximum current ripple is about 13.9% of the output current and the effects of SSCCM and DCM are relatively small. In this case, the odd harmonics are monotonically decreasing with the harmonic order. The analytical and numerical model give the similar estimation of the odd harmonics. However, the presented numerical model has a better accuracy compared to the analytical one, especially for the dominant harmonics, as shown in Table II. Although the analytical model seems to give a better estimation of the ninth harmonic compared to the numerical model and simulation at this operating point, it is not always true under other conditions. As can be seen from Fig. 14(b), the ninth harmonic derived from the analytical model has a larger error compared to both numerical model and simulation. For those low magnitude harmonics close to the noise floor, a small nonlinear factor other than dead-time can result in a relatively large deviation in practice. In other words, the estimation of the harmonics of lower magnitude is more sensitive.

With $L = 0.55$ mH, the maximum current ripple is about 50% of the output current and the effects of SSCCM and DCM become more obvious on the output spectrum. The measured third harmonic is 6.72-dB lower than fifth harmonic and 7.36-dB lower than the seventh harmonic, which goes against the analytical model but accords with the numerical one. The numerical model gives a much more accurate result than the analytical one, especially for the third harmonic, which is 14.84-dB closer to the measured value, as shown in Table II. Compared to the measurement result for $L = 2$ mH, the relative magnitude of

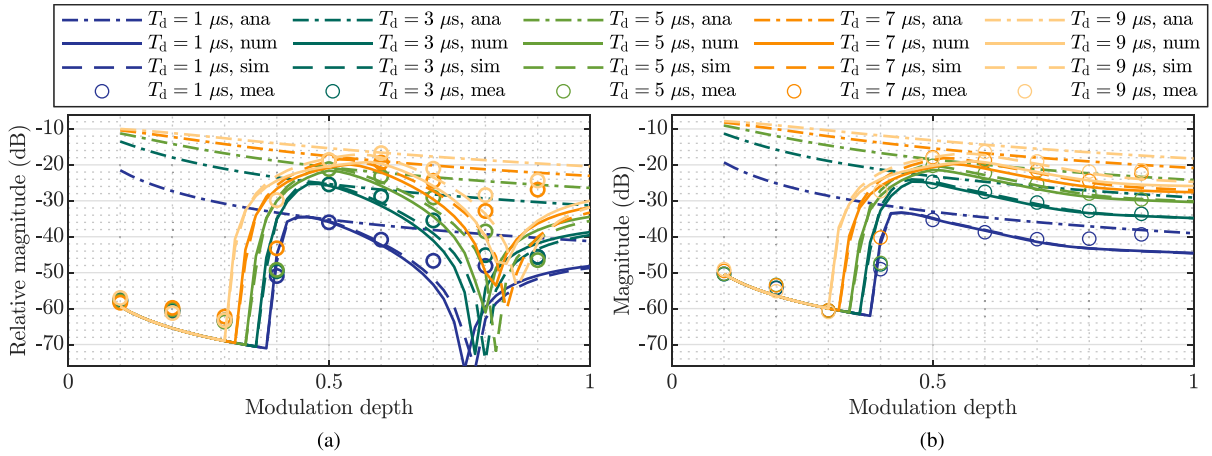

Fig. 17. (a) Relative magnitude of third harmonic and (b) magnitude of the THD for the inductive load under different dead-time and modulation depth, where "ana", "num", "sim", and "mea" represent the results of the analytical model, presented numerical model, simulation, and experimental measurement, respectively.

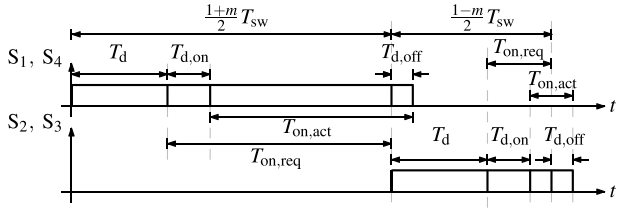

Fig. 18. Effect of switch delay on actual duty cycle.

third harmonic is reduced by 14.10 dB due to the effect of SSCCM and DCM. In both case, the accuracy of the presented numerical methods is comparable to the simulation.

C. Measurement With Different Dead-Time Percentage

In order to further compare the accuracy of different methods with different load under different conditions, calculation, simulation, and experiment were done by varying the working condition with a fixed filter inductor of 0.55 mH. In this subsection, measurement results with different dead-time under different modulation depth are presented.

When SSCCM is achieved in the full fundamental period, both the numerical model and the simulation give the zero or quasi-zero results for all the frequency components other than the fundamental one. However, the minimal magnitude of the output harmonic is limited to a practical noise floor, which is determined by all the components in the inverter system. The noise floor is frequency dependent and for a fundamental frequency of $f_o = 50\,\text{Hz}$ with $f_{sw} = 10\,\text{kHz}$, its absolute value is 3.2 mV (-50 dB). This noise floor is considered in the calculation. All frequency components obtained by the analytical model, numerical model, and simulation, which are lower than the noise floor, are set to 3.2 mV.

The results of the relative magnitude of third harmonic and the magnitude of the total harmonic distortion (THD) up to ninth order for the resistive load are depicted in Fig. 15(a) and (b), respectively. Furthermore, the time ratios of the different switching modes for this resistive load calculated by the constraint functions are displayed in Fig. 16 in order to visualize how operating points affect the boundaries. The time ratios are calculated as $2(N_{sp1} - N_{sn2})/N_{sw}$, $2(N_{cn1} - N_{sn1} + N_{sn2} - N_{cn2})/N_{sw}$, and $2(N_{cn2} - N_{cn1})/N_{sw}$ for SSCCM, DCM, and HSCCM, respectively.

The effect of SSCCM can be seen from Fig. 15 in the region, where the modulation depth $M \leq 0.3$ for each dead-time. In those regions, SSCCM is achieved in the full fundamental period as shown in Fig. 16 and the harmonic distortion is significantly reduced. In those regions where $M \leq 0.3$, even though the dead-time values are increased from 1 to 9 μs, the harmonic distortion just changes slightly. According to the proposed model, since dead-time does not cause voltage error when SSCCM is achieved in the full fundamental period, all the frequency components other than the fundamental one should be equal to the noise floor. However, the third harmonic is higher than the noise floor, as seen from the measurement results in Fig. 15(a), revealing the fact that there are other nonlinear factors dominant in those regions, which might be the output capacitance or the on-resistance variation.

For the modulation depth $M > 0.3$, SSCCM is not guaranteed and the voltage errors in DCM and HSCCM lead to the most dominant distortion in the output. In these regions, the higher dead-time causes higher distortion in general. The magnitude of THD decreases with an increasing modulation depth, due to the outweighing increase of the fundamental component magnitude. Differently, when increasing the modulation depth, the relative magnitude of the third harmonic first decreases and reaches a minimum which varies with dead-time and then increases again. As indicated in Fig. 16, the time ratio of DCM first increases when increasing the modulation depth and then decreases after HSCCM appears while the time ratio of SSCCM and HSCCM are decreasing and increasing, respectively.

As a comparison, the results for the inductive load are depicted in Fig. 17(a) and (b), respectively. As can be seen, Fig. 17 shares the very similar pattern with Fig. 15, showing that the effect of

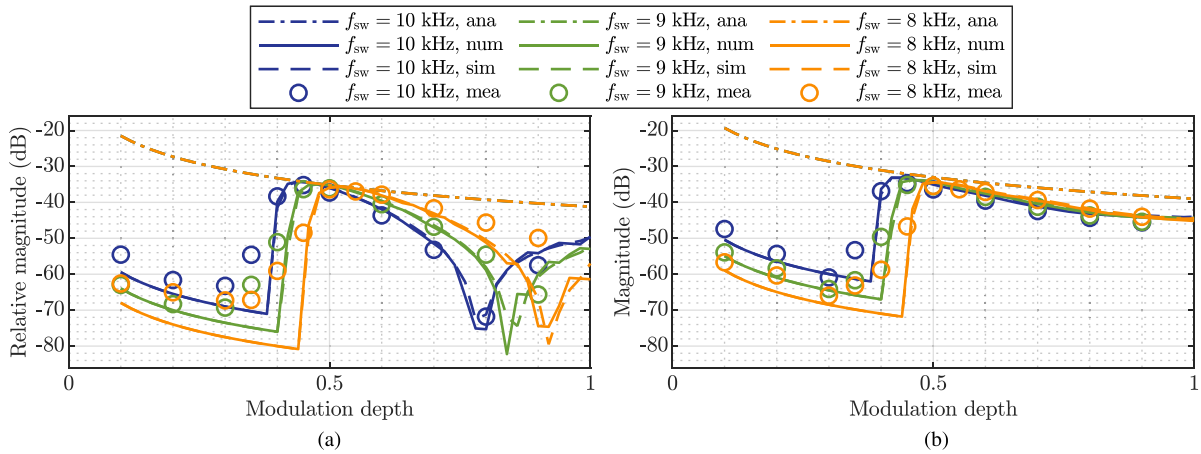

Fig. 19. (a) Relative magnitude of third harmonic and (b) magnitude of the total harmonic distortion under different switching frequency and modulation depth for the resistive load, where "ana", "num", "sim", and "mea" represent the results of the analytical model, presented numerical model, simulation, and experimental measurement, respectively.

the load phase angle on the output spectrum is minor in this case. However, it can be noted that the measured harmonic distortion are higher compared to the numerical model and the simulation, especially with higher modulation depth. The reason is that the inductive load can be saturated, which generates extra nonlinear harmonic distortion. The difference between the measurement and the numerical model and simulation is more obvious at higher modulation depth, indicating that this saturation effect is more severe at higher output current. Moreover, the results measured with $M = 0.9$ under $T_{\rm d} = 7\ \mu$s and $T_{\rm d} = 9\ \mu$s greatly deviate with both numerical method and the simulation in both Figs. 15 and 17. The reason of the deviation is that turn-ON and turn-OFF of the switches are assumed to be infinitely fast in both simulation and calculation. However, there are turn-ON and turn-OFF delays during MOSFET switching transients, as shown in Fig. 18. Taking the MOSFET $\rm S_2$ and $\rm S_3$ for example, during a switching cycle, the ideal on-time of the MOSFET is $\frac{1-m}{2}T_{\rm sw}$. Considering the dead-time, the required on-time $T_{\rm on,req}$ is

$$T_{\rm on,req} = \frac{1-m}{2}T_{\rm sw} - T_{\rm d}. \tag{34}$$

This value is used in the numerical model and simulation. Due to the turn-ON delay $T_{\rm d,on}$ and turn-OFF delay $T_{\rm d,off}$, the actual ON-time $T_{\rm on,act}$ is equal to

$$T_{\rm on,act} = \frac{1-m}{2}T_{\rm sw} - T_{\rm d} - T_{\rm d,on} + T_{\rm d,off} \tag{35}$$

where $T_{\rm d,on}$ is typically larger than $T_{\rm d,off}$. Therefore, the MOSFET ON-time used in numerical model and simulation is different with the actual experiment due to the switching transients. Normally this difference is small enough to be neglected. Nonetheless, when $M = 0.9$, the duty cycle of the switch can be as low as 0.05. For a switching frequency $f_{\rm sw} = 10$ kHz (with a switching period $T_{\rm sw} = 100\ \mu$s) and dead-time $T_{\rm d} \geq 5\ \mu$s, some switching cycles require the MOSFETs to be ON for a very short time interval, during which the mismatch of the turn-ON and turn-OFF delay turns to be significant and cannot be neglected, thus resulting in the deviation. In practice, this extreme case should be avoided, which can be governed by

$$\frac{T_{\rm d} + T_{\rm d,on}}{T_{\rm sw}} + \frac{M+1}{2} < 1. \tag{36}$$

D. Measurement With Different Switching Frequency

In this subsection, measurement results with different switching frequency under different modulation depth for the resistive load are presented in order to see the effect of different inductor current ripple. The filter inductor is 0.55 mH. The switching frequency is decreased from 10 to 8 kHz. Besides, the dead-time is also adjusted with the switching frequency so that in each measurement the dead-time is 1% of the switching period. In this case, the inductor current ripple is proportional to the switching period according to (9). In addition, different noise floor under different switching frequency has also been taken into account and the results are shown in Fig. 19.

As depicted in the figure, for a same dead-time percentage, both the third harmonic and the THD are of similar pattern. With a larger inductor current ripple, the measurement results are shifted in the figure to the right since SSCCM are guaranteed in a wider region. The results for the inductive load are very similar so they are omitted here.

In short, the results calculated by the presented numerical models fit with both simulation and experiment measurement generally, underlining the accuracy and effectiveness of the model. The results under different operating points with different loads also exposed that the proposed numerical model has a wide scope of application. Compared to the analytical model, an accuracy improvement up to about 30 dB can be achieved with the numerical model.

IV. Conclusion

Previous research on the output spectrum modeling of the SPWM H-bridge inverter with dead-time has not fully investigated the effect of different switching modes, which results

TABLE III
COMPARISON OF THE ANALYTICAL MODEL, NUMERICAL MODEL, AND SIMULATION

	Analytical	Numerical	Simulation
Accuracy	-	+	+
Computation speed	+	+	-
Feed-forward compensation	+	+	-
Simplicity	+	-	+

in an inaccurate model, especially with a large filter inductor current ripple. The aim of this article is to improve modeling accuracy for the output spectrum by taking the effects of different switching modes into consideration. The characteristics and effects of SSCCM, DCM, and HSCCM, respectively, caused by the inductor current ripple during dead-time are demonstrated. The voltage errors caused by the different switching modes in a fundamental period were calculated accurately. Four constraint functions were proposed to define the boundaries of the switching modes. By finding the zero-crossing points of the constraint functions, the existence and time position of the different switching modes have been determined. In addition, the proposed constraint functions can be used for filter inductance optimization in order to obtain SSCCM within a fundamental period. Based on the analytical expression of the voltage error and the time position of different switching modes, the moving average value of the output voltage can be obtained and the output spectrum can be modeled numerically. This numerical model was compared to the traditional analytical one given in [3], [26], and [27], and verified with both simulation and experiments.

The simulated and experimental results show that the presented numerical model improves the accuracy significantly compared to the traditional analytical one. When the filter inductor current ripple is low, the analytical and the presented numerical model give similar results. When the inductor current ripple is high, the presented model yields a much better accuracy. Compared to the analytical model, the presented numerical one gives more insight on the influence of SSCCM and DCM on output harmonics. Moreover, the numerical model shows similar accuracy compared to simulation but considerably saves computational cost especially at high switching frequencies. A basic comparison considering different aspects of the three methods is given in Table III. Additionally, the measurement results show that with a combination of high modulation index and high dead-time, the switch-node voltage pulses can be missing due to the very limited turn-ON time as explained in the above section. In this extreme case, none of the analytical model, numerical model, and simulation with ideal components is able to give the accurate output spectrum. Normally, this extreme case is not of interest and should be avoided in practice.

The proposed model provides a basis for accurate feed-forward dead-time compensation. The experimental measurements have demonstrated that when SSCCM is achieved in a fundamental period, the harmonic distortion is dominated by other factors which are not covered by the presented model. Hence, further research can be focused on the modeling of the distortion in this region, for example by taking the output capacitance of the switch and the on-resistance variation into consideration. Besides, bipolar modulation is used as an example of switching mode analysis. the principle of switching mode analysis still stands and can be extended for unipolar modulation with necessary adaptions. The exploration of unipolar modulation is desired in the future work. What's more, sensitivity analysis of the model with respect to different operating parameters, including the filter inductance, dead-time percentage, modulation depth, load impedance, and phase angle, should also be investigated in the future.

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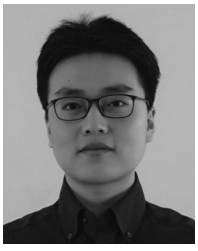

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