Modular Circulating Current and Second Harmonic Current Suppression Strategy by Virtual Impedance for DC Solid-State Transformer

Xiangqi Meng, Yanbing Jia, *Member, IEEE*, Chunguang Ren, *Member, IEEE*, Xiaoqing Han, *Member, IEEE*, and Peng Wang, *Fellow, IEEE*

***Abstract*—This article proposes a circulating current and second harmonic current (SHC) suppression method by introducing virtual impedance into the circulating current and output current feedback control loops of the dc solid-state transformer (DCSST). The virtual impedance is employed to adjust impedance in the circulating current feedback control loop to decrease the circulating current when the transmission efficiency of each dual active bridge is different. And a SHC suppression method, which introduces the virtual impedance containing a bandpass filter, is adopted to reduce the SHC and improve the dynamic performance of the DCSST. Moreover, a relatively independent modular control method, which is conducive to the modular expansion of the DCSST, is proposed. Compared with traditional DCSST control methods, the proposed method can simultaneously realize the output current sharing and effectively reduce the SHC with modular control. Finally, a DCSST prototype is built and the results of the experiment verify the validity and effectiveness of the proposed control strategy and solutions.**

***Index Terms*—Circulating current, dc microgrid, dc solid-state transformer (DCSST), second harmonic current (SHC), virtual impedance.**

I. Introduction

With a wide application of distributed power supplies and power electronic products, the proportion of dc power supplies and loads in the power grid is increasing. A dc microgrid is very convenient for the distributed power supplies and dc loads to plug in with less ac/dc conversion devices [1]–[3]. Also, the dc microgrid has a series of advantages, such as the easy expansion of the capacity, no issues of frequency and phase synchronization, improved the power quality of the user side, and fault isolation between ac and dc subsystems [4], [5]. Thus, the dc microgrid will have a broad prospect of development and application.

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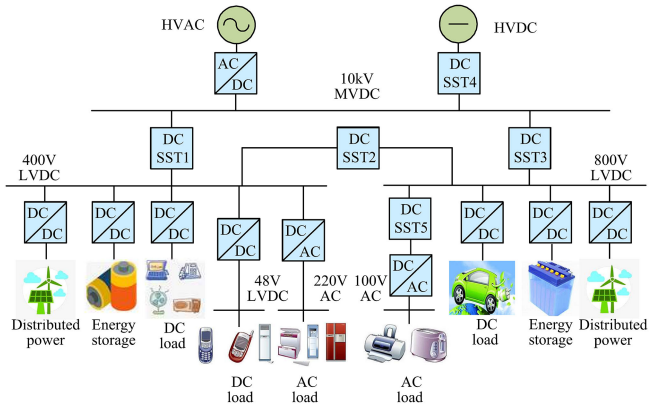


Fig. 1. Structure of the dc microgrid.

The structure of the dc microgrid is shown in Fig. 1. In the dc microgrid, dc/dc converters are essential for voltage conversion and energy interaction between distributed power sources and dc buses of different voltage levels. As the key dc/dc converter connecting dc bus bars with different voltage levels, dc solid-state transformer (DCSST) has attracted more attention [6], [7] and has been studied in a lot of literature [8]–[11]. In operation, different power parameters and line reactance between each dual active bridge (DAB) submodule can cause uneven transmission efficiency and power distribution imbalance among each submodule. Therefore, the output currents of DABs are different and the circulating current is generated; thus, the possibility of damaging some DABs and the system losses are increasing, and the operating efficiency of the whole system is reducing.

Given the uneven output current of each submodule of the DCSST, traditional current-sharing control methods, including the maximum current method, the average current method, and the droop control method are proposed. However, these control methods mainly rely on PI parameter adjustment for current-sharing, which requires a complex calculation but has limited effect. Besides, the adjusting methods for each submodule of the DCSST control the output current indirectly [12]–[15], such as comparing the actual power calculated by sampling voltage and current with the reference value of power [12], adjusting the

duty ratio of each DAB according to the active power component of duty ratio as feedback quantity [13], controlling the power with virtual power balance [14], controlling the power balance directly [15], and so on. These methods are complicated and slow in the calculation.

To overcome these shortcomings of power and current control, the circulating current suppression strategy based on virtual impedance has been proposed by scholars [16], [17]. Based on the closed-loop control of the inverter, the virtual impedance is added to regulate the output current equalization [18], [19]. The virtual impedance droop control is adopted to DCSST [20]. However, the strategy of virtual impedance selection to simultaneously suppress the circulating current and output voltage sags needs to be further discussed.

When the ac load is connected to the dc microgrid by inverters, the instantaneous output power of the inverter pulsates at twice the output frequency and a second harmonic current (SHC) will be generated in the DCSST. When the peak-to-peak value of the SHC in the DCSST exceeds 8% of the rated current, the conduction loss of the switch tube will be increased and the efficiency of the DCSST will be reduced. Furthermore, the SHC will increase the loss and decrease the use range and conversion efficiency of soft switch technology which is often used in the DAB control [21]. Once the SHC is transmitted to the distributed power and energy storage devices through the DCSST, the energy conversion efficiency and life of the devices will be greatly reduced [22], [23].

For the SHC suppression, large capacitance is adopted in [24], and a bidirectional converter is connected to the dc output bus in parallel to provide pulsating frequency for the inverter [25], [26]. But the additional equipment will increase the system losses and reduce energy density. Therefore, different SHC suppression control strategies are proposed, such as voltage and current two-loop control [27], adding virtual resistance to the current feedback [28], cascade voltage regulator with band-stop filter [29], capacitive voltage feedback of bandpass filter [30], and load current feedforward of notch-filter [31]. Although the [29]−[31] improves the dynamic response of the system, the control is more complex.

A control strategy is proposed in this article to suppress the circulating current and the SHC simultaneously. A virtual impedance is added to the circulating current feedback loop to suppress the circulating current and does not change the output characteristics of the DCSST. The virtual impedance with bandpass filter is added to the current loop, and the SHC suppression strategy with simple control logic is adopted based on the structure to ensure the dynamic response of the system. Moreover, the modularized control strategy of the DCSST is proposed to facilitate modularized expansion. Experimental results show that the proposed control strategy can suppress the circulating current and the SHC of DCSST and can improve the dynamic response characteristics under different power parameters and line reactance.

The rest of this article is organized as follows. Section II analyzes the causes of the circulating current and SHC in the DCSST. Section III proposes the circulating current suppression method. Section IV presents the SHC suppression method based on circulating current suppression. Section V shows modular DCSST control strategy with circulating current and SHC suppression. Section VI gives a comprehensive simulation and experimental verification. Finally, Section VII draws the conclusion.

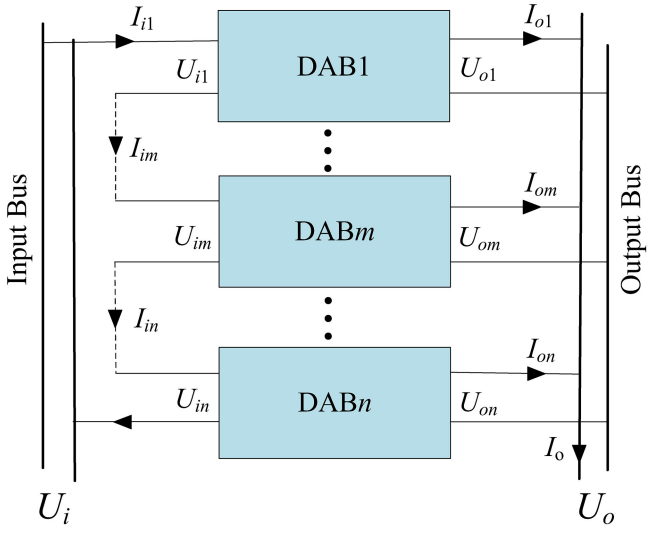


Fig. 2. Topology of the DCSST.

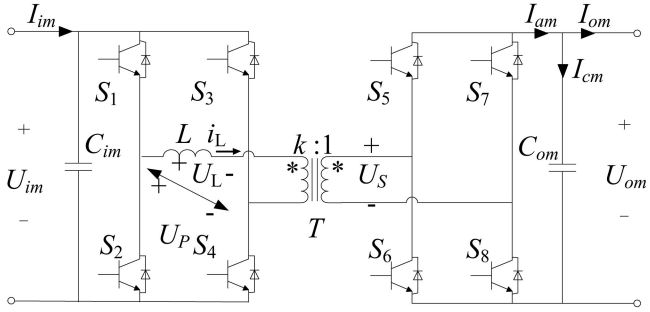


Fig. 3. Topology of each DAB.

II. Cause of the Circulating Current and SHC in DC Solid Transformer

A. Cause of the Circulating Current

The topology of the DCSST is shown in Fig. 2. The DCSST is composed of n modular DAB converters, and all the DABs are connected in series on the input side and in parallel on the output side. Each DAB is composed of one inductance (L), two full-bridge (FB), two capacitances (C_{im} and C_{om}), and one high-frequency isolated transformer (T), as shown in Fig. 3.

In Fig. 2, U_{im} and I_{im} are, respectively, the input voltage and current of the mth ($m = 1, 2, \ldots, n$) modules. U_{om} and I_{om} are, respectively, the output voltage and current of the mth modules. U_i and U_o are, respectively, the input voltage and output voltage of the DCSST. I_i and I_o are, respectively, the input current and output current of the DCSST.

In Fig. 3, C_{im} and C_{om} are the input and output capacitances of the mth DAB. I_{cm} is the current flowing through C_{om}. I_{am} is the current composed by I_{cm} and I_{om}.

For the DCSST, the power flows to each DAB can be described as follows:

$$I_{im}U_{im}\lambda_m = P_{im}\lambda_m = P_{om} = I_{om}U_{\mathrm{om}} \tag{1}$$

where λ_m is the efficiency of the *m*th DAB ($m = 1, 2, \ldots, n$) and P_{im} and P_{om} are, respectively, the input power and output power of the *m*th DAB.

When the DCSST adopts input voltage equalization control, the input voltage of each DAB module is equal, we have

$$U_{i1} = U_{i2} = \cdots = U_{\mathrm{in}}. \tag{2}$$

Since all the DABs are connected in series on the input side, the current of each DAB module on the input side is equal. The input power of each DAB module in DCSST can be expressed as

$$P_{i1} = P_{i2} = \cdots = P_{\mathrm{in}}. \tag{3}$$

Since all the DABs are connected in parallel on the output side, the voltage of each DAB module on the output side is equal. From (1) and (3), we have

$$\frac{I_{o1}}{\lambda_1} = \frac{I_{o2}}{\lambda_2} = \cdots = \frac{I_{\mathrm{on}}}{\lambda_n}. \tag{4}$$

Thus, the output current of each DAB module is related to the efficiency of itself as (4). The different line impedance and hardware parameters between each DAB module lead to different power losses, λ_m, and $I_{\mathrm{o}m}$. Due to the parallel output of each DAB module, the circulating current will be formed between different output branches.

As the definition of the circulating current of the *m*th DAB module, I_{hm} is

$$I_{hm} = I_{\mathrm{av}} - I_{om} \tag{5}$$

where $I_{\mathrm{av}} = \frac{1}{n}\sum_{m=1}^{n} I_{om}$ is the average value of the current on the output side of the DCSST. Once one of the output currents of the DAB modules $I_{\mathrm{o}m}$ is not equal to the others, $I_{hm} \neq 0$.

B. Cause of the SHC

For a linear load, the output voltage and current of the inverter can be described as

$$\begin{cases} u_{\mathrm{ac}} = \sqrt{2}U_{\mathrm{ac}}\sin\omega t \\ i_{\mathrm{ac}} = \sqrt{2}I_{\mathrm{ac}}\sin\left(\omega t - \theta\right) \end{cases} \tag{6}$$

where u_{ac} and i_{ac} are, respectively, the output voltage and current of the inverter, U_{ac} and I_{ac} are, respectively, the effective value of u_{ac} and i_{ac}, $\omega = 2\pi f_0$ is the angular frequency of the inverter, f_0 is the output frequency of the inverter, and θ is the phase shift angle between u_{ac} and i_{ac}.

Then the instantaneous output power of the inverter can be derived as

$$P_{\mathrm{oac}} = u_{\mathrm{ac}}i_{\mathrm{ac}} = U_{\mathrm{ac}}I_{\mathrm{ac}}\left[\cos\theta - \cos\left(2\omega t - \theta\right)\right]. \tag{7}$$

From (7), the output current of DCSST can be derived as

$$\begin{aligned} I_o &= \frac{P_{\mathrm{oac}}}{U_o} = \frac{U_{\mathrm{ac}}I_{\mathrm{ac}}}{U_o}\cos\theta - \frac{U_{\mathrm{ac}}I_{\mathrm{ac}}}{U_o}\cos\left(2\omega t - \theta\right) \\ &= I_{\mathrm{dc}} + I_{2\mathrm{ac}}. \end{aligned} \tag{8}$$

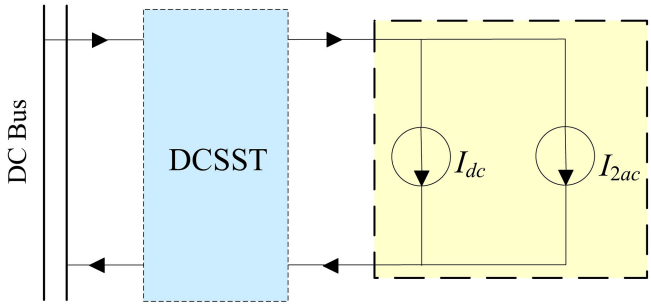


Fig. 4. Simplified dc microgrid with the inverter connected on one side.

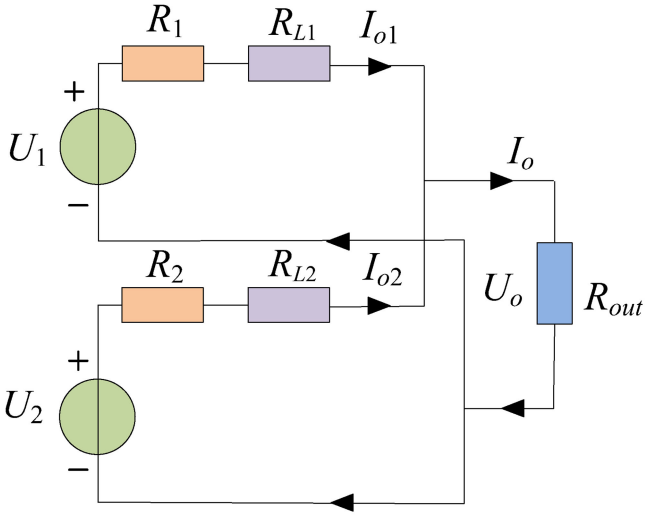


Fig. 5. Equivalent circuit diagram of the DCSST with two DAB modules.

According to (8), the output current of DCSST is composed of the dc component I_{dc} and the SHC component $I_{2\mathrm{ac}}$, where I_{dc} and $I_{2\mathrm{ac}}$ are

$$I_{\mathrm{dc}} = \frac{U_{\mathrm{ac}}I_{\mathrm{ac}}}{U_o}\cos\theta \tag{9}$$

$$I_{2\mathrm{ac}} = -\frac{U_{\mathrm{ac}}I_{\mathrm{ac}}}{U_o}\cos\left(2\omega t - \theta\right). \tag{10}$$

It can be seen from (10) that the SHC component pulsates at twice the output frequency.

The simplified dc microgrid with the inverter connected on one side is shown in Fig. 4. It is obvious that the SHC $I_{2\mathrm{ac}}$ caused by the inverter is flowing through the DCSST.

III. Circulating Current Suppression Method

A. Equivalent Circuit of DCSST

According to Thevenin's theorem, each DAB converter can be regarded as a series of the voltage source and equivalent resistance. The resistance of a low voltage line is much greater than that of a reactance [32]; so the reactance is neglected in this article.

The equivalent circuit of the DCSST with two DAB modules connected in parallel on the output side is shown in Fig. 5, where R_{L1} and R_{L2} are the line equivalent resistances, R_1 and R_2 are the equivalent internal resistances of DAB, U_1 and U_2 are the

equivalent voltage sources of two DAB modules, R_{out} is the load equivalent resistance, and U_o is the output voltage.

As shown in Fig. 5, the equivalent voltage source of two DAB modules can be derived as

$$U_1 = U_o + (R_1 + R_{L1})\, I_{o1} \tag{11}$$

$$U_2 = U_o + (R_2 + R_{L2})\, I_{o2}. \tag{12}$$

Subtracting (12) from (11), we have

$$U_1 - U_2 = (R_1 + R_{L1})\, I_{o1} - (R_2 + R_{L2})\, I_{o2}. \tag{13}$$

From (5), the circulating current of the first DAB module can be derived as

$$I_{h1} = \frac{I_{o2} - I_{o1}}{2}. \tag{14}$$

The traditional control strategy of DCSST is a two-loop control strategy combining the input voltage equalizing loop and output voltage loop. From (2), we have

$$U_1 = U_2. \tag{15}$$

According to (13) and (15), we have

$$(R_1 + R_{L1})\, I_{o1} = (R_2 + R_{L2})\, I_{o2}. \tag{16}$$

The output current of DCSST I_o can be described as

$$I_o = I_{o1} + I_{o2}. \tag{17}$$

From (16) and (17), we have

$$I_{o1} = \frac{(R_2 + R_{L2})\, I_o}{R_1 + R_{L1} + R_2 + R_{L2}}. \tag{18}$$

The circulating current of the first DAB module can be calculated from (14) and (18) as

$$\begin{aligned} I_{h1} &= \frac{(R_1 + R_{L1})\, I_o/2}{R_1 + R_{L1} + R_2 + R_{L2}} - \frac{(R_2 + R_{L2})\, I_o/2}{R_1 + R_{L1} + R_2 + R_{L2}} \\ &= \frac{(R_1 + R_{L1} - R_2 - R_{L2})\, I_o/2}{R_1 + R_{L1} + R_2 + R_{L2}} \\ &= \frac{(R_1 + R_{L1} - R_2 - R_{L2})\, U_o/2}{(R_1 + R_{L1} + R_2 + R_{L2})\, R_{\text{out}}}. \end{aligned} \tag{19}$$

Similar to (19), the circulating current of the *m*th DAB module can be expressed as

$$I_{hm} = \frac{R_m + R_{Lm} - \sum_{i=1, i\neq m}^{n} (R_i + R_{Li})}{2\sum_{i=1}^{n} (R_i + R_{Li})} \frac{U_{om}}{R_{\text{out}}}. \tag{20}$$

Since all the DABs are connected in parallel on the output side, the voltage of each DAB module on the output side can be derived as

$$U_{o1} = \cdots = U_{om} = \cdots = U_{on} = U_o. \tag{21}$$

It is obvious from (20) that the circulating current is related to the equivalent resistance and the resistance of the line of each DAB module.

Set

$$\begin{cases} R_{A1} = R_1 + R_{L1} = R \\ R_{Am} = R_m + R_{Lm} = \beta_{m-1} R \end{cases} \tag{22}$$

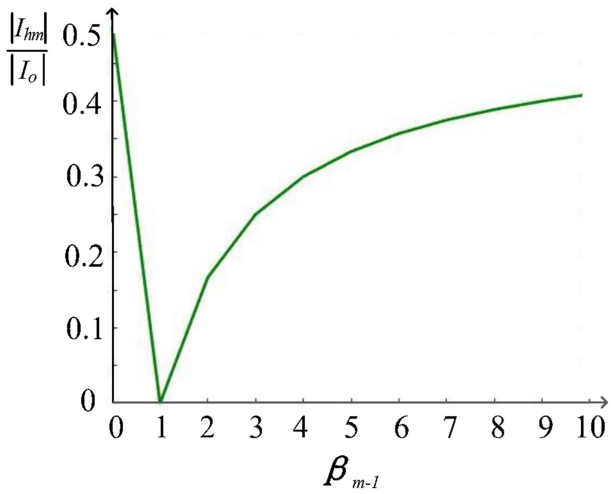


Fig. 6. Circulating current ratio of the *m*th DAB with different resistance coefficient.

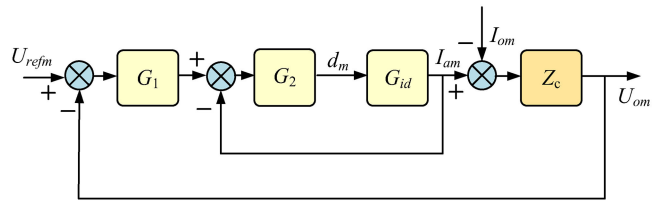


Fig. 7. Closed-loop control strategy of DAB.

where β_{m-1} is the resistance coefficient of the equivalent resistance of the *m*th DAB to the first DAB, and the value of β_{m-1} is between 0 and ∞. Derived from (22), the relationship between the circulating current to output current can be derived as

$$\left| \frac{I_{hm}}{I_o} \right| = \left| \frac{(1 - \beta_{m-1})}{2(1 + \beta_{m-1})} \right|. \tag{23}$$

The relation diagram of (23) can be expressed as Fig. 6.

It can be seen from Fig. 6 that the absolute value of circulating current increases following the resistance difference between DAB modules. The circulating current is equal to zero only when the resistances are the same, i.e., the β_{m-1} is equal to 1.

B. Circulating Current Impedance

The traditional closed-loop control block diagram adopted for DAB [33] is shown in Fig. 7.

In Fig. 7, $U_{\text{ref}m}$ is the reference voltage of the *m*th DAB. G_1 is the transfer function of the PI controller in the outer voltage loop. G_2 is the transfer function of the P controller in the current loop. G_{id} is the gain of the DAB. Z_c is the capacitance impedance. Then the output voltage function of DAB can be derived as

$$U_{om}(s) = \frac{G_1 G_2 G_{id} Z_c}{B_{om}(s)} U_{\text{ref}m}(s) - \frac{Z_c(1 + G_2 G_{id})}{B_{om}(s)} I_{om}(s) \tag{24}$$

where

$$B_{om}(s) = 1 + G_2 G_{id} + G_1 G_2 G_{id} Z_c. \tag{25}$$

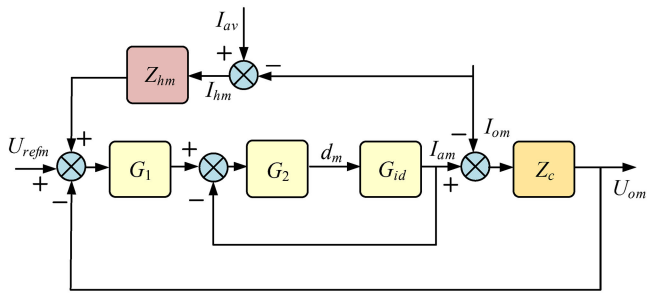


Fig. 8. Block diagram of DAB with virtual impedance.

Assuming control parameters and capacitive reactance of all the DABs are the same, we have

$$B_{o1} = B_{om} = \cdots = B_{on} = B_o \tag{26}$$

The output characteristic equation of the whole DCSST system can be derived from (24) and (26) as

$$U_o(\mathrm{s}) = \frac{G_1G_2G_{id}Z_c}{B_o}U_{rav}(s) - \frac{Z_c(1+G_2G_{id})}{B_o}I_{av}(s) \tag{27}$$

where $U_{rav}(s) = \frac{1}{n}\sum_{m=1}^{n} U_{refm}(s)$ is the average reference voltage, and $I_{rav}(s) = \frac{1}{n}\sum_{m=1}^{n} I_{om}(s)$ is the average output current.

From (24) and (27), the circulating current of the *m*th DAB can be derived as

$$I_{hm}(s) = \frac{G_1G_2G_{id}}{1+G_2G_{id}}\left[U_{rav}(s) - U_{refm}(s)\right]. \tag{28}$$

According to the concept of the circulating current impedance Z_{hm} [34], Z_{hm} is defined as

$$Z_{hm} = \frac{\Delta U_{\mathrm{refm}}}{\Delta I_{hm}} \tag{29}$$

From (28) and (29), the closed-loop circulating current impedance can be derived as

$$Z_{hm} = -\frac{1+G_2G_{id}}{G_1G_2G_{id}}. \tag{30}$$

The circulating current impedance is reduced due to the large gain under the closed-loop control, which is not conducive to the suppression of circulating current.

C. Circulating Current Suppression Strategy With Additional Virtual Impedance

The closed-loop circulating current impedance is not large enough to suppress the circulating current. Thus, the virtual impedance is introduced into the circulating current feedback loop to adjust the circulating current impedance, as shown in Fig. 8.

With the virtual impedance Z_{vm} in the circulating current feedback loop, the closed-loop circulating current impedance can be derived as

$$Z_{hm} = -\frac{Z_c(1+G_2G_{id}) + Z_{vm}}{Z_cG_1G_2G_{id}}. \tag{31}$$

Similar to (28), we have

$$I_{hm}(s) = \frac{G_1G_2G_{id}Z_c}{Z_c(1+G_2G_{id}) + Z_{vm}}\left[U_{rav}(s) - U_{refm}(s)\right]. \tag{32}$$

According to (27) and (32), the DAB output characteristic equation with additional virtual impedance can be derived as

$$U_{om}(s) = \frac{G_1G_2G_{id}Z_c}{B_{om}}U_{\mathrm{refm}}(s) - \frac{Z_c(1+G_2G_{id})}{B_{om}}I_{om}(s) + \frac{Z_{vm}}{B_{om}}I_{hm}(s). \tag{33}$$

It is obvious that the circulating current can be controlled by the value of additional virtual impedance to the circulating current feedback.

Since all the DABs are connected in parallel on the output side, the voltage of each DAB module on the output side is equal. The relationship of the output current of each DAB can be derived according to (5) and (33) as follows:

$$\begin{aligned}&\left(Z_c(1+G_2G_{id}) + Z_{vm}\right)I_{o1}(s)\\ &\quad= \cdots = \left(Z_c(1+G_2G_{id}) + Z_{vm}\right)I_{om}(s)\\ &\quad= \cdots = \left(Z_c(1+G_2G_{id}) + Z_{vm}\right)I_{on}(s).\end{aligned} \tag{34}$$

When Z_{vm} is large enough to neglect the effect of $Z_c(1+G_2G_{id})$, the output current of each DAB module is equal, which means the circulating current is suppressed.

The sum of the circulating currents between the DAB modules can be derived from (5) as

$$I_{h1} + I_{h2} + \cdots + I_{hm} + \cdots I_{hn} = 0. \tag{35}$$

It can be seen from (33) and (35) that the output characteristic equation of the whole system (DCSST) after adding virtual impedance can be derived as

$$U_o(\mathrm{s}) = \frac{G_1G_2G_{id}Z_c}{B_o}U_{rav}(s) - \frac{Z_c(1+G_2G_{id})}{B_o}I_{av}(s). \tag{36}$$

The output characteristic of the whole system is the same as that of the traditional system (27). Therefore, the introduction of virtual impedance does not change the output characteristics of DCSST and does not cause output voltage sags, nor does it change the stability of DCSST.

Since Z_{vm} is large enough, the simplified relationship between circulating current impedance and virtual impedance can be derived as

$$Z_{vm} \approx -G_1G_2G_{id}Z_cZ_{hm}. \tag{37}$$

The circulating current impedance is configured as $Z_{hm} = R_{hm}s$.Since G_2G_{id} is a coefficient, a new PI could be defined as

$$G_m = G_1G_2G_{id} = K_{pm} + \frac{K_{im}}{\mathrm{s}}. \tag{38}$$

The virtual impedance can be derived from (37) and (38) as

$$Z_{vm} = K_{phm} + K_{ihm}/\mathrm{s} \tag{39}$$

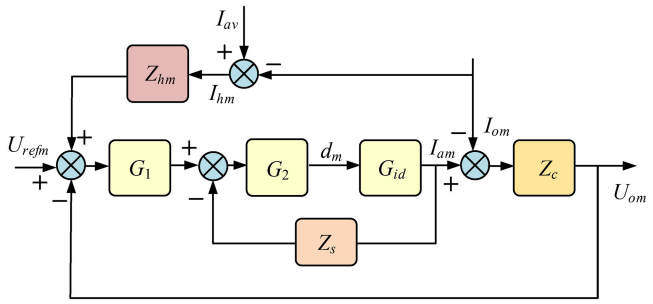


Fig. 9. Block diagram of the proposed SHC suppression method.

where

$$\begin{cases} K_{phm} = -K_{pm} \times Z_{hm} Z_c \\ K_{ihm} = -K_{im} \times Z_{hm} Z_c. \end{cases}$$

Since the virtual impedance contains an integral part, the virtual impedance in this article can adaptively adjust the circulating current feedback according to the size of the circulating current.

IV. SHC Suppression Method

A. SHC Suppression Method

The SHC is generated by the inverters connected to the output side of the DCSST; to avoid its inflow into DCSST, the output closed-loop impedance of each DAB module needs to be increased. In this article, the SHC is suppressed by adding a virtual impedance Z_s to the output current feedback loop, as shown in Fig. 9.

The virtual impedance with large constant resistance R_s in the whole frequency band was selected in [28]. However, the worse dynamic performance of the system comes with SHC suppression.

The virtual impedance that has a high resistance at the twice frequency and low resistance at other frequencies is needed to ensure the good dynamic performance of the system. Therefore, the virtual impedance of the bandpass filter is chosen in this article, as shown in the following equation:

$$Z_s = R_s G_{\mathrm{BPF}} \tag{40}$$

where R_s is the impedance amplitude of Z_s at $2f_0$and G_{BPF} is a bandpass filter with a central frequency of $2f_0$.

The G_{BPF} can be expressed as

$$G_{\mathrm{BPF}} = \frac{s/\left(Q \times \omega_{\mathrm{BPF}}\right)}{\left(s/\omega_{\mathrm{BPF}}\right)^2 + s/\left(Q \times \omega_{\mathrm{BPF}}\right) + 1} \tag{41}$$

where $\omega_{\mathrm{BPF}}= 2f_0 \times 2\pi$ is the central angular frequency of the bandpass filter and Q is the quality factor of the bandpass filter.

The Bode diagrams of the $Z_s = R_s G_{\mathrm{BPF}}$ and $Z_s = R_s$ are shown in Fig. 10.

It is shown in Fig. 10 that $Z_s = R_s$ is a high amplitude resistance in the whole frequency band, which will harm the dynamic performance of the system. But $Z_s = R_s G_{\mathrm{BPF}}$ presents a resistance with a high amplitude at $2f_0$ and a small amplitude at other frequencies.

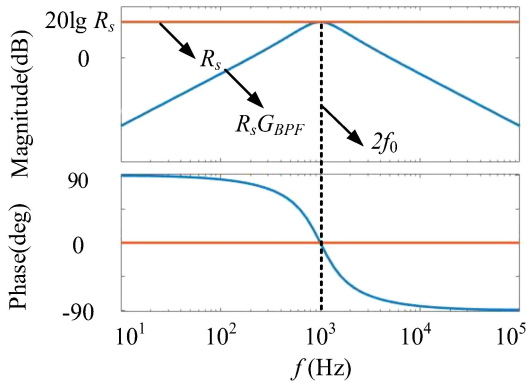


Fig. 10. Bode diagrams of the virtual impedance.

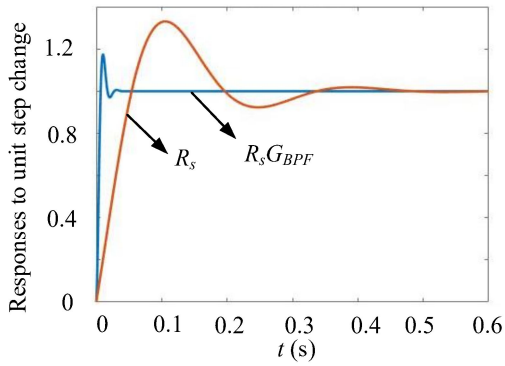


Fig. 11. Unit step dynamic responses of the DAB.

With the virtual impedance added to the output current loop, the transfer function of the voltage can be derived as

$$\frac{U_{om}(\mathrm{s})}{U_{\mathrm{ref}m}(s)} = \frac{G_1 G_2 G_{id} Z_c}{1 + Z_s G_2 G_{id} + G_1 G_2 G_{id} Z_c}. \tag{42}$$

Fig. 11 gives unit step dynamic responses of the DAB. It can be seen that the virtual resistance with the bandpass filter has better dynamic performance than the virtual resistance at the characteristics of the regulation time and overshoot. That means the virtual impedance control strategy proposed in this article combined with the bandpass filter can not only ensure the suppression effect of the SHC but also have a faster response speed of the system when the load changes.

B. Selection of Main Parameters and Stability Analysis

The Bode diagrams of the bandpass filter with different quality factor Q are expressed in Fig. 12.

It is shown in Fig. 12 that the larger the quality factor Q, the better the pass-wave performance of the bandpass filter, but the smaller the frequency range.

The unit step dynamic responses of the DAB with different quality factor Q are expressed as Fig. 13.

As shown in Fig. 13, when the Q value increases, the regulation time and overshoot of the DAB increase, which affects the dynamic performance of the DCSST when the load changes suddenly. Therefore, the Q value is selected as 1 after comprehensive consideration of the pass-wave property and dynamic characteristics.

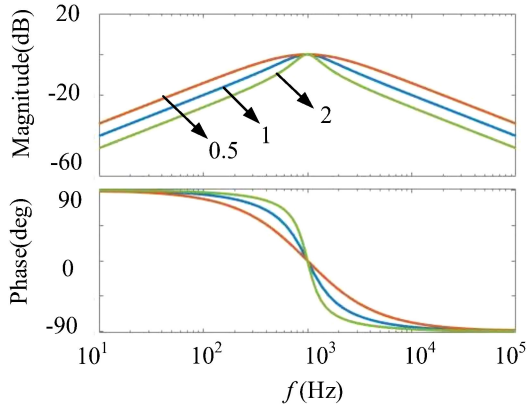


Fig. 12. Bode diagrams of $Q = 0.5, 1, 2$.

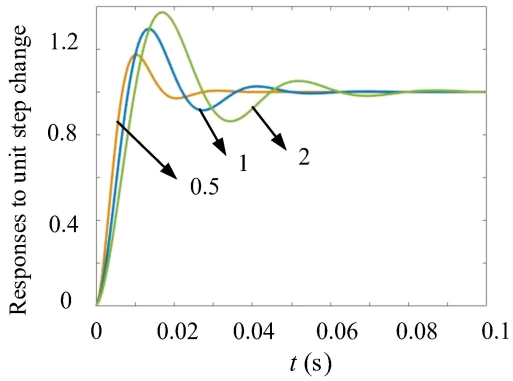


Fig. 13. Unit step dynamic responses of $Q = 0.5, 1, 2$.

TABLE I
ROUTH TABLE OF THE CLOSED-LOOP SYSTEM

Rank	Routh array		
S^4	H_1	H_3	H_5
S^3	H_2	H_4	0
S^2	M_1=(H_2 H_3- H_1 H_4)/ H_2	M_2= H_5	0
S^1	M_3=(M_1 H_4- M_2 H_2)/M_1	0	0
S^0	M_6= M_2=H_5	*0*	0

The characteristic root equation of the closed-loop transfer function of the DAB can be obtained from (42) as

$$H_1 s^4 + H_2 s^3 + H_3 s^2 + H_4 s^1 + H_5 s^0 = 0 \qquad (43)$$

where

$$\begin{cases} H_1 = C_{o1}Q \\ H_2 = C_{o1}\omega_{\mathrm{BPF}} + C_{o1}G_{id}R_s\omega_{\mathrm{BPF}}k_{p2} + QG_{id}k_{p1}k_{p2} \\ H_3 = QG_{id}k_{p2}k_{i1} + G_{id}k_{p1}k_{p2}\omega_{\mathrm{BPF}} + C_{o1}Q{\omega_{\mathrm{BPF}}}^2 \\ H_4 = G_{id}\omega_{\mathrm{BPF}}k_{p2}k_{i1} + G_{id}k_{p1}k_{p2}Q{\omega_{\mathrm{BPF}}}^2 \\ H_5 = G_{id}k_{p1}k_{p2}Q{\omega_{\mathrm{BPF}}}^2 \end{cases}$$

where k_{p1} and k_{i1} are the parameters of the PI controller in the voltage loop, and k_{p2} is the parameter of the P controller in the current loop.

From (43), Routh table of the closed-loop system can be written as shown in Table I.

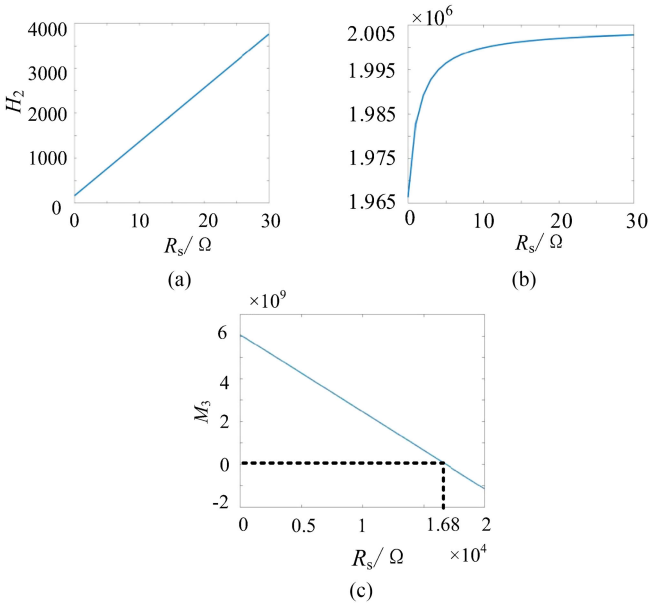


Fig. 14. Relationship between the virtual resistance and the first column coefficient. (a) Coefficient of H_2. (b) Coefficient of M_1. (c) Coefficient of M_3.

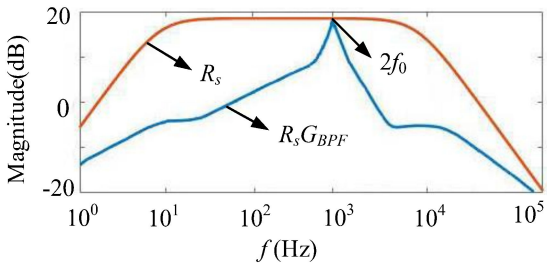


Fig. 15. Bode diagram of DAB's equivalent output impedance.

The steady condition of the system is that the coefficients in the first column of the Routh table are all positive, that is, the roots of its characteristic equation are all in the left half plane of s.

The relationship between the virtual resistance and the first column coefficient in the Routh criterion table can be expressed as Fig. 14.

The coefficients H_1 and H_5 are always above zero. From Fig. 14(a) and (b), with the change of R_s, the coefficients H_2 and M_1 are always above zero. From Fig. 14(c), the coefficient M_3 decreases with the increase of R_s.

Therefore, when the value of the virtual resistance R_s is less than 1.68×10^4, the system is stable.

The Bode diagram of DAB's equivalent output impedance under the control strategy proposed in this article can be expressed as Fig. 15.

Fig. 15 compared the equivalent output impedance between the method in [28] and this article. The strategy in this article has a large impedance at twice the frequency, but a smaller impedance at other frequencies, which is conducive to the suppression of the SHC and the improvement of the dynamic performance of the DAB.

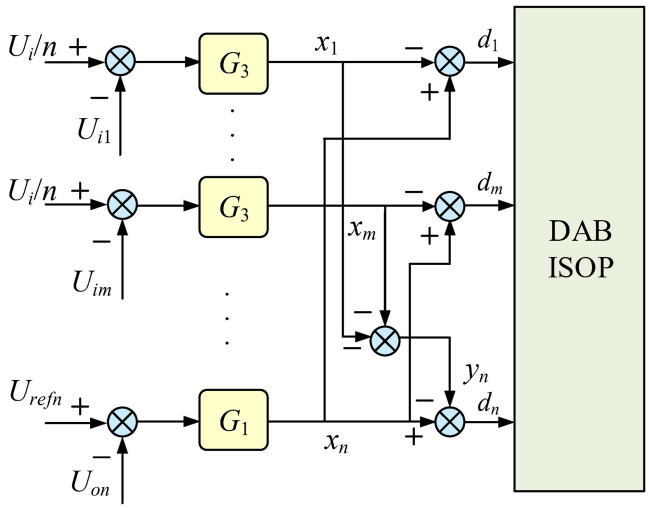


Fig. 16. Traditional DCSST control strategy.

V. Modular DCSST Control Strategy With Circulating Current and SHC Suppression

The DCSST is a cascade of n DAB modules. When the DCSST is used in different voltage systems, the number of DAB modules in the DCSST is variable to meet different requirements for input voltage and output current. It is conducive to the modular expansion of the DCSST that controls each DAB relative independent.

The traditional DCSST control strategy is shown in Fig. 16 [10].

Here, $x_m (m = 1, 2, \ldots, n)$ and y_n are the control quantity of the DAB modules. G_3 is the PI controller of input voltage equalizing loop. It can be found from Fig. 16 that the control amount of the last module is related to the previous modules, which is not conducive to the expansion of the system modularization.

It can be noticed from Fig. 16 that y_n can be expressed as

$$y_n = -\sum_{m=1}^{n-1} x_m = -\sum_{m=1}^{n-1} (U_i/n - U_{im}) G_3. \tag{44}$$

According to (44), we have

$$y_n = -G_3[(n-1)\,U_i/n - \sum_{m=1}^{n-1} U_{im}]. \tag{45}$$

As the DAB module is connected in series on the input side of DCSST, the input side voltage of DCSST is U_i, we can get

$$\sum_{m=1}^{n-1} U_{im} = \left(U_{i1} + U_{i2} + \cdots + U_{im} + \cdots + U_{i(n-1)}\right) = (U_i - U_{\text{in}})\,. \tag{46}$$

From (45) and (46), we have

$$\begin{aligned} y_n &= -G_3[(n-1)\,U_i/n - (U_i - U_{\text{in}})] \\ &= G_3(U_i/n - U_{\text{in}}). \end{aligned} \tag{47}$$

From (47), after the modularization derivation, the control quantity of the last module is independent of the previous modules. According to Fig. 16, when the control of the last module is independent of the previous modules, the control of each module is relatively independent, which is conducive to the expansion of the DAB module in DCSST. The improved modular control strategy can be expressed in Fig. 17.

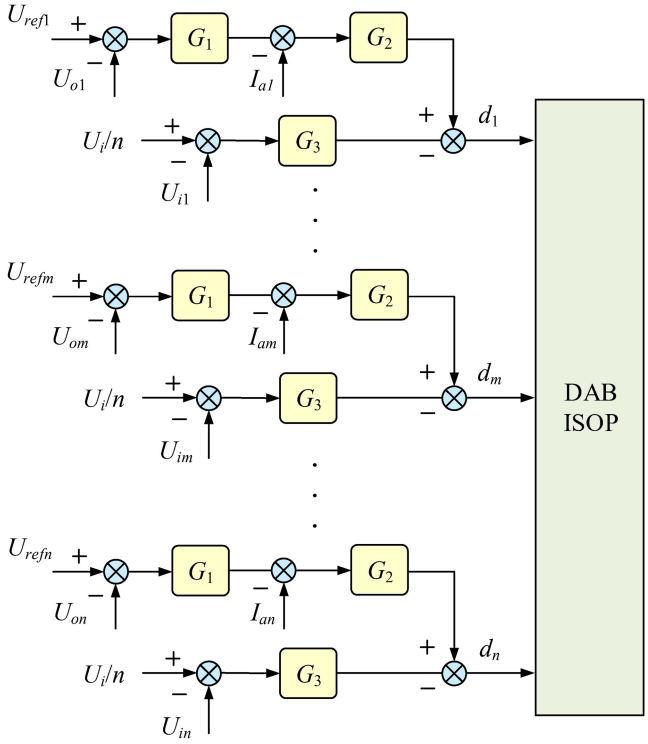


Fig. 17. Improved modular DCSST control strategy.

TABLE II
Parameters

DAB parameters	Inductance L/μH	Line resistance R/Ω	Capacitance C/μF	Switching frequency f/kHz
DAB 1	22	0.5	1000	50
Other DABs	20	0	1000	50

The improved modular control strategy enables each DAB module in DCSST to work relatively independently, while the whole DCSST system can expand the number of modules better.

Based on the improved modular control strategy of the DCSST, the circulating current and SHC suppression methods based on virtual impedance are added. The control block diagram is shown in Fig. 18.

VI. Experimental and Simulation Results Analysis

The DCSST composed of n DAB modules was built. The parameters are shown in Table II. The high frequency transformer ratio is 1:1. The rated voltage on the input side is $n \times 100$ V, and the rated voltage on the output side is 100 V. The input rated current is 10 A and the output rated current is $n \times 10$ A.

To verify the effect of different control methods, three control methods are adopted in this article.

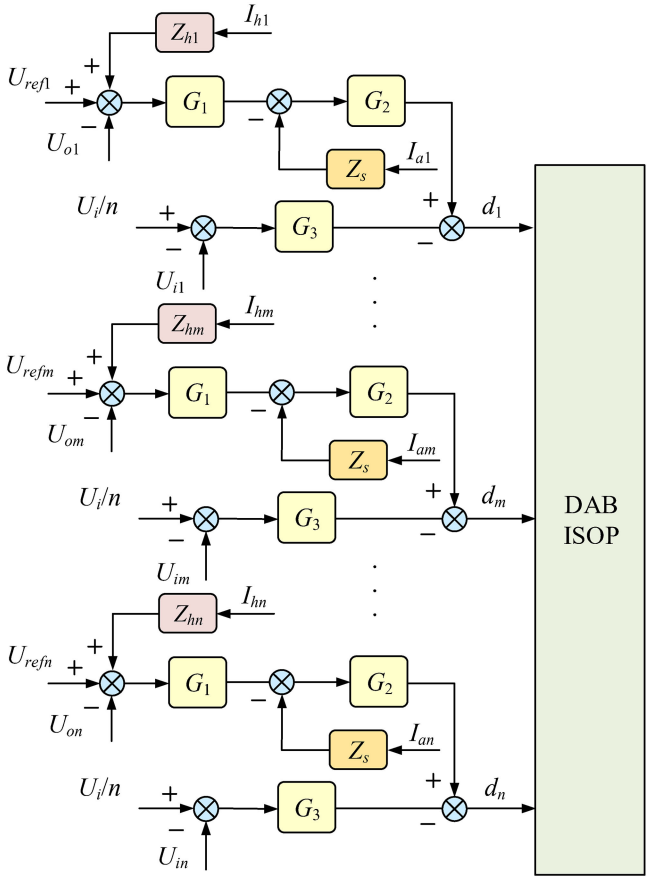


Fig. 18. Modular DCSST control strategy with circulating current and SHC suppression methods.

1) Control Method I: the traditional control method without circulating current and SHC suppression method.
2) Control Method II: with the circulating current suppression method only.
3) Control Method III: the control strategy proposed in this article.

A. Simulation Results

The DCSST with 2, 3, 4, and 5 DAB modules is built in MATLAB/Simulink separately, and the output frequency of the inverter is 50 Hz. Two kinds of disturbance are added to the system: The first one is to decrease the output load of the DCSST at $t = 0.01$ s, and the second one is to increase the output load of the DCSST at $t = 0.06$ s. Because the simulation waveforms are very similar, only the simulation waveforms with 5 DAB modules by three control methods are shown in Figs. 19 –21.

Here, I_{a1}, I_{a2}, I_{a3}, I_{a4}, and I_{a5} are the output current of the first, second, third, fourth, and fifth modules, respectively. U_o is the output voltage of the DCSST in Figs. 19−21.

Figs. 19–21 show the simulation waveform of control methods I, II, and III, respectively.

The output current deviation and SHC of DCSST with different control methods are compared in Table III.

In Table III, it is obvious that the circulating current suppression method can reduce the output current deviation between

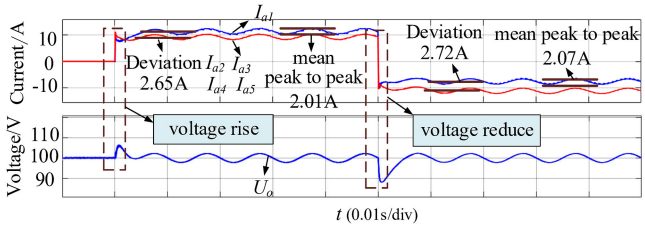


Fig. 19. Simulation waveform of control method 1.

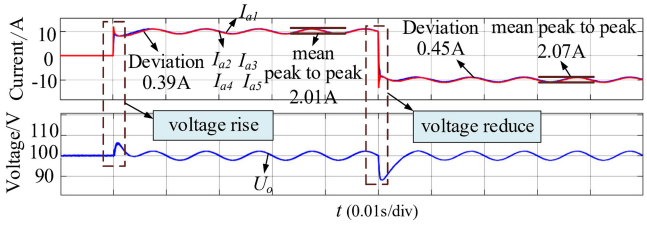


Fig. 20. Simulation waveform of control method II.

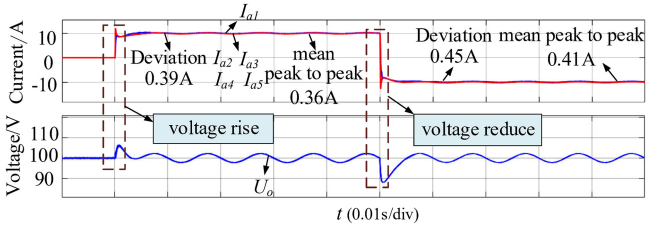


Fig. 21. Simulation waveform of control method III.

TABLE III
CHARACTERS OF DCSST WITH DIFFERENT CONTROL METHODS

SCENE	CHARACTER OF DCSST		METHOD I	METHOD II	METHOD III
Load decreases	deviation	Value(A)	2.65	0.39	0.39
		Ratio(%)	28.2	4.1	4.1
	SHC	Value(A)	2.01	2.01	0.36
		Ratio(%)	21.4	21.4	3.8
Load increase	deviation	Value(A)	2.72	0.45	0.45
		Ratio(%)	27.8	4.6	4.6
	SHC	Value(A)	2.07	2.07	0.41
		Ratio(%)	21.1	21.1	4.2

five DAB modules regardless of whether the SHC suppression method is used or not. The SHC can be suppressed by the SHC suppression method.

The simulation results with 2, 3, or 4 DAB modules are very similar to the results with 5 DAB modules. The ratios of circulating current and SHC with the proposed method are less than 5% and much less than the traditional method, which means the performance of the proposed method is independent of the number of DAB modules. The proposed method is effective.

B. Experimental Results

A DCSST prototype composed of two DAB modules is constructed, as shown in Fig. 22. The switch tube selects the CAS120M12BM2 type SiC MOSFET of CREE. TMS320F28335 was selected for DSP chip. The circulating current impedance

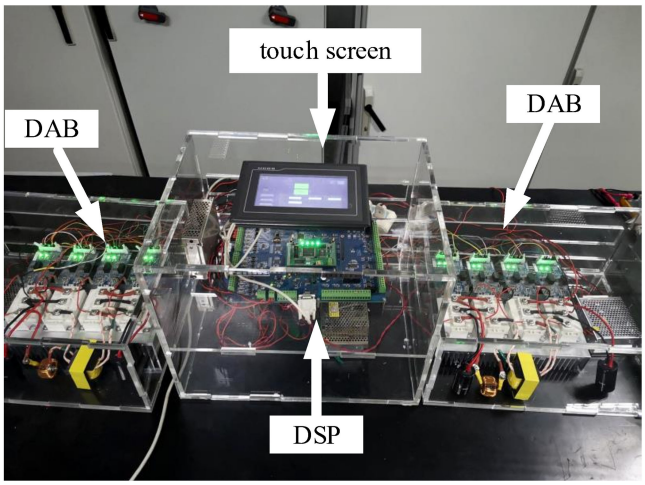


Fig. 22. Prototype of DCSST.

is configured as Z_{hm}. In order to suppress the SHC, the virtual impedance added in the output current feedback loop is Z_s. The output frequency of the inverter is 500 Hz.

The experiment sets the allowable fluctuation range of dc bus voltage on the output side to be 92−105 V. When the dc bus voltage of the output side is greater than 105 V, power flows from the output side to the input side; when the dc bus voltage of the output side is less than 92 V, power flows from the input side to the output side.

The experimental waveforms of the three control methods are shown in Figs. 23–25. Two kinds of disturbance are added to the system: the first one is to decrease the output load of DCSST at $t = 170$ ms in Figs. 23–25(a), and the second one is to increase the output load of DCSST at $t = 238$ ms in Figs. 23–25(b).

Here, I_{a1} and I_{a2} are the output current of the first and second modules. I_i is the input current of the DCSST. U_o is the output voltage of the DCSST. U_{i1} and U_{i2} are the input voltages of the first and second modules, respectively, as shown in Figs. 23−25.

Fig. 23 shows the experimental waveform of control method I.

As shown in Fig. 23(a), the output current deviation of the two DAB modules is 1.4 A, 24.9% of rated current. And the peak-to-peak value of the SHC of the output current is 1.1 A, 19.6% of rated current. As shown in Fig. 23(b), the output current deviation of the two DAB modules is 1.3 A, 27.4% of rated current. The peak-to-peak value of the SHC of the output current is 1 A, 21.1% of rated current.

Figs. 24 and 25 show the experimental waveform of control methods II and III, respectively.

The output current deviation and SHC of DCSST with different control methods are compared in Table IV.

In Table IV, it is obvious that the circulating current suppression method can reduce the output current deviation between two DAB modules regardless of whether the SHC suppression method is used or not. And the SHC can be suppressed by the SHC suppression method.

In order to verify the dynamic performance of virtual resistance containing bandpass filter in SHC suppression method, the

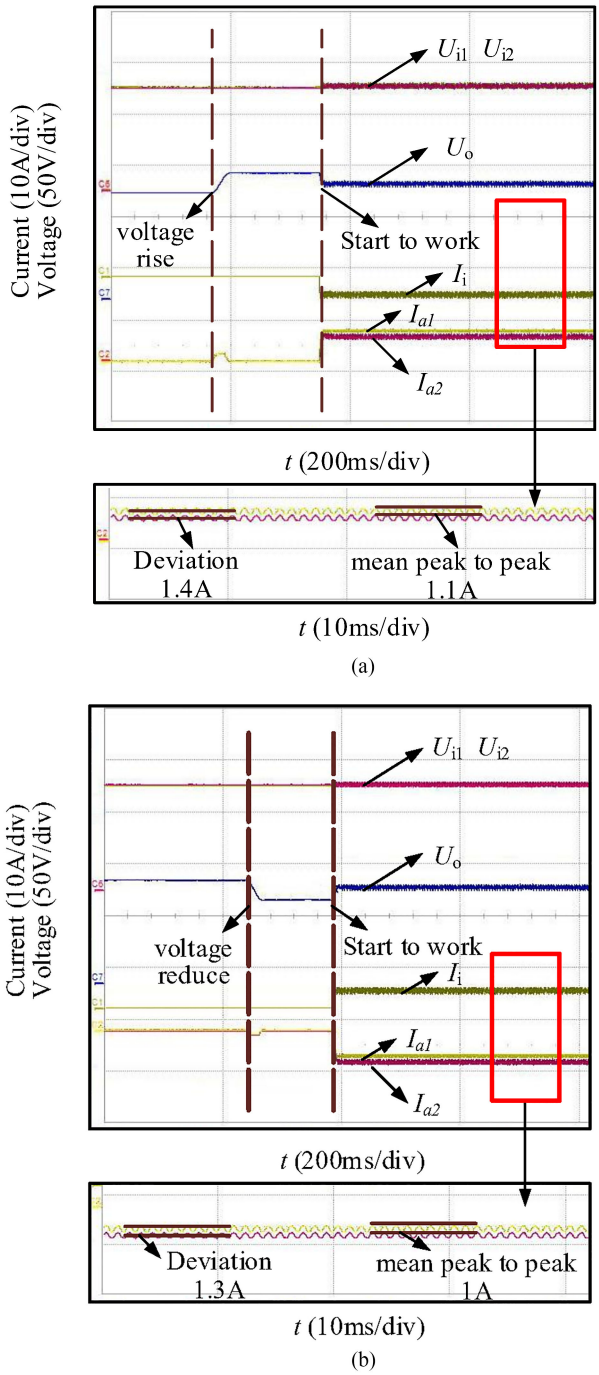
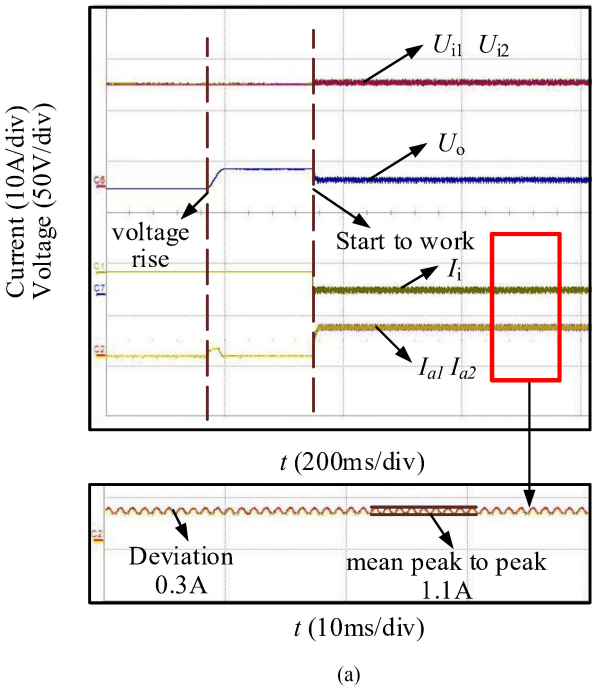


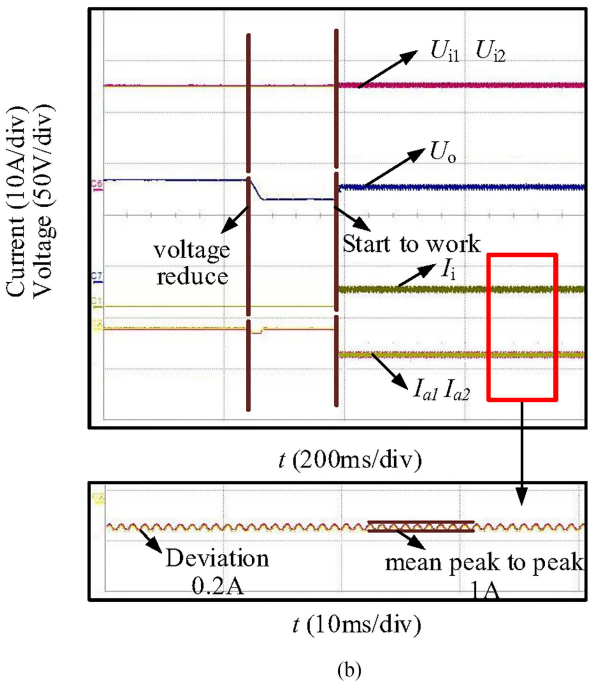
Fig. 23. Experimental waveform of control method 1. (a) Load decreases. (b) Load increases.

output waveforms of DCSST adopted control method III, with virtual impedance containing or not containing a bandpass filter, are compared in Fig. 26.

As can be seen from Fig. 26(a) and (b), when the virtual resistance containing a bandpass filter is added into the SHC suppression, the bus bar voltage regulation process is 12 ms, and there is no significant voltage overshoot in the dynamic regulation process. When the virtual resistance without the

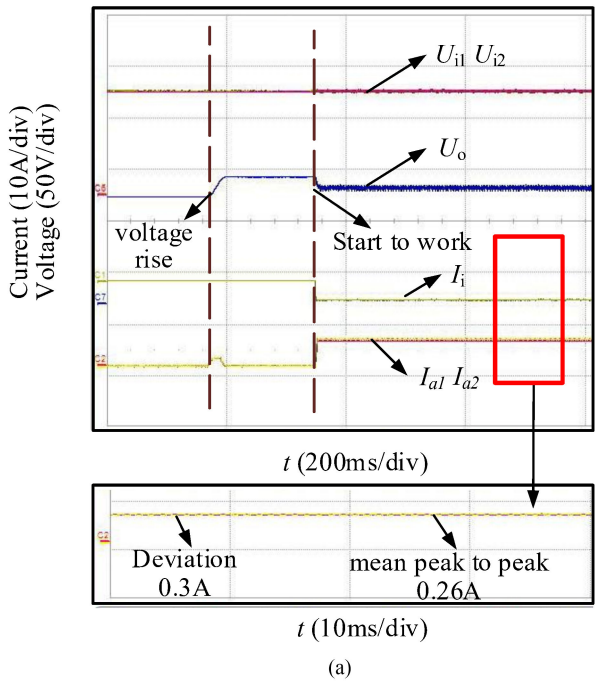


(a)

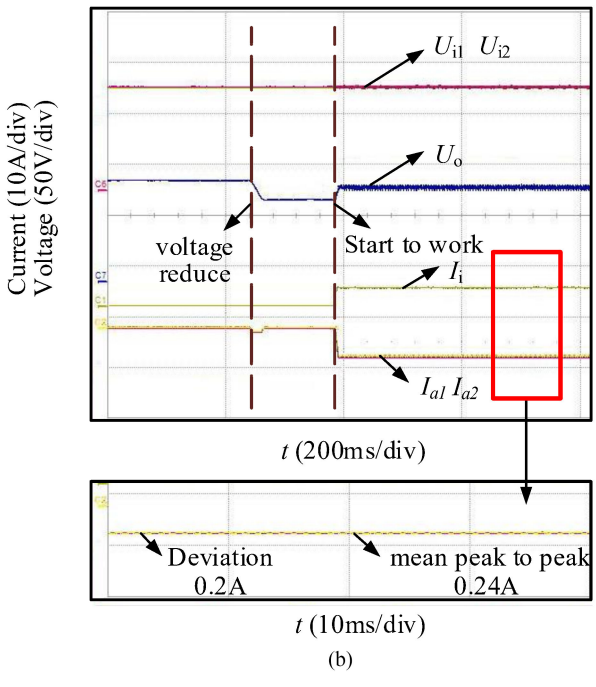


(b)

Fig. 24. Experimental waveform of control method II. (a) Load decreases. (b) Load increases.



(a)



(b)

Fig. 25. Experimental waveform of control method III. (a) Load decreases. (b) Load increases.

bandpass filter is added in the SHC suppression, the bus bar voltage regulation process is 25 ms, and there is an obvious voltage overshoot of 5.8 V in the dynamic regulation process.

As can be seen from Fig. 26(c) and (d), when the virtual resistance containing a bandpass filter is added into the SHC suppression, the bus bar voltage regulation process is 10 ms, and there is no significant voltage overshoot in the dynamic regulation process. When the virtual resistance without the bandpass filter is added in the SHC suppression, the bus bar voltage regulation process is 23 ms, and there is an obvious voltage overshoot of 4.7 V in the dynamic regulation process.

According to the above experimental results, compared with method I (traditional method), method III (proposed in this article) effectively reduces the DCSST circulating current (about 20%) and the SHC (about 15%). When the virtual resistance with a bandpass filter is added, the overshoot of the system (by about

TABLE IV
CHARACTER OF DCSST WITH DIFFERENT CONTROL METHODS

SCENE	CHARACTER OF DCSST		METHOD I	METHOD II	METHOD III
Load decreases	deviation	Value(A)	1.4	0.3	0.3
		Ratio(%)	24.9	5.3	5.3
	SHC	Value(A)	1.1	1.1	0.26
		Ratio(%)	19.6	19.6	4.6
Load increase	deviation	Value(A)	1.3	0.2	0.2
		Ratio(%)	27.4	4.2	4.2
	SHC	Value(A)	1	1	0.24
		Ratio(%)	21.1	21.1	5.0

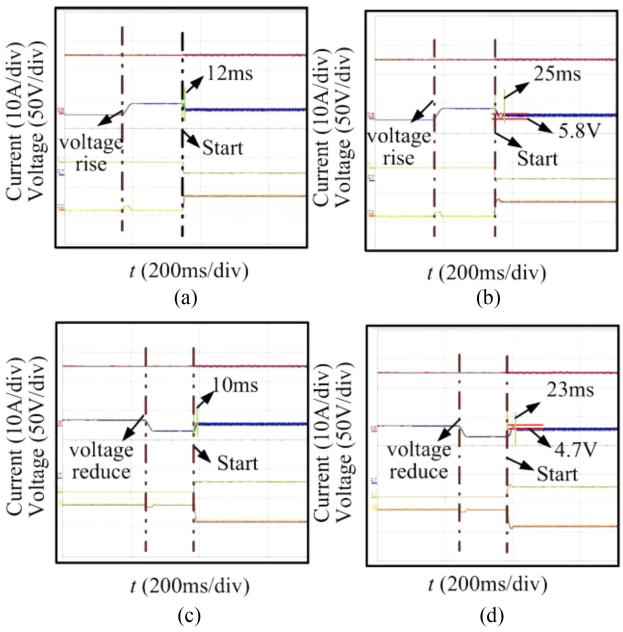


Fig. 26. Experimental waveform of control method III for dynamic performance comparison. (a) Load decrease with a bandpass filter. (b) Load decrease without bandpass filter. (c) Load increase with a bandpass filter. (d) Load increase without bandpass filter.

5 V) and the regulation time (by about 50%) are reduced, and the dynamic performance is effectively improved.

VII. CONCLUSION

The circulating current and SHC suppression methods are proposed in this article for DCSST. The circulating current suppression method adjusts the circulating current by adding virtual impedance in the circulation feedback loop of each DAB module in DCSST, which solves the problem of circulating current caused by different parameters and line resistance of each DAB module. The SHC suppression method by virtual resistance containing a bandpass filter for the DCSST not only effectively reduces the SHC, but also improves the dynamic performance of the system. In particular, the modular DCSST control strategy with circulating current and SHC suppression methods can not only suppress SHC and circulating current but also facilitate the modular expansion of DCSST.

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