GaN-Based ZVS Bridgeless Dual-SEPIC PFC Rectifier With Integrated Inductors

Yunfeng Liu, *Student Member, IEEE*, Xiaosheng Huang, *Member, IEEE*, Yi Dou, *Student Member, IEEE*, Ziwei Ouyang, *Senior Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—This article investigates the gallium nitride based bridgeless dual single-ended primary inductor converter (SEPIC) power factor correction (PFC) with full input voltage range zero-voltage-switching (ZVS) turn-ON for the application of step down ac–dc converter. The operation principle for the bridgeless Dual-SEPIC PFC and the theoretical analysis for the ZVS operation has been investigated. Furthermore, a new magnetic integration has been proposed to assemble all three inductors, including one input inductor and two output side inductors into one E-I-E core. The integrated inductor reduces the total ferrite volume and makes the converter more compact. The inductance design for ZVS SEPIC PFC and the magnetic reluctance modeling for the E-I-E core with the coupled inductor has been analyzed. The effective equivalent inductance of the input inductor can be implemented with a much less number of turns by a carefully designed coupling coefficient. Finally, a 300 W GaN-based MHz bridgeless dual-SEPIC PFC with the integrated inductors is developed and tested with full–range ZVS, 97% peak efficiency based on the ZVS extension strategy.**

***Index Terms*—Bridgeless sepic power factor correction (PFC), E-I-E core, integrated inductors, zero-voltage-switching (ZVS) turn-ON.**

I. Introduction

THE MAIN power supplies used in telecom, on-board chargers, servers, and industrial PSU systems need to convert the ac line power to a constant dc output voltage. Thus, rectifiers have been employed unavoidably. These systems usually range from a hundred watts to several kilowatts. The major problem for conventional rectifiers is severe harmonic pollution. Therefore, front-end power factor correction (PFC) converters are widely used to shape the input current of the power supply to meet the power factor (PF) standard and the current THD norms such as IEC 61000-3-2 [1]–[3].

As the most efficient and simple PFC circuit, the boost-type PFC is extensively adopted. Because of the intrinsic boost characteristic, the output voltage of the boost PFC must be higher than the peak of the ac line voltage, which is typically 400 V [4]–[8]. Thus, in some step-down applications, a second stage is required to convert the output voltage of the boost PFC to a specific voltage lower than the peak input ac voltage. The two-stage converter will degrade the system efficiency as well as the power density. Therefore, the single-ended primary inductor converter (SEPIC) PFC is prevailing in those applications. The output voltage of SEPIC PFC can be regulated either higher or lower than the ac input voltage. Thus, SEPIC converters are widely employed in LED lighting systems, wireless power transfer systems, standalone photovoltaic systems, and portable power applications [9], [10].

The conventional SEPIC PFC consists of a bridge rectifier followed by a dc–dc SEPIC converter, as shown in Fig. 1(a) [9]–[13]. The high conduction loss caused by the forward voltage drop of the diode bridge rectifier will degrade the overall system efficiency dramatically, and the heat generated by the bridge rectifier may need an extra heatsink. Hence, to increase the power supply efficiency, the bridgeless SEPIC PFC circuit topologies have been extensively researched [14]–[30]. Fig. 1(b) [19]–[21] and Fig. 1(c) [18], [25]–[27] are two typical types bridgeless SEPIC PFC topologies. Without the forward bridge rectifier, it allows the current to flow through a minimum number of semiconductor devices. Thus, the converter conduction losses can be significantly reduced. Type I bridgeless SEPIC PFC in Fig. 1(b) has two more diodes on the input side that will introduce more conduction loss. Type II bridgeless SEPIC PFC in Fig. 1(c) has two more passive components.

To reduce the volume of the passive component, increasing the switching frequency has been proved as an effective method [7]. The emerging of gallium nitride (GaN) devices, which have a low ON-resistance, fast switching speed, and zero reverse recovery loss, have pushed the switching frequencies to the megahertz range for power electronics equipment [39]. Thus, the size of the magnetic components has been dramatically reduced. Since the state-of-the-art SEPIC PFC prototypes mainly work under discontinuous conduction mode (DCM), the converters are operating in hard switching, which will still cause a substantial turn-ON power loss when the switching frequency increased. Hence, the switching frequency of the state-of-the-art SEPIC PFC ranges from tens to hundreds of kHz, it has still big challenge to push the switching frequency to megahertz.

To further increase the switching frequency, the switching loss must be dealt with. In particular, the turn-ON loss of GaN FET dominates the power loss and is the major limitation for

Manuscript received October 13, 2020; revised January 7, 2021 and February 24, 2021; accepted March 27, 2021. Date of publication April 5, 2021; date of current version June 30, 2021. Recommended for publication by Associate Editor F. J. Azcondo. *(Corresponding author: Ziwei Ouyang.)*

Yunfeng Liu, Yi Dou, Ziwei Ouyang, and Michael A. E. Andersen are with the DTU Elektro, Department of Electrical Engineering., Technical University of Denmark, 2800 Lyngby, Denmark (e-mail: yuliu@elektro.dtu.dk; yidou@elektro.dtu.dk; zo@elektro.dtu.dk; ma@elektro.dtu.dk).

Xiaosheng Huang is with the School of Information Science and Engineering, Fujian University of Technology, Fuzhou 350108, China (e-mail: hxs@fjut.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3070961.

Digital Object Identifier 10.1109/TPEL.2021.3070961

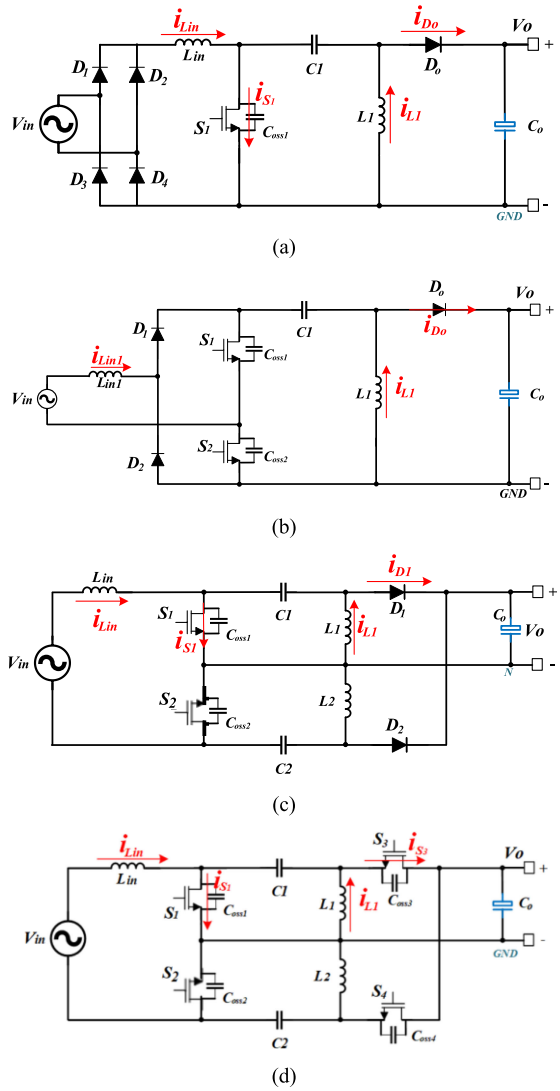


Fig. 1. (a) Conventional Sepic PFC with the diode bridge rectifier. (b) Type I bridgeless SEPIC PFC. (c) Type II bridgeless dual SEPIC PFC. (d) Modified bridgeless dual SEPIC PFC.

achieving high efficiency. Conventional SEPIC PFC with the output diode has low efficiency at high switching frequency since the zero-voltage-switching (ZVS) operation cannot be obtained for all switches. [9], [13]. Thus, the realization of ZVS for the main switch is a key point to design a high-frequency, high-efficiency SEPIC PFC rectifier.

Some researches have been done to implement ZVS for SEPIC PFC [10], [30], [31]. In [30], a soft-switching cell composed of an active switch, a resonant inductor, and a resonant capacitor was applied into the SEPIC PFC to obtain ZVS to promote the converter efficiency. The active clamped SEPIC PFC was studied in [10] and [31]. By adding extra clamping capacitance and MOSFET, partial ZVS can be achieved. However, All the existing studies cannot accomplish the fully ZVS operation without adding any auxiliary components. This article investigates the bridgeless dual SEPIC PFC with the full range ZVS for all switches, as shown in Fig. 1(d). By replacing the output diode with MOSFET, the negative current is provided for

TABLE I
COMPARISON OF THREE BRIDGELESS SEPIC TOPOLOGIES

Count	Type I Bridgeless SEPIC PFC	Type II Bridgeless SEPIC PFC	Modified SEPIC PFC
MOSFET	2	2	4
Diode	3	2	0
Inductor	2	3	3 → 1
Capacitor	1	2	2
Total	8	9	9 → 7
ZVS	Partial	Partial	Full range

main switches $S1$/$S2$ to discharge the output capacitors. So ZVS is guaranteed in the full range of the input voltage. Thus, without adding any extra components, it can maximize efficiency at a high switching frequency.

The comparison of the three bridgeless SEPIC PFC topologies is given in Table I. By integrating all the three discrete inductors of the proposed topology in one E-I-E magnetic core, it has seven components in total, which has the minimum components among the three topologies. In addition, there are no diodes in the line current path. For conventional two types bridgeless SEPIC PFC, the ZVS turn-ON cannot be fully achieved, which will limit the switching frequency as well as the efficiency.

The operation mode of the conventional PFC can be roughly classified into three categories depending on the waveform of the input inductor current, namely, the continuous conduction mode (CCM), the critical conduction mode (CRM), and the DCM [36]. In CRM mode, ZVS can be achieved with the correct digital control for the boost-type PFC [6]–[8], [38]–[40]. However, when the it comes to the SEPIC PFC, the operation mode cannot be classified with the same principle because SEPIC PFC consists of two inductors. In contrast, the operation mode is determined by the sum of two inductor current (i_{Lin}+i_{L1}), which is the current flows through the main switch S_1 when S_1 is ON. When S_1 is OFF, and S_3 is ON, (i_{Lin}+i_{L1}) is output current i_{S3} flow through the synchronous switch S_3. The input inductor current i_{Lin} commonly designs to work at CCM. The inductor current waveforms of SEPIC PFC for three operation modes are depicted in Fig. 2. If the main switch S_1 turns ON when i_{S3} is exactly decreased to zero, this is CRM mode, as shown in Fig. 2(b). If the main switch S_1 turns ON before the i_{S3} decease to zero, this is CCM. Otherwise, it is DCM.

The DCM has been widely used for SEPIC PFC because of the ZCS turn-OFF for the diode [8]–[29]. However, the ZVS cannot be achieved in the DCM mode. The modified bridgeless SEPIC PFC is working under CRM mode (also call boundary conduction mode, BCM) by adding extended conduction time for the synchronous MOSFET device. However, the input inductor still works under CCM with a small current ripple even the converter is working in the DCM or CRM mode, which may increase the system efficiency and minimize the volume of the EMI filter design.

To further make the converter more compact and reduce the cost, the integrated inductors have been investigated for the bridgeless dual-SEPIC PFC in this article. In the dc–dc SEPIC converter, the integrated inductor has been used [33],

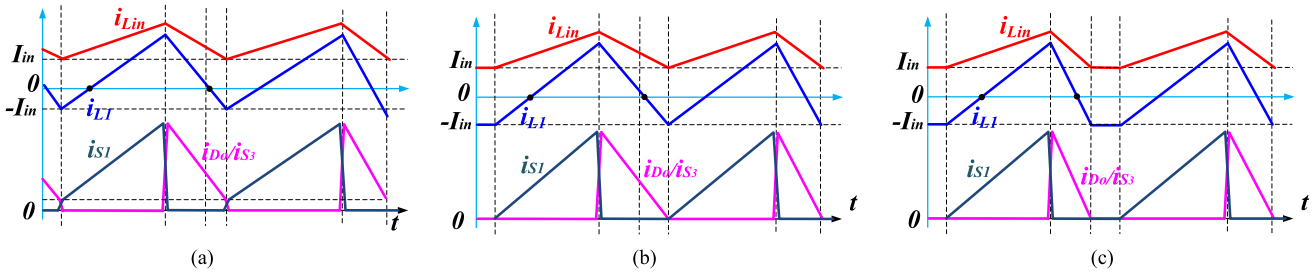


Fig. 2. Three operation modes for Sepic PFC. (a) Continuous conduction mode. (b) Critical conduction mode. (c) Discontinuous conduction mode.

[34]. By tightly coupled the input inductor and output inductor, the effective inductance can be double, and thus the current ripple can be reduced. For the ac–dc SEPIC PFC converter, this integrated inductor usually applied to dual-phase interleaved SEPIC PFC with a bridge rectifier [11], [12], the two input inductors, and two output inductors integrated separately with different magnetic cores. In [37], two integrated inductors have been conducted for the four inductors of the bridgeless SEPIC PFC. Still, two magnetics core needed. This article proposed the integrated inductors, making it possible to assemble all the three inductors of the bridgeless dual-SEPIC PFC into one E-I-E magnetic core. Based on the equivalent magnetic reluctance model, the theoretical analysis shows that the equivalent inductance can be enlarged several times to the self-inductance. The effective equivalent inductance of the input inductor can be implemented with fewer turns by an appropriately designed coupling coefficient.

In this article, the full-range ZVS for the bridgeless GaN-based MHz Dual-SEPIC PFC is achieved. The operation principle of the topology and the ZVS control is investigated. Then the integrated inductors are designed to assemble all the magnetic components into one E-I-E magnetic core. The inductance design for the bridgeless SEPIC PFC and the magnetic modeling for the E-I-E core with the coupled inductor has been analyzed.

This article is organized as follows. The principle of the operation stage and the theoretical analysis of ZVS implementation are presented in Section II. The inductance design and the coupling coefficient selection are presented in Section III. Hardware implementation is introduced in Section IV. Furthermore, a 300 W prototype of the SEPIC PFC is demonstrated, and the experimental results are shown in Section V. Finally, Section VI concludes this article.

II. Analysis of the Dual-SEPIC PFC Topology

A. Principle of Operation

The bridgeless dual-SEPIC PFC converter has two identical SEPIC converters, each operating in alternate half-line cycles, based on the polarity of the input ac voltage. It consists of three inductors: one input inductor $L_{\rm in}$ and two output inductors L_1, L_2. L_1 and $L_{\rm in}$ conduct at the positive half-line cycle, and L_2 and $L_{\rm in}$ conduct at the negative half-line cycle. S_2 is always ON, and S_4 is always OFF in the positive half-line cycle. In the negative half-line cycle, S_1 is always ON, and S_3 is always OFF. The analysis and discussions of the positive half-line cycle are

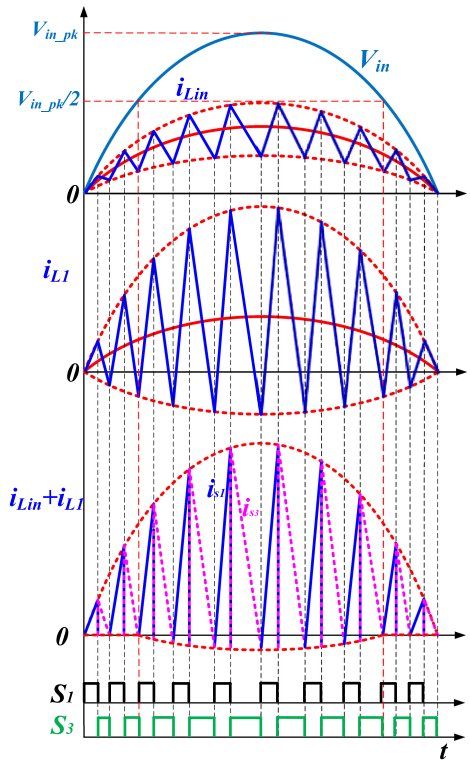


Fig. 3. Current waveform during the positive half-line cycle.

similar to the negative half-line cycle, so only the positive half-line cycle has been analyzed in this article. Assuming the input current $i_{\rm Lin(}{}_{t)}$ is in phase with the input voltage $V_{\rm in(}{}_{t)}$, defining the input ac line voltage and input current as

$$V_{\rm in}(t) = \sqrt{2} \cdot V_{\rm in\_rms} \cdot \sin(w_{\rm line} t) \tag{1}$$

$$i_{\rm Lin}(t) = \sqrt{2} \cdot I_{\rm in\_rms} \cdot \sin(w_{\rm line} t) \tag{2}$$

where $V_{\rm in\_rms}$ and $I_{\rm in\_rms}$ are the input rms voltage and rms current, respectively, $w_{\rm line} = 2\pi f_{\rm line}$, and $f_{\rm line}$ *is* the line frequency.

Fig. 3 shows the theoretical current waveforms in the positive half-line cycle. The input inductor $L_{\rm in}$ works under continuous conducting mode with a small current ripple. When S_1 is ON, and S_3 is OFF, the switch current, i_{S1} is the sum of $i_{L\rm in}$ and i_{L1}. When S_1 is OFF, and S_3 is ON, the output current i_{S3} is the sum of $i_{L\rm in}$ and i_{L1}. A typical waveform of the inductor current in each switching cycle is shown in Fig. 4. $D_{\rm ON}$ is the turn-ON duty cycle

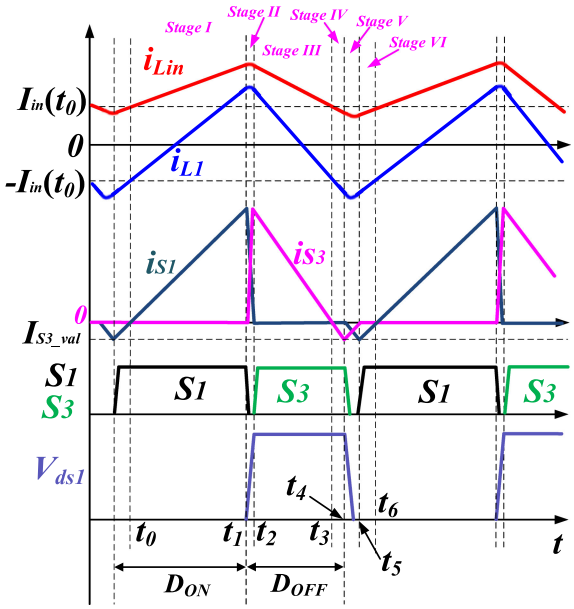


Fig. 4. Typical current waveform in each switching cycle.

for S_1. According to the operation principle, the instantaneous current of S_1 and S_3 in each switching cycle can be expressed as

$$i_{S1}(t)=\begin{cases} i_{Lin}(t)+i_{L1}(t), & 0<t<D_{ON}\cdot T_S \\ 0, & D_{ON}\cdot T_S<t<T_S \end{cases} \tag{3}$$

$$i_{S3}(t)=\begin{cases} 0, & 0<t<D_{ON}\cdot T_S \\ i_{Lin}(t)+i_{L1}(t) & D_{ON}\cdot T_S<t<T_S. \end{cases} \tag{4}$$

When S_1 turns OFF, and S_3 turns ON, the average current of S_3 in each switching cycle can be obtained as

$$i_{S3\_avg}(t)=\frac{i_{S3\_pk}\cdot T_{OFF}}{2\cdot T_S}=\frac{(i_{Lin\_pk}+i_{L1\_pk})\cdot T_{ON}\cdot V_{in}(t)}{2\cdot T_S\cdot V_O}. \tag{5}$$

Then the average of S_3 in the half-line cycle is derived

$$I_{S3\_avg}=\frac{1}{\pi}\cdot\int_0^{\pi} i_{S3\_avg}(t)\cdot dt=\frac{{V_{in\_rms}}^2\cdot(L_1+L_{in})\cdot {T_{ON}}^2}{2\cdot L_1\cdot L_{in}\cdot T_S\cdot V_O}. \tag{6}$$

Substituting $I_{S3\_avg}=P_O/V_O$, based on (1) to (6), T_{ON} and T_{OFF} yields

$$T_{ON}=\frac{V_O}{V_{in\_rms}}\cdot\sqrt{\frac{2\cdot L_1\cdot L_{in}\cdot T_S}{(L_1+L_{in})\cdot R_O}} \tag{7}$$

$$T_{OFF}=\frac{V_{in}(t)}{V_O}\cdot T_{ON}=\frac{V_{in}(t)}{V_{rms}}\cdot\sqrt{\frac{2\cdot L_1\cdot L_{in}\cdot T_S}{(L_1+L_{in})\cdot R_O}}. \tag{8}$$

Since $T_{ON}+T_{OFF}=T_S=1/f_S$ under CRM mode, hence the switching frequency is

$$f_S(t)=\frac{(L_{in}+L_1)\cdot {V_O}^2\cdot V_{in\_rms}^2}{2\cdot P_O\cdot L_{in}\cdot L_1\cdot(V_{in}(t)+V_O)^2}. \tag{9}$$

In Fig. 5, the red line shows the theoretical analysis variable switching frequency for the CRM mode of the bridgeless dual-SEPIC PFC during the half-line cycle. It can be seen that the

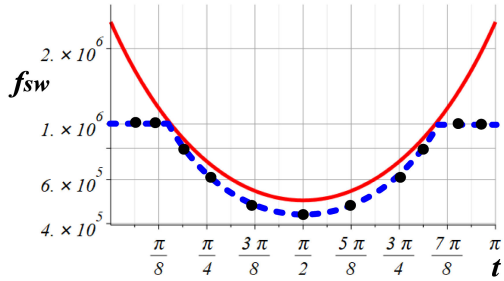


Fig. 5. Variable switching frequency during half-line cycle.

maximum switching frequency occurs in the crossing section of the line cycle, and the minimum switching frequency occurs in the middle of the half-line cycle when the input voltage reaches the peak value.

To achieve ZVS for the main switch S_1, the negative current of i_{S1} is needed to discharge the output capacitors of S_1. The conventional SEPIC PFC can not provide the discharged negative current. In order to obtain the negative current, the output diode D_o is replaced by the MOSFET S_3. Then S_3 turns OFF when i_{S3} declined to the required negative current rather than zero, i.e., $i_{S3}=i_{Lin}+i_{L1}\leq 0$; after S_3 is OFF, the negative current will transfer to i_{S1} to realize ZVS for S_1.

To limit the high switching frequency at the crossing section of the ac line cycle, the maximum switching frequency is limited to 1 MHz. Moreover, the practical switching frequency is shown as the blue dash line. The practical switching frequency is lower than the theoretical switching frequency because the extended conduction time is added to the synchronous switch S_3.

Assuming the intermediate capacitors C_1 and C_2 are large enough, the voltage ripples of C_1 and C_2 in each switching cycle are negligible. The voltage ripple of the ac input voltage $V_{in}(t)$ also can be seemed as a constant value since the switching frequency is much higher than the line frequency, i.e., $V_{C1}=V_{in}(t)=V_{in}(t_0)$. The value is selected at the beginning of each switching cycle. Based on the aforementioned assumptions, the circuit operation can be divided into six stages, separated by time instants (t_0, $t_1 \ldots t_6$), as marked in Fig. 4. The equivalent circuit of each stage is given in Fig. 6, and the corresponding analytical model is derived.

1) Stage I (t_0–t_1): As shown in Fig. 4, this stage starts when the switch current i_{S1} crosses zero. The equivalent circuit is shown in Fig. 6(a), L_{in} is charged by the input voltage, and L_1 is charged by the intermediate capacitor C_1. The voltages of both inductors L_1 and L_{in} equal to $V_{in}(t_0)$. Hence, the inductor current i_{Lin} and i_{L1} starts to rise linearly. Based on the operation mentioned above, the following equations can be obtained:

$$\begin{cases} i_{Lin}(t)=I_{in}(t_0)+\frac{V_{in}(t_0)}{L_{in}}(t-t_0) \\ i_{L1}(t)=-I_{in}(t_0)+\frac{V_{in}(t_0)}{L_1}(t-t_0) \\ i_{S1}(t_1)=i_{L1}(t)+i_{Lin}(t)=\frac{V_{in}(t_0)}{L_{eq}}(t-t_0)\geq 0 \\ i_{S3}(t)=0 \end{cases} \tag{10}$$

where $I_{in}(t_0)$ is the average input current, L_{eq} is the equivalent inductor $L_{eq}=L_1\cdot L_{in}/(L_1+L_{in})$.

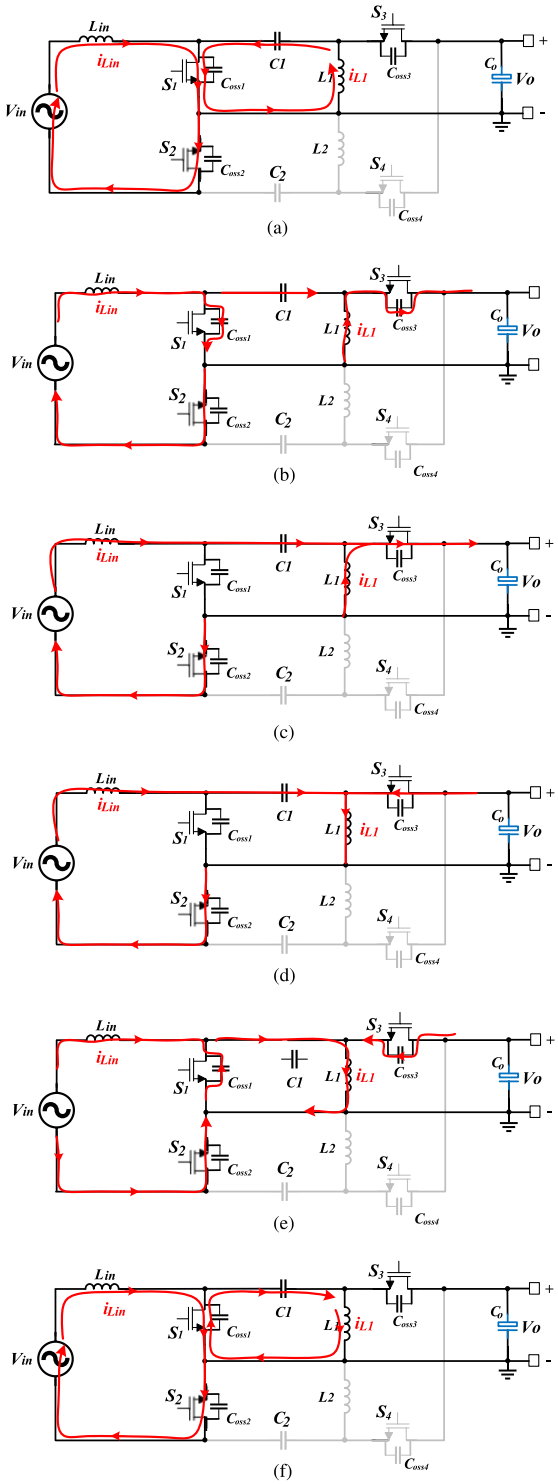


Fig. 6. Six operation stages for the modified SEPIC PFC. (a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV. (e) Stage V. (f) Stage VI.

2) Stage II (t1–t2): Stage II starts at t_1 when S_1 is OFF, as shown in Fig. 6(b), S_3 is also in the OFF state and ready to turn ON. The two parallel GaNFETs output capacitors $C_{\mathrm{oss}1}$ and $C_{\mathrm{oss}\,3}$, begin to resonate with the two parallel inductors L_{in} and L_1. During this resonant period, $C_{\mathrm{oss}1}$ is charged while $C_{\mathrm{oss}\,3}$ is discharged simultaneously. This stage ends when the voltage of $C_{\mathrm{oss}1}$ is charged from 0 to $(V_{\mathrm{in}}+V_o)$, and the voltage of $C_{\mathrm{oss}\,3}$ is released from $(V_{\mathrm{in}}+V_o)$ to 0. In this short resonant transition period, the currents of i_{Lin} and i_{L1} can be seemed as constant.

3) Stage III (t2–t3): This stage begins by turning S_3 ON at t_2. Since the $C_{\mathrm{oss}\,3}$ of S_3 is already discharged to zero, thus ZVS of S_3 is realized. The input inductor current i_{Lin} and the output inductor current i_{L1} flow through S_3 to the load, and both inductor voltages are $-V_o$. This stage ends when the current of i_{S3} drops to zero at t_3. The equations of the currents can be obtained

$$\begin{cases} i_{\mathrm{Lin}}(t) = i_{\mathrm{Lin}}(t_2) - \frac{V_o}{L_{\mathrm{in}}}(t-t_2) \\ i_{L1}(t) = i_{L1}(t_2) - \frac{V_o}{L_1}(t-t_2) \\ i_{S1}(t) = 0 \\ i_{S3}(t) = i_{L1}(t_2) + i_{\mathrm{Lin}}(t_2) - \frac{V_o(t_0)}{L_{\mathrm{eq}}}(t-t_2) > 0. \end{cases} \tag{11}$$

4) Stage IV (t3–t4): For the conventional SEPIC PFC shown in Fig. 1(a)–(c), the output diode Do turns OFF automatically when the diode current i_{Do} declines to zero. However, the main switch S_3 of the modified dual-SEPIC PFC remains ON after the switch current i_{S3} reaches zero. i_{S3} continues to decrease by adding an extended conduction time T_{ex} as shown in Fig. 4 from t_3 to t_4, here $T_{\mathrm{ex}} = t_4 - t_3$. Thus, after S_3 is OFF, the negative current is transferred to S_1. Hence, the negative current is provided to discharge $C_{\mathrm{oss}1}$ to achieve ZVS for S_1. As shown in Fig. 6(d), the equivalent circuit is the same as stage III, except for the polarity of current i_{S3}. This stage ends when i_{S3} drops to the required negative current value I_{S3_val} for ZVS realization

$$i_{S3}(t) = i_{L1}(t_2) + i_{\mathrm{Lin}}(t_2) - \frac{V_o(t_0)}{L_{\mathrm{eq}}}(t-t_2) < 0. \tag{12}$$

Thus, I_{S3_val} can be expressed as

$$I_{S3\_\mathrm{val}} = -\frac{V_o(t_0)}{L_{\mathrm{eq}}} T_{\mathrm{ex}} < 0. \tag{13}$$

5) Stage V (t4–t5): This stage is also a resonated stage, which is similar to stage II. It starts when S_3 is OFF at t_4. Then the negative current in S_3 is transferred to S_1. The two parallel GaNFETs output capacitors $C_{\mathrm{oss}1}$ and $C_{\mathrm{oss}\,3}$ start to resonate with the two parallel inductors. During this resonant period, the voltage of $C_{\mathrm{oss}1}$ is discharging from $(V_{\mathrm{in}}+V_o)$ to 0, and the voltage of the $C_{\mathrm{oss}3}$ is discharged from 0 to $(V_{\mathrm{in}}+V_o)$, as shown in Fig. 6(e). This stage ends when S_1 turns ON. Here assuming that $C_{\mathrm{oss}1} = C_{\mathrm{oss}3} = C_{\mathrm{oss}}$, the input voltage is considered as constant value as $V_{\mathrm{in}} = V_{\mathrm{in}}(t_0)$. The voltages of $C_{\mathrm{oss}1}$ and $C_{\mathrm{oss}3}$ are $V_{\mathrm{ds}1}(t)$ and $V_{\mathrm{ds}3}(t)$. The inductor current i_{S3} and the voltages $V_{\mathrm{ds}1}(t)$, $V_{\mathrm{ds}3}(t)$ can be expressed by

$$\begin{cases} i_{S3}(t) = I_{S3} \cdot \cos(w_0 t) - \frac{V_o}{Z_n}\sin(w_0 t) \\ V_{\mathrm{ds}1}(t) = V_{\mathrm{in}} + V_o \cdot \cos(w_0 t) + I_{S3} \cdot Z_n \sin(w_0 t) \\ V_{\mathrm{ds}2}(t) = V_o - V_o \cdot \cos(w_0 t) - I_{S3} \cdot Z_n \sin(w_0 t) \\ w_o = 1/\sqrt{L_{\mathrm{eq}} C_{\mathrm{eq}}},\ Z_n = \sqrt{L_{\mathrm{eq}}/C_{\mathrm{eq}}},\ C_{\mathrm{eq}} = C_{\mathrm{oss}1} + C_{\mathrm{oss}3} \end{cases} \tag{14}$$

where Z_n is the characteristic impedance in the resonant period, C_{eq} is the equivalent capacitor, and w_o is the resonant angular frequency. $I_{S3} = I_{L1} + I_{\mathrm{Lin}}$, where I_{Lin} and I_{L1} are the inductor current value at the beginning of the resonant stage. Based on

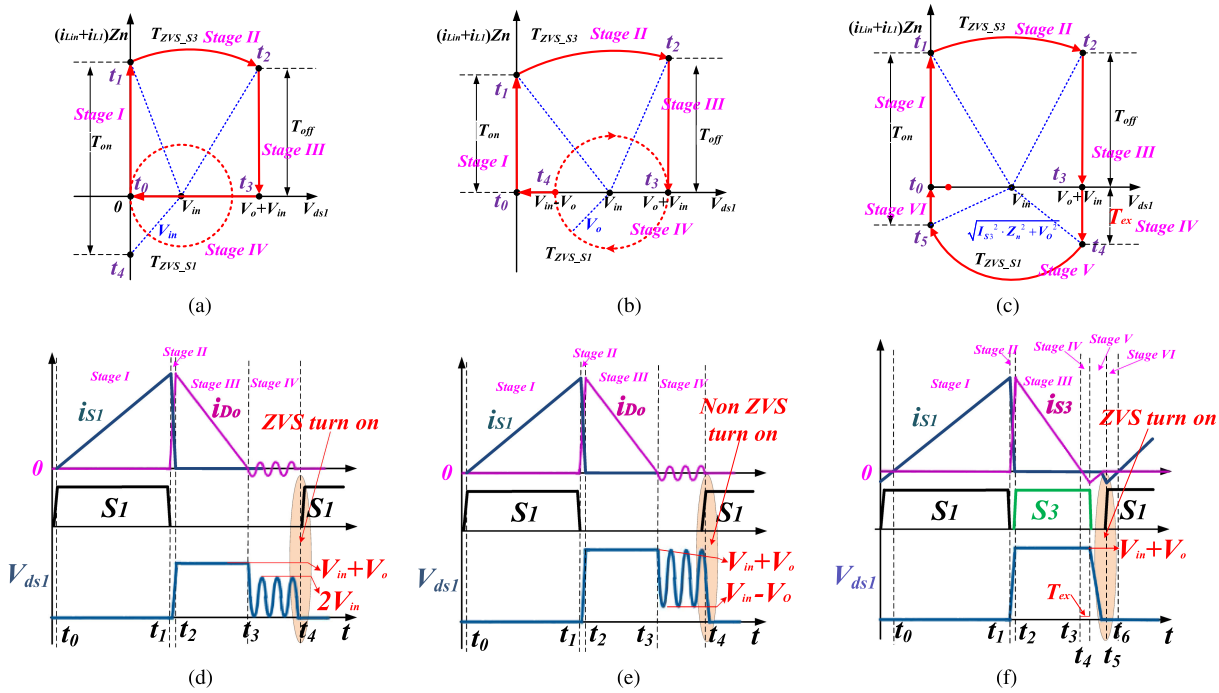


Fig. 7. (a). State plane trajectory for conventional SEPIC PFC when $V_{\rm in} \le 0.5Vo$. (b). State plane trajectory for conventional SEPIC PFC when $V_{\rm in} \ge 0.5Vo$. (c). State plane trajectory for the modified SEPIC PFC. (d). Operation waveforms for conventional SEPIC PFC when $V_{\rm in} \le 0.5Vo$. (e). Operation waveforms for conventional SEPIC PFC when $V_{\rm in} \ge 0.5Vo$. (f). Operation waveforms for the modified SEPIC PFC.

(14), then the following equation can be obtained

$$Z_n{}^2 \cdot i_{S3}(t)^2 + (V_{\rm ds1}(t) - V_{\rm in})^2 = I_{S3}{}^2 \cdot Z_n{}^2 + V_o{}^2. \quad (15)$$

It shows that the trajectory of the drain-source voltage $V_{\rm ds1}$ at this resonant stage is a circle, with the center at (0, $V_{\rm in}$), and the radius is $\sqrt{I_{S3}{}^2 \cdot Z_n{}^2 + V_o{}^2}$, as shown in Fig. 7(c). For the conventional DCM SEPIC PFC with the diode, the $I_{\rm D0} = I_{L\rm in} + I_{L1} = 0$. Therefore, the radius is *Vo* when the input voltage exceeds the output voltage ($V_{\rm in} > V_O$). With a similar analysis, it also can be obtained that the radius is $V_{\rm in}$ when $V_{\rm in} < V_O$ for the conventional SEPIC PFC. The state plane trajectories for the conventional DCM SEPIC PFC are also shown in Fig. 7(a) and (b), respectively.

6) Stage VI (t5–t6): This stage starts by turning S_1 ON at t_5. Since the voltage of output capacitor $C_{\rm oss1}$ is already discharged to 0 in stage V, hence, the ZVS operation of S_1 is obtained. Both the two inductor currents flow through S_1, and the voltages across the two inductors are $V_{\rm in}$. This stage ends when the current of i_{S1} rises to zero. Then another switching cycle starts as stage I.

B. Conditions for ZVS Implementation

Compared with the modified dual-SEPIC PFC, the conventional DCM SEPIC PFC with the diode rectifier only has four stages because no negative output current existed. When the diode current $i_{\rm Do}$ is decreased to zero, as shown in Fig. 7(d) ($V_{\rm in} < V_O$) and Fig. 7(e) ($V_{\rm in} > V_O$), the two parallel inductors start to resonate with the two parallel capacitors, including the output capacitor of S_1 and the parasitic capacitors of the diode D_O. The valley switching can be applied with the correct turn-ON instant time control. Thus, the minimum value of $V_{\rm ds1}$ is achieved at the valley switching is ($V_{\rm in} - V_O$). Hence the ZVS for the conventional SEPIC PFC can only be achieved when the input voltage $V_{\rm in}$ is lower than the output voltage V_o as shown in Fig. 7(d). The state plane trajectories for conventional DCM SEPIC PFC shown in Fig. 7(a) ($V_{\rm in} < V_O$) and (b) ($V_{\rm in} > V_O$) also indicate that the ZVS operation can only be achieved when $V_{\rm in} < V_O$. As shown in Fig. 7(e), when the input voltage exceeds the output voltage, the minimum value of drain-source voltage $V_{\rm ds1}$ can only resonate to a valley point ($V_{\rm in} - V_O$). Therefore, at least $0.5C_{\rm eq}(V_{\rm in} - V_O)^2$ power loss occurs when S_1 starts turning ON.

In order to achieve the fully ZVS in the whole line cycle, the diode D_O is replaced by the high-speed GaN device S_3, as shown in Fig. 1(d), and then, the ZVS extension strategy explained in [6], [8], and [39]–[41] is used. Then, the negative current can be provided to guarantee the ZVS for the main switch S_1. Thus, instead of automatically turning OFF the diode D_O in the DCM mode when the diode current decreases to zero, a short extended conduction time $T_{\rm ex}$ is added on purpose for S_3 shown in Fig. 7(f) and Stage IV (t3–t4). Then the negative current flows through S_1 is provided to discharge the output capacitor $C_{\rm oss1}$ to help to achieve ZVS for the main switch S_1. It also can be seen from the state plane trajectory in Fig. 7(c), the negative current i_{S3} enlarges the radius from V_o to $\sqrt{I_{S3}{}^2 \cdot Z_n{}^2 + V_o{}^2}$. Hence the voltage $V_{\rm ds1}$ can drop to zero. Based on the state plane trajectory as shown in Fig. 7(c) and (14), the minimum required negative current $i_{S3\_\rm val}$, and the extended conduction time $T_{\rm ex}$ to achieve

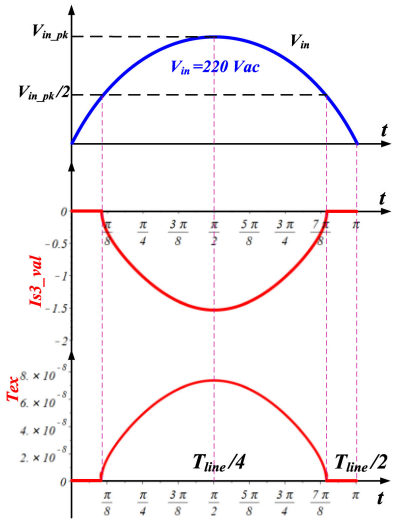


Fig. 8. Required negative current and required extended conduction time for S_3 in the positive half-line cycle.

TABLE II
SPECIFICATION OF BRIDGELESS DUAL-SEPIC PFC

Circuit parameters	Value
Input voltage	220 Vac
Nominal Output voltage	100 Vdc
Input current ripple	20%*Iin
Output voltage ripple	10%*Vo
Power rating	300 W

ZVS operation for S_1 in the half-line cycle is calculated as

$$i_{S3\_\mathrm{val}}(t) = -\sqrt{\frac{V_{\mathrm{in}}(t)^2 - {V_O}^2}{{Z_n}^2}} \tag{16}$$

$$T_{\mathrm{ex}}(t) = \frac{|i_{S3\_\mathrm{val}}(t)| \cdot L_{\mathrm{eq}}}{V_O}. \tag{17}$$

Finally, the theoretical analysis for the required negative current i_{S3_val} and the required extended conduction time T_{ex} are plotted in Fig. 8. Here the input voltage V_{in} is 220 Vac, and the output voltage is 100 Vdc.

III. INTEGRATED INDUCTORS DESIGN

The specification of the bridgeless dual-SEPIC PFC is given in the Table II.

A. Inductance Design for the SEPIC PFC

There are three constraints for the inductance design of the integrated inductors.

1) The ZVS turn-ON in the full range of the input voltage.
2) Input inductor current ripple limitation.
3) The output inductor current ripple limitation.

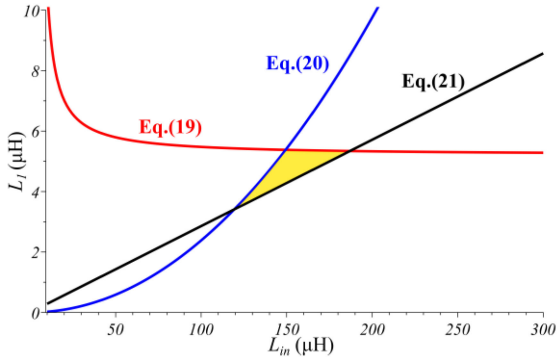


Fig. 9. Inductance design be three constraints.

For the bridgeless dual-SEPIC PFC converter, based on (7) and (8), the duty cycle can be derived

$$\begin{cases} D_{\mathrm{ON}} = \frac{V_o}{V_{\mathrm{in\_rms}}}\sqrt{\frac{2L_1 \cdot L_{\mathrm{in}}}{(L_1+L_{\mathrm{in}})R_0T_s}} \\ D_{\mathrm{OFF}} = \sqrt{\frac{2L_1 \cdot L_{\mathrm{in}}}{(L_1+L_{\mathrm{in}})R_0T_s}}. \end{cases} \tag{18}$$

As mentioned before, D_{ON} and D_{OFF} are the turn-ON duty cycle and turn-OFF duty cycle for the main switches S_1 and S_2. To make sure the output current i_{S3} can drop below zero, the sum of D_{ON} and D_{OFF} should always small than 1. Thus, the first constraint can be obtained

$$D_{\mathrm{ON}} + D_{\mathrm{OFF}} \le 1 \Rightarrow \frac{2L_1 \cdot L_{\mathrm{in}}}{(L_1 + L_{\mathrm{in}})R_0T_s} \le \frac{\left(\sqrt{2}V_{\mathrm{in\_rms}}\right)^2}{\left(\sqrt{2}V_{\mathrm{in\_rms}} + V_o\right)^2}. \tag{19}$$

The relationship between L_{in} and L_1 for the inequality is shown in Fig. 9 as the red line. It can be seen that if the equivalent inductance L_{in} becomes large to obtain a smaller input current ripple, then the equivalent inductance of L_1 should be limited to a smaller value. This limitation comes from the output current $i_{S3} = i_{L\mathrm{in}} + i_{L1} \le 0$ when S_3 turns OFF, the more negative current is needed for i_{L3} since the input current ripple becomes small.

Denoting K_1 is the peak input current ripple $\Delta i_{L\mathrm{in}\_pk}$ over the peak input current $I_{\mathrm{in\_pek}}$, based on (7), since $\Delta i_{L\mathrm{in}\_pk} = V_{\mathrm{in}}(t)T_{\mathrm{on}}/L_{\mathrm{in}}$, then K_1 can be deduced by the following equation:

$$K_1 = \frac{\Delta i_{L\mathrm{in\_pek}}}{\sqrt{2} \cdot I_{\mathrm{in\_rms}}} = \frac{1}{L_{\mathrm{in}}}\sqrt{\frac{2L_1 \cdot L_{\mathrm{in}} \cdot T_s}{(L_1 + L_{\mathrm{in}})P_O}}\sqrt{2}V_{\mathrm{in\_rms}} \le 0.2 \tag{20}$$

where K_1 is determined by the output power, the inductance values, and the switching frequency. According to Table II, here, $K_1 \le 0.2$ is selected, and this inequality is shown in Fig. 9 as the blue line.

As mention before, the voltages crossed the input inductor L_{in} and output side inductor L_1 are always the same in each operation stage. Hence, the ratio of the output side inductor ripple Δi_{L1} and the input inductor current ripple $\Delta i_{L\mathrm{in}}$ equals to the ratio of the inductance L_{in} to L_1 shown in (21). To limit the ripple current of L_1, the inductance ratio K_2 between L_{in} and L_1 should also keep as low as possible. K_2 is selected smaller than 35, and this

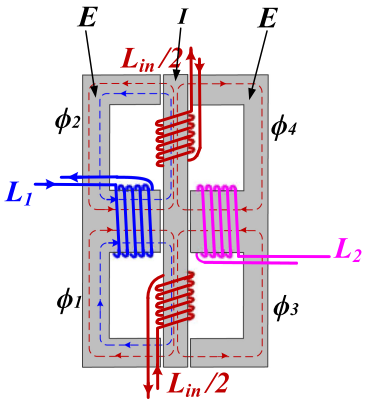


Fig. 10. Proposed E-I-E core structure for the coupled inductor.

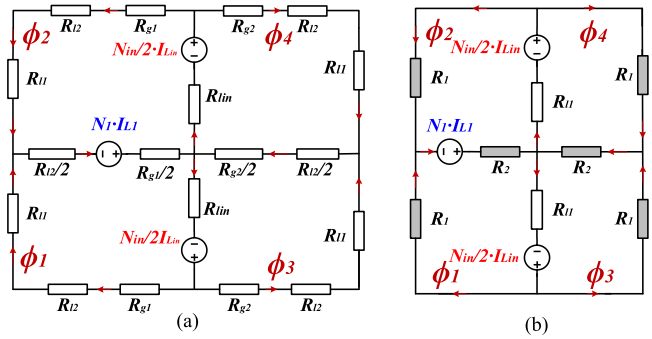


Fig. 11. Magnetic reluctance model of the E-I-E core. (a) Original model. (b) Simplified model.

inequality is shown in Fig. 9 as the black line

$$\frac{\Delta i_{L1}}{\Delta i_{L\text{in}}} = \frac{L_{\text{in}}}{L_1} \le K_2 = 35. \tag{21}$$

Based on the three constraints aforementioned in (19)–(21), the available values for L_1 and L_{in} can be selected from Fig. 9 in the yellow area as

$$\begin{cases} L_{\text{in\_eq}} = 120 \sim 190\mu\text{H} \\ L_{1\_\text{eq}} = 4 \sim 6\mu\text{H} \\ L_{2\_\text{eq}} = 4 \sim 6\mu\text{H}. \end{cases} \tag{22}$$

B. E-I-E Core With a Specified Coupling Coefficient

For general three coupled inductors, the relationships among the voltage of each winding, the self-inductance, and the mutual inductance are given as

$$\begin{bmatrix} V_{L\text{in}} \\ V_{L1} \\ V_{L2} \end{bmatrix} = \begin{bmatrix} L_{\text{in\_self}}, \pm M_{\text{in\_1}}, \pm M_{\text{in\_2}} \\ L_{1\_\text{self}}, \pm M_{1\_\text{in}}, \pm M_{1\_2} \\ L_{2\_\text{self}}, \pm M_{2\_\text{in}}, \pm M_{2\_1} \end{bmatrix} \begin{bmatrix} \frac{di_{L\text{in}}}{dt} \\ \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \end{bmatrix}. \tag{23}$$

The inductors can be coupled directly or inversely. The sign before M is "+" or "−" depended on the inductors are coupled directly or inversely. $V_{L\text{in}}$, $V_{L1,}$ and V_{L2} are the voltages across the three inductors, respectively. $L_{\text{in\_self}}$, $L_{1\_\text{self},}$ and L_{2_self} are the self-inductance value of the windings. M is the mutual inductance between inductors, where $M_{1\_\text{in}} = M_{\text{in\_1}}$, $M_{2\_\text{in}} = M_{\text{in\_2}}$, $M_{1\_2} = M_{2\_1}$.

For the three inductors in the proposed topology, the output inductors L_1 only works in the positive half-line cycle, and L_2 only works in the negative half-line cycle. Therefore, L_1 and L_2 are directly coupled with the input inductor L_{in} separately. L_1 and L_2 need to be always decoupled from each other. In this article, the symmetric E-I-E core geometry is selected. The magnetics structure is shown in Fig. 10. The output side inductors L_1 and L_2 are wound on the center legs of the E-cores individually. The input inductor L_{in} is wound in the middle I-core with two identical parts in series, where each part has the same number of turns. Due to the low reluctance path provided by the middle I-core, the flux induced by L_1 and L_2 will return from the middle I-core rather than the E-core. Thus, L_1 can be decoupled with L_2 by the middle I-core.

Since L_1 is always decoupled with L_2, M_{1_2} is equal to 0. Taking the positive half-line cycle as an example, the identical voltages are applied to L_{in} and L_1 at all times throughout the switching period, which means $V_{L\text{in}}$ is equal to V_{L1}. Since L_2 does not work at the positive line cycle, the inductor voltage is zero, $V_{L2} = V_{C2} \approx 0$. Then, (23) can be rewritten

$$\begin{cases} V_{L\text{in}} = L_{\text{in\_self}} \frac{di_{L\text{in}}}{dt} + M_{\text{in\_1}} \frac{di_{L1}}{dt} - M_{\text{in\_2}} \frac{di_{L2}}{dt} \\ V_{L1} = L_{1\_\text{self}} \frac{di_{L1}}{dt} + M_{1\_\text{in}} \frac{di_{L\text{in}}}{dt} \\ 0 = L_{2\_\text{self}} \frac{di_{L2}}{dt} - M_{2\_\text{in}} \frac{di_{L\text{in}}}{dt}. \end{cases} \tag{24}$$

Assuming $M_{\text{in\_1}} = M_{\text{in\_2}} = M$, $L_{1\_\text{self}} = L_{2\_\text{self}}$, the equivalent inductance of each inductor can be obtained as

$$\begin{cases} L_{\text{in\_eq}} = \frac{L_{1\_\text{self}} L_{\text{in\_self}} - 2M^2}{L_{1\_\text{self}} - M} = \frac{(1-2k_c^2) L_{\text{in\_self}}}{1 - k_c \sqrt{L_{\text{in\_self}} / L_{1\_\text{self}}}} \\ L_{1\_\text{eq}} = \frac{L_{1\_\text{self}} L_{\text{in\_self}} - M^2}{L_{\text{in\_self}} - M} = \frac{(1-k_c^2) L_{1\_\text{self}} L_{\text{in\_self}}}{L_{\text{in}} - k_c \sqrt{L_{1\_\text{self}} L_{\text{in\_self}}}} \\ L_{2\_\text{eq}} = \frac{L_{2\_\text{self}} L_{\text{in\_self}} - M^2}{L_{\text{in\_self}} - M} = \frac{(1-k_c^2) L_{2\_\text{self}} L_{\text{in\_self}}}{L_{\text{in\_self}} - k_c \sqrt{L_{2\_\text{self}} L_{\text{in\_self}}}} \\ M = k_c \sqrt{L_{\text{in\_self}} L_{1\_\text{self}}}. \end{cases} \tag{25}$$

Based on (25), it shows that the equivalent inductance of the input inductor $L_{\text{in\_eq}}$ can be enlarged several times over the self-inductance $L_{\text{in\_self}}$ when the self-inductance L_{1_self} and L_{2_self} are very close to the mutual inductance M. The required equivalent inductance of the input inductor $L_{\text{in\_eq}}$ can be achieved by much smaller self-inductance $L_{\text{in\_self}}$ by appropriate coupling coefficient (k_c).

The magnetic flux flows in the proposed E-I-E core in the positive half-line cycle are shown in Fig. 11. Here i_{L2} is almost zero, only L_{in} and L_1 coupled with each other. N_{in}, $N_{1,}$and N_2 are the number of turns for L_{in}, $L_{1,}$ and $L_{2,}$ respectively. Φ_1, Φ_2, $\Phi_{3,}$ and Φ_4 are the flux flow in four outer legs of the E-I-E core geometry, respectively. Fig. 11(a) shows an equivalent magnetic reluctance model of the proposed E-I-E core module. Where R_{l1} and R_{l2} are the reluctance of E-core, R_{lin} is the reluctance of I-core, here $R_{l1} = R_{\text{lin}}$. R_{g1} and R_{g2} represent the reluctance of the air gap between the I-core, and two E-cores, The air-gap of g_1 is also identical to g_2, i.e., $R_g = R_{g1} = R_{g2}$. By defining $R_1 = R_{l1} + R_{l2} + R_g$, $R_2 = (R_{l2} + R_g)/2$, the magnetic reluctance model can be simplified to Fig. 11(b).

Based on the equivalent magnetic reluctance model, four reluctance equations in each subloop can be obtained

$$\begin{cases} \frac{N_{\rm in}i_{L\rm in}}{2} + N_1 i_{L1} = \Phi_1 \cdot R_1 + (\Phi_1 + \Phi_2) \cdot R_2 \\ \quad + (\Phi_1 + \Phi_3) R_{l1} \\ \frac{N_{\rm in}i_{L\rm in}}{2} + N_2 i_{L2} = \Phi_2 \cdot R_1 + (\Phi_1 + \Phi_2) \cdot R_2 \\ \quad + (\Phi_2 + \Phi_4) R_{l1} \\ \frac{N_{\rm in}i_{L\rm in}}{2} = \Phi_3 \cdot R_1 + (\Phi_3 + \Phi_4) \cdot R_2 + (\Phi_1 + \Phi_3) R_{l1} \\ \frac{N_{\rm in}i_{L\rm in}}{2} = \Phi_4 \cdot R_1 + (\Phi_3 + \Phi_4) \cdot R_2 + (\Phi_2 + \Phi_4) R_{l1}. \end{cases} \tag{26}$$

Since the flux Φ_1 is identical to Φ_2, and Φ_3 is identical to Φ_4 because of the symmetrical core structure and windings, then (26) can be simplified into two equations

$$\begin{cases} \frac{N_{\rm in}i_{L\rm in}}{2} + N_1 i_{L1} = \Phi_1 \cdot R_1 + \Phi_1 \cdot 2 \cdot R_2 + (\Phi_1 + \Phi_3) R_{l1} \\ \frac{N_{\rm in}i_{L\rm in}}{2} = \Phi_3 \cdot R_1 + \Phi_3 \cdot 2 \cdot R_2 + (\Phi_1 + \Phi_3) R_{l1}. \end{cases} \tag{27}$$

Solving (27), then the flux in each loop is obtained

$$\begin{cases} \Phi_1 = \Phi_2 = \frac{(R_1+2R_2)N_{\rm in}i_{L\rm in}+4R_1N_1i_{L1}}{2(R_1+2R_2)(2R_1+R_{l1})} \\ \Phi_3 = \Phi_4 = \frac{(R_1+2R_2)N_{\rm in}i_{L\rm in}-2R_{l1}N_1i_{L1}}{2(R_1+2R_2)(2R_1+R_{l1})}. \end{cases} \tag{28}$$

The total flux flows through the winding L_1 is $\Phi_1+\Phi_2 = 2\Phi_1$, and the total flux flows through L_{in} is $\Phi_1+\Phi_2+\Phi_3+\Phi_4 = 2(\Phi_1+\Phi_3)$. Taking the partial derivative of the total flux in each winding

$$\begin{cases} V_{L1} = N_1 \cdot \frac{d(\Phi_1+\Phi_2)}{dt} = \frac{4N_1^2 \cdot R_1}{\Delta} \cdot \frac{di_{L1}}{dt} + \frac{N_{\rm in} \cdot N_1}{2R_1+R_{l1}} \cdot \frac{di_{L\rm in}}{dt} \\ V_{L\rm in} = N_{\rm in} \cdot \frac{d(\Phi_1+\Phi_3)}{dt} = \frac{N_{\rm in}^2}{2R_1+R_{l1}} \cdot \frac{di_{L\rm in}}{dt} \\ \qquad + \frac{N_{\rm in} \cdot N_1}{2R_1+R_{l1}} \cdot \frac{di_{L1}}{dt}. \end{cases} \tag{29}$$

Equation (29) can be rewritten

$$\begin{aligned} \begin{bmatrix} V_{L1} \\ V_{L\rm in} \end{bmatrix} &= \begin{bmatrix} \frac{4N_1^2 \cdot R_1}{\Delta} & \frac{N_{\rm in} \cdot N_1}{2R_1+R_{l1}} \\ \frac{N_{\rm in} \cdot N_1}{2R_1+R_{l1}} & \frac{N_{\rm in}^2}{2R_1+R_{l1}} \end{bmatrix} \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L\rm in}}{dt} \end{bmatrix} \\ &= \begin{bmatrix} L_{1\_\rm self} M \\ M L_{\rm in\_self} \end{bmatrix} \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L\rm in}}{dt} \end{bmatrix}. \end{aligned} \tag{30}$$

Here, $\triangle = (2R_1 + R_{l1})(R_1 + 2R_2)$, then self-inductances and mutual inductances can be obtained

$$\begin{cases} L_{1\_\rm self} = \frac{4N_1^2 \cdot R_1}{(2R_1+R_{l1})(R_1+2R_2)} \\ L_{\rm in\_self} = \frac{N_{\rm in}^2}{2R_1+R_{l1}} \\ M = \frac{N_{\rm in} \cdot N_1}{2R_1+R_{l1}}. \end{cases} \tag{31}$$

Finally, the theoretical coupling coefficient can be derived

$$k_C = \frac{M}{\sqrt{L_{1\_\rm self} \cdot L_{\rm in\_self}}} = \sqrt{\frac{R_1 + 2R_2}{4R_1}} \approx \sqrt{\frac{1}{2}} = 0.707. \tag{32}$$

Here, it can be seen that the coupling coefficient is related to the core structure, the air-gap, and the material of the magnetic core. R_g is much bigger than R_{l1} and R_{l2} due to the air-gaps between the E-core and I-core. Hence, the theoretically calculated value of the coupling coefficient is around 0.7. It has also been verified in the 2-D finite-element analysis (FEA) simulation.

TABLE III
PARAMETERS OF E-I-E CORE

Circuit parameters	Value
Ferrite core material	3F36 (300 kHz to 1 MHz)
Initial permeability (μ_0)	1600
E-core size	E43/10/28
I-core size	PLT43/28/4.1

IV. HARDWARE IMPLEMENTATION

A 300-W GaN-based MHz bridgeless dual-SEPIC PFC prototype is built to verify the ZVS control method with the integrated E-I-E inductors. The integrated inductor design for the dual-SEPIC PFC, and control scheme are described as follows.

A. Integrated Inductor Design

Ferrite material with 3F36 is selected since it is suitable for high frequency from 300 kHz to 1 MHz. The detailed parameters of the integrated E-I-E core are given in Table III.

Defining $K_{L\rm in}$ and K_{L1} are the ratios of the equivalent inductance over the self-inductance for the input inductor $L_{\rm in}$ and the output side inductor L_1, respectively. According to (25) and (31), $K_{L\rm in}$ and K_{L1} can be obtained as

$$K_{L1} = \frac{L_{1\_\rm eq}}{L_{1\_\rm self}} = \frac{1 - k_c^2}{1 - k_c\sqrt{L_{1\_\rm self}/L_{\rm in\_self}}} = \frac{1 - k_c^2}{1 - \sqrt{2}k_c\frac{N_1}{N_{\rm in}}} \tag{33}$$

$$K_{L\rm in} = \frac{L_{\rm in\_eq}}{L_{\rm in\_self}} = \frac{1 - 2k_c^2}{1 - k_c\sqrt{L_{\rm in\_self}/L_{1\_\rm self}}} = \frac{1 - 2k_c^2}{1 - \frac{1}{\sqrt{2}}k_c\frac{N_{\rm in}}{N_1}}. \tag{34}$$

It can be seen that $K_{L\rm in}$ and K_{L1} are determined by the number of winding turns and coupling coefficient k_c. According to the equivalent inductance requirement based on (22) and the flux saturation limitation, here, $N_{\rm in} = 12$, $N_1 = N_2 = 5$ are selected. The relationship between $K_{L\rm in}$ and K_{L1} with the coupling coefficient k_c is shown in Fig. 12. Fig. 12(a) shows that the equivalent inductance $L_{\rm in\_eq}$ can be enlarged several times to self-inductance L_{in_self}. On the other side, the ratio K_{L1} for L_1 is around 1, as shown in Fig. 12(b), meaning that the self-inductance $L_{1\_\rm self}$ is almost equal to the inductance $L_{1\_\rm eq}$.

As shown in Fig. 12(a), when the coupling coefficient k_c is large than 0.59, the value of equivalent inductance $L_{\rm in\_eq}$ is negative, which means the rate of the flux change and the rate of the current change, are negative as shown in Fig. 13 in the dashed line. To obtain the same negative current $I_{S3\_\rm val}$ when S_3 is OFF to achieve ZVS for S_1, more current rippled will be introduced for L_1 when $k_c > 0.59$. Therefore, to minimize the inductor ripple, the coupling coefficient should be designed to less than 0.59.

Since the self-inductance $L_{\rm in\_self}$ is around 15 μH and $L_{1\_\rm self}$ is around 5 μH, to satisfy the equivalent inductance requirement (22), the ratio $K_{L\rm in} = L_{\rm in\_eq}$ /$L_{\rm in\_self}$ is designed between 8 and 10. Thus, according to Fig. 14, the coupling coefficient k_c ranges from 0.562 to 0.568.

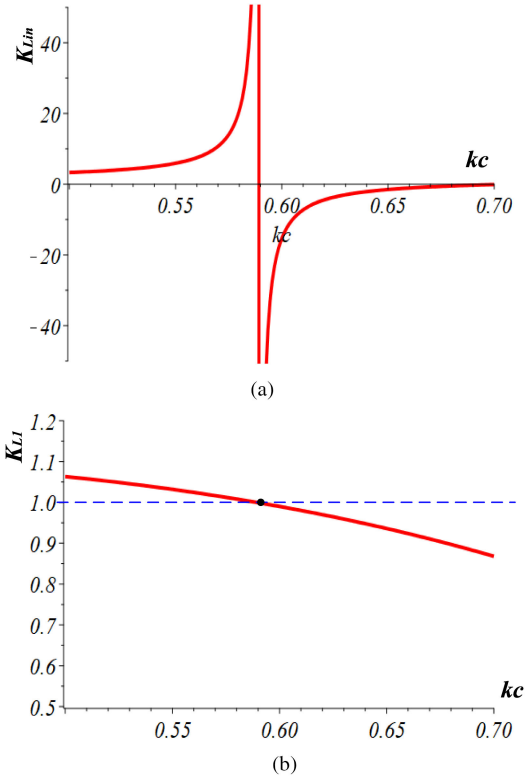


Fig. 12. Relationship between k_c and ratios of equivalent-inductance over self-inductance: (a) $K_{L\text{in}}$; (b) K_{L1}.

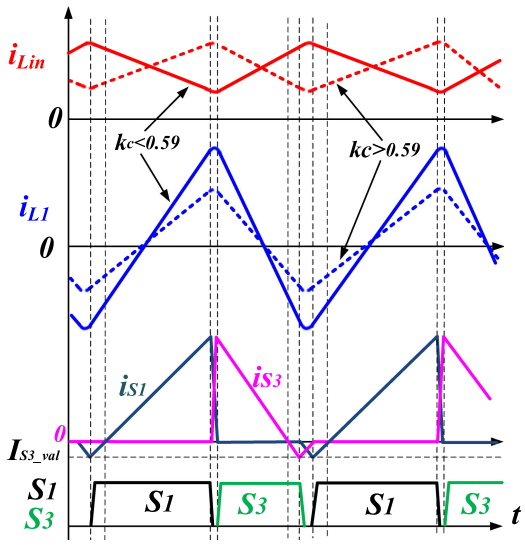


Fig. 13. Current waveform when k_c is large than 0.59.

To verify the equivalent magnetic reluctance model and select the air-gap for the E-I-E integrated inductors, 2-D FEA simulation has been conducted. As shown in Fig. 15(a), the flux is symmetrical in the E-I-E core. Fig. 15(b) shows the integrated inductors with four windings for the E-I-E core. The practical value of the coupling coefficient has been obtained based on the decoupled T model of the coupled inductor for the proposed E-I-E core geometry.

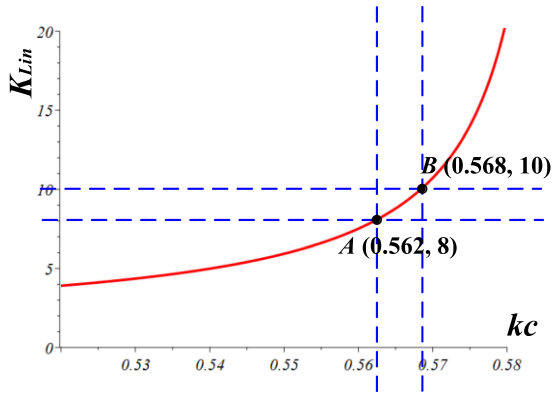


Fig. 14. Relationship between k_c and $K_{L\text{in}}$.

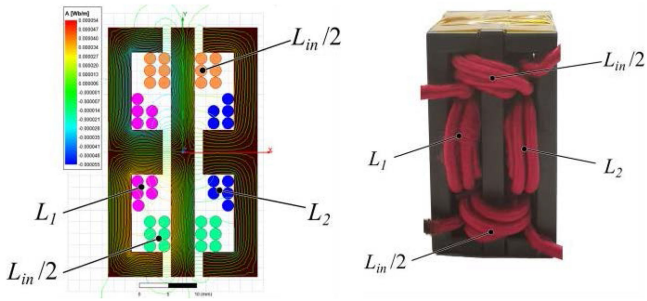


Fig. 15. Proposed E-I-E core. (a) Flux distribution for 2-D FAE simulation. (b) Practical E-I-E core structure.

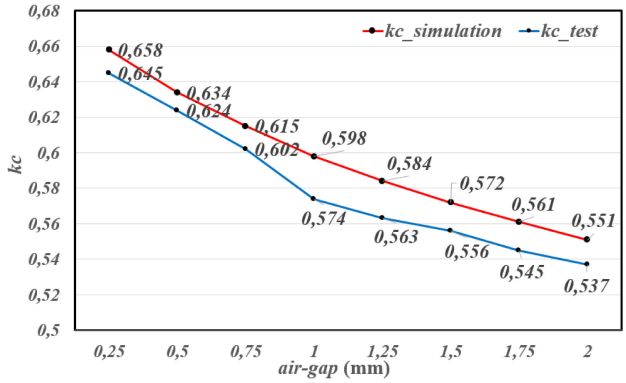


Fig. 16. Coupling coefficient value with different air-gap under 2-D FEA simulation and practical test.

Finally, the relationship between the air-gap and coupling coefficient both for FEA simulation and practical test are shown in Fig. 16. It can be seen that the coupling coefficient k_c is decreased when the length of the air-gap increases. Both of them are smaller than the theoretical analysis value 0.7 due to the leakage flux and fringing effect [41], [42].

According to the aforementioned analysis, the air-gap $g_1 = g_2 = 1.3$ mm is selected for the integrated E-I-E core inductors. According to $L_{\text{eq}} = V_{\text{in}} T_{\text{on}} / \Delta i_L$, the practice equivalent inductance can be obtained by the testing inductor current waveform. The self-inductances are directly obtained by the precision impedance analyzer Agilent 4294A. Finally, Table IV gives the actual inductance of the E-I-E integrated inductors.

TABLE IV
DESIGN INDUCTANCE OF THE INTEGRATED INDUCTOR

	E-I-E core parameters	Value (μH)
Self-inductance	L_{in_self}	14.14
	L_{1_self}	5.18
	L_{2_self}	5.30
Equivalent inductance	L_{in_eq}	140.27
	L_{1_eq}	5.81
	L_{2_eq}	5.63
Mutual inductance	M_{1_in}	5.6
	M_{2_in}	5.4

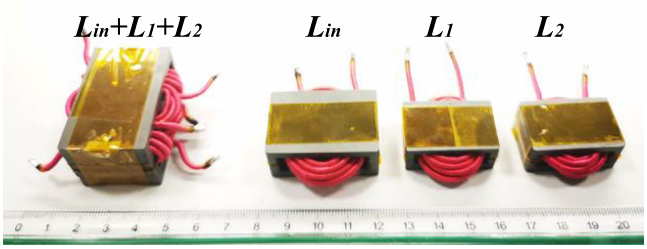


Fig. 17. Size comparison between the integrated inductors and three isolated inductors.

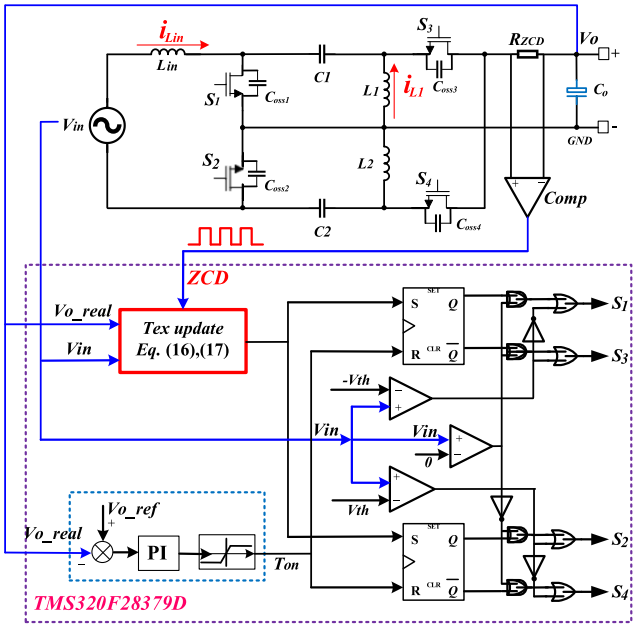


Fig. 18. Simplified control diagram for the SEPIC PFC.

Fig. 17 shows the size comparison between the proposed E-I-E integrated inductors and the conventional discrete inductors. Here, it shows that the integrated inductors can make the magnetic components more compact and reduce the volume of the inductor size.

B. Control Scheme

Fig. 18 shows the simplified control diagram with the MCU-based digital controller for the bridgeless dual-SEPIC PFC. The voltage-mode control method is selected since it does not require a high-speed current sensor and is easy to implement than the current-mode control. To attenuate the double line voltage ripple on the dc bus, the bandwidth of the voltage loop is designed around 10 Hz. The difference between the output voltage reference V_{o_ref} and the real output voltage V_{o_real} is sent to the voltage PI controller. The PI controller determines the ON-time (T_{on}) of the main switches S_1 and S_2 in different half-line cycles.

The turn-OFF instant for the synchronous switches S_3 and S_4 are triggered by the zero current detection (ZCD) signal. The ZCD signal is obtained by the shunt resistor R_{ZCD} placed before the output capacitor. After the ZCD signal is sent to the digital controller, the extended conduction time T_{ex} for S_3 and S_4 is added based on (16) and (17) to achieve the required negative current i_{S3_val}. The gate driver signals for S_2 and S_4 in the positive half-line cycle are determined by the input voltage and threshold voltage V_{th}.

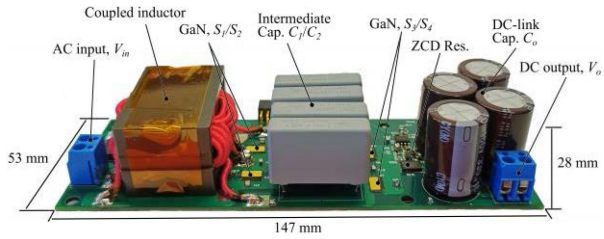


Fig. 19. Prototype of the proposed SEPIC PFC.

TABLE V
PARAMETERS OF KEY COMPONENTS

Circuit parameters	Value
S_1~S_4	GS66508T, 650 V, 50 mΩ
Isolate driver	SI8271AB-IS
Digital isolator	ADUM1100
Optically Isolated Amplifiers	ACPL-C87
C_1/C_2, Film Capacitor	MKP385E44740JKI2B0, 4*470 nF
Output electrolytic capacitor	UCY2C331MHD6, 4*330 uF
Shunt resistor for ZCD circuit	WSHM2818R0150FEA, 15 mΩ
Comparator for ZCD circuit	LMV7219
Switching frequency	400 kHz~1 MHz
Digital controller	TMS320F28379D, 200 MHz

V. EXPERIMENTAL SETUP AND MEASUREMENT

A. Experimental Prototype

Fig. 19 shows the photograph of the 300-W prototype converter. The size of this prototype is 14.7 cm × 5.3 cm × 2.8 cm; the parameters of the key components are given in Table V. The intermediate capacitor is 940 nF with two film capacitors paralleled. The dc-link bulky capacitors are 1320 uF with four electrolytic capacitors in parallel. The film capacitor has been used for the intermediate capacitors C_1 and C_2. But, the size of the intermediate capacitors can further be reduced by using few high voltage ceramic capacitors in parallel (such as CKC33C224JCGACTU, C0G, 500 V, and 0.22 uF) since the capacitance is not very high.

B. Measurement

Fig. 20(a) and (b) shows the two different situations for DCM conventional SEPIC PFC with the output diode. After the current

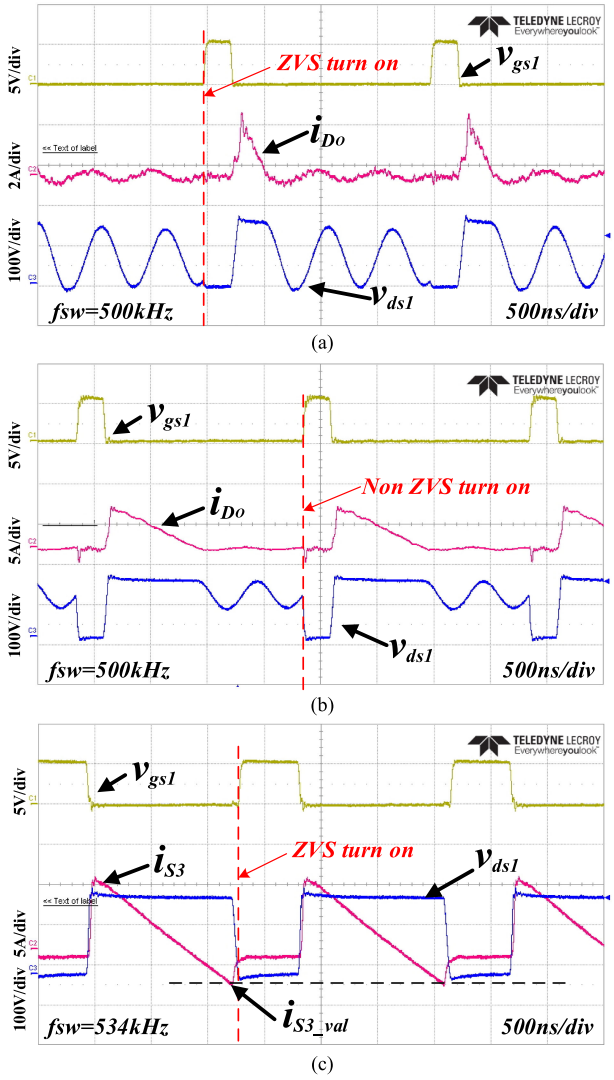


Fig. 20. Waveform for ZVS turn-ON and non ZVS turn-ON. (a) ZVS turn-ON for conventional SEPIC PFC with synchronous diode when $V_{\rm in} \leq V_{\rm o}$. (b) Non ZVS turn-ON for conventional SEPIC PFC with synchronous diode when $V_{\rm in} > V_{\rm o}$. (c) ZVS turn-ON for the modified SEPIC PFC.

of the diode $i_{\rm Do}$ decreases to zero, the resonance happened between $V_{\rm ds}$ and $i_{\rm Do}$. In Fig. 20(a), when $V_{\rm in} \leq V_O$, the ZVS operation for S_1 can be achieved since $V_{\rm ds1}$ can resonate to zero. However, when $V_{\rm in} > V_O$, only partial ZVS turn-ON can be achieved at the valley switching, as shown in Fig. 20(b). Fig. 20(c) shows the waveform of ZVS for the modified SEPIC PFC with an extended conduction time $T_{\rm ex}$ added for the synchronous GaNFETs S_3. The negative current i_{S3} transfer to the main switch S_1 to help achieve ZVS for S_1 after the S_3 turns OFF. The drain-source voltage $V_{\rm ds1}$ is discharged to zero before the main switch S_1 turns ON, thus the ZVS is guaranteed in the full range of the input voltage.

Fig. 21 shows the waveform of the drain-source voltage $V_{\rm ds1}$, $V_{\rm ds3,}$ and the gate driver signal in one switching cycle in the positive half-line cycle. Here, it can be seen that the ZVS for both the main switch and synchronous switch is achieved.

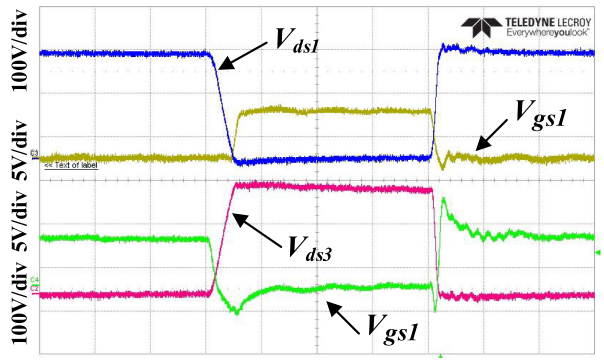


Fig. 21. Waveform of ZVS turn ON for S_1 and S_3.

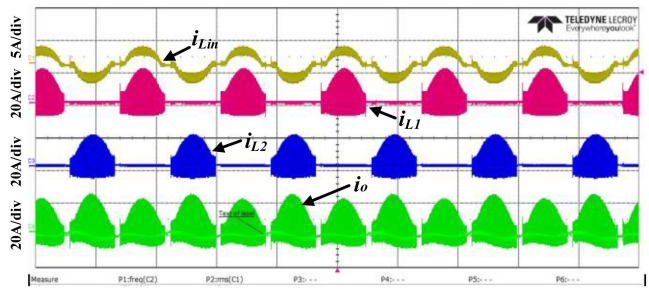


Fig. 22. Waveform of inductor current and input voltage.

Fig. 22 shows the waveform of three inductor currents i_{Lin}, i_{L1}, $i_{L2,}$ and the output current before the dc bulk capacitors i_o for the bridgeless dual-SEPIC PFC. The output current i_o is equal to the sum of the three inductor currents in the whole line cycle. It can be seen that the input current i_{Lin} is working in the CCM mode, and the input current ripple is much smaller than the output current ripple.

Fig. 23 shows the detailed waveform of the three inductor currents in different switching period with variable switching frequencies. The top two subfigures show the switching cycle in the positive half-line cycle. Here, it can be seen that the output side inductor current i_{L2} is almost 0. The output current i_o is equal to $i_{S3,}$ which is the sum of i_{Lin} and i_{L1}. Identically the bottom two subfigures show the inductor currents in the negative half-line cycle. Here, the inductor current i_{L1} is almost 0, and i_o is equal to the sum of i_{Lin} and i_{L2}. The switching frequency of the SEPIC PFC ranges from 400 kHz in the middle half-line cycle to 1 MHz in the crossing section of the line-cycle.

Figs. 24 and 25 show the experimental results for the transient performance of the proposed integrated inductors. The output voltage reference is changed from 60 to 100 Vdc. Here, it shows the integrated inductors work well under the transient change without any overshoot or undershoot.

Fig. 26 shows the testing waveform of the input current, input voltage, and dc-link voltage. The dc-link voltage is maintained at around 100 Vdc. Fig. 27 shows that the voltage of the intermediate capacitor V_{C1} and V_{C2} equal to the input voltage $V_{\rm in}$ in the positive half-line cycle and negative half-line cycle, respectively.

Fig. 28 shows the input current THD of the bridgeless dual-SEPIC PFC. Fig. 29 shows the input current of each harmonic

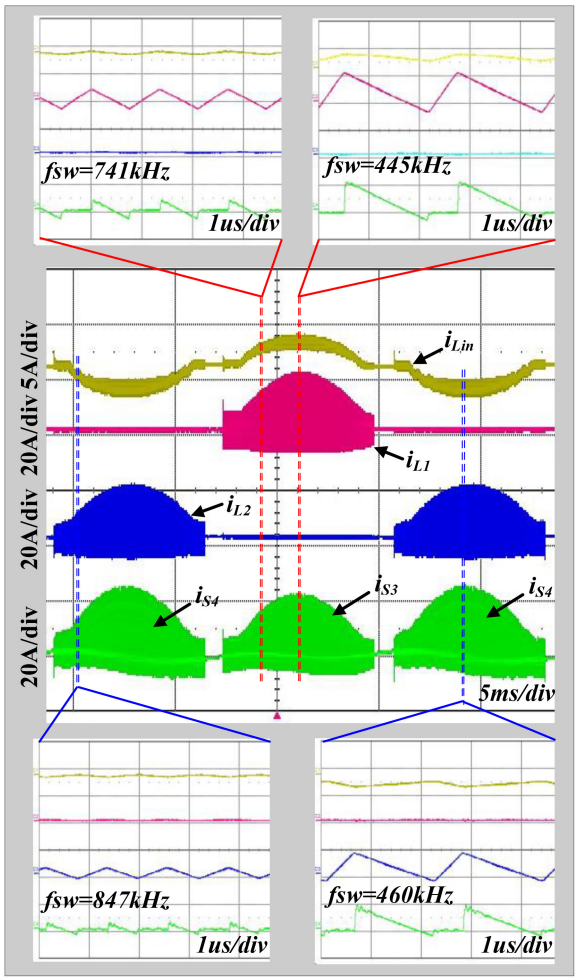


Fig. 23. Waveform of inductor current and input voltage.

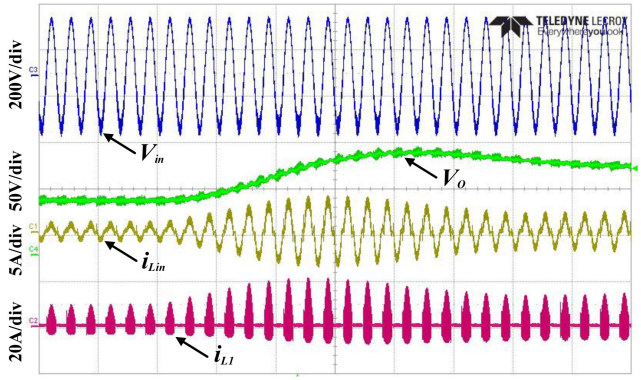


Fig. 24. Dynamic response from $V_{o\_ref} = 60$ Vdc to 100 Vdc.

order for the bridgeless dual-SEPIC PFC is under the limitation of the international standard EN61000-3-2 Class-A. Due to the negative current in the switching cycle and the no power transfer mode near the zero-crossing input voltage, some distorted input current has happened around the zero-crossing section of the input voltage [39], [44].

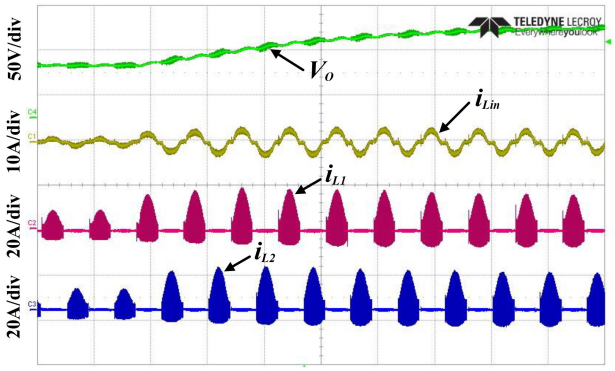


Fig. 25. Three inductor current waveforms of the integrated inductors under dynamic response.

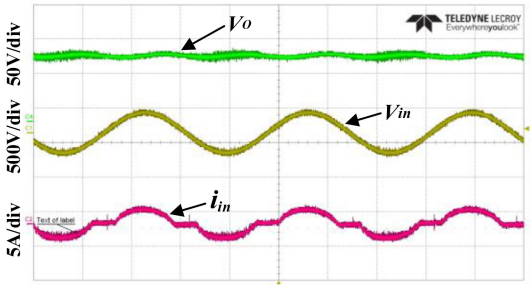


Fig. 26. Waveform of input current, input voltage, and dc-link voltage.

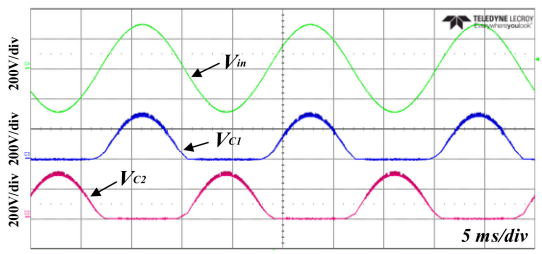


Fig. 27. Waveform of input volage $V_{\rm in}$, intermediate capacitors voltage V_{C1} *and* V_{C2}.

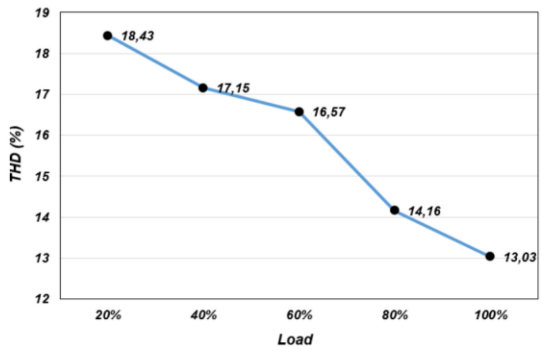


Fig. 28. Measured THD of the SEPIC PFC ($V_{\rm in} = 220$ Vac).

The system efficiency (including the dc-link bulky capacitors) of the porotype from 10% to 100% of full load under the $V_{\rm in} = 220$ Vac, $V_o = 100$ Vdc, as shown in Fig. 30. The peak efficiency is 97% under full load.

TABLE VI
COMPARISON OF DIFFERENT SEPIC PFC

Topology	Power (W)	Work Mode	Switching frequency(kHz)	ZVS	Peak Efficiency	Switch device information		
						Input rectifier	Main switches	Output side switches
Sepic PFC with diode bridge[13]	1000	DCM	100	No	<94%	1*Rectifier: GBPC3506W 600V, Vf: 1.1 V	2*Si: FCH041N60F 600V, 36 mΩ	1*Diode: VS-60APU04 400 V, Vf: 0.87 V
Interleaved Sepic PFC with diode bridge[11]	500	DCM	150	No	96%	1*Rectifier: unknown	2*Si: unknown	2 * Diode: unknown
Active Clamped Isolated Sepic PFC[10]	2000	DCM	200	Partial ZVS	96.56%	1*Rectifier: unknown	2*SiC: SCT3040KL 1200V, 40 mΩ	2*SiC Diode: 4D40120D 1200 V, Vf: 1.5 V 1*Clamp Diode: RURP8100 1000 V, Vf:1.8 V
Bridgeless Sepic PFC[22]	60	DCM	50	No	96%	No	2*Si: FQA48N20 200V, 50 mΩ	2*Diode: MUR840 400 V, Vf: 1.3 V
Bridgeless Sepic PFC with Power decoupling[21]	500	CCM	20	No	95.6%	No	2*Si: IPW60R099P6 600V, 99 mΩ 2*Diode: DSEI60-06A 600V, Vf:1.8 V	1*Diode: DSEI60-06A 600V, Vf:1.8 V
Bridgeless Sepic PFC with output diode[26]	760	CCM	20	No	92%	No	2*Si: unknown	2 * Diode: unknown
Improved Bridgeless SEPIC Converter[16]	100	DCM	65	No	94%	No	2*Si:IPP60R125C6 600V, 125 mΩ 2*Diode: SF20L60U 600 V,Vf: 3 V	2*Diode: SF20L60U 600 V, Vf: 3 V
Proposed converter	300	CRM	400~1000	Yes	97%	No	2*GaN: GS66508T 650V, 50 mΩ	2*GaN: GS66508T 650V, 50 mΩ

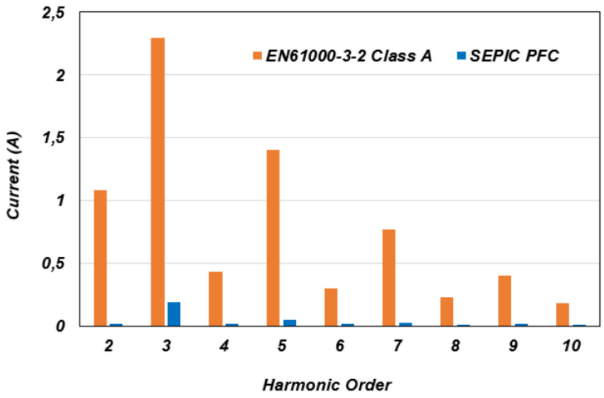


Fig. 29. Harmonics of dual SEPIC PFC and Class-A equipment harmonic current limit standard.

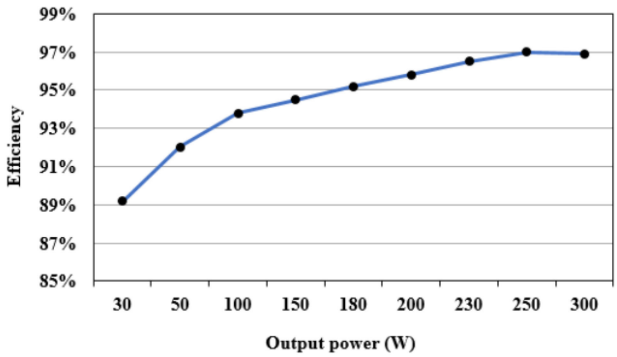


Fig. 30. Measured efficiency curve of the SEPIC PFC prototype.

Table VI gives the comparison of the state-of-the-art SEPIC PFC with the modified SEPIC PFC. It can be seen that the GaN-based MHz dual-SEPIC PFC developed by the author's group is the only one that can achieve the ZVS in the full range of the input voltage. It achieves the highest peak efficiency in a high switching frequency.

VI. CONCLUSION

This article presents a bridgeless GaN-based Dual-SEPIC PFC with ZVS operation for the application of a step-down ac–dc converter. The input current is working in the CCM mode, and the sum of the input current and output current is working in the CRM mode. To achieve the ZVS operation for the main switch, the extra negative current is provided by adding the extended conduction time for the synchronous switch after the current of the synchronous switch decrease to zero. Moreover, The E-I-E integrated inductors have been proposed for the bridgeless dual-SEPIC PFC. All the inductors, including one input inductor and two output inductors, have been integrated into the E-I-E core, reducing the total ferrite volume and making the converter more compact. The inductance design and magnetic modeling for the coupled inductor have been analyzed. With a carefully designed coupling coefficient, the equivalent input inductance can be implemented with a much smaller number of winding turns. A 300-W GaN-based MHz bridgeless dual-SEPIC PFC with the integrated inductors is developed to verify the theoretical analysis and design. The experimental results show that full–range ZVS is realized, and the peak efficiency is 97%.

REFERENCES

[1] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications— An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
[2] J. A. Garcia, R. Cobos, P. Prieto, and J. Uceda Alou, "Single phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.
[3] *Limits for Harmonic Current Emissions (Equipment Input Current ≤16A per Phase)*, IEC Standard 61000-3-2, Ed. 3.2, 2009.
[4] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[5] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost PFC," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2574–2587, Jul. 2009.

[6] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[7] F. C. Lee, Q. Li, Z. Liu, Y. Yang, C. Fei, and M. Mu, "Application of GaN devices for 1 kW server power supply with integrated magnetics," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 3–12, Dec. 2016.

[8] Q. Huang, and A. Q. Huang, "Review of GaN totem-pole bridgeless PFC," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 187–196, Sep. 2017.

[9] D. S. Lyrio Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and Cuk power factor preregulators: Analysis and design,", *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.

[10] D. Wu, R. Ayyanar, M. Sondharangalla, and T. Meyers, "High-Performance active-clamped isolated SEPIC PFC converter with SiC devices and lossless diode clamp," *IEEE J. Emerg. Sel. Topics. Power Electron.*, vol. 8, no. 1, pp. 567–577, Mar. 2020.

[11] C. Shi, A. Khaligh, H. Wang, "Interleaved SEPIC power factor preregulator using coupled inductors in discontinuous conduction mode with wide output voltage," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3461–3471, Jul./Aug. 2016.

[12] H. Wang, and A. Khaligh, "Interleaved SEPIC PFC converter using coupled inductors in PEV battery charging applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 586–591.

[13] R. Chen and J. S. Lai, "Analysis and design of DCM SEPIC PFC with adjustable output voltage," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 477–484.

[14] C. Zheng *et al.*, "An improved bridgeless SEPIC PFC rectifier with optimized magnetic utilization minimized circulating losses and reduced sensing noise," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 1906–1911.

[15] P. J. S. Costa, C. H. Illa Font, and T. B. Lazzarin, "A family of single-phase voltage-doubler high-power-factor SEPIC rectifiers operating in DCM," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4279–4290, Jun. 2017.

[16] H. Ma, Y. Li, J. S. Lai, C. Zheng, and J. Xu, "An improved bridgeless SEPIC converter without circulating losses and input-voltage sensing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1447–1455, Sep. 2018.

[17] A. J. Sabzali, E. H. Ismail, M. A. Al Saffar, and A. A. Fardoun, "New bridgeless DCM SEPIC and cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.

[18] M. Sahid, A. Yatim, and T. Taufik, "A new ac–dc converter using bridgeless SEPIC," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, 2010, pp. 286–290.

[19] M. Mahdavi and H. Farzanehfard, "New bridgeless PFC converter with reduced components," in *Proc. Int. Conf. Electron. Devices Syst. Appl.*, 2011, pp. 125–130.

[20] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[21] Y. Liu, Y. Sun, and M. Su, "A control method for bridgeless cuk/sepic PFC rectifier to achieve power decoupling," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7272–7276, Sep. 2017.

[22] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009.

[23] V. Bist *et al.*. "An adjustable speed PFC bridgeless-SEPIC fed brushless dc motor drive," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4886–4893.

[24] A. M. Al Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless PFC-modified SEPIC rectifier with extended gain for universal input voltage applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4272–4282, Aug. 2015.

[25] X. Shen, T. Yan, Q. Li, Y. Wang, W. Chen, "Variable on-time controlled boundary conduction mode single-ended primary inductor converter power factor correction converter," *Electron. Lett.*, vol. 54, no. 2, pp. 97–99, 2018.

[26] B. Singh and R. Kushwaha, "A PFC based EV battery charger using a bridgeless isolated SEPIC converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 477–487, Jan./Feb. 2020.

[27] M. R. Sahid, A. H. M. Yatim, and T. Taufik, "A new AC-DC converter using bridgeless SEPIC," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, 2010, pp. 286–290.

[28] Y. Onal and Y. Sozer, "Bridgeless SEPIC PFC converter for low total harmonic distortion and high power factor," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2693–2699.

[29] R. Kushwaha and B. Singh, "An improved SEPIC PFC converter for electric vehicle battery charger," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2019, pp. 1–8.

[30] C. Shen, Y. Wu, and C. Tsai, "Coupled-inductor Sepic-type PFC with soft-switching feature for LED lighting applications," in *Proc. 6th IEEE Conf. Ind. Electron. Appl.*, 2011, pp. 2384–2389,.

[31] P. Athalye, D. Maksimovic, and R. Erickson, "Improving efficiency of the active-clamped SEPIC rectifier at high line frequencies," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2005, pp. 1152–1157.

[32] Andersen MAE, inventor, "Bidirectional switched mode resonant type ac-dc converter and method for operating a bidirectional switched mode resonant type ac-dc converter," H02M 7/48 A I, 2019.

[33] Z.-W. Xu, Z.-L. Zhang, K. Xu, Z. Dong, and X. Ren, "2-MHz GaN PWM isolated SEPIC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017.

[34] Y. Dou, Z. Ouyang, P. Thummala, and M. A. E. Andersen, "PCB embedded inductor for high-frequency ZVS SEPIC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 98–104.

[35] B. Ulrich, "Analysis of a ZVS synchronous sepic/zeta DC/DC converter," in *Proc. Int. Exhib. Conf. for Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2018, pp. 1–8.

[36] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.

[37] P. Prabhu and V. Urundady, "Design of coupled inductors using split winding scheme for bridgeless SEPIC," *IET Power Electron.*, vol. 13, no. 7, pp. 1434–1444, 2020.

[38] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-Frequency high-efficiency gan-Based interleaved CRM bidirectional buck/boost converter with inverse coupled inductor," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4343–4352, Jun. 2016.

[39] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of gan-Based MHz totem-pole PFC rectifier," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.

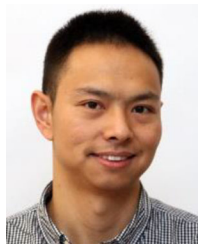
[40] Z. Liu, Z. Huang, F. C. Lee, Q. Li, and Y. Yang, "Operation analysis of digital control based MHz totem-pole PFC with GaN device," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 281–286.

[41] Z. Liu, X. Huang, M. Mu, Y. Yang, F. C. Lee, and Q. Li, "Design and evaluation of gan-based dual-phase interleaved MHz critical mode PFC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 611–616.

[42] M. Chen, M. Araghchini, K. K. Afridi, J. H. Lang, C. R. Sullivan, and D. J. Perreault, "A systematic approach to modeling impedances and current distribution in planar magnetics," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 560–580, Jan. 2016.

[43] A. Ayachit and M. K. Kazimierczuk, "Sensitivity of effective relative permeability for gapped magnetic cores with fringing effect," *IET Circuits, Devices Syst.*, vol. 11, no. 3, pp. 209–215, 2017.

[44] X. Ren, Y. Zhou, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Simple analog-based accurate variable on-time control for critical conduction mode boost power factor correction converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4025–4036, Dec. 2020.



Yunfeng Liu (Student Member, IEEE) received the M.Sc. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016. He is currently working toward the Ph.D. degree with the Technical University of Denmark, Lyngby, Denmark.

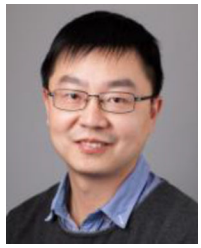
From 2016 to 2018, he was a Senior Research and a Development Engineer in the areas of power electronics in Delta Electronics. His research interests include design of high-frequency high power density ac–dc converters, high power bidirectional dc–dc converter, modelling for magnetic components, digital controller design, wireless power transfer.

Xiaosheng Huang (Member, IEEE) received the B.E. and Ph.D. degrees, from Fuzhou University, Fuzhou, China, in 2009 and 2015, respectively.

He is currently an Associate Professor with the School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou, China. He is also with the Fujian Provincial University Engineering Research Center for Industrial Automation, Fujian University of Technology. He is a member of the Magnetic Component Specialty Committee of the China Power Supply Society. His current research interests include power conversion, high-frequency magnetics, wireless power transfer, and electromagnetic field analysis and applications.

Yi Dou (Student Member, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016, and the M.Sc. degree in power electronics in 2018 from Technical University of Denmark, Lyngby, Denmark, where he is currently working toward the Ph.D. degree.

His research focuses on design of high-frequency/very-high-frequency dc–dc converters, modelling for magnetic components, and modelling and optimization of MHz-range wireless power transfer systems.



Ziwei Ouyang (Senior Member, IEEE) received the Ph.D. degree from Technical University of Denmark (DTU), Lyngby, Denmark, in 2011.

From 2011 to 2013, he was a Postdoc Researcher with DTU. From 2013 to 2016, he was an Assistant Professor with DTU. Since from April 2016, he has been an Associate Professor with DTU. He has more than 70 high-impact IEEE journal and conference publications, co-author on a book chapter on Magnetics for the *Handbook of Power Electronics* and is currently the holder of eight international patents. His research interests include high-frequency planar magnetics modeling and integration, high-density high efficiency power converters, PV battery energy storage system, wireless charging, etc.

Dr. Ouyang was the recipient of the Young Engineer Award at PCIM Asia 2014, and the Best Ph.D. Dissertation of the Year Award 2012 in Technical University of Denmark. He received several best paper awards in IEEE sponsored international conferences. He has been invited to give lectures in many universities, enterprises and educational seminars and workshops around the world including USA, Europe, and China. He was a Session Chair in some IEEE sponsored conferences and an Associated Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

Michael A. E. Andersen (Member, IEEE) received the M.Sc. and Ph.D. degrees in power electronics from the Technical University of Denmark, Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor of power electronics with the Technical University of Denmark, where since 2009, he has been the Deputy Head of the Department of Electrical Engineering. He is the author or co-author of more than 300 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.