# Datasheet-Driven Compact Model of Silicon Carbide Power MOSFET Including Third-Quadrant Behavior

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***Abstract*—This article presents a simulation model of silicon carbide (SiC) power MOSFET that accurately predicts both the static and dynamic third-quadrant behavior without compromising the first-quadrant's accuracy. Unlike existing models, this model features an asymmetric third-quadrant behavior for MOSFET characteristics necessary for the accurate synchronous rectifier simulations. Moreover, it includes the gate-dependent body diode behavior, essential for the accurate prediction of freewheeling high-side device behavior in half-bridge configurations with significant gate voltage oscillation. The model also includes reverse recovery characteristics for the accurate overshoot and power loss prediction. Despite having these added features, the model demonstrates good convergence and efficiency due to the replacement of conditional piecewise equations with continuous ones consisting of weighted variables. The model's convergence capability and efficiency have been verified by simulating a five-level cascaded H-bridge multilevel inverter. The model's superior efficiency and accuracy have been validated by comparing it with an established SiC power MOSFET model. Also, an easy-to-follow parameter extraction procedure is documented that only requires data commonly available in commercial datasheets for broader utility. Considering accuracy, efficiency, and convenience, the model is useful for all power electronics converter applications.**

***Index Terms*—Body diode, freewheeling diode, power MOSFET, reverse recovery, silicon carbide (SiC), synchronous rectification.**

## I. Introduction

SILICON carbide (SiC) power MOSFETs have started to dominate applications, such as three-phase inverters, pulsewidth modulation rectifiers, and dc–dc converters, in the voltage range of 1.2–3.3 kV [1], [2]. These applications require freewheeling diodes. For the majority of Si insulated gate bipolar transistors (IGBTs), the only option is to use external antiparallel diodes. SiC Schottky barrier diodes (SBDs) are widely used as the antiparallel diode for Si IGBTs. In contrast to the IGBT, power MOSFETs have an intrinsic body diode comprised of p-body, n-drift region, and n+ drain contact. This intrinsic body diode can act as a freewheeling diode. Since the body diode is a p-i-n configuration, it requires removing minority carriers before blocking the reverse voltage. This phenomenon gives rise to the reverse recovery current ($I_{rr}$). For the SiC power MOSFET, this reverse recovery current is significantly smaller than the Si power MOSFET because of the thinner and highly doped drift region.

In contrast, SiC SBDs do not have any reverse recovery, and the forward voltage drop is almost half of that from the body diode of the SiC power MOSFET. Even though during the early generations, reliability issues, notably surge current tolerance, were very poor for body diodes [3]; the newer generations of SiC MOSFETs have improved reliability due to better substrate quality. At the same time, reverse recovery characteristics have progressed to the point that the power loss has become comparable with the antiparallel SBD [4]. Also, external antiparallel SBDs increase the capacitance. Although the power loss has become similar for these two cases, the intrinsic body diode will free up space for additional devices in a power module. Thus, the use of the body diode in place of an SBD will increase the current rating and lower cost. So, the intrinsic body diodes of SiC power MOSFETs must be taken into consideration for efficient circuit designs.

To truly utilize the power of the SiC MOSFET in power electronics circuit design, the accurate, numerically attractive, and efficient simulation model is required. One of the earliest contributions to SiC power MOSFET modeling was by McNutt *et al.* [5]. This physics-based compact model introduced unique expressions for low-voltage turn-ON of the corners of the MOSFET and enhanced transconductance for the linear region due to the carrier concentration gradient for nonuniform doping in the channel. However, the model used a proprietary tool for parameter extraction and, thus, was not accessible for many users. Mudholkar *et al.* [6] presented a modified version of the article presented in [5] and included the more accurate description of the MOS channel, drift region, nonlinear capacitances, and the internal charges. The parameter extraction procedure was documented and described in a user-friendly way for easy extraction of the parameter set from only the data available in datasheets. The work in [6] was groundbreaking in this regard. Another physics-based compact model developed by Kraus and Castellazzi [7] incorporated the effect of interface trapped charge on mobility and surface potential. A unique approach adopted in [7] for modeling bias-dependent drift resistance is the first of its kind. Nevertheless, the model does not give any details about the third-quadrant performance. A summary of other compact models published before 2014 can be found in [8]. None of the

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models described the third-quadrant characteristics of the power MOSFET. Since then, several new attempts have been undertaken to develop more accurate and efficient models [9]–[12]. Among these, Mukunoki *et al.* [9] present a model for the accurate gate current prediction. The model can be beneficial for gate driver optimization. However, transient simulation results show a significant mismatch with the measured results. Lee *et al.* [10] present a groundbreaking idea of using neural network training to develop a power MOSFET model. But the model does not show any capacitance–voltage ($C$–$V$) characteristics. The usefulness of the model was also not verified by demonstrating how well it matches with the transient results. None of these articles document the third-quadrant characteristics. A summary of more recent works on the modeling of SiC power MOSFET can be found in [13].

Reverse recovery of the body diode due to its p-i-n structure is a serious concern because of the loss of switching speed and the high *di/dt* during turn-ON. Moreover, reverse recovery can turn ON the parasitic BJT, creating reliability issues [14]. So, it is very important to model the reverse recovery effect. According to the authors' knowledge, none of the existing physics-based or behavioral models of SiC power MOSFETs provide the reverse recovery effect modeling. Due to heavier doping and lower thickness, the drift region of SiC power MOSFET accumulates less minority carriers during forward conduction, but the reverse recovery current ($I_{rr}$) cannot be ignored as it can reach up to 30% of the load current during the turn-ON switching [15]. Peng *et al.* [15] provide a physics-based Fourier-based-solution analytical model for the body diode with reverse recovery. However, the model is not incorporated in a MOSFET model, and the gate-bias dependency on the body diode is not captured.

This article presents a physics-based compact model that incorporates the gate-dependent body diode effect, including reverse recovery, and is, therefore, capable of accurately and efficiently simulating both the first- and third-quadrant characteristics of a SiC power MOSFET. So far, only a few empirical models provided by commercial vendors have gate-dependent body diode characteristics. However, the fit in the third quadrant is not very accurate [16]. These empirical models do not incorporate the reverse recovery characteristics, which are not entirely negligible for SiC power MOSFETs. Moreover, a diligent smoothing approach has been presented to improve the model's convergence properties and efficiency in terms of simulation time despite adding the third-quadrant characteristics and computationally expensive reverse recovery. This approach also makes the equations used in the model continuous in their higher order derivatives. A new parameter extraction procedure is developed to extract the model parameters from data that are available in the datasheet. A comparison with a previous model [6] has been put forward both in terms of the static and dynamic performance to justify the presented model's importance. The significance of the presented model has been validated further with a complex circuit simulation. The key contributions of this article are as follows.

1) inclusion of bias-dependent body diode in SiC power MOSFET model;
2) inclusion of the SiC body diode's reverse recovery effect;
3) the accurate simulation of the third-quadrant characteristics that combine both channel current and bias-dependent body diode current;
4) a new approach of smoothing to incorporate different effects into the model without degrading the convergence properties;
5) verification of the model's efficiency and convergence properties in a complex power electronics circuit application.

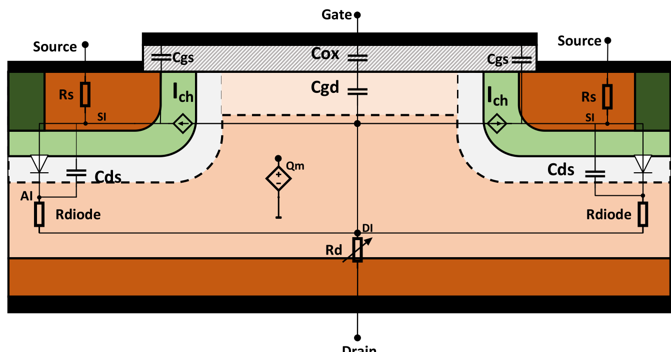


Fig. 1. Subcircuit representation of the model components of the different parts of SiC power MOSFET.

The rest of this article is organized as follows. Section II presents the model description, consisting of channel current, ON-resistance, body diode and reverse recovery characteristics, and capacitance characteristics. This section also describes the smoothing approach adopted for improving the model's convergence properties. Section III describes the new parameter extraction procedure of the developed model. Section IV validates the accuracy of the model in both static and dynamic performance. This section also justifies the developed model's importance by comparing it with a previous model of the article presented in [6]. Section V describes a convergence assessment of the model by simulating a five-level cascaded H-bridge multilevel inverter (CHB-MLI). Finally, Section VI draws the article to the conclusion by summarizing the descriptions and contributions.

## II. Model Development

Different characteristics of the SiC power MOSFET are modeled in separate sections. Each section contains a table that lists the parameters and their definitions used in developing that particular section of the model. The extracted values of the parameters for a commercial SiC power MOSFET (C2M0080120D) are also provided in the tables. The model parameters are highlighted by boldface italics (example: $\boldsymbol{V_{thxy}}$) in rest of the article, whereas a simple italic font (example: $Vgs$) denotes the bias points (voltages, currents, and charges).

The model represents various physical parts of the SiC power MOSFET as the different components of the subcircuit, as shown in Fig. 1. Besides three external nodes of gate, drain, and source, there are three internal nodes (DI, SI, and AI) to accommodate voltage drop in the drain, the source, and the base region.

### A. Channel Current Modeling

The expressions for the channel current are modified from the articles presented in [5] and [6]. The channel current ($I_{ch}$) consists of four components: two components, each for the first and third quadrants, as shown in (1). From here on, if not specified, otherwise $x = l, h$ stands for the low- and high-current region, and $y = f, r$ stands for the first- and third-quadrant operation, respectively.

The two components ($I_{mosl}, I_{mosh}$) in each quadrant represent the low-current region and the high-current region, respectively

$$I_{ch} = I_{moslf} + I_{moshf} + I_{moslr} + I_{moshr}. \quad (1)$$

McNutt *et al.* [5] explain the reasons behind these two components' existence as the early turn ON of the corner regions, which have lower threshold voltage ($\boldsymbol{V_{thl}}$) and transconductance. An alternative explanation is that the two components have different threshold voltages ($\boldsymbol{V_{thl}}, \boldsymbol{V_{thh}}$) because of the gradual emptying of interface states close to the conduction band. As a result, effective MOS capacitances, seen by two components, and their respective mobilities also differ. These effects can be captured by having different transconductance parameters in the saturation region ($\boldsymbol{k_{pl}}, \boldsymbol{k_{ph}}$) [6]. The different transconductances in the triode region are represented by using different parameters ($\boldsymbol{k_{fl}}, \boldsymbol{k_{fh}}$). The gradual transition from linear to saturation region, a distinct characteristic of SiC MOSFET, has been captured by pinch-off parameters ($\boldsymbol{pvf_l}, \boldsymbol{pvf_h}$). Due to a large density of interface charge and their gradual emptying, the transition trajectory for low- and high-gate voltages is different. So, to accurately model this gate voltage dependency on the gradual transition, the channel current equations are modified in this article by two control parameters ($\boldsymbol{pvf_l}, \boldsymbol{pvf_h}$) instead of one ($\boldsymbol{pvf_l}$) used in [5] and [6].

In the third-quadrant operation, i.e., ($Vds < 0$) and ($Ids < 0$), the current flows in the opposite direction compared with the first quadrant. In this state of operation, there are two possible paths for the current to flow. The first is the inversion channel-induced MOSFET path. The second is the body diode. For $Vgs$ higher than the threshold voltage, the inversion layer exists in the channel region, and the current flows through the channel path following the MOSFET characteristics. In this range of operation, when the voltage drop across the p-n junction is not sufficient to forward bias, the MOSFET characteristics dominate.

Even from the measured data, it is seen that the threshold voltages in the third quadrant and the first quadrant are not the same. This difference in the two quadrants can be explained by the existence of the depletion layer between the p-base and n-drift layers. For a negative drain bias compared with the source, the depletion layer thickness is less. Thus, the inversion channel is formed at a lower gate voltage due to less distance between two electron-rich regions. The concept is verified using technology computer aided design (TCAD) simulation. In Fig. 2, we can see that the depletion region between the p-body and n-drift region is thinner for the third-quadrant bias condition. Therefore, there is a continuous inversion channel. However, for the first-quadrant bias condition, the depletion region is wider. Hence, there is no inversion channel at the same gate voltage.

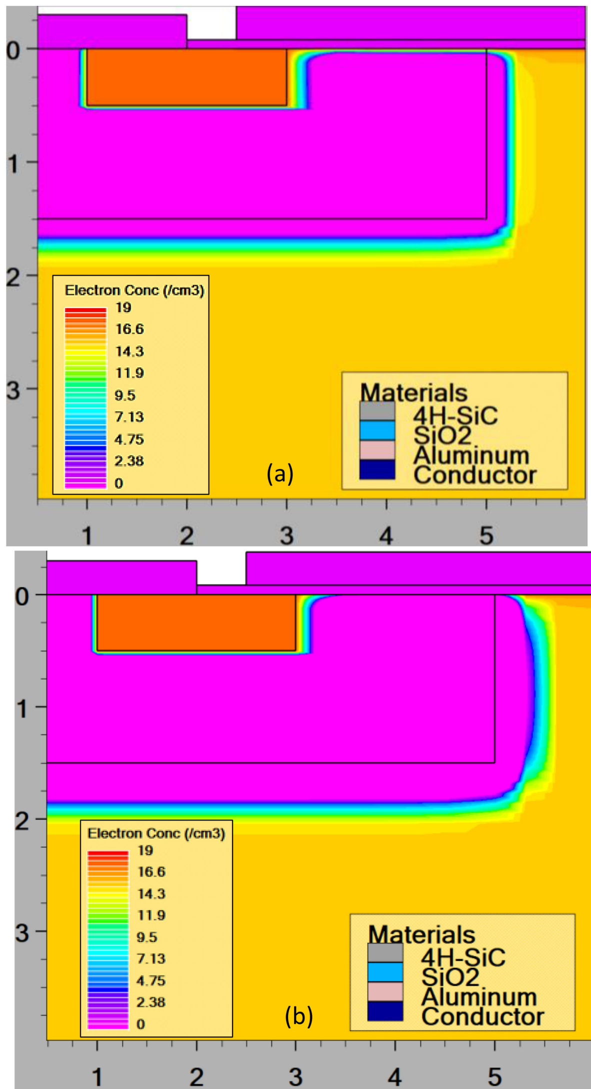


Fig. 2. Numerical simulation of SiC power MOSFET to observe inversion channel condition. (a) For $Vgs = 5.6$ V and $Vds = -1$ V. (b) For $Vgs = 5.6$ V and $Vds = 1$ V.

The simulated transfer characteristics for the first- and third-quadrant conditions are shown in Fig. 3. The difference in threshold voltage and transconductance of the first and third quadrant are easily distinguishable from the TCAD simulation results. So, MOSFET characteristics in the first and third quadrant require different threshold voltages and transconductance-related parameters. Hence, the third-quadrant characteristics are decoupled from the first-quadrant MOSFET channel characteristics with two separate current components ($I_{moslr}, I_{moshr}$). The components have their respective threshold voltages ($\boldsymbol{V_{thlr}}, \boldsymbol{V_{thhr}}$) and transconductance parameters. This decoupling allows the model to accurately capture the SiC power MOSFETs' behavior in synchronous rectification where the reverse MOSFET characteristics are used for the low-voltage drop. Each of the four components of the channel current has been formulated with single continuous equations, as shown in (2). Equation (3) makes the transconductance parameter and its first derivative

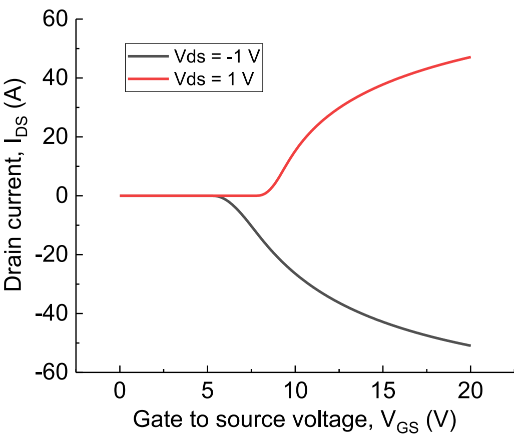


Fig. 3. TCAD simulated transfer characteristics of a SiC power MOSFET at the first- and third-quadrant operation.

continuous at the pinch-off voltage [5] using an intermediary transconductance term $K_{xy}$

$$I_{mosxy} = \boldsymbol{k_{fxy}} \cdot \boldsymbol{k_{pxy}} \cdot Vgs_{effxy} \cdot Vds_{effxy} - \boldsymbol{pvf_x}^{K_{xy}-1} \cdot Vds_{effxy}^{K_{xy}} \cdot \frac{Vgs_{effxy}^{\frac{2-K_{xy}}{K_{xy}}}}{1+\ \theta_{\boldsymbol{xy}} \cdot Vgs_{effxy}} \tag{2}$$

where $K_{xy}$ is expressed by

$$K_{xy} = \frac{\boldsymbol{k_{fxy}}}{\boldsymbol{k_{fxy}} - \frac{\boldsymbol{pvf_x}}{2}}. \tag{3}$$

Although accurate and physics based, the piecewise models developed in [5] and [6] lack continuity in the higher order derivatives. This lack of continuity limits the order of integration and step size in transient analyses and reduces the accuracy in distortion analyses [17]. The model presented in this article removes the necessity of piecewise equations by using continuous weighted functions of the gate-to-source voltage (*Vgs)* and the drain-to-source voltage (*Vds),* namely $Vgs_{effxy}$ and $Vds_{effxy}$, as shown in (4) and (8). Equation (5) expresses the saturation voltage ($Vds_{satxy}$). Equations (6) and (7) decouple *Vds* for the first- and third-quadrant operations with the effective first-quadrant drain-to-source voltage ($Vds_f$) and the effective third-quadrant drain-to-source voltage ($Vds_r$). This approach makes the model continuous without any conditional statements and removes discontinuities in higher order derivatives. Here, $\boldsymbol{\partial}$ is the smoothing parameter. The value of $\boldsymbol{\partial}$ should be $\leq$ 1 $\mu$ to ensure minimum impact on the device characteristics while maintaining continuity of the equation. Table I lists the parameters related to model the channel current.

$$Vgs_{effxy} = \frac{\ln\left(1+e^{Vgs-\mathbf{V_{thxy}}}\right)}{1+e^{-(Vgs-\boldsymbol{V_{thxy}}-2\boldsymbol{\partial})}} \tag{4}$$

$$Vds_{satxy} = \frac{Vgs_{effxy}}{\boldsymbol{pvf_x}} \tag{5}$$

$$Vds_f = \frac{1}{2}\left(Vds + \sqrt{Vds^2 + 4\boldsymbol{\partial}^2}\right) \tag{6}$$

TABLE I
PARAMETERS FOR CHANNEL CURRENT MODELING

| Notation | Definition | Value ($y$ =f/$r$) | Unit |
|---|---|---|---|
| $\boldsymbol{V_{thly}}$ | Low current threshold voltage | 4.735 /4.163 | V |
| $\boldsymbol{V_{thhy}}$ | High current threshold voltage | 10.63 /10.63 | V |
| $\boldsymbol{\theta_{ly}}$ | Transverse electric field mobility factor at the low gate voltages | 0.0291 /0.050 | V$^{-1}$ |
| $\boldsymbol{\theta_{hy}}$ | Transverse electric field mobility factor at the high gate voltages | 15.33 /15.33 | V$^{-1}$ |
| $\boldsymbol{k_{ply}}$ | Saturation region transconductance parameter at low gate voltages | 4.69 /17.65 | A/V$^2$ |
| $\boldsymbol{k_{phy}}$ | Saturation region transconductance parameter at high gate voltages | 2285 /2285 | A/V$^2$ |
| $\boldsymbol{k_{fly}}$ | Triode region transconductance parameter at low gate voltages | 27.06 /0.2197 | - |
| $\boldsymbol{k_{fhy}}$ | Triode region transconductance | 56.27 /56.27 | - |
| | parameter at high gate voltages | | |
| $\boldsymbol{pvf_l}$ | Pinch-off parameter for low-gate voltage region | 0.1731 | - |
| $\boldsymbol{pvf_h}$ | Pinch-off parameter for high-gate voltage region | 0.01256 | - |
| $\boldsymbol{\partial}$ | Smoothing parameter | 1E-6 | - |

$$Vds_r = Vds - \frac{1}{2}\left(Vds + \sqrt{Vds^2 + 4\boldsymbol{\partial}^2}\right) \tag{7}$$

$$Vds_{effxy} = Vds_{satxy} - \frac{1}{2}\left((Vds_{satxy} - Vds_y - \boldsymbol{\partial}) + \sqrt{(Vds_{satxy} - Vds_y - \boldsymbol{\partial})^2 + 4\cdot\boldsymbol{\partial}\cdot Vds_{satxy}}\right). \tag{8}$$

### B. ON-Resistance Modeling

The total resistance ($R_{total}$) of the conduction path is divided into three components: channel resistance ($R_{ch}$), source resistance ($R_s$), and the drain resistance ($R_d$). $R_{ch}$ is the intrinsic resistance of the MOSFET. The voltage–current relationship in (2) automatically models that. The contact resistance forms the majority of resistance seen in the source terminal. Due to the constant ohmic contact between the metal and a heavily doped source region, it is modeled by a constant parameter (***rs***).

$$R_{total} = R_{ch} + \boldsymbol{rs} + R_{dy}. \tag{9}$$

TABLE II
PARAMETERS FOR ON-RESISTANCE MODELING

| Notation | Definition | Value | Unit |
|---|---|---|---|
| ***rs*** | Parasitic source resistance | 0.01715 | Ω |
| ***rd*** | Constant drain resistance for forward conduction | 0.0104 | Ω |
| ***rdr*** | Constant drain resistance for reverse conduction | 0.0054 | Ω |
| ***RDVD*** | Drain-dependency parameter of the drift resistance | 0.00085 | $A^{-1}$ |
| ***RDVG1*** | First gate-dependency parameter of the drift resistance | 1.797 | Ω |
| ***RDVG2*** | Second gate-dependency parameter of the drift resistance | 999.9 | $V^{-1}$ |

$R_d$, on the other hand, is viewed as a summation of three components: a constant part, resistance in the undepleted accumulation region ($R_A$), and junction field effect transistor (JFET) region resistance ($R_{jfet}$). The drain contact resistance and the resistance of the highly doped substrate are constant (***rd***). $R_A$ depends on *Vds*-induced depletion region and is modeled by (12)–(14). Here, (12) expresses the drain-to-source depletion thickness ($W_{dep}$) in the forward bias condition. $W_a$ in (13) represents the effective accumulation layer width. Symbols *e* and $\mu_e$ stand for the electron charge and bulk electron mobility, respectively. The JFET region's resistance has been modeled using the empirical relation of (15) described in [18]. Since the high-current region is dominated by the body diode characteristics in the third quadrant, $R_{jfet}$ and $R_A$ can be neglected using a different constant drain resistance (***rdr***). Table II lists the parameters for ON-resistance modeling.

$$R_{df} = \boldsymbol{rd} + R_A + R_{jfet} \tag{10}$$

$$R_{dr} = \boldsymbol{rdr} \tag{11}$$

$$W_{dep} = \sqrt{2 \cdot \varepsilon_{sic} \cdot \frac{vds_f}{e \cdot nd}} \tag{12}$$

$$W_a = \boldsymbol{wb} - W_{dep} \tag{13}$$

$$R_A = \frac{W_a}{e \cdot \boldsymbol{a} \cdot \boldsymbol{nb} \cdot \mu_e} \tag{14}$$

$$R_{jfet} = (Vds_f \cdot \boldsymbol{RDVD}) \cdot \left(1 + \boldsymbol{RDVG}1 + \frac{\boldsymbol{RDVG}1}{\boldsymbol{RDVG}2} \cdot Vgs\right). \tag{15}$$

### C. Body Diode Modeling

In the power MOSFET structure, the n+ source and p-type body are shorted physically and electrically to suppress the parasitic n-p-n BJT. As a result, a p-i-n diode structure is formed, such as it is connected in an antiparallel configuration across the MOSFET conduction path. This inherent diode structure is called the body diode. When the voltage drop across the p-body and n-drift junction is greater than the turn-ON voltage ($V_f$), the body diode turns ON in the third quadrant. The diode current starts to flow through this low-resistive path. So, the body diode characteristics dominate in the high-voltage region of the third quadrant. For *Vgs* less than the threshold voltage of the MOSFET path, there is no inversion layer in the channel region. Thus, the body diode is the only path for current flow. Body diode conduction starts when $Vsd > V_f$. Here, $V_f$ is a function of gate voltage *Vgs*. This dependency is explained as the increase in the potential barrier between the p-type body and n-drift junction due to the negative gate bias [19], [20]. The potential at the drift region under the gate oxide, also known as the JFET region, remains close to zero when $Vgs = 0$ V. An accumulation layer forms under the gate with increasingly positive gate voltage. This accumulation layer reduces the potential barrier of the junction between the body and drift region and, thus, reduces the turn-ON voltage of the diode [19]. The maximum positive gate voltage for which this accumulation layer dominates the conduction is ***vk1***. ***vk1*** is a model parameter of this model and termed as the positive knee gate voltage. In the accumulation layer's presence, the injection efficiency changes from theoretical SiC p-i-n configuration and becomes gate dependent. The presented model expresses this phenomenon as a change in the ideality factor [21]. The constant part of the ideality factor (***ND***) is a parameter of the model. The gate dependency of the body diode's injection efficiency is modeled using (16)–(21) by the modification of the ideality factor ($ND_1$). Equation (16) makes the expression for the voltage across the body diode ($V_{bdiode}$) continuous across the first and third quadrant removing the need for conditional expressions. However, (17) is the expression for the effective gate-to-source voltage for the body diode ($V_{gsnreff_vk1}$) modified by ***vk1***. Here, $t_1$, $t_2$, and $t_{mp1}$ are the intermediary terms of the calculation and $V_T$ is the thermal voltage

$$V_{bdiodeff} = V_{bdiode} - \frac{1}{2}\left(V_{bdiode} + \sqrt{V_{bdiode}^2 + 4\boldsymbol{\partial}^2}\right) \tag{16}$$

$$V_{gsnreff_vk1} = (Vgs - \boldsymbol{vk}1) - \frac{1}{2}\left((Vgs - \boldsymbol{vk}1) + \sqrt{(Vgs - \boldsymbol{vk}1)^2 + 4\boldsymbol{\partial}^2}\right) \tag{17}$$

$$t_1 = -\boldsymbol{kvsg}_1 \cdot V_{gsnreff_vk1} \tag{18}$$

$$t_2 = t_1 \text{ if } t_1 > 0, \quad \text{else } t_2 = \frac{-t_1}{2t_1 - 1} \tag{19}$$

$$N\,D_1 = \boldsymbol{ND} + t_2 \tag{20}$$

$$t_{mp1} = e^{\frac{-V_{bdiodeff}}{Nd_1 * V_T}}. \tag{21}$$

The negative gate bias creates a depletion layer in the JFET region, and the depletion layer extends with increasing negative gate bias. As a result, the potential barrier increases, and so the $V_f$ increases as well. After a certain negative gate bias, the potential barrier reaches its maximum and remains practically the same for more negative gate voltages [19]. We see the effect in the third-quadrant output characteristics with very tightly packed curves for $Vgs < $ ***vk2***. In the presented model, ***vk2*** is a model

TABLE III
PARAMETERS FOR BODY DIODE AND REVERSE RECOVERY MODELING

| Notation | Definition | Value | Unit |
|---|---|---|---|
| ***Isbody*** | Diode saturation current | 1E-10 | A |
| ***vk1*** | Positive knee gate voltage | 3.614 | V |
| ***vk2*** | Negative knee gate voltage | 3.847 | V |
| ***kvsg₁*** | Gate dependent body diode gain factor | 0.4523 | $V^{-1}$ |
| ***kvsg₂*** | Gate dependent body diode gain factor for negative gate voltages | 0.7906 | V |
| ***ND*** | Body diode ideality factor | 1.582 | - |
| ***rdiode*** | Series resistance of the body diode | 0.05628 | Ω |
| ***τ*** | Lifetime of the minority carriers in the drift region | 20E-09 | second |
| ***TT*** | Diffusion transit time | 4E-10 | $\text{second}^{-1}$ |

parameter, and it is termed as the negative knee gate voltage. Gate voltages lower than ***vk2*** show no additional effect on the body diode characteristics. The presence of the electric field along the body diode junction controls the overall injected carriers through it. Hence, this gate dependency is modeled as a multiplier of the body diode saturation current (***Isbody***) and expressed with (22)–(26).

Here, (26) is the total body diode current ($I_{bdiode}$) expression. $V_{gsnreff_vk2}$ is the effective gate voltage smoothed out for $Vgs <$ ***vk2,*** and $t_3$, $t_4$, and $t_{mp2}$ are the intermediary terms of the overall equation. The body diode is situated in the junction between the p-body and n- drift region. The lightly doped body region has its own resistance and is modeled by a series resistance parameter ***rdiode***. Table III lists the parameters for body diode and reverse recovery modeling.

$$V_{gsnreff_vk2} = (Vgs - \boldsymbol{vk}2) - \frac{1}{2}\left((Vgs + \boldsymbol{vk}2) + \sqrt{(Vgs + \boldsymbol{vk}2)^2 + 4\boldsymbol{\partial}^2}\right) \quad (22)$$

$$t_3 = -\frac{V_{gsnr_{eff_vk2}}}{\boldsymbol{kvsg}_2} \quad (23)$$

$$t_4 = t_3 \text{ if } t_3 > 0, \quad \text{else } t_4 = \frac{-t_3}{2t_3 - 1} \quad (24)$$

$$t_{mp2} = e^{-t_4} \quad (25)$$

$$I_{bdiode} = \frac{\boldsymbol{Isbody}}{t_{mp2}} \cdot (t_{mp1} - 1). \quad (26)$$

## D. Reverse Recovery Modeling

The reverse recovery current has been modeled based on the article presented in [22]. In this approach, a virtual node $Q_m$ is added, representing the total stored charge in the drift region. The total injected charge ($Q_{e1}$) into the drift region is proportional to the body diode current ($I_{bdiode}$), as expressed in (27). The amount of charge recombined is expressed as ($Q_{e1}$ - $Q_m$), and (28) expresses the relation between the recombination current ($I_m$) with the recombined charge. $Q'_{m1}$ stands for the stored charge before recombination and $Q_{m1}$ stands for the stored charge after recombination in each time step. Equations (28) and (29) are iteratively solved for the reverse recovery current. This approach is computationally expensive due to iteration. There are two parameters associated with the reverse recovery. First is the $\tau$ associated with the carrier lifetime, and ***TT*** is associated with the total transit time.

$$Q_{e1} = \boldsymbol{\tau} \cdot I_{bdiode} \quad (27)$$

$$I_m = (Q_{e1} - Q_{m1})/\boldsymbol{TT} \quad (28)$$

$$Q_{m1} = \boldsymbol{\tau} \cdot \left(I_m - \frac{d}{dt} Q'_{m1}\right). \quad (29)$$

Inclusion of the body diode and reverse recovery makes it necessary to ensure the model's convergence and efficiency. Hence, the first- and the third-quadrant characteristics are decoupled with separate continuous equations instead of piecewise equations. So, different weighted effective values of the voltage biases are used for the first and third quadrants. Equations (4), (16), (17), and (22) express the decoupling technique. With this approach, the first- and third-quadrant equations remain continuous without affecting the opposite part. The same weighted function approach of decoupling is also applied for other piecewise equations in the model.

## E. Parasitic Capacitance Modeling

Dynamic characteristics of the power MOSFET rely primarily on internal parasitic capacitances. The expressions for these internal capacitances are modified from the articles presented in [5] and [6]. The gate-to-source capacitance is expressed as a constant parameter (***cgs***). The total charge stored in the gate–source capacitor ($Qgs$) is expressed in terms of the constant gate–source capacitance (***cgs***), as follows:

$$Qgs = \boldsymbol{cgs} \cdot Vgs. \quad (30)$$

The drain-to-source capacitance (*Cds*) is voltage dependent. It varies with the thickness of the depletion layer in the drift–body junction. This capacitance is modeled by the junction capacitance of the body diode, as shown in the following equations. Instead of piecewise equations, such as the article presented in [6], for negative and positive bias, continuous equations are used for modeling the total charge stored in the drain–source capacitor (*Qds)* by weighted voltages ($V_{bdiodefp}$, $V_{bdiodefn}$). $Qds_n$ and $Qds_p$ stand for the drain–source charge corresponding to the constant and bias-dependent part of *Cds,* respectively. Here, *k* is Boltzmann's constant, $n_i$ is the intrinsic carrier concentration of SiC, and *Vbi* is the junction's built-in potential

$$Qds = Qds_n + Qds_p \quad (31)$$

$$Q\,ds_n = \boldsymbol{cds} \cdot V_{bdiodefn} \quad (32)$$

$$Q\,ds_p = \boldsymbol{cds} \cdot Vbi^m \cdot \frac{(Vbi + V_{bdiodefp})^{1-\boldsymbol{m}} - Vbi^{\boldsymbol{m}}}{1 - \boldsymbol{m}} \quad (33)$$

$$Vbi = \frac{kT}{e} \ln\left(\frac{\boldsymbol{nb} \cdot 10^{16}}{n_i^2}\right). \quad (34)$$

TABLE IV
PARAMETERS FOR CAPACITANCE MODELING

| Notation | Definition | Value | Unit |
|---|---|---|---|
| ***cgs*** | Gate to source capacitance | 1.469E-9 | F |
| ***cds*** | Drain to source initial capacitance | 1.611E-9 | F |
| ***coxd*** | Oxide capacitance | 1.0E-9 | F |
| ***vtd*** | Gate drain overlap depletion threshold voltage | 0.001 | V |
| ***m*** | Junction grading coefficient | 0.98 | - |
| ***nb*** | Drift region doping concentration | 8.598E17 | $cm^{-3}$ |
| ***wb*** | Metallurgical drift region width | 0.00015 | µm |
| ***a*** | Device active area | 0.1667 | $µm^2$ |
| ***agd*** | Gate length overlap active area | 9.88E-05 | $µm^2$ |

The gate–drain capacitance (*Cgd*) consists of gate-oxide capacitance (***cox***) and gate–drain overlap depletion capacitance (*Cgdj*). For *Vgd* less than the depletion threshold voltage (***vtd***), this capacitance is equal to oxide capacitance (***coxd***). For *Vgd* greater than ***vtd***, the total capacitance becomes a series combination of ***coxd*** and *Cgdj*. This relation is captured in the model with (35)–(40). The presented model has smoothed these expressions to improve the convergence and efficiency using the weighted function of the drain-to-gate voltage (*Vdg*) in (41) and (42). Table IV lists the parameters for parasitic capacitance modeling.

$$Qgd = Qgd_n + Qgd_p \tag{35}$$

$$Qgd_n = \ Vdgeffn \cdot \boldsymbol{coxd} \tag{36}$$

$$Qgd_p = \ Vdgeffp \cdot Cgd \tag{37}$$

$$C_{gd} = \frac{\boldsymbol{coxd} \cdot Cgdj}{\boldsymbol{coxd} + Cgdj} \tag{38}$$

$$Cgdj = \varepsilon_{sic} \cdot \frac{\boldsymbol{agd}}{wgdj} \tag{39}$$

$$wgdj = \sqrt{2 \cdot \ \varepsilon_{sic} \cdot \ \frac{Vdgeffp}{q \cdot nb}} \tag{40}$$

$$Vdgeffp = \frac{1}{2}\left((Vdg + \boldsymbol{vtd}) + \sqrt{(Vdg + \boldsymbol{vtd})^2 + 4\boldsymbol{\partial}^2}\right) \tag{41}$$

$$Vdgeffn = (Vdg + \boldsymbol{vtd}) - -Vdgeffp. \tag{42}$$

## III. Parameter Extraction

For any compact model, there should be a well-defined parameter extraction process. It allows the users to extract the model parameters from the available sets of data and use the extracted model to accurately predict the intended circuit designs. The parameter extraction procedure, as described in [6], is a straightforward yet accurate way to extract model parameters from the data available in the datasheet. This article follows the same approach.

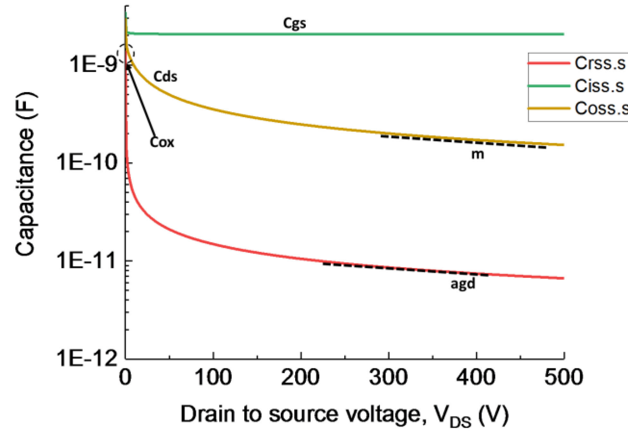


Fig. 4. Capacitance-related parameters extraction procedure [6].

In the authors' experience, many datasheets provide mismatched transfer and dc output curves. This means that the drain current magnitudes do not correspond to the same drain and gate biases in the transfer curve and the dc output curves. If the transfer and dc output curves correspond, then the extraction procedure in [6] can be followed for the parameter extraction of the first quadrant. Otherwise, it will be easier for users to rely on the dc output characteristics. The modified extraction procedure presented in this article relies solely on the dc output characteristics to extract the static *I–V* parameters to give the users an alternative.

Here, a 1200 V, 80 mΩ SiC MOSFET from Wolfspeed (C2M0080120D) is selected to extract the model parameters. Due to the availability of Keysight B1505A curve tracers, the measured data are used for the extraction. However, these data are also commonly available in datasheets. Before extracting the dc characteristics, the parameters related to parasitic capacitances need to be extracted. Since the *C–V* modeling has not been changed except making the equations used in [6] continuous, the process, as described in [11], is followed to extract these parameters. Fig. 4 shows the specific parts of the *C–V* curves, where the shown parameters play the most important role, and hence, those parameters can be extracted from curve fitting those places in the *C–V* curve. More details can be found in [6].

After extracting the capacitance-related parameters, the remaining parameters are extracted from *I–V* characteristics. If not specified, otherwise all these parameters are extracted by curve fitting the model with the measured results. The parameter extraction tools, such as IC-CAP, can be a good resource. The curve fitting functions in MATLAB or Python can also be used. The first parameter to be extracted is $\boldsymbol{V_{thlf}}$. In the output curves, the gate voltage value for the lowest curve (usually in the range of 2–5 V) is the closest to the value of $\boldsymbol{V_{thlf}}$. So, extract the $\boldsymbol{V_{thlf}}$ value by curve fitting the *Ids–Vds* curve for the lowest gate voltage. $\boldsymbol{k_{plf}}$ is the saturation transconductance parameter for low *Vgs* curves. Here, low-gate voltage means $Vgs <$ Miller voltage

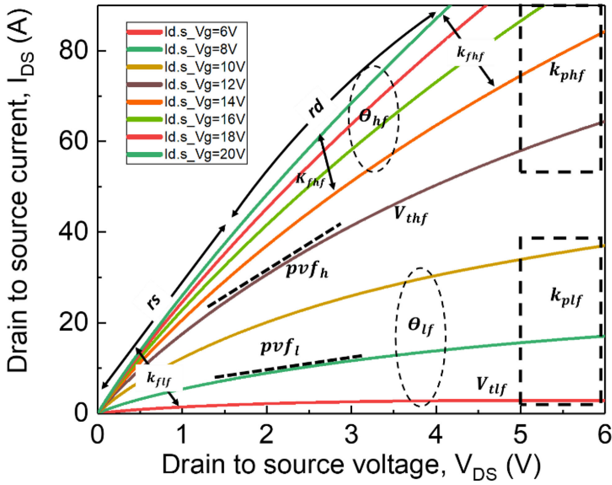


Fig. 5. First-quadrant-related parameters extraction from the output curves.

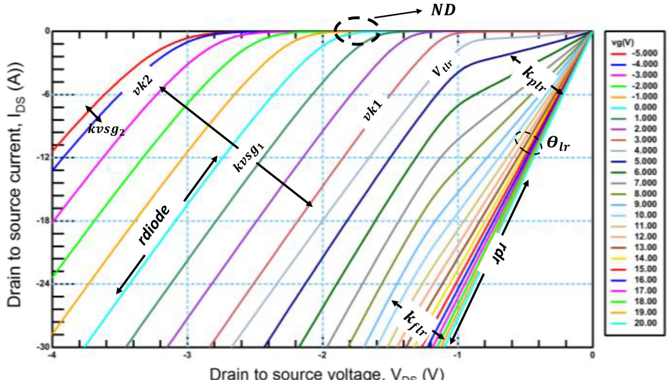


Fig. 6. Third-quadrant-related parameter extraction from the output curves.

($V_{miller}$). $V_{miller}$ value can be obtained from the datasheet or gate-charge plot. In the case of C2M0080120D, it is about 8.6 V. $\boldsymbol{k_{plf}}$ is extracted by fitting the saturation region of these low-gate voltage *Ids–Vds* curves. $\boldsymbol{k_{flf}}$ is used to fit the triode region of the low-gate voltage curves. $\boldsymbol{\theta_{lf}}$ is the transverse electric field parameter and is used to fit the *Id–Vds* curves' compression at the low-gate voltages.

$\boldsymbol{V_{thhf}}$ is the high-current threshold voltage. The value is obtained by matching the first curve at the *Ids–Vds* plot where $Vgs > V_{miller}$. The transconductance of the higher $Vgs$ curves is tuned using parameters $\boldsymbol{k_{phf}}$ and $\boldsymbol{k_{fhf}}$ for saturation and triode region, respectively. Reduction in the mobility at the high transverse gate field is tuned using the parameter $\boldsymbol{\theta_{hf}}$. Series drain resistance parameter ***rd*** is used to control the bending of the curves at high-gate voltages. In contrast, ***rs*** is used to fit the slope of the curves. All these parameters are extracted by curve fitting the dc output curves, as shown in Fig. 5. The difference in the slopes of the curves for higher gate voltages can be adjusted using voltage-dependent drift-resistance parameters ***RDVD***, ***RDVG1***, and ***RDVG2***.

Due to the presence of a large number of interface charges and their gradual emptying, the transition between the triode and saturation region is gradual in SiC MOSFET compared with its Si counterpart. This transition is tuned using pinch-off voltage parameters ($\boldsymbol{pvf_l}$, $\boldsymbol{pvf_h}$), as shown in Fig. 5. The lateral electric field generated by the interface charges influences the carrier velocity at the channel. So, carrier velocity saturates gradually in the presence of interface charge [23]. The extent of the velocity saturation depends on the gate voltage since the occupation of interface states with carriers is gate voltage dependent. Hence, the low-gate voltage region and the high-gate voltage region need separate parameters for the accurate fitting.

After extracting parameters related to the first-quadrant characteristics, the third-quadrant-related parameters are extracted. Fig. 6 shows the third quadrant of the output characteristics and highlights the particular regions where each parameter plays the most dominant role. $\boldsymbol{V_{thlr}}$, $\boldsymbol{V_{thhr}}$, $\boldsymbol{k_{plr}}$,$\boldsymbol{k_{phr}}$, $\boldsymbol{k_{flr}}$, $\boldsymbol{k_{fhr}}$, and ***rdr*** are initially assigned to the same values of their first-quadrant counterparts. These values should be fine tuned to match their respective area in the third-quadrant characteristics where the MOSFET channel current dominates, i.e., $Vsd < V_f$, in this case, about 1.8 V.

The body diode ideality factor (**ND**) is tuned to fit the turn-ON voltage for the curve of $Vgs = 0$ V. Parameter ***vk2*** is fixed to the magnitude of the negative gate voltage value after which the body diode transconductance saturates due to depletion. This means that the effect of the gate voltage remains almost the same. The gate voltage dependency of the body diode for $Vgs < \boldsymbol{vk2}$ is controlled using the parameter $\boldsymbol{kvsg_2}$. The value of the parameter ***vk1*** is assigned to the highest positive gate voltage for which only the body diode characteristics dominate, i.e., for $Vgs < \boldsymbol{vk1}$, the MOSFET characteristics are negligible due to the absence of the inversion channel layer. Parameter $\boldsymbol{kvsg_1}$ is tuned to fix the spacing between these curves where the body diode characteristics dominate. Parameter ***rdiode*** is fine tuned to fix the slope of the body diode curves. The curves for $Vgs > \boldsymbol{V_{thlr}}$ show both diode and MOSFET characteristics. So, the value of $\boldsymbol{V_{thlr}}$ is tuned to match the first curve that shows these two characteristics. The MOSFET characteristics dominate in the low-current region and diode characteristics in the high-current region. ***kplr*** is tuned to match the transconductance of the MOSFET characteristics. $\boldsymbol{\theta_{lr}}$ is tuned to match the spacing between these curves. $\boldsymbol{k_{flr}}$ needs to be adjusted to fit the slopes of the MOSFET characteristics' curves. Finally, if the value of $\boldsymbol{rdr} = \boldsymbol{rd}$ is too large to fit the slope of the MOSFET characteristics' curves, the reduction of ***rdr***'s value will give a perfect fit. The overall optimization of the third-quadrant parameters is required to get the best fit.

Once the *C–V* and static parameters have been extracted, the reverse recovery parameters ***TT*** and $\tau$ can be extracted. $\tau$ is the lifetime of the minority carriers in the drift region, and ***TT*** is the diffusion transit time of the stored charge [22]. $\boldsymbol{\tau}$ allows user to fit the peak reverse recovery current. ***TT*** is to be adjusted to get the total reverse recovery time. The fitting regions of these two parameters are highlighted in Fig. 7. The values of peak reverse recovery current and total reverse recovery time can be found from the datasheet. However, a simulation setup, as shown in Fig. 8, can be simulated with the given condition in the datasheet to get a visual representation of the parameters.

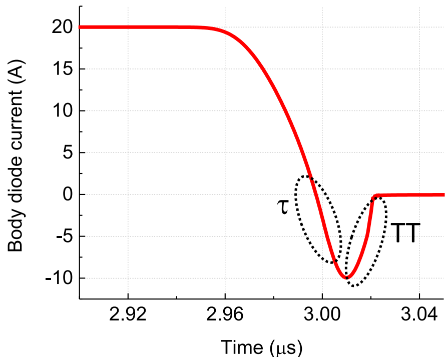


Fig. 7. Reverse recovery related parameter extraction.

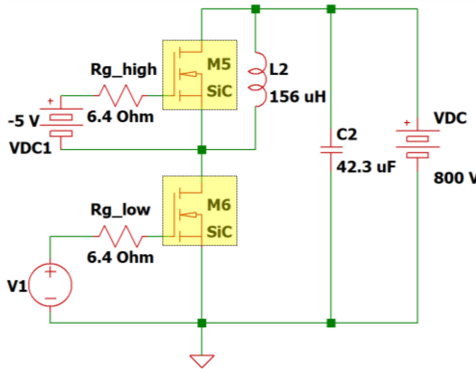


Fig. 8. Body diode reverse recovery test circuit from the datasheet of C2M008120D.

Once the parameters related to reverse recovery have been extracted, the users need to revisit the fit of *C–V* and third-quadrant *I–V* characteristics and optimize the third-quarter transconductance parameters. Fig. 9 shows a flowchart depicting this parameter extraction flow.

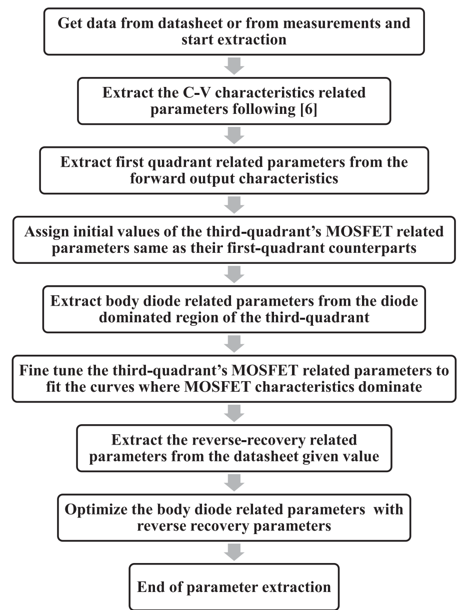


Fig. 9. Parameter extraction flow.

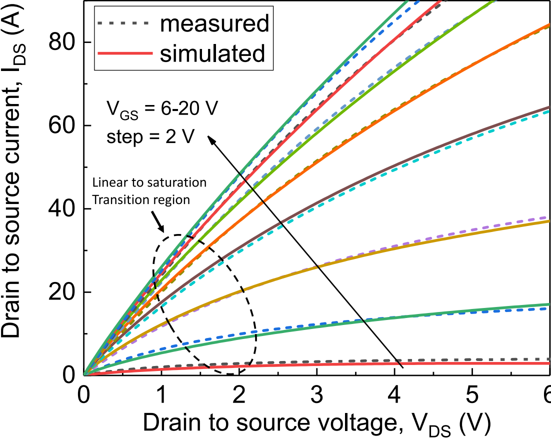


Fig. 10. Simulated with the presented model (solid line) and measured (dash line) first-quadrant output characteristics of C2M0080120D.

## IV. Model Validation

Following the parameter extraction procedure, as described in Section III, the accurate fit of the output characteristics in both the quadrants and the *C–V* characteristics are achieved. The fit of the model with the measured data is shown in the following figures. Fig. 10 shows the fit of the simulated results (solid lines) of the presented model with the measured data (dash line) in the first-quadrant characteristics. The simulated results match very closely with the measured data. For comparison, the fit of the previous model [6] upon which this model has been built is shown in Fig. 11. Both models share the fundamental equations, as mentioned before, and so the accuracy is very close in the first-quadrant operation. However, due to having two pinch-off voltage parameters ($\boldsymbol{pvf_l}$, $\boldsymbol{pvf_h}$), the presented model can accurately fit all the linear to saturation transition regions more closely than the previous model [6].

Fig. 12 shows the fit of the presented model's third-quadrant characteristics with the measured data. With the gate-bias-dependent body diode and MOSFET characteristics, the presented model can accurately fit the third quadrant with any gate bias, unlike any previous SiC power MOSFET model. Many previous models, the article presented in [6] for example, have symmetric first- and third-quadrant output characteristics for $Vgs > |V_{threshold}|$. As explained before in Section II, the first- and the third-quadrant MOSFET characteristics are not the same. Consequently, those models cannot accurately fit the MOSFET characteristics in the third quadrant for $Vgs > |V_{threshold}|$, as shown in Fig. 13 . The presented model can fit the third-quadrant MOSFET characteristics with less than 0.2% error [see Fig. 13(a)], while the model of the article presented in [6] has an error of around 9% [see Fig. 13(b)]. This is important for the simulation of applications where MOSFET's third-quadrant characteristics are used, such as synchronous rectifiers. There will be an error of around 9% only in the conduction loss calculation, even

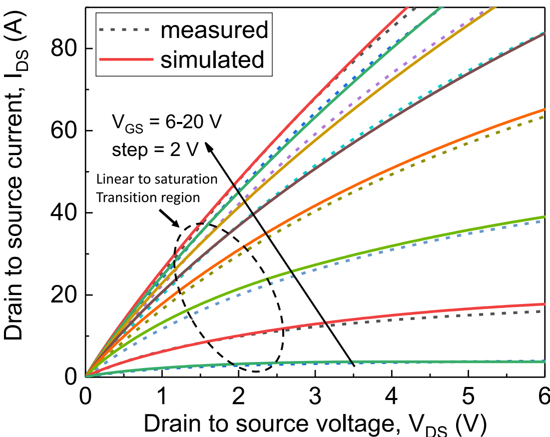


Fig. 11. Simulated with the previous model of the article presented in [6] (solid line) and measured (dash line) first-quadrant output characteristics of C2M0080120D.

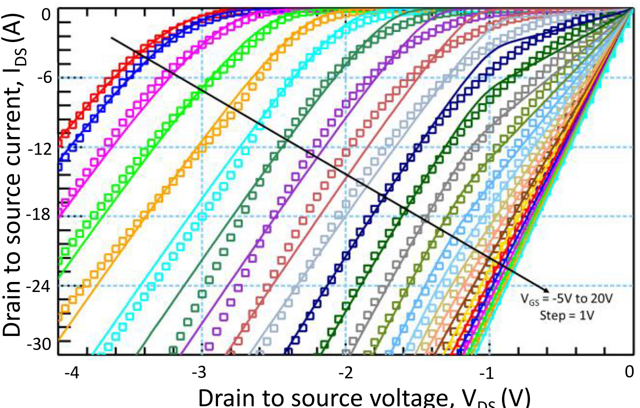


Fig. 12. Simulated with the presented model (solid line) and measured (symbols) third-quadrant output characteristics of C2M0080120D.

if the switching loss mismatch due to reverse recovery is not considered.

In the case of the body diode, the accurate gate-dependency modeling is important for calculating the diode's conduction loss. In most circuit applications, the MOSFET is either biased to −5 V or 0 V to make it article as a freewheeling diode. A separate diode model can be used for the simulation by fitting the diode characteristics for a particular gate voltage. However, this approach cannot predict the body diode's behavior when there is a gate ringing due to the high *di/dt* and *dv/dt* of the switching device or any parasitic coupling. So, for the accurate simulation at the high-frequency applications ($\geq$ 100 kHz), the body diode's gate-dependency modeling is required. An example can be electromagnetic interference simulation, as described in [24]. Fig. 14 shows the fit of simulated CV characteristics with the measured results.

Apart from the fitting during the parameter extraction, the extracted parameter set correctly fits the measured transfer curve at $Vds = 10$ V, as shown in Fig. 15. The static characteristics' accuracy is further verified by the close fit of the simulated $Rds$(on) with the measured data. Fig. 16 shows the fit of $Rds$(on) at $Vgs = 20$ V.

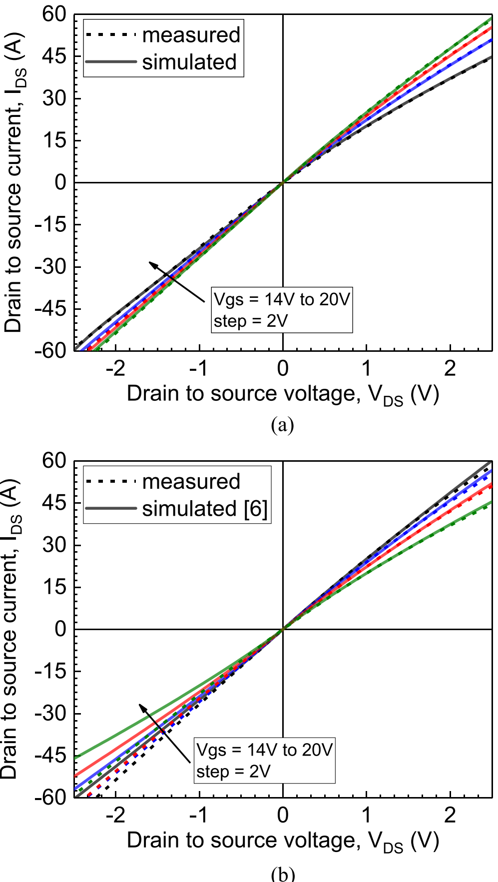


Fig. 13. Comparison with the measured asymmetric output characteristics at the first and third quadrant with the simulated results of (a) presented model and (b) model of the article presented in [6].

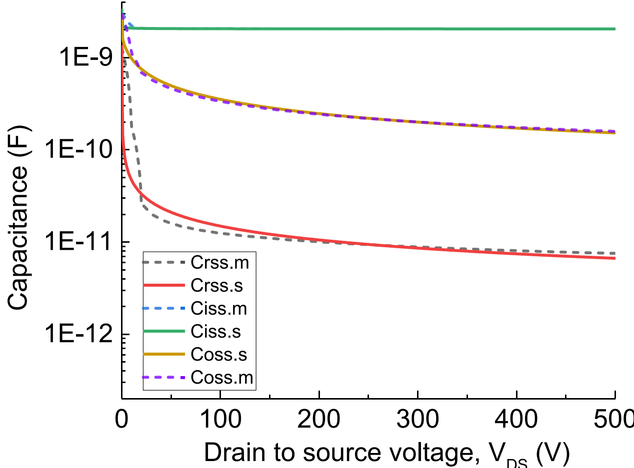


Fig. 14. Fit of the model simulation results with the measured data for the capacitance–voltage characteristics of C2M0080120D at 100 kHz.

The validation of the model's dynamic performance is performed with a 700 V, 26 A double-pulse test (DPT) bench. A commercially available SiC MOSFET DPT fixture from CREE [25] is used for performing the test. C2M0080120Ds are used both as the high-side and low-side device. As a result, dynamic

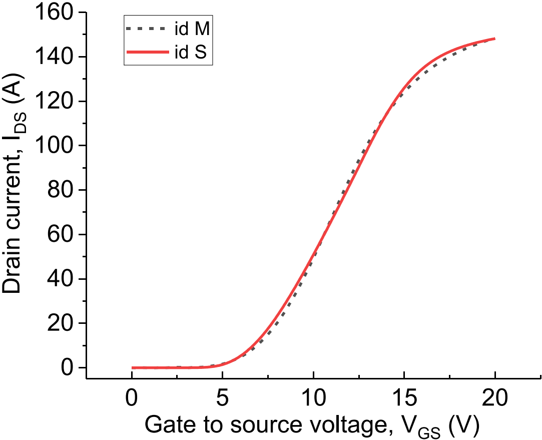


Fig. 15. Measured and simulated transfer characteristics of C2M0080120D.

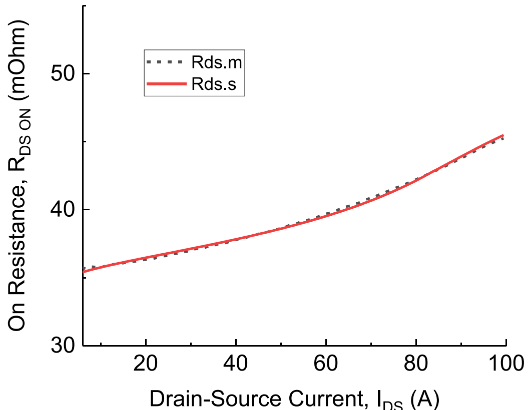


Fig. 16. Measured and simulated $Rds_{(\mathrm{on})}$ at $Vgs = 20$ V of C2M0080120D.

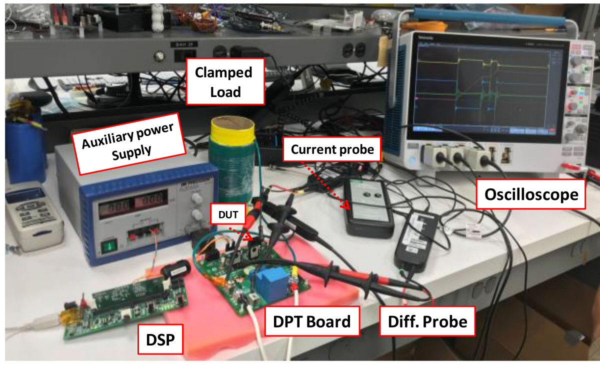


Fig. 17. Test setup for DPT.

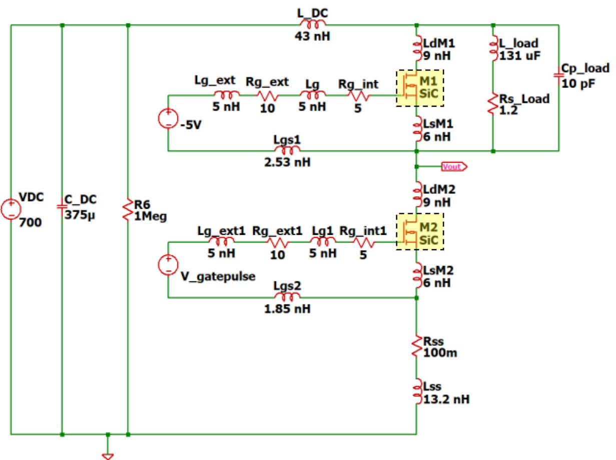


Fig. 18. Schematic of the DPT bench for model verification.

switching performance also relied on the body diode characteristics of the device. For performing the dynamic characterization and recording switching waveforms, a six-channel 05 series MSO Tektronix oscilloscope of 6.25 GS/s sampling rate and 2 GHz bandwidth oscilloscope has been used. The device voltage has been measured using 200 MHz 1.5-kV rated Tektronix differential probes. The device current is measured using a Rogowski coil with a bandwidth of 20 MHz. Although possessing limited bandwidth, the Rogowski coil was chosen because of its flexibility in converters with compact designs. As we progress to an electrothermal model and validation in a converter study, this aspect will remain consistent. The entire test setup is shown in Fig. 17.

The overall test bench is depicted in the simplified circuit schematic of Fig. 18. The shaded part indicates the modeled device, including the parasitic capacitances and body diode. The parasitics of the test board are extracted using Q3D.

The high-side device's body diode is working as a freewheeling diode. It is connected in parallel with the load inductor. The hand-made air-core inductor is represented by a parallel-connected *LCR* model from the measured impedance data. The gate driver is simplified using a pulse voltage source, external gate resistance, and parasitic gate-loop inductance. Internal gate resistances are measured using Keysight B1505A. Package inductances are lumped with the external inductances to form the drain, source, and gate terminal inductances for the top- and low-side devices.

Apart from validating the presented model, a comparison in dynamic performance with a previous model [6] is also presented here. The presented model includes body diode characteristics with reverse recovery. If the parameter extraction procedure is followed, no external diode model is required for simulation where the body diode works as the freewheeling diode. But for the model, as described in [6], a separate diode model needs to be fit with the body diode characteristics to simulate freewheeling. A SPICE diode model is fit to the *I–V* curve of the body diode for $Vgs =$ -5 V. The disadvantage of this approach is that the diode model needs to be refit if the gate bias changes. So, the effects of gate ringing in the high-side device will not be captured accurately. The junction capacitance of the SPICE diode model is fitted with the *Coss* characteristics of the body diode.

Figs. 19–21 show the accuracy of simulated *Vgs, Vds,* and *Ids* switching curves to predict the measured results for turn-ON and turn-OFF. The simulated results from the presented model are labeled as "simulated_new," while the simulated results from the article presented in [6] are labeled as "simulated_old."

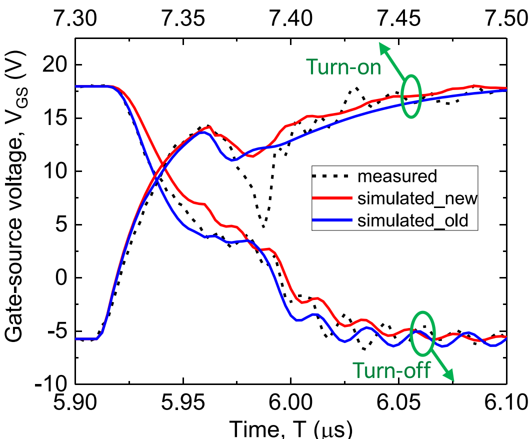


Fig. 19. Turn-ON (top $x$-axis) and turn-OFF (bottom $x$-axis) transient of the gate voltage.

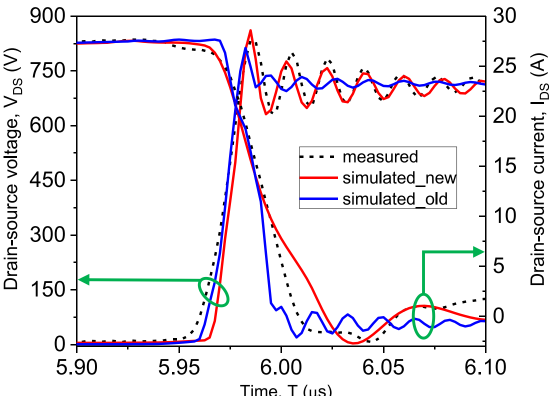


Fig. 20. Turn-OFF transient of the drain voltage and drain current.

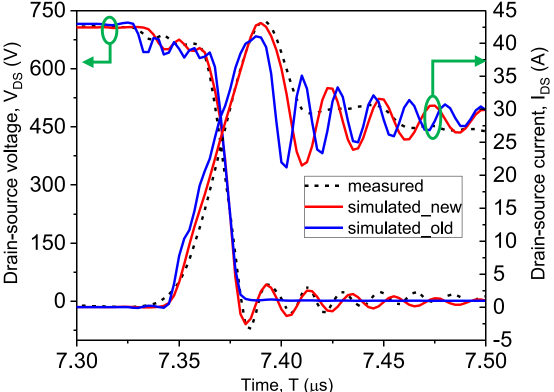


Fig. 21. Turn-ON transient of the drain voltage and drain current.

Turn-OFF *Vgs* in Fig. 19 shows the accurate fit between the measured and simulated waveforms. Both the new and the old model fit closely with the measured result. The old model of the article presented in [6] has a lower threshold voltage ($V_{thl}$) value extracted from the transfer curve. For turn-ON, the measured and simulated results also show a good fit except for one deep downward spike visible at $t = 7.38$ $\mu$s (top $x$-axis). Although the spike is not perfectly matched, both models can predict the trend. Both models match the gate voltage's rise time and initial peak and then the downward notch. This is an SiC MOSFET characteristic due to the gradual transition of linear to saturation region. Having two pinch-off parameters ($pvf_l$, $pvf_h$), the new model can fit the characteristics better as compared with the old model [6], which has only one pinch-off parameter. The reverse recovery of the freewheeling diode plays a role in the negative spike [26]. The "V-shape" spike is a bit more prominent in the presented new model, which has reverse recovery. The negative spike could be more accurately fit if the body diode's reverse recovery parameters were extracted from the measured data instead of using the datasheet value.

Fig. 20 shows the turn-OFF transient characteristics of the drain voltage (*Vds*) and the drain current (*Ids*). In *Vds* waveform, the presented model's turn-OFF simulated result matches very closely with the simulated result, even for several oscillations. Matching of the overshoot and the oscillation frequency validates the *Coss* modeling. Having the same *C–V* modeling approach, the simulated result from the article presented in [6] gives almost the same oscillation frequency. However, due to the lack of reverse recovery, the simulated result of the article presented in [6] does not match the overshoot magnitude properly, unlike the presented model. There is a slight mismatch in the rise time (at $t = 5.95$ $\mu$s) between the measured and simulated waveform of the new model. This small mismatch could be caused by the slightly incorrect extraction of the threshold voltage parameters extracted from the output characteristics alone. In the previous model of the article presented in [6], this mismatch is less as the threshold voltage value is extracted from the transfer curve. A slight mismatch in the turn-OFF *Ids* plot at $t = 6$ $\mu$s is due to the reversible threshold voltage hysteresis in the SiC power MOSFET. This reversible threshold voltage hysteresis is caused by the interface states in the gate oxide [27] and cannot be predicted from the device's static characteristics.

Fig. 21 shows the turn-ON transient characteristics of the drain voltage (*Vds*) and the drain current (*Ids*). The simulated *Vds* waveforms match accurately with the measured waveform. The simulated *Ids* curves also show the accurate fit with the measured result. Overshoot oscillation in the measured result is not prominent due to the relative low bandwidth of the Rogowski coil. Still, the new model, having reverse recovery current characteristics, is more accurate in predicting the overshoot magnitude than the model of the article presented in [6].

Based on the DPT results, the calculated turn-ON switching energy ($E_{\text{on}}$) and the turn-OFF switching energy ($E_{\text{off}}$) are given in Table V. Due to the low-bandwidth Rogowski coil, the measured switching loss is higher than expected. The presented model shows less error (9.04%) compared with the old model [6] (15.51%) in predicting the total switching loss for the case, as shown in Figs. 19–21.

Table V also includes the switching energy losses at different drain voltages and currents. From the table, it can be seen that the new model has better accuracy than the old model, especially at the higher drain currents. This is because the higher *di/dt* increases the reverse recovery loss in the body diode. This

TABLE V
SWITCHING LOSS COMPARISON

| Switching Voltage / Current | Results | Turn-off Switching Energy $E_{off}$($\mu$J) | Turn-on Switching Energy $E_{on}$($\mu$J) | Total Error (%) |
|---|---|---|---|---|
| 700 V / 26 A | Measured | 194 | 702 | - |
| | New model | 153 | 662 | 9.04 |
| | Old model [6] | 144 | 613 | 15.51 |
| 450 V / 30 A | Measured | 121.1 | 452.9 | - |
| | New model | 94.49 | 386.6 | 16.30 |
| | Old model [6] | 90.3 | 345.1 | 24.14 |
| 300 V / 20 A | Measured | 44.84 | 134.8 | - |
| | New model | 44.2 | 123.1 | 6.80 |
| | Old model [6] | 39.07 | 117.2 | 13.0 |
| 100 V / 10 A | Measured | 22.88 | 46.52 | - |
| | New model | 21.7 | 43.23 | 6.44 |
| | Old model [6] | 19.93 | 41.33 | 11.72 |

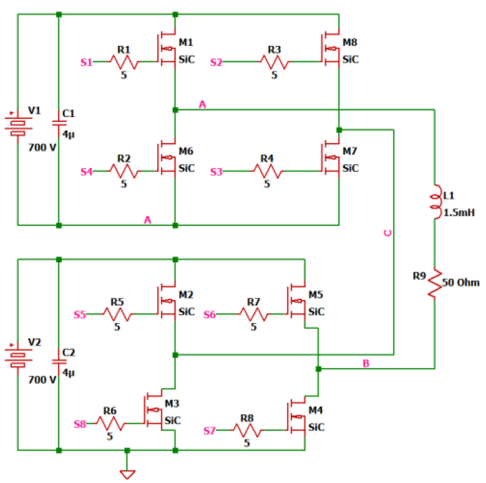


Fig. 22. Topology of the simulated CHB-MLI.

validates the utility of the presented model for the accurate circuit simulation.

## V. CONVERGENCE EVALUATION STUDY

Due to the increasing high-frequency high-power applications of wide bandgap power devices, it is necessary to ensure that the developed compact model shows good convergence behavior in complex circuit topologies. The developed model's convergence capability is first tested using a five-level CHB-MLI topology. Fig. 22 shows the topology of the inverter. A total of eight devices, including their inherent body diodes, are used in the

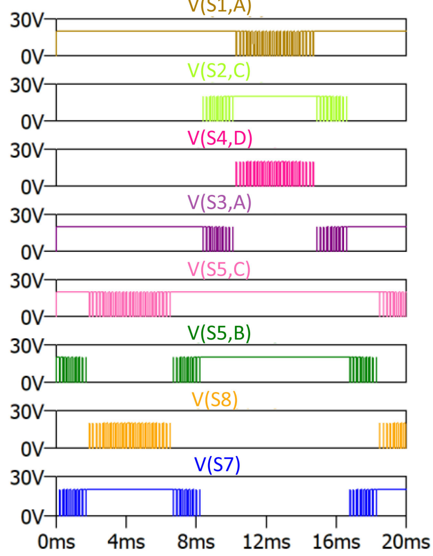


Fig. 23. Gate control signals for the simulation.

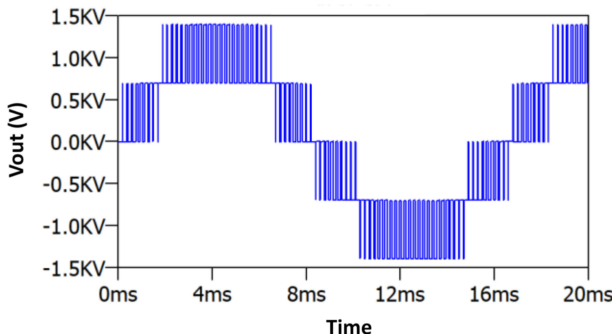


Fig. 24. Simulated output voltage waveform.

simulation to drive a 1.5 mH, 50 Ω load. Fig. 23 shows the gate control signal used in the simulation. Fig. 24 shows the simulated output voltage waveform.

In LTSpice, the total simulation time for the circuit was 23.02 s using the presented model. The total iteration count was 76 857. The previous model of the article presented in [6] takes 30.32 s for total simulation. A generic SPICE diode model is used for the body diode conduction with the model of the article presented in [6]. The total iteration count is 106 537 in this case. When the vendor's empirical model was used, the total simulation time was 37.4 s, with a much larger total iteration count of 348 744. In Fig. 25, the comparison of the models' total simulation time at different common topologies is shown. In all the cases, the new model shows better performance than the old model [6] and the vendor's empirical model. The presented model is more efficient than the previous model [6], despite having gate-dependent body diode and reverse recovery characteristics. This study validates the utility of the new model for more efficient simulation.

This simulation's objective was to verify that the model converges well in a complex application, and this has been accomplished.

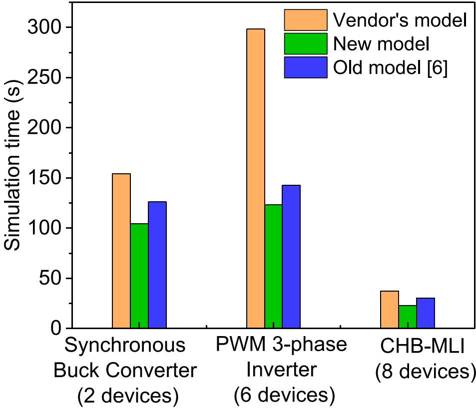


Fig. 25. Total simulation time comparison at different topologies.

## VI. Conclusion

In this article, a physics-based compact model for an SiC power MOSFET that includes both the first- and third-quadrant characteristics has been presented and validated. The model's uniqueness is to capture the body diode characteristics, including reverse recovery phenomena, without compromising the first-quadrant characteristics' accuracy and convergence properties. The accurate and efficient third-quadrant characteristics modeling is essential for circuit applications with synchronous rectification. Also, body diode modeling with reverse recovery allows the accurate simulation of the circuit when the body diode is used as the freewheeling diode. Moreover, the accurate gate-dependency modeling will enable circuit designers to think about more innovative approaches to utilize the power MOSFET's body diode. This article also describes a new parameter extraction procedure that can be followed with ease to develop a device model only from the available datasheet. The developed extraction procedure only relies on the output characteristics, removing the confusion caused by the mismatch between the dc transfer curve and the dc output curves, which is prevalent in many datasheets. The model's convergence properties have been validated through the simulation of a five-level CHB-MLI, ensuring the usefulness of the model for broader power electronics circuit designs. In addition, a comparison with a previous model [6] proves the presented model's utility in terms of accuracy and efficiency, despite adding computationally expensive third-quadrant features. Hence, the presented model is a significant contribution to more accurate and efficient simulation of all kinds of power converters.

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