Current-Fed *LC* Series Resonant Converter With Load-Independent Voltage-Gain Characteristics for Wide Voltage Range Applications

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***Abstract*—This article proposes a current-fed *LC* series resonant converter, which integrates a two-phase interleaved boost circuit with a full-bridge *LC* series resonant converter. All switches can achieve zero voltage switching (ZVS) under full load range without utilizing a magnetizing inductor or an auxiliary inductor, and synchronous rectification (SR) can be realized without SR driving detection. With the proposed modulation, the resonant current is discontinuous without circulating current. Moreover, the voltage gain of the *LC* series resonant conversion is fixed, which is independent of load; therefore, the design of voltage regulation range and related parameters can be simplified. The integrated boost circuit works in the critical current mode to achieve ZVS for all the switches. Meanwhile, digital adaptive frequency modulation is presented to ensure ZVS realization and to minimize the boost inductor current ripple. The working characteristics and design considerations for the key parameters of the proposed modulation are also presented in detail in this article. Finally, a 600-W prototype with 27–54 V input and 360 V output is built, and experimental results validate the effectiveness and the advantages of the proposed solution.**

***Index Terms*—Current-fed converter, digital adaptive frequency control, resonant converter, wide voltage gain range.**

I. Introduction

ISOLATED dc/dc converter (IDC) utilizing high-frequency transformer to achieve galvanic isolation is widely adopted in renewable energy generation [1], [2]. Fig. 1 shows the typical structure of a grid-connected renewable power generation system [3], [4]. The voltage of renewable energy sources varies over a wide range because of their intermittence and instability, such as photovoltaic (PV) and fuel cells [5], [6]. To interface with renewable energy sources, it is necessary to realize IDC working in a wide input voltage range while maintaining high power conversion efficiency.

Among various IDC converters, the *LLC* resonant converter is an attractive topology, which has significant advantages, such as soft switching, high efficiency, and low electromagnetic interference issue [7]–[10]. For the traditional pulse frequency modulation (PFM) of the *LLC* resonant converter, the efficiency is very high when operating near the resonant frequency. However, if the voltage gain needs to be widely adjusted, the switching frequency needs to be away from the resonant frequency, which could generate high circulating energy and reduce the efficiency [11], [12]. Therefore, the performance of the traditional *LLC* resonant converter with PFM is heavily reduced for wide input voltage range applications [13]–[16].

To extend the voltage gain range while maintaining high efficiency, many control schemes and topologies have been proposed. In [17], a phase-shift modulation (PSM) of the secondary side switch is proposed. The voltage gain range has been expanded, but the circulating current of the converter increases with the phase shift angle. A hybrid control combining PFM and PSM is proposed in [18]. Both voltage regulation capability and efficiency are improved, but the control strategy becomes more complicated. An asymmetrical duty cycle control method for full-bridge *LLC* (FB-*LLC*) is proposed in [19]. This method has an additional 0.5 step-down gain compared with the conventional FB-*LLC* resonant converter because the input of the resonant tank is half of the input voltage. Another effective solution is the reconstruction of topology [20], [21]. The idea of this method is to transit the primary side of FB-*LLC* into half-bridge *LLC*. Two operation modes of full-bridge and half-bridge can then obtain a double gain range. However, the two modes are difficult to switch smoothly. Auxiliary switches or components are adopted in [22]–[24]. In [22] and [23], an auxiliary switch is added on the secondary side to achieve voltage regulation such that the switching frequency is constantly equal to the resonant frequency. Unfortunately, the complexity of the model and control is increased. Hu *et al.* [24]

Manuscript received July 26, 2020; revised December 11, 2020 and February 18, 2021; accepted March 27, 2021. Date of publication April 8, 2021; date of current version June 30, 2021. This work was supported in part by the National Natural Science Foundation of China under Grants 51907206 and 61933011, in part by the Science and Technology Innovation Program of Hunan Province under Grant 2020RC4002, in part by the Hunan Provincial Key Laboratory of Power Electronics Equipment and Grid under Grant 2018TP1001, in part by the Major Project of Changzhutan Self-dependent Innovation Demonstration Area under Grant 2018XK2002, in part by the Project of Innovation-Driven Plan in Central South University under Grant 2019CX003, in part by the Key R&D Projects in Hunan Province under Grant 2019GK2211, in part by the Fundamental Research Funds in the Central South University under Grant 2020zzts128. Recommended for publication by Associate Editor M. Harfman Todorovic. *(Corresponding author: Guo Xu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3071845.

Digital Object Identifier 10.1109/TPEL.2021.3071845

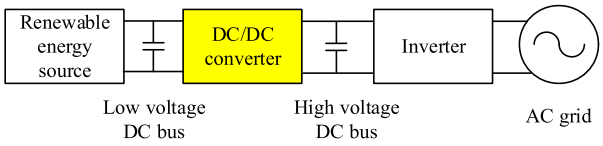

Fig. 1. Structure of a grid-connected renewable power generation system.

change the equivalent turn-ratio and magnetizing inductance by an auxiliary transformer. However, the utilization of auxiliary transformers is low because only the main transformer transmits energy. The voltage regulation ability is improved to a certain extent with the added auxiliary devices and increased control complexity.

Even though the aforementioned methods [17]–[24] can improve the permanence, the control and working modes are complex. To deal with this, the cascaded two-stage solution consisting of a conventional nonisolated dc/dc converter (e.g., boost converter) and an *LLC* resonant converter can be used [25], [26]. In this case, the *LLC* converter is unregulated, which only provides fixed voltage gain and galvanic isolation as a dc transformer (*LLC*-DCX). In [27], to improve the overall operation efficiency, *LLC*-DCX is cascaded with the critical current mode (CRM) boost converter. Zero voltage switching (ZVS) can be realized for both stages, and the switching loss of the whole system is decreased.

Compared with the single-stage converter, the voltage regulation ability of the two-stage topology is improved. However, more switches are used in these cascade converter topologies, which could increase the volume and cost. Consequently, the integration of the boost circuit and the *LLC* resonant converter is studied [28]–[31]. These integrated topologies can eliminate power switches and gate driver circuits. However, they also have some drawbacks. First, the pulsewidth modulation (PWM) is adopted for an integrated boost circuit, which needs to realize voltage regulation by controlling the duty cycle of switches. However, the voltage gain of the *LLC* resonant converter will also be affected when the duty cycle is changed [28], [29]. The gain characteristics are heavily dependent on the duty cycles or load, which loses the benefit of DCX operation for the two-stage solution. Therefore, the design of component parameters and the voltage controller could become complex. Second, after the integration, due to the effect of the boost inductor current, the ZVS achievement for lower switches of sharing arm becomes more difficult and calculation of ZVS conditions becomes very complicated. Consequently, in [29], the excitation inductor needs to be designed smaller to enlarge the ZVS region, and the auxiliary parallel inductor is adopted to achieve ZVS in [30] and [31]. However, the additional inductor could increase the related loss such as circulating current and magnetic losses.

In this article, an improved current-fed *LC* series resonant converter (CF-sRC) is proposed for wide input voltage range applications. The CF-sRC is integrated by a two-phase interleaved boost circuit and a full-bridge *LC* series resonant converter. The proposed topology and control strategies possess the following two main advantages.

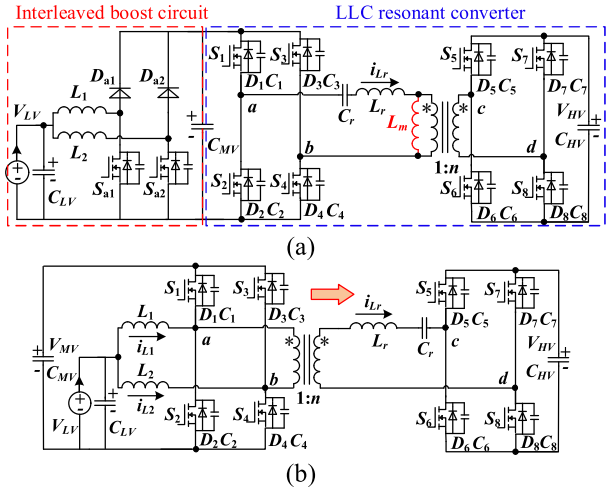

Fig. 2. Topology of dc/dc converter. (a) Two-stage topology implemented with a two-phase interleaved boost converter and an FB-*LLC* resonant converter. (b) Proposed CF-sRC converter.

1) All switches can achieve ZVS without utilizing excitation inductor or auxiliary inductor, which simplifies the design of the magnetic components.
2) The resonant current is discontinuous, and the voltage gain of the *LC* series resonant conversion is fixed under the proposed modulation and control methods. Therefore, only a simple PWM control for the boost circuit is used to regulate voltage, and the design of the voltage regulation range and voltage controller is simple. In addition, the realization of ZVS is independent of the resonant current, and hence ZVS analysis can be much simplified.

The rest of this article is organized as follows. The operating principles and characteristics of CF-sRC are presented in Section II. The converter characteristic analysis is presented in Section III. To optimize the circulating current when ZVS is achieved, a digital frequency control is introduced in Section IV. The design considerations are given in Section V. Experimental results based on a prototype are shown in Section VI, which verifies the effectiveness of the proposed solution. Finally, Section VII concludes this article.

II. Characteristic Analysis and Comparison

A. Topology of CF-sRC

The proposed CF-sRC is an integration of a two-phase interleaved boost circuit and a full-bridge *LC* series resonant converter, as shown in Fig. 2(b). The power transmission direction is from V_{LV} to V_{HV}. Compared with the traditional two-stage topology as shown in Fig. 2(a), the number of semiconductor devices in CF-sRC is reduced from 12 to 8, and the inductor L_m is removed. On the primary side, S_1, S_2, and L_1 form a boost circuit, whereas S_3, S_4, and L_2 form another boost circuit. The upper and lower switches of each bridge arm operate in a complementary manner. The two boost circuits adopt two-phase interleaving-control, whereas v_{ab} generates an ac square wave as the input of the resonant tank. On the secondary side, S_5–S_8

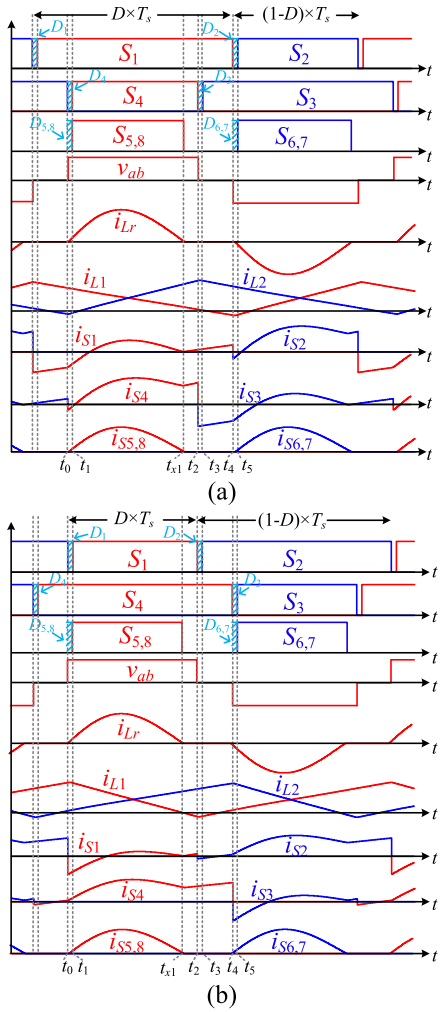

Fig. 3. Key operation waveforms of the proposed CF-sRC under DCM. (a) $D \geq 0.5$. (b) $D < 0.5$.

operates in the synchronous rectification (SR) state. The driving logics of the secondary bridge (S_5–S_8) are as follows:

1) when $D \geq 0.5$, S_5 (S_8) is turned ON simultaneously with S_4, and S_6 (S_7) is turned ON simultaneously with S_2;
2) when $D < 0.5$, S_5 (S_8) is turned ON simultaneously with S_1, and S_6 (S_7) is turned ON simultaneously with S_3;
3) conduction duration of S_5–S_8 is fixed as $T_r/2$.

The secondary-side switches work in SR, so the conduction duration of each group switch is equal to half period of resonance. When CF-sRC works in discontinuous current mode (DCM), the zero-crossing point of resonant current is fixed, and hence the conduction duration of all secondary-side (S_5–S_8) switch is fixed as $T_r/2$.

B. Operation Principle

The key waveforms of the proposed modulation are illustrated in Fig. 3. In the proposed modulation strategy, the resonant current works in DCM, which is a half-sine wave, and the zero-crossing time of resonant current is independent of voltage and load. Therefore, according to the above drive logic, SR can be realized without any additional auxiliary circuits to detect

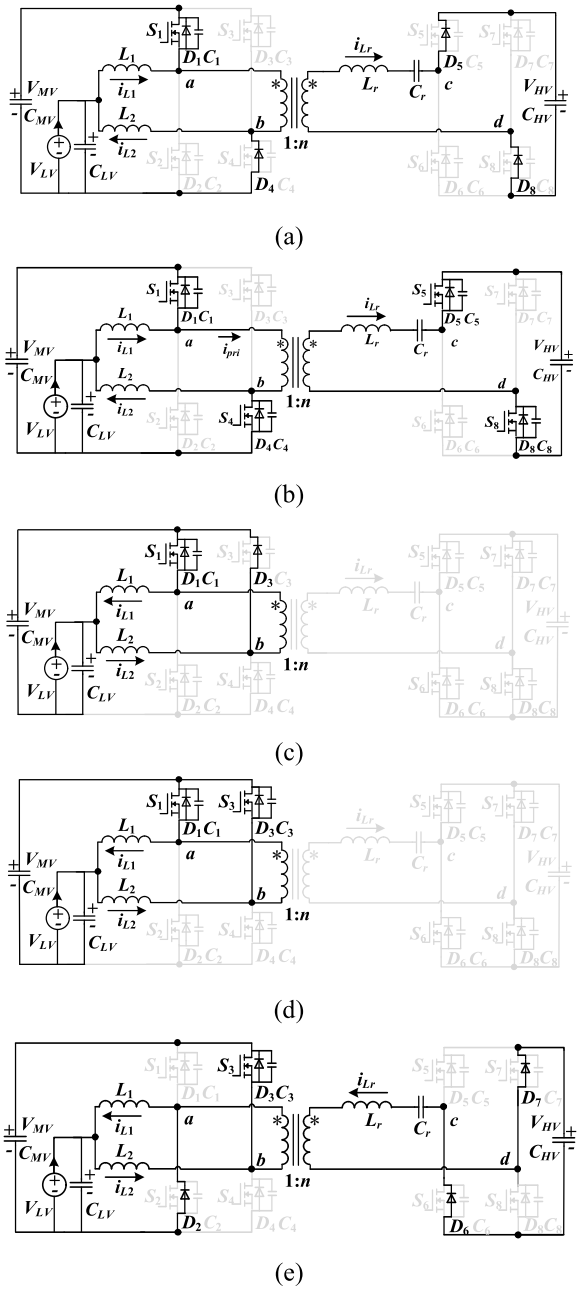

Fig. 4. Operating modes of the proposed CF-sRC under DCM. (a) Stage 1 [t_0, t_1]. (b) Stage 2 [t_1, t_2]. (c) Stage 3 [t_2, t_3]. (d) Stage 4 [t_3, t_4]. (e) Stage 5 [t_4, t_5].

the current zero-crossing point. In addition, the inductor current of the integrated boost circuit (i_{L1} and i_{L2}) operates in CRM to realize ZVS. The working principles of duty cycle D greater than 0.5 and less than 0.5 are similar, so only the former case is analyzed in this article.

Stage 1 [t_0, t_1] [see Fig. 4(a)]: At t_0, S_1 is turned ON and S_4 is turned OFF. i_{L1} flows through S_1 to charge C_{MV} and i_{L2} flows back to C_{LV} through D_4. During this time interval, v_{ab} is equal to V_{MV}. Hence, the input voltage of the resonant tank equals V_{MV}, and the resonant current i_{Lr} will rise from zero, which is sinusoidal. Synchronous rectifier switches S_5 and S_8 are turned OFF at this time, so the resonant current i_{Lr} flows through the

body diodes D_5 and D_8. v_{ab}, i_{L1}, i_{L2}, and i_{Lr} can be expressed as

$$\begin{cases} v_{ab} = V_{MV} \\ i_{L1} = i_{L1}(t_0) - \frac{(V_{MV}-V_{LV})\cdot(t-t_0)}{L_1} \\ i_{L2} = i_{L2}(t_0) + \frac{V_{LV}\cdot(t-t_0)}{L_2} \\ i_{Lr}(t) = \frac{nV_{MV}-V_{HV}-v_{Cr}(t_0)}{Z_r} \sin w_r(t-t_0) \end{cases} \tag{1}$$

where $Z_r = \sqrt{L_r/C_r}$ and $\omega_r = 2\pi f_r$.

Stage 2 [t_1, t_2] [see Fig. 4(b)]: At t_1, S_4, S_5, and S_8 are turned ON with ZVS at the same time. The voltage of the boost inductor and the input voltage of the resonant tank remain constant, so i_{L1}, i_{L2}, i_{Lr}, and v_{ab} keep in the state of stage 1. i_{Lr} completes half resonant period and decreases to 0 at t_{x1}. According to the driving logics described above, at t_{x1}, synchronous rectifier switches S_5 and S_8 are turned OFF when the current is near zero.

Stage 3 [t_2, t_3] [see Fig. 4(c)]: At t_2, S_4 is turned OFF, whereas S_1 keeps on conducting. S_3 is still turned OFF at the moment, so i_{L2} flows through D_3 to charge C_{MV}. The voltage levels at points a and b are both V_{MV}, so v_{ab} is equal to zero. At this stage, S_1 has no switch action and v_{ab}, i_{L1}, i_{L2}, and i_{Lr} can be expressed as

$$\begin{cases} v_{ab} = 0 \\ i_{L1} = i_{L1}(t_0) - \frac{(V_{MV}-V_{LV})\cdot(t-t_0)}{L_1} \\ i_{L2} = i_{L2}(t_2) - \frac{(V_{MV}-V_{LV})\cdot(t-t_2)}{L_2} \\ i_{Lr}(t) = 0. \end{cases} \tag{2}$$

Stage 4 [t_3, t_4] [see Fig. 4(d)]: At t_3, S_3 is turned ON with ZVS, and v_{ab}, i_{L1}, i_{L2}, and i_{Lr} keep in the state of stage 3. In the scheme proposed in this article, the integrated boost circuit operates in CRM; hence, before the end of this stage (before t_4), the boost inductor current i_{L1} will be reversed.

Stage 5 [t_4, t_5] [see Fig. 4(e)]: At t_4, S_1 is turned OFF, whereas S_2 is kept OFF; therefore, i_{L1} flows back to C_{LV} by D_2. v_{ab} is equal to $-V_{MV}$, hence the resonant current i_{Lr} begins to resonate for another half period. Before the turning ON of another group of synchronous rectifier switches S_6 and S_7, the resonant current i_{Lr} flows through their body diodes D_6 and D_7. During this stage, v_{ab}, i_{L1}, i_{L2}, and i_{Lr} can be expressed as

$$\begin{cases} v_{ab} = -V_{MV} \\ i_{L1} = i_{L1}(t_4) + \frac{V_{LV}\cdot(t-t_4)}{L_1} \\ i_{L2} = i_{L2}(t_2) - \frac{(V_{MV}-V_{LV})\cdot(t-t_2)}{L_2} \\ i_{Lr}(t) = \frac{-nV_{MV}-(-V_{HV})-v_{Cr}(t_4)}{Z_r} \sin w_r(t-t_4). \end{cases} \tag{3}$$

After stage 5, S_2, S_6, and S_7 can be turned ON with ZVS. Another half switching period begins, and the remaining operation modes are similar, which are omitted in this article.

III. Converter Characteristic Analysis

A. Boundary Conditions of Resonant Current Operation Mode

When the resonant current i_{Lr} decreases to zero, there are two working states including continuous current mode (CCM) and DCM, as shown in Fig. 5. When the resonant current works in CCM mode, i_{Lr} is reversed at t_a or t_b, as shown in Fig. 5(b) and (c). Under CCM, the circulating power is generated, and the conversion efficiency will be reduced. Meanwhile, the voltage gain of *LC* series resonant converter is no longer fixed. Therefore, i_{Lr} needs to avoid working in CCM.

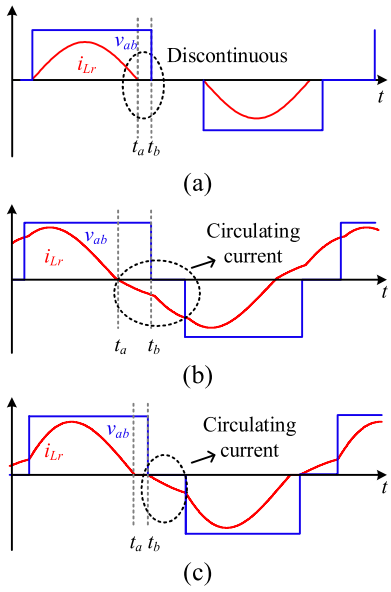

Fig. 5. Comparison of working state of resonant current i_{Lr}. (a) DCM. (b) CCM (reverse at t_a). (c) CCM (reverse at t_b).

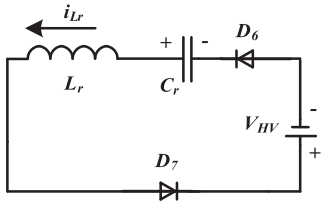

Fig. 6. Equivalent circuit of i_{Lr} in reverse under CCM.

When the resonant current is reversed, i_{Lr} will flow through D_6 and D_7, as shown in Fig. 6. Ignoring the forward voltage drop of the diodes, then the conduction condition of D_6 and D_7 is expressed as

$$\Delta V_{C_r} - V_{HV} - V_{Lr} > 0. \tag{4}$$

When the resonant current is critical continuous, the voltage drop of V_{Lr} is approximately equal to zero. Hence, (4) can be derived as

$$\begin{aligned} &\Delta V_{Cr} - V_{HV} > 0 \\ &\Rightarrow \frac{P}{4V_{HV} f_s C_r} - V_{HV} > 0 \\ &\Rightarrow P > 4V_{HV}^2 f_s C_r. \end{aligned} \tag{5}$$

According to (5), when $P < 4V_{HV}^2 f_s C_r$ is satisfied, all the diodes are reversed; hence, the resonance cannot continue by reversing the current direction, which means i_{Lr} will operate in DCM. Therefore, the maximum power in DCM mode is equal to $4V_{HV}^2 f_s C_r$. When i_{Lr} works in DCM, i_{Lr} is sinusoidal half-wave and the conduction duration is $T_r/2$ under different power and voltage. The driving logics of the secondary rectifier

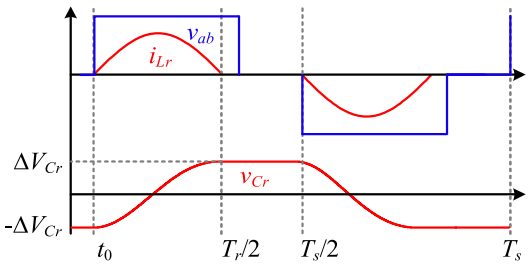

Fig. 7. Waveforms of i_{Lr} and v_{Cr} under DCM.

switches can be given according to this characteristic without zero crossing detection (ZCD) circuits.

B. Gain Characteristic

The voltage gain of the boost circuit operating in CRM M_{boost} can be obtained by the volt-second balance rule on the boost inductor

$$M_{\text{boost}} = \frac{V_{MV}}{V_{LV}} = \frac{1}{D} \tag{6}$$

where D is the duty cycle of the up-switches (S_1 and S_3).

The voltage gain of *LC* series resonant converter can be analyzed in the time domain. The waveforms of the resonant current i_{Lr} and resonant voltage v_{Cr} are shown in Fig. 7.

The peak voltage of the resonant capacitor ΔV_{Cr} at t_0 can be expressed as

$$\Delta V_{Cr} = \frac{\int_0^{Tr/2} i_{Lr}(t)\cdot dt}{2C_r}. \tag{7}$$

According to the definition of the output filter current I_{HV}, ΔV_{Cr} can be deduced as

$$\begin{cases} I_{HV} = \frac{2\int_0^{Tr/2} i_{Lr}(t)\cdot dt}{T_s} = \frac{P}{V_{HV}} \\ \Delta V_{Cr} = \frac{\int_0^{Tr/2} i_{Lr}(t)\cdot dt}{2C_r} \end{cases}$$

$$\Rightarrow \Delta V_{Cr} = \frac{I_{HV}}{4f_sC_r} = \frac{P}{4I_{HV}f_sC_r}. \tag{8}$$

The output filter current of I_{HV} can also be expressed as

$$\begin{cases} i_{Lr}(t) = \frac{nV_{MV}-V_{HV}-\Delta V_{Cr}}{Z_r}\sin w_r(t-t_0) \\ I_{HV} = \frac{2\int_0^{Tr/2} i_{Lr}(t)\cdot dt}{T_s} \end{cases}$$

$$\Rightarrow I_{HV} = \frac{2\int_0^{Tr/2} \frac{nV_{MV}-V_{HV}+\Delta V_{Cr}}{Z_r}\sin w_r(t-t_0)}{T_s}$$

$$\Rightarrow I_{HV} = \frac{2\frac{nV_{MV}-V_{HV}-\Delta V_{Cr}}{Z_r}\cdot\int_0^{Tr/2}\sin w_r(t-t_0)}{T_s}$$

$$\Rightarrow 4f_s\frac{nV_{MV}-V_{HV}+\Delta V_{Cr}}{Z_r\omega_r} = \frac{P}{V_{HV}}. \tag{9}$$

By substituting (8) into (9), the relationship between V_{MV} and V_{HV} can be derived as

$$nV_{MV} - V_{HV} + \frac{P}{4V_{HV}f_sC_r} = \frac{PZ_r\omega_r}{4f_sV_{HV}}$$

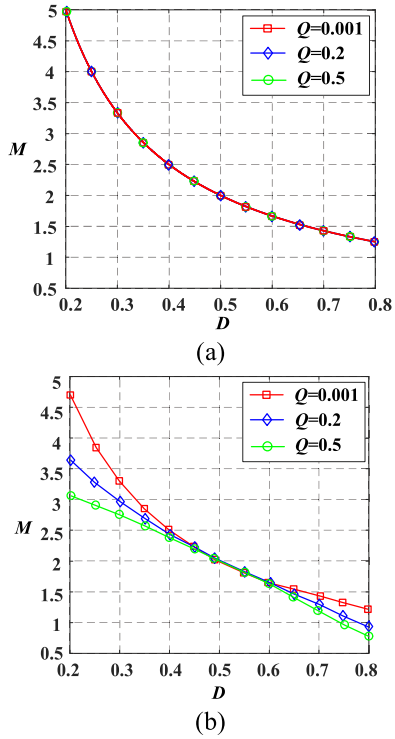

Fig. 8. Voltage-gain characteristics for (a) proposed CF-sRC under DCM and (b) topology proposed in [29].

$$\Rightarrow nV_{MV} - V_{HV} + \frac{P}{4V_{HV}f_sC_r} = \frac{P}{4f_sV_{HV}}\cdot\frac{1}{\sqrt{L_rC_r}}\cdot\sqrt{\frac{L_r}{C_r}}$$

$$\Rightarrow nV_{MV} = V_{HV}. \tag{10}$$

The voltage gain of the *LC* series resonant converter M_{sRC} can be obtained by

$$M_{\text{sRC}} = \frac{V_{HV}}{V_{MV}} = n. \tag{11}$$

It can be seen from (9) that the voltage gain of *LC* series resonant converter itself is constant, which is independent of duty cycle D, switching frequency f_s, and load. Hence, the *LC* series resonant converter of the proposed topology can be regarded as a dc transformer (DCX).

Combining (6) and (11), the voltage gain of CF-sRC $M_{\text{CF-sRC}}$ can be expressed as

$$M_{\text{CF-sRC}} = M_{\text{boost}}\cdot M_{\text{sRC}} = \frac{n}{D}. \tag{12}$$

According to (12), the normalized voltage gain curves ($n = 1$) can be obtained, as shown in Fig. 8(a). It can be seen that the total gain curve of CF-sRC is similar to a boost circuit. The voltage gain curve of the topology proposed in [29] is shown in Fig. 8(b). In contrast, the voltage gain of the latter topology will be affected by the quality factor Q, which changes with the load. Although compared with the traditional *LLC* resonant converter, the voltage regulation range of [29] is expanded; this feature will increase the complexity of converter design.

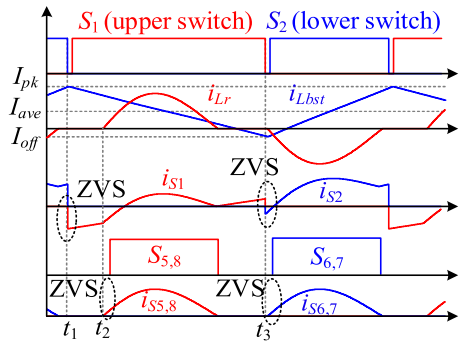

Fig. 9. Waveforms of ZVS.

C. ZVS Analysis

The waveforms of ZVS are shown in Fig. 9. For the convenience of analysis, the boost inductor and current of one switch bridge are defined as L_{bst} and i_{Lbst}, respectively.

1) *Lower Switches of Primary Side (S_2 and S_4):* The boost inductor L_{bst} of CF-sRC works in CRM whose direction can alternate in every switching period in order to achieve ZVS for lower switches. As shown in Fig. 9, before the lower switches are turned ON, i_{Lbst} has been reversed. Hence, once the upper switches are turned OFF, i_{Lbst} will continue to flow through the body diode of the lower switches. At this time, the boost inductance current is the valley value I_{off}. Therefore, the energy storage of the inductor needs to be large enough, and the dead time is long enough to realize ZVS. The ZVS conditions of the lower switches are expressed as

$$\begin{cases} t_d > \frac{2V_{MV}\cdot C_{oss}}{I_{\text{off}}} \\ \frac{1}{2}L_{bst}I_{\text{off}}^2 > C_{oss}V_{MV}^2. \end{cases} \tag{13}$$

The minimum value of the boost inductor current to realize ZVS can be derived as

$$I_{\text{ZVS}} = \sqrt{\frac{2C_{oss}V_{MV}^2}{L_{bst}}}. \tag{14}$$

2) *Upper Switches of Primary Side (S_1 and S_3):* For the upper switches, after the lower switches are turned OFF, the boost inductance current i_{Lbst} will be forced through the body diode of upper switches. As shown in Fig. 9, at t_1, the boost inductance current is the peak value I_{pk}. The ZVS conditions of the upper switches are similar to (13). The difference is that the current of ZVS is the peak value of inductor current, so it is easier to realize ZVS

$$\begin{cases} t_d > \frac{2V_{MV}\cdot C_{oss}}{I_{\text{pk}}} \\ \frac{1}{2}L_{bst}I_{\text{pk}}^2 > C_{oss}V_{MV}^2. \end{cases} \tag{15}$$

3) *Switches of Secondary Side (S_5 to S_8):* The secondary side switches work in SR mode, so ZVS is realized by the resonant current. For example, as shown in Fig. 9, at t_3, S_1 is turned OFF and i_{Lbst} is reversed. At this moment, i_{Lbst} flows through D_2, and the resonant current i_{Lr} begin to increase. In this way, before S_6 and S_7 are turned ON, the resonant current has flowed through their body diodes. In other words, with the proposed modulation, the premise of ZVS achievement of the secondary side switches is that the boost inductor of CF-sRC works in CRM.

D. Comparison

A comparison of the other four solutions is illustrated in Table I. The main disadvantage of the traditional FB-*LLC* converter is narrow gain range, which is not favored in two-stage cascaded topology. On the basis of cascaded topology, the method of topology integration reduces the number of switches and improves the power density. However, in the integrated topology, the analysis of voltage gain becomes more complicated. In addition, the realization of ZVS is difficult, and it is necessary to design smaller excitation inductors or add auxiliary inductors. As for the proposed CF-sRC, the range of voltage regulation is wide, and the voltage gain is independent of the load. In addition, the proposed CF-sRC does not need to design excitation inductor or auxiliary inductor to realize ZVS. The analysis of ZVS and the design of magnetic components are simpler. In voltage control, as with other integrated topologies with fixed frequency (FF), a simple PWM control is adopted. In addition, the regulation of switching frequency is added in this article for the optimization of current ripple and conduction loss.

IV. Digital Adaptive Frequency Control

Variable switching frequency with CRM operation can achieve ZVS and optimize circulating current under various conditions. The optimal switching frequency (period) can be calculated by sampling the input, output voltage and the average value of inductor current. This method can be realized by a digital controller without an additional analog ZCD circuit.

A. Frequency Constraint Conditions

1) *DCX Constraint:* In order to keep the voltage gain of *LC* series resonant converter constant, it is necessary to ensure that the resonant current can accomplish a complete resonant period. Therefore, the minimum conduction duration of the primary side switch needs to be longer than the half resonant period. Frequency constraints can be expressed as

$$\begin{cases} T_s \cdot D \geq T_r/2 \\ T_s \cdot (1-D) \geq T_r/2 \end{cases}$$
$$\Rightarrow f_s \leq \min\{(2f_r \cdot D), (2f_r \cdot (1-D))\}. \tag{16}$$

According to (16), it can be seen that the switching frequency needs to be lower than the resonant frequency when the *LC* series resonant converter is working as a DCX. When $D = 0.5$, the upper limit of the switching frequency is the highest, which is equal to the resonant frequency. In this case, the switching frequency can be close to the resonant frequency, and the input supply utilization is high. When D is increased or decreased, the input supply utilization will be reduced.

2) *ZVS Constraint:* Increasing the switching frequency is beneficial to reduce the current ripple, but too low current ripple will lead to the loss of ZVS. In order to ensure

TABLE I
COMPARISON OF OTHER RESONANT CONVERTER TOPOLOGIES

Topologies	Conventional full-bridge LLC converter	Interleaved boost cascaded full-bridge LLC converter [26]	Interleaved boost integrated full-bridge LLC converter-I [29]	Interleaved boost integrated full-bridge LLC converter-II [30][31]	Proposed CF-sRC
Number of switches (primary side)	4	8	4	4	4
Bus capacitor	-	Bulky	Small	Small	Small
Soft switching	Primary: ZVS Secondary: ZCS	Boost: hard switching LLC: ZVS, ZCS	Primary: ZVS Secondary: ZCS	Primary: ZVS Secondary: ZCS	Primary: ZVS Secondary: ZCS
Utilize excitation inductor or auxiliary inductor for ZVS	Needed	Needed	Needed	Needed	Not needed
Analysis of ZVS	simple	simple	complex	complex	Simple
Modulation	PFM	Boost: PWM LLC: PFM	PWM	PWM	PWM
Gain independent of load	×	√	×	√	√
Voltage regulation range	Narrow	Wide	Wide	Wide	Wide

ZVS under full range voltage and load, it is necessary to calculate the optimal switching frequency, which is obtained as

$$\begin{cases} \Delta I_L = 2\cdot(I_{\rm ave}+I_{\rm ZVS}) \\ T_{\rm on} = \frac{L_{bst}\cdot\Delta I_L}{V_{MV}-V_{LV}} \\ T_{\rm off} = \frac{L_{bst}\cdot\Delta I_L}{V_{LV}} \end{cases}$$

$$\Rightarrow f_s = \frac{1}{(T_{\rm on}+T_{\rm off})} = \frac{V_{LV}\cdot(V_{MV}-V_{LV})}{L_{bst}\cdot\Delta I_L\cdot V_{MV}} \quad (17)$$

where ΔI_L is the peak-to-peak value of the boost inductor current and $I_{\rm ave}$ is the average value by sampling.

The minimum current $I_{\rm ZVS}$ to realize ZVS in formula (14) needs to be considered here. The current state f_s should be adjusted according to (17) to ensure ZVS and reduce the current ripple.

B. Control Strategy

According to the ZVS analysis in the previous section, it can be seen that the key is to realize ZVS of primary side lower switches. The system needs to adjust the switching frequency according to the current working state regularly. The control flowchart, shown in Fig. 10, can be mainly divided into the following two steps.

1) According to formula (16), limit the range of frequency regulation from current operating conditions.
2) According to formula (17), calculate the optimal switching frequency f_s.

For the convenience of the study, the frequency regulation processes of different input power (the rated power is $P_{\rm rated}$) are shown in Fig. 11. The gray region is the DCX area, which satisfies the constraint condition (16). Formula (18) can be deduced as

$$f_s \le \frac{DV_{MV}\cdot(V_{MV}-DV_{MV})}{L_{bst}\cdot\frac{2\cdot P_{\rm rated}}{DV_{MV}}\cdot V_{MV}}$$

$$\Rightarrow f_s \le \frac{D^2\cdot(V_{MV}-DV_{MV})}{2L_{bst}\cdot P_{\rm rated}}. \quad (18)$$

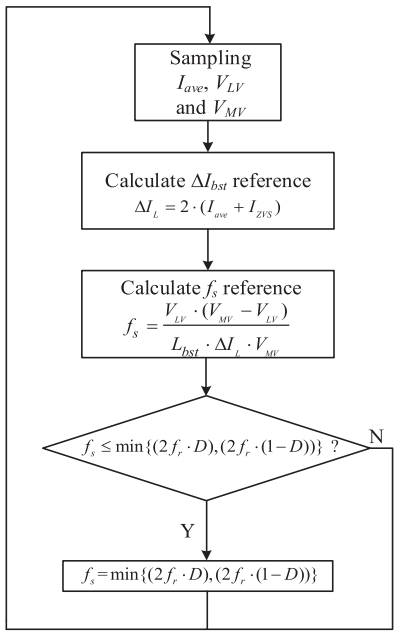

Fig. 10. Flowchart of digital adaptive frequency control.

Equation (18) is represented by a red curve in Fig. 11, and the ZVS area is below the red curve. The blue curve is the frequency regulation track. It can be seen that the frequency is adjusted at the boundary of the intersection of the red and gray areas.

The control block diagram of the proposed CF-sRC is shown in Fig. 12. The traditional double closed-loop control is used to regulate the output voltage. According to the sampling average value of boost current and voltage, the proposed digital adaptive frequency control is used to adjust the switching frequency f_s, which can ensure the realization of ZVS and optimize the current ripple.

V. DESIGN CONSIDERATIONS

A design example of a 600-W prototype is introduced in this section. The basic specifications of the converter prototype

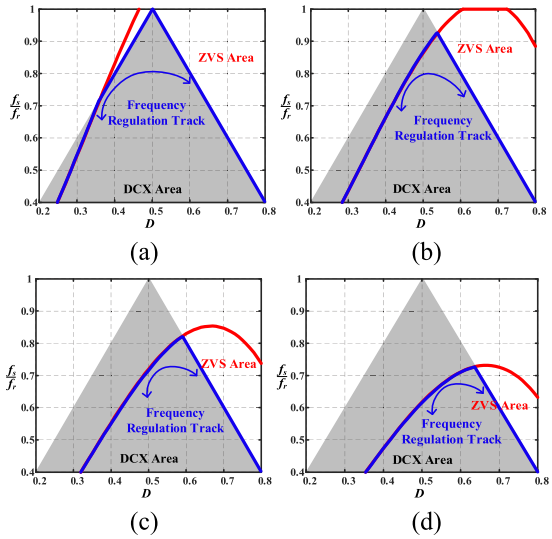

Fig. 11. Different input power frequency regulation track. (a) $0.4P_{\rm rated}$. (b) $0.6P_{\rm rated}$. (c) $0.8P_{\rm rated}$. (d) $P_{\rm rated}$.

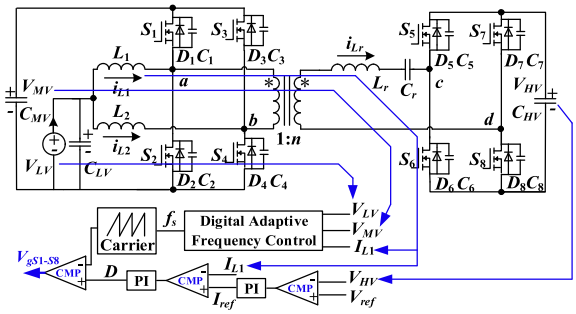

Fig. 12. Proposed control block diagram.

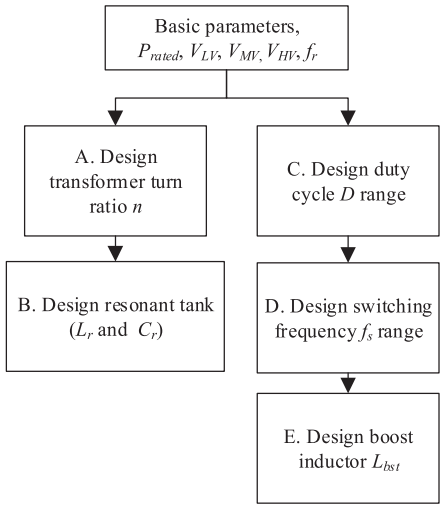

Fig. 13. Parameters design process.

are as follows: input voltage $V_{LV} = 27$–54 V, intermediate bus voltage $V_{MV} = 72$ V, output voltage $V_{HV} = 360$ V, and resonant frequency $f_r = 200$ kHz. The design process is shown in Fig. 13. According to the basic parameters, the design process is mainly divided into five parts, and the details are as follows.

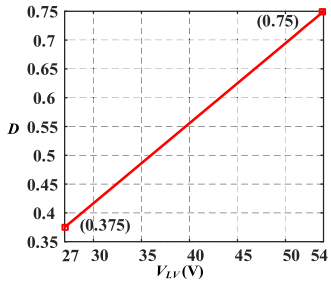

Fig. 14. Relationship between input voltage and duty cycle.

A. Turns Ratio of the Transformer

Based on (9), the voltage gain for V_{MV} to V_{HV} is equal to the transformer turns ratio n, which is independent of load. Hence, n of the prototype can be designed as

$$n = \frac{V_{HV}}{V_{MV}} = \frac{360}{72} = 5. \tag{19}$$

B. Resonant Tank

The resonant frequency is designed to be about 200 kHz. As seen from the conditions of DCM operation, $\mathrm{C_r} > \mathrm{P}/(4\mathrm{V_{HV}^2 f_s})$ needs to be satisfied to ensure that the converter operates in DCM. Meanwhile, $\mathrm{Z_r} = \sqrt{\mathrm{L_r}/\mathrm{C_r}}$ needs to be appropriately high to reduce the peak value of the resonant current at start-up.

According to the above conditions, the final design parameters of the resonant tank are shown as follows: $C_r = 66$ nF and $L_r = 10\ \mu$H.

C. Duty Cycle Range

The voltage gain of CF-sRC is n/D ($n = 5$). When output voltage V_{HV} is constant, the relationship between input voltage and duty cycle is $D = V_{LV}/72$, which is shown in Fig. 14. When the input voltage changes from 27 to 54 V, the corresponding duty cycle regulation range is 0.375–0.75.

D. Switching Frequency Range

According to the frequency of adaptive control in Section IV, the range of switching frequency can be calculated as

$$\begin{aligned} &\tfrac{1}{2} f_r \le f_s \le f_r \\ &\Rightarrow 100\ \text{kHz} \le f_s \le 200\ \text{kHz}. \end{aligned} \tag{20}$$

The diagram of switching frequency, input voltage, and input power is shown in Fig. 15. Under the proposed adaptive frequency control, the switching frequency can be adjusted according to different input voltage and power.

E. Boost Inductor Designing

It is necessary to properly design the boost inductor L_{bst} to consider both the ZVS achievement under full load and the low current ripple. According to the volt-second balance rule on the boost inductor, the peak-to-peak value of inductor current ΔI_L can be determined as

$$\Delta I_L = \frac{V_{LV}}{L_{bst}}(1 - D)T_s. \tag{21}$$

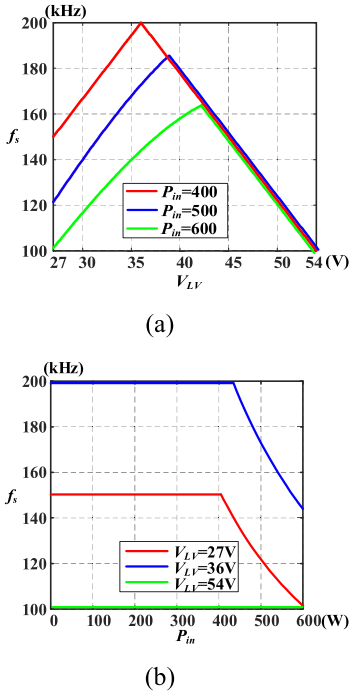

Fig. 15. Switching frequency regulation strategy. (a) Relationship between switching frequency and input voltage. (b) Relationship between switching frequency and input power.

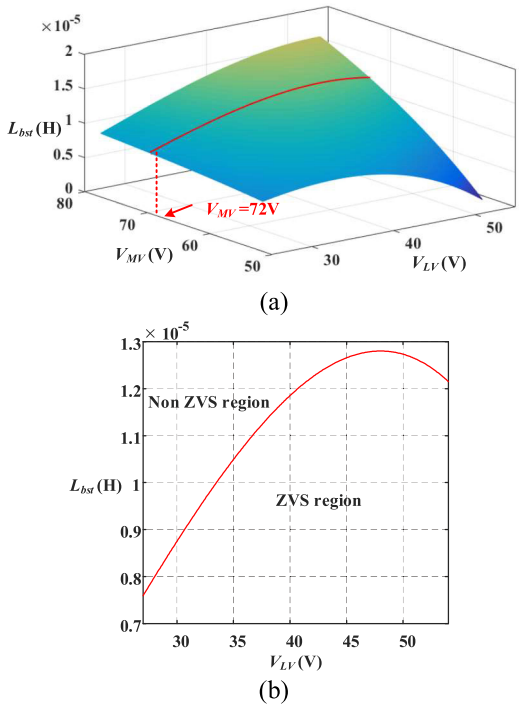

Fig. 16. Critical inductance to operate in CRM. (a) Critical inductance under different working voltage. (b) Critical inductance under $V_{MV} = 72$ V.

When the boost inductor L_{bst} works in CRM, the relationship between ΔI_L and average current I_{ave} is

$$\Delta I_L \geq 2 \cdot I_{\text{ave}} = 2 \cdot \frac{P_{\text{rated}}}{V_{LV}} \cdot \frac{1}{2} \tag{22}$$

where P_{rated} is the rated power.

Combining (21) and (22), the design range of L_{bst} can be obtained as

$$L_{bst} \leq \frac{2 \cdot (1-D) \cdot V_{LV}^2}{2 \cdot P_{\text{rated}} \cdot f_s} = \frac{V_{LV}^2}{P_{\text{rated}} f_s} \cdot \frac{V_{MV} - V_{LV}}{V_{MV}}. \tag{23}$$

Boost inductor needs to be designed at maximum power 600 W and minimum switching frequency 100 kHz to ensure the realization of ZVS under full range. Hence, according to (23), the critical value of boost inductor L_{bst} can be drawn as shown in Fig. 16. Fig. 16(a) shows the maximum allowable inductor to operate in CRM under different V_{MV} and V_{LV}. Under the surface is the ZVS region, so the value of boost inductance needs to be selected in this region. According to the parameters of the prototype, the rated value of V_{MV} is 72 V [as shown in the red curve in Fig. 16(a), and the inductance range under this condition is shown in Fig. 16(b)]. It can be seen that when the input voltage V_{LV} is equal to 27 V, the upper limit of inductor value is the smallest. In addition, in order to reduce the circulating current and current ripple, the inductor should be large enough, so the boost inductor is designed as 7.5 μH.

F. Theoretical Loss Analysis

The full-load power losses of CF-sRC are compared at three important benchmarks ($V_{LV} = 27$, 36, and 54 V). In CF-sRC,

TABLE II
LOSS ANALYSIS UNDER 600 W

Losses (W)	27V (f_s=100kHz, D=0.375)	36V (f_s=140kHz, D=0.5)	54V (f_s=100kHz, D=0.75)
Conduction losses	6.79	4.71	5.28
Turning-off losses	6.80	9.25	5.07
Driving losses	2.41	3.41	2.41
Core losses of transformer	1.45	2.29	1.28
Copper losses of transformer	0.84	1.40	0.84
Core losses of boost inductor	10.20	11.02	5.15
Copper losses of boost inductor	2.61	1.43	0.93
Total	31.10	33.51	20.96

all the MOSFETs are turned ON with ZVS. Hence, the turning-ON losses are zero. The theoretical losses dates under different input voltage are listed in Table II. The total losses consist of eight parts, namely switches conduction loss, switches turn-ON loss, switches turn-OFF loss, driving loss, transformer core loss, transformer copper loss, inductor core loss, and inductor copper loss. According to the data in Table II, the loss analysis histogram is shown in Fig. 17. When the input voltage is 54 V, because the working current is the lowest, turning-OFF losses and boost inductor losses are lower than the other two cases. Hence, the total loss is the lowest at 54 V, and the converter efficiency is the highest. When the input voltage is 36 V, the current ripple of the boost inductor is the largest. Under the adaptive frequency modulation control, the switching frequency will be higher than

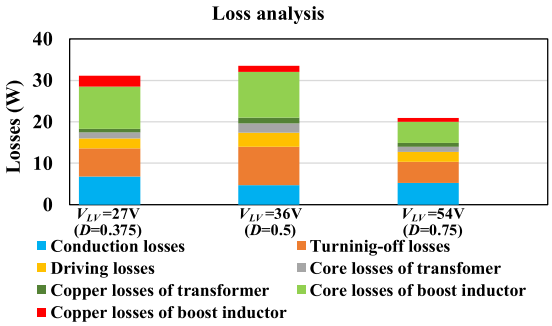

Fig. 17. Theoretical loss calculation results of full load.

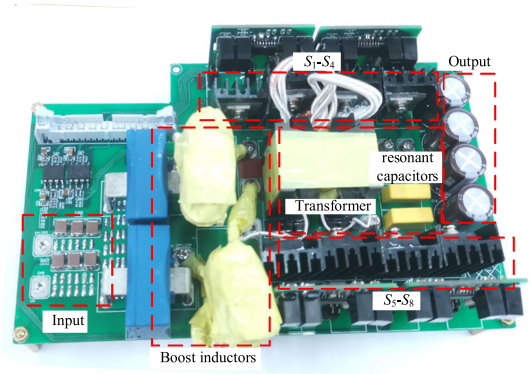

Fig. 18. Laboratory prototype.

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Designed parameters	Value
Input voltage (V_{LV})	27-54V
Intermediate side (V_{MV})	72V
Output voltage (V_{HV})	360V
Rated power (P_{rated})	600W
Turns ratio (n)	5
Resonant capacitor (C_r)	66nF
Resonant inductor (L_r)	10μH
boost inductor (L_{bst})	7.5μH
LV-side capacitor	120μF
MV-side capacitor	47μF
HV-side capacitor	100μF
Resonant frequency (f_r)	200kHz
Switching frequency (f_s)	100-200kHz

other working conditions. This leads to the increase of drive loss, turn-OFF loss, and core loss.

VI. EXPERIMENTAL VERIFICATION

A 600-W laboratory prototype, as shown in Fig. 18, has been built based on the design procedures introduced in Section V. The specifications of the prototype are as follows: input voltage V_{LV} = 27–54 V, output voltage V_{HV} = 360 V, rated output power P_o = 600 W, switching frequency f_s = 100–200 kHz, and resonant frequency f_r = 200 kHz. The detailed parameters of CF-sRC are listed in Table III. A conventional double closed loop is used for the boost circuit, and the output voltage V_{HV} can remain constant when the input voltage and load change.

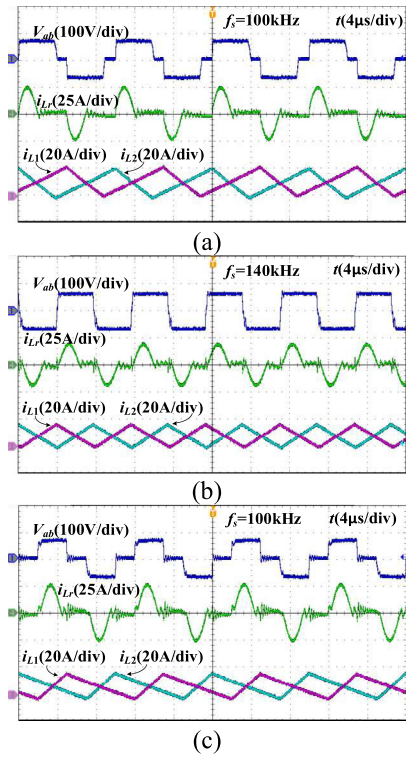

Fig. 19. Steady-state working waveform under full load (600 W). (a) V_{LV} = 27 V. (b) V_{LV} = 36 V. (c) V_{LV} = 54 V.

The steady-state working waveforms at full load under different input voltage V_{LV} are shown in Fig. 19. It can be seen that, over a wide input voltage range of 27–54 V, the proposed CF-sRC operates well with the proposed modulation. The inductor currents i_{L1} and i_{L2} operate in interleaved state and v_{ab} can generate a high-frequency square waves. In each switching cycle, the inductor current is reversed once for realizing ZVS, and the current ripple can be optimized by proposed variable frequency (VF) control. In addition, during each half of the switching cycle, the resonant current is a complete sinusoidal half-wave, and no circulating current is generated. When the resonant current decreases to zero, the resonant inductor and the junction capacitance of the switch can continue to resonate. During this duration, the resonant current has a small amplitude oscillation and decays quickly. Hence, the experimental waveforms are consistent with the theoretical analysis.

Under different input voltage and power, the operating waveforms of synchronous rectifier switches are shown in Fig. 20. Due to the symmetry of the structure, only the waveforms of S_5 and S_6 are shown. As can be seen, the zero-crossing time of resonant current is kept constant during steady-state operation, which is independent of input voltage and power. Therefore, without an additional auxiliary circuit, the prototype can realize SR only by digital controller.

According to the ZVS analysis in Section III, the ZVS conditions for two groups of bridge arm on the primary side are identical, and the ZVS conditions of all secondary switches are the same. Hence, the ZVS waveforms of one bridge arm on the primary side (S_1 and S_2) and one switch on the secondary side

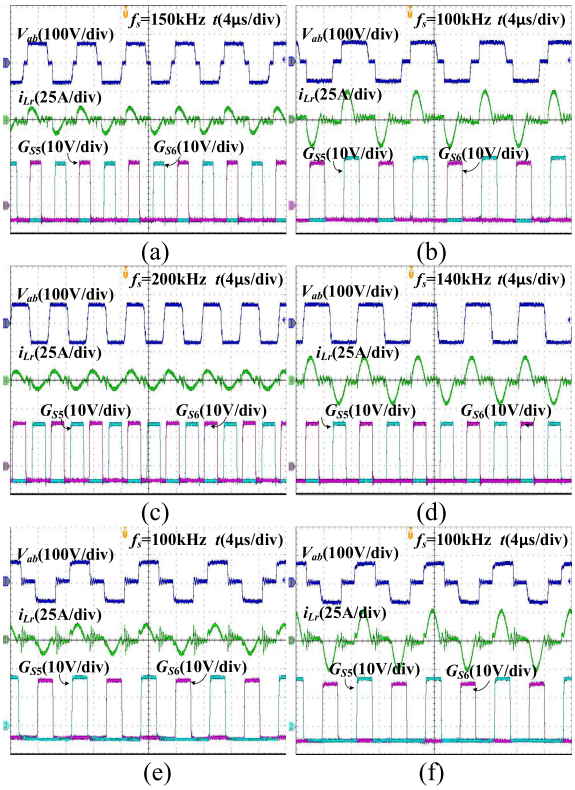

Fig. 20. Working waveforms of SR. (a) $V_{LV} = 27$ V, $P = 300$ W. (b) $V_{LV} = 27$ V, $P = 600$ W. (c) $V_{LV} = 36$ V, $P = 300$ W. (d) $V_{LV} = 36$ V, $P = 600$ W. (e) $V_{LV} = 54$ V, $P = 300$ W. (f) $V_{LV} = 54$ V, $P = 600$ W.

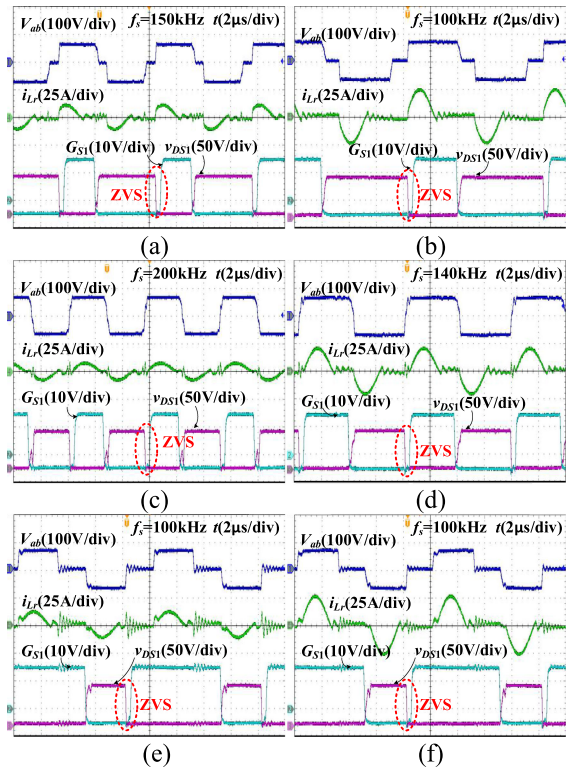

Fig. 21. ZVS-ON waveforms of S_1. (a) $V_{LV} = 27$ V, $P = 300$ W. (b) $V_{LV} = 27$ V, $P = 600$ W. (c) $V_{LV} = 36$ V, $P = 300$ W. (d) $V_{LV} = 36$ V, $P = 600$ W. (e) $V_{LV} = 54$ V, $P = 300$ W. (f) $V_{LV} = 54$ V, $P = 600$ W.

(S_5) are shown in Figs. 21, 22, and 23, respectively. It can be seen that the drain–source voltage v_{DS} of all switches is reduced to zero before the rising of the driving signal under different working voltage and power. As illustrated, for the proposed topology and control strategy, all switches can realize ZVS.

To verify the dynamic performance regarding input voltage changes, the dynamic response waveforms when the input voltage V_{LV} changes are shown in Fig. 24. It can be seen that when the input voltage changes within twice the range (27–54 V), the output voltage V_{HV} is kept at 360 V. Therefore, the proposed CF-sRC has a good performance in the application of wide range input voltage. The dynamic waveforms of switching between half load (300 W) and full load (600 W) are shown in Fig. 25. It can be seen that, when the load changing occurs, the output voltage V_{HV} can also be adjusted rapidly and maintained at 360 V.

The voltage gain curves for the part of *LC* series resonant converter (V_{HV}/nV_{MV}) under different input voltage are shown in Fig. 26. The measured results are the actual values including the voltage drop of switches conduction and line conduction. As can be seen, the measured voltage gain is close to 1 under different load conditions, which matches the theoretical analysis. The results show that the *LC* series resonant converter in CF-sRC works as DCX.

Fig. 27 depicts the curves of measured conversion efficiency for different input voltages and power. For comparison, the efficiency under FF control is also shown in Fig. 27. In order

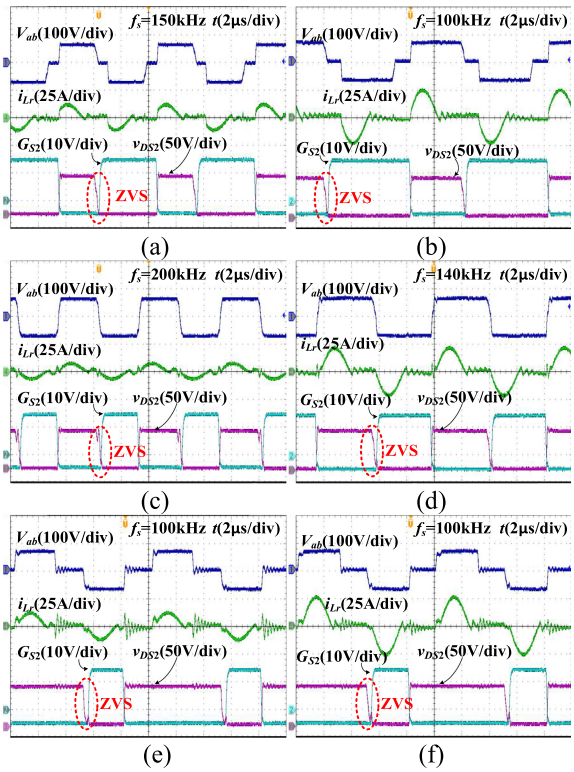

Fig. 22. ZVS-ON waveforms of S_2. (a) $V_{LV} = 27$ V, $P = 300$ W. (b) $V_{LV} = 27$ V, $P = 600$ W. (c) $V_{LV} = 36$ V, $P = 300$ W. (d) $V_{LV} = 36$ V, $P = 600$ W. (e) $V_{LV} = 54$ V, $P = 300$ W. (f) $V_{LV} = 54$ V, $P = 600$ W.

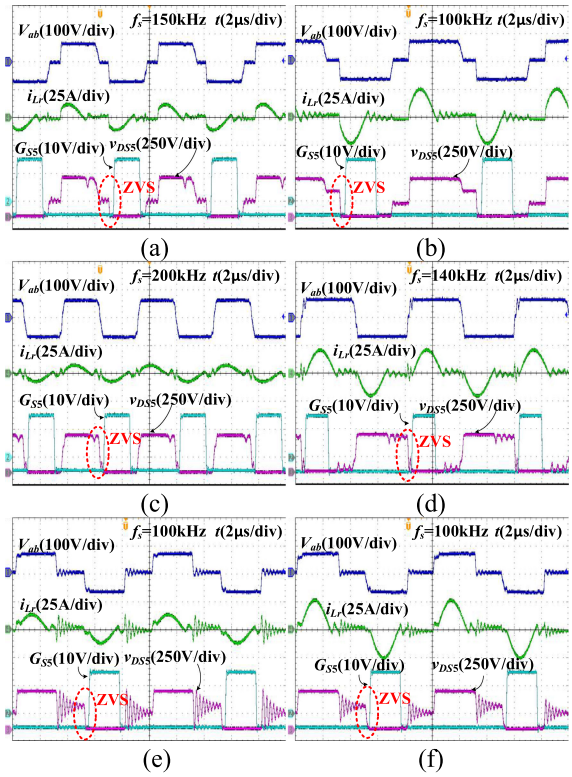

Fig. 23. ZVS-ON waveforms of S_5. (a) $V_{LV} = 27$ V, $P = 300$ W. (b) $V_{LV} = 27$ V, $P = 600$ W. (c) $V_{LV} = 36$ V, $P = 300$ W. (d) $V_{LV} = 36$ V, $P = 600$ W. (e) $V_{LV} = 54$ V, $P = 300$ W. (f) $V_{LV} = 54$ V, $P = 600$ W.

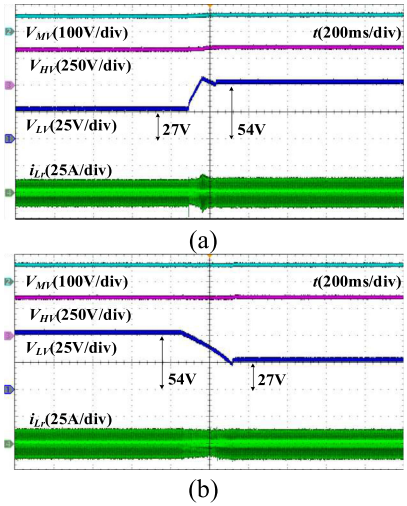

Fig. 24. Dynamic waveforms of input voltage V_{LV} variation. (a) 27 to 54 V. (b) 54 to 27 V.

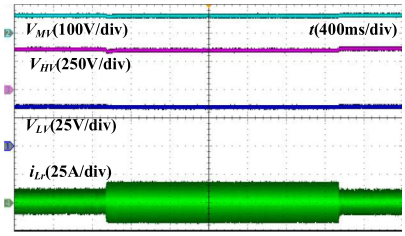

Fig. 25. Dynamic waveforms of load variation (300–600–300 W).

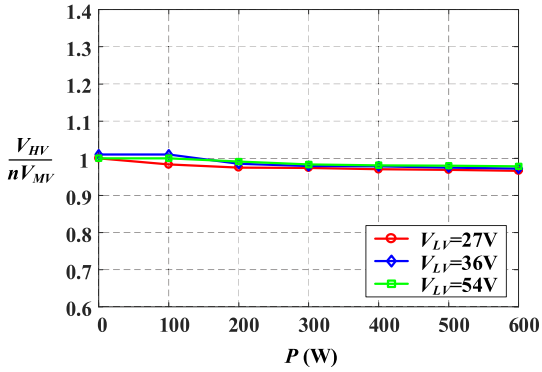

Fig. 26. Gain curve of series resonant converter (V_{HV}/nV_{MV}) under different input voltages.

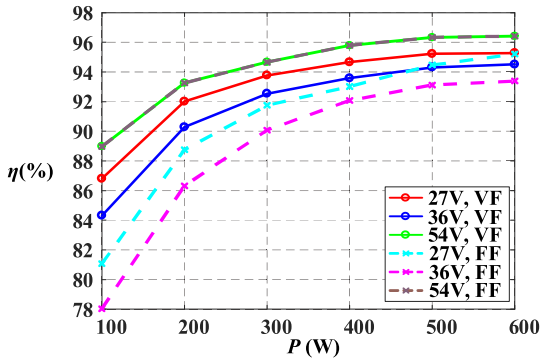

Fig. 27. Measured efficiency cures.

to realize ZVS, the switching frequency should be selected as the lowest value (100 kHz) under FF control. The solid line and dotted line present the working efficiency of VF and FF (100 kHz), respectively. Under half load (300 W), when the input voltage is 36 V, the working efficiency is only 90% under FF control. After using the adaptive frequency control, the working efficiency is up to 92%, and the efficiency is increased by 2%. When the input voltage is 27 V, the efficiency is also improved under adaptive frequency control. Therefore, under the same working voltage, the proposed digital adaptive frequency control can improve the total efficiency. In addition, according the frequency control strategy, when input voltage is 54 V, f_s is always adjusted to 100 kHz. Hence, the working efficiency of VF and FF is identical under 54 V.

VII. Conclusion

In this article, a CF-sRC converter is proposed and explored. The topology is obtained by integrating a two-phase boost circuit into the full-bridge *LC* series resonant converter with the sharing of primary H-bridge. All switches can achieve ZVS without utilizing a magnetizing inductor or an auxiliary inductor under full load range, which simplifies the design of magnetic components. The *LC* series resonant converter can work as a DCX where its voltage gain is fixed and completely decoupled with the boost circuit. The voltage gain of the whole converter is similar to the boost circuit. This characteristic can simplify the ZVS analysis and design of voltage regulation range and related

parameters. The integrated boost circuit works in the CRM that can achieve ZVS for all the switches. In steady-state operation, the switching frequency can be adjusted by proposed digital adaptive frequency control to ensure the realization of ZVS and to optimize the current ripple of the boost inductor. The working modes of the converter, control strategy, and design process are presented in detail. The experimental results have shown that the proposed solution is effective to be applied in wide range input voltage applications.

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