An Si MOSFET-Based High-Power Wireless EV Charger With a Wide ZVS Operating Range

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***Abstract*—This article proposes a new digitized modulation scheme suitable for a high-power wireless electric vehicle charger employing an integrated boost multilevel converter (IBMC) as its primary-side converter. Using the proposed modulation scheme, an IBMC can generate a boosted square-wave-shaped ac voltage with a controllable amplitude, enabling it to regulate the power efficiently over a wide load and/or coupling range while achieving zero voltage switching for all switches. This article focuses on the steady-state operating principles of the proposed digitized modulation scheme. Key practical considerations, such as capacitor voltage balancing and semiconductor device selection, are highlighted. To verify the benefits of the proposed modulation scheme, an SAE J2954 WPT2/Z2 compliant wireless EV charger prototype that uses an IBMC as the primary converter is designed and built. 200 V Si MOSFETs are employed in the 12 submodules (SMs) that compose the IBMC. The secondary side employs a passive rectifier, and the power flow is controlled using only the IBMC. This system maintains an efficiency between 90% and 93% when regulating power transfer at 7.7 kW under a 220% variation in coupling factor (i.e., 0.14–0.31) and a 150% variation in battery voltage (i.e., 280–420 V).**

***Index Terms*—Electric vehicle (EV), inductive power transfer (IPT), multilevel converters, SAE J2954, zero voltage switching (ZVS).**

I. Introduction

INDUCTIVE power transfer (IPT) is becoming increasingly popular as one of the most suitable solutions to charge electric vehicles (EVs). Wirelessly charging EVs using IPT technology is safe, efficient, aesthetically pleasing, convenient, and enables automated charging when an EV is parked over a ground-based charging pad [1]. In recent years, to reduce the refueling time of EVs, the industry and researchers have moved their focus to higher power wireless charging systems [2], [3]. To accommodate this shift, industry standards have made adjustments accordingly. For example, SAE J2954 recently introduced higher power classes, such as WPT3 (11 kW), WPT4 (22 kW), and WPT5 (50 kW) [4].

Manuscript received November 4, 2020; revised February 9, 2021; accepted April 3, 2021. Date of publication April 12, 2021; date of current version June 30, 2021. Recommended for publication by Associate Editor O. Lucia. *(Corresponding author: Wenwei Victor Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3071516.

Digital Object Identifier 10.1109/TPEL.2021.3071516

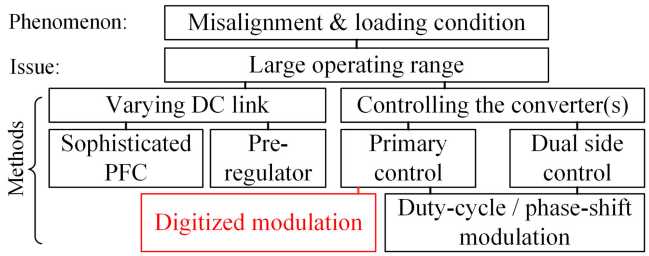


Fig. 1. Methods used to overcome the large operating range of a wireless EV charger (red is the focus of this article).

One of the challenges with the high-power wireless EV charging is that the system needs to cope with a large operating range. As shown in Fig. 1, there are two main factors that contribute to the need for a large operating range: the large variation in the battery voltage with its state of charge (typically 280 V $< V_{\text{battery}} <$ 420 V), and the large variation in the coupling factor due to the misalignment between the primary and secondary couplers (typically $0.1 < k < 0.3$) [4], [5]. Combining these two factors, the loading condition can be varying up to 450%. As shown in Fig. 1, to maintain the rated power transfer while coping with the large operating range, the two most widely adopted methods are identified: varying dc-link voltage and controlling the converters.

To vary the dc-link voltage, researchers have developed sophisticated power factor correction circuits (PFCs) [6]. However, in this case, a significantly large dc-link voltage variation is required, leading to a PFC stage and a primary IPT converter stage design with overrated switches. As an example, consider a single-phase boost-type PFC. The minimum output dc voltage it can produce is typically 350 V. Since the loading condition can change by 450%, the PFC is required to generate up to 1575 V. This means the entire primary-side power conversion system needs to handle at least 1600 V. As such, even the 1700-V-rated SiC devices cannot be used when a 20% safe margin is considered. In comparison to the conventional PFC designs, the more sophisticated PFC designs often need either more complex filters or more complex sensing/control circuitry [7]. Alternatively, in some designs, the dc-link voltage is regulated using an additional dc–dc preregulator that is placed between the PFC and the primary IPT converter [8], [9]. Such a design minimizes the losses in the primary IPT converter, which operates at or near

85 kHz, and simplifies the requirements of the PFC circuit. As shown in [8], a four-switch buck–boost can be used as the dc–dc preregulator. However, even with the aid of the PFC stage voltage regulation, the dc–dc stage still needs to handle a wide operating range. The buck–boost inductor will have to be significantly large to maintain a continuous mode operation, which could result in a bulky and expensive solution. The four switches will also need to be rated for a high-current rating, and typically multiple parallel-connected power semiconductors are necessary to form each switch [8], further increasing the cost of the system.

Apart from varying the dc-link voltage, the IPT converters can also be controlled to achieve power regulation. The most straight forward design uses only the primary-side control, which typically employs either phase-shift or duty-cycle modulation of a full-bridge (FB) converter to regulate the current in the primary coupler [10]. Modulating the FB converter to maintain constant power transfer across the entire operating range causes significantly higher semiconductor losses due to higher current stress and unfavorable switching conditions (i.e., hard switching). Often expensive power modules are utilized to ensure the semiconductors operate within their safe operating area [10], [11]. Filters and snubbers are also required to minimize the generation of electromagnetic interference (EMI) from hard switching [12]. To reduce the burden on the primary-side power electronics (i.e., PFC and the primary IPT converter), dual-side control is often utilized in high-power systems to counter the wide operating range [13]–[15]. Dual-side control uses phase-shift or duty-cycle modulation for both the primary and secondary sides, thus enabling impedance matching and improving the ac–ac efficiency. However, inevitably, this solution increases the cost and complexity of the secondary-side electronics, making it undesirable from the EV manufacturers' perspective.

As an alternative solution, this article proposes a new digitized modulation scheme, which allows the converter to use primary-side control and maintain a zero voltage switching (ZVS) through the entire operating range specified in SAE J2954. A schematic of the IPT system using the proposed modulation scheme is shown in Fig. 2.

The primary IPT converter is built with Si MOSFETs and is implemented using the integrated boost multilevel converter (IBMC) topology proposed in [16]. It consists of six series-connected half-bridge SMs forming each arm of the converter, and the two arms are connected to the dc power source $V_{\rm DC}$ through dc inductors L_1 and L_2. Each arm, together with the associated dc inductor of an IBMC, functions as a boost converter, therefore, enabling it to generate a boosted ac output voltage to drive the primary IPT coupler, $L_{\rm pt}$. This unique configuration also allows the IBMC topology to be controlled using the proposed digitized modulation scheme. Unlike the duty-cycle modulation scheme that was used in [16], when an IBMC is controlled using the proposed digitized modulation scheme, each SM will only operate at either a 0%, 50%, or 100% duty cycle. As a result, this new modulation scheme generates a square-wave output voltage, $v_{\rm pi}$, that has a controllable amplitude without the need for a preregulator. The primary IPT converter in Fig. 2, when controlled using the proposed

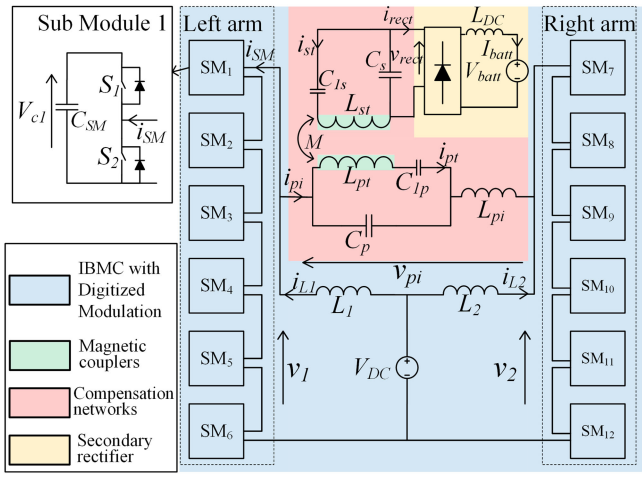


Fig. 2. Si MOSFET-based IPT system with the proposed digitized modulation.

modulation scheme, can generate 12 different $v_{\rm pi}$ amplitudes, and hence, this new modulation scheme is named a "digitized modulation" scheme. The ability to generate a square-wave $v_{\rm pi}$ with a variable amplitude ensures ZVS over a wide operating range, reducing switching losses, generation of EMI, and the complexity of the gate-driver circuitry.

The main focus of this article is to discuss the operating principles of the proposed digitized modulation scheme in the context of an IBMC-based primary-side-controlled IPT system. This article is structured as follows. First, using the IPT system shown in Fig. 2 as a case study, the proposed digitized modulation scheme is explained. This is followed by a discussion on the capacitor voltage balancing algorithm. After deriving a detailed mathematical model of the IPT system shown in Fig. 2, the ZVS operation range is explored. Next, several key converter design considerations are discussed, such as semiconductor device selection. Finally, a 7.7-kW standard-compliant IPT system that employs 200-V Si MOSFETs is built and experimentally tested under the conditions stated in SAE J2954 WPT2/Z2, to highlight the key features of the proposed digitized modulation scheme.

II. Proposed Digitized Modulation Scheme

Although an IBMC can have any number of SMs, this article studies an IBMC with 12 SMs, shown in Fig. 2, to highlight the operating principles of the proposed digitized modulation scheme. The IBMC, being a voltage source converter (VSC), drives the LCL compensation network on the primary-side of the IPT system, consisting of L_{pi}, C_p, C_{1p}, and L_{pt}. The magnetic flux in the primary magnetic coupler, $L_{\rm pt}$, is coupled with the secondary-side magnetic coupler, $L_{\rm st}$. $L_{\rm st}$ forms a parallel compensation network on the secondary-side consisting of $L_{\rm st}$, C_{1s}, and C_s. The parallel compensation network on the secondary feeds the EV battery through a diode rectifier. The parameters of this system are shown in Table I.

Each SM of an IBMC consists of two switches (S_1 and S_2) and a storage capacitor ($C_{\rm SM}$), as shown in Fig. 2. Turning on the top switch of each SM inserts its storage capacitor in series with the current flow, $i_{\rm SM}$, while turning ON the bottom switch

TABLE I
PARAMETERS OF THE IBMC-BASED IPT SYSTEM

Parameter	Value
L_{pi} & R_{ac}	26.5 μH & 28 mΩ
C_p & ESR	137 nF & 10 mΩ
L_{pt} & R_{ac}	64.0 μH & 93 mΩ
C_{1p} & ESR	93.7 nF & 17 mΩ
L_{st} & R_{ac}	18.3 μH & 24 mΩ
C_{1s} & ESR	423 nF & 3.6 mΩ
C_s & ESR	348 nF & 4.5 mΩ
L_{DC} & DCR	480 μH & 30 mΩ
L_1,L_2 & DCR	440 μH & 27 mΩ
C_{SM} & ESR	90 μF & 1.4 mΩ
f_{sw}	85 kHz
Coupling factor k	0.138 - 0.31
V_{DC}	350 - 450 V
V_{batt}	280 - 420 V
Power	7.7 kW
Switches	200V MOSFET IPP110N20N3
Diodes	DSEI30-10A

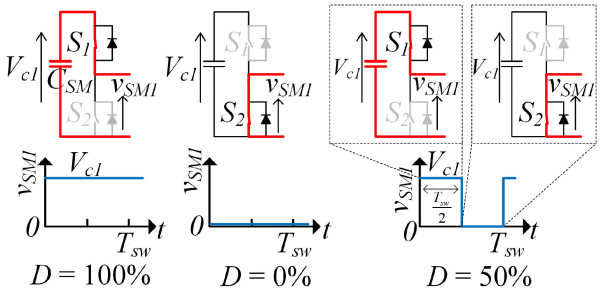


Fig. 3. Three duty-cycle operations of an SM when utilizing digitized modulation.

bypasses the current flow. As discussed in [16], the mth SM of each arm of this IBMC could be operated at any duty cycle, D_m, where D_m is the ratio between the time the mth SM is inserted and the switching period, T_{sw}. m in this case ranges between 1 and 6 as there are six SMs in each arm. However, with the proposed digitized modulation scheme, during one switching period T_{sw}, each SM could only be operated in the following three duty cycles: 100%, 0%, or 50%. These three duty-cycle operations are shown in Fig. 3.

In order to model the proposed system, initially, assume that the voltage across the capacitor in each SM, V_{Cm}, is maintained on average at an equal voltage, $V_{C_{\text{avg}}}$, using a voltage balancing algorithm [17]. Details of the voltage balancing algorithm will be explained in Section IV. In each arm, a number of SMs are operated with duty cycle of 100%, b number of SMs are operated with duty cycle of 0%, and c number of SMs are operated with duty cycle of 50%. Each combination of $a, b,$ and c is referred as a duty-cycle pattern. Using this convention, the average output voltage produced by each arm can be expressed by

$$\overline{v_1} = \overline{v_2} = \sum_{m=1}^{6} [V_{Cm} \cdot D_m] = V_{C_{\text{avg}}}(a \cdot 100\% + b \cdot 0\% + c \cdot 50\%) \tag{1}$$

TABLE II
IBMC OUTPUT VOLTAGE LEVELS AT DIFFERENT DUTY-CYCLE PATTERNS WHEN $V_{\text{DC}} = 400$ V

Duty-Cycle Pattern No.	a*	b*	c*	SM voltage (2)	$\hat{v_{pi}}$ (7)
#1	0	0	6	133 V	800 V
#2	1	0	5	114 V	571 V
#3	1	1	4	133 V	533 V
#4	1	2	3	160 V	480 V
#5	2	0	4	100 V	400 V
#6	2	1	3	114 V	343 V
#7	3	0	3	89 V	267 V
#8	3	1	2	100 V	200 V
#9	4	0	2	80 V	160 V
#10	3	2	1	114 V	114 V
#11	4	1	1	89 V	89 V
#12	5	0	1	73 V	73 V

*Note: a = Number of SMs running 100% duty cycle;
b = Number of SMs running 0% duty cycle;
c = Number of SMs running 50% duty cycle.

where $\overline{v_1}$ and $\overline{v_2}$ are the averages of v_1 and v_2, respectively. Under steady-state conditions, because of the volt-second rule, the average voltages across L_1 and L_2 should be zero. Therefore, $\overline{v_1}$ and $\overline{v_2}$ should be also equal to V_{DC} (i.e., $\overline{v_1} = \overline{v_2} = V_{\text{DC}}$), and substituting this in (1) results in

$$V_{C\text{avg}} = \frac{V_{\text{DC}}}{\sum_{m=1}^{6}[D_m]} = \frac{V_{\text{DC}}}{a + 0.5c} \tag{2}$$

The key feature of the proposed digitized modulation scheme is its ability to generate a square-wave output voltage waveform with varying amplitudes using different duty-cycle patterns. Since each a, b, and c can have a value between 0 and 6, and $a + b + c$ must add up to 6 as well, there are 28 possible duty-cycle patterns. However, not all 28 duty-cycle patterns can generate meaningful waveforms. Table II illustrates the realizable duty-cycle patterns and the corresponding output voltage amplitudes of the 12 SM IBMC when V_{DC} is 400 V. These duty-cycle patterns also ensure V_{C_m} is less than 200 V as the IBMC employs 200-V MOSFETs.

Fig. 4 demonstrates how the output voltage can be regulated in an IBMC using the digitized modulation. In Fig. 4(a), the operating points OP_1, OP_2, and OP_3 represent, respectively, 100%, 70%, and 40% of normalized $\hat{v_{pi}}$ and these points correspond to the duty-cycle patterns #1, #2, and #6. As illustrated in Fig. 4(b), at each of the three operating points, the digitized modulation scheme enables the IBMC to generate a square-wave output while varying its amplitude. For comparison, the operating points OP_1', OP_2', and OP_3' represent, respectively, 100%, 70%, and 40% of the normalized $\hat{v_{\text{pi}}}$ generated by a FB converter using duty-cycle/phase-shift modulation. Duty-cycle/phase-shift modulation of a FB converter leads to hard switching at OP_2' and OP_3'. In contrast, the digitized modulation ensures all SMs in the IBMC soft-switch when generating any one of the 12 duty-cycle patterns. To demonstrate how a duty-cycle pattern can be synthesized, consider the operation of the IBMC during the first and last half of the switching period.

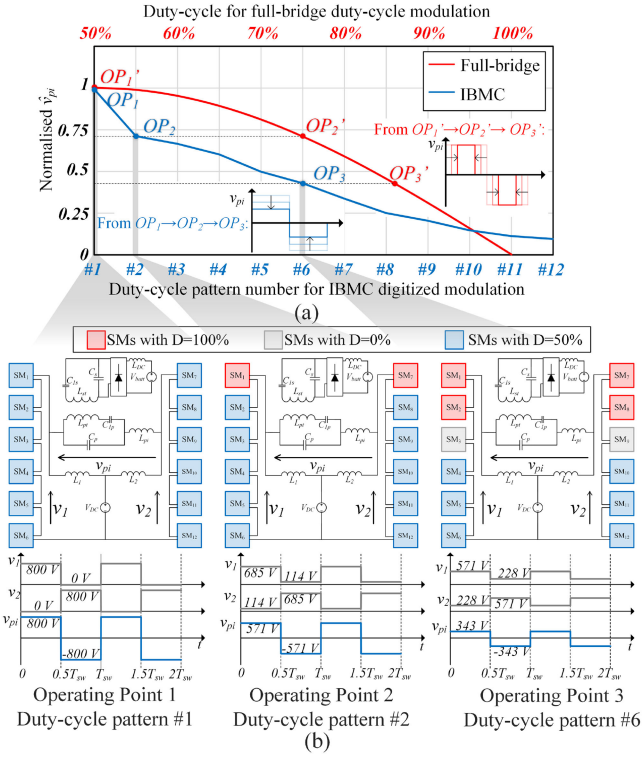


Fig. 4. (a) Regulating $\hat{v_{\rm pi}}$ in an IBMC with digitized modulation versus in a traditional FB with duty-cycle modulation. (b) Digitized modulation at point "OP1" (duty-cycle pattern #1, generating 100% of normalized $\hat{v_{\rm pi}}$), at point "OP2" (duty-cycle pattern #2, generating 70% of normalized $\hat{v_{\rm pi}}$), and at point "OP3" (duty-cycle pattern #6, generating 40% of normalized $\hat{v_{\rm pi}}$) .

1) *From 0 to 0.5T_{sw}:* The SMs in the left arm that are operating with 50% duty cycle are inserted during this half of the switching period. Therefore, the amplitude of v_1 is the sum of voltages across the left arm SMs operating with 50% and 100% duty cycles, as given by

$$v_1(t) = (a+c)V_{C\rm avg} = \frac{a+c}{a+0.5c}V_{DC},\ \ 0 \le t < 0.5T_{\rm sw}. \tag{3}$$

The SMs in the right arm that are operating with 50% duty cycle are bypassed during this half of the switching period. Therefore, v_2 is the sum of voltages across the right arm SMs operating with 100% duty cycle as given by

$$v_2(t) = aV_{C\rm avg} = \frac{a}{a+0.5c}V_{DC},\ \ 0 \le t < 0.5T_{\rm sw}. \tag{4}$$

2) *From 0.5T_{sw} to T_{sw}:* During this half of the switching period, the SMs in the left arm that are operating with 50% duty cycle are bypassed, while the SMs in the right arm that are operating with 50% duty cycle are inserted. Therefore

$$v_1(t) = \frac{a}{a+0.5c}V_{\rm DC}\quad v_2(t) = \frac{a+c}{a+0.5c}V_{\rm DC},$$
$$0.5T_{\rm sw} \le t < T_{\rm sw}. \tag{5}$$

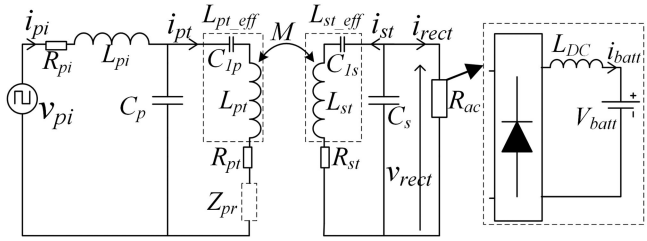


Fig. 5. Overview of a typical IPT system.

Since $v_{pi} = v_1 - v_2$, combining (3)–(5), $v_{\rm pi}$ can be expressed by the periodic piecewise function as

$$v_{\rm pi}(t) = v_{\rm pi}(t+T_{\rm sw}) = \begin{cases} \dfrac{c}{a+0.5c}V_{\rm DC}, & 0 \le t < 0.5T_{\rm sw} \\ \dfrac{-c}{a+0.5c}V_{\rm DC}, & 0.5T_{\rm sw} \le t < T_{\rm sw}. \end{cases} \tag{6}$$

The amplitude of $v_{\rm pi}$, which always takes the shape of a square-wave, depends on the duty-cycle pattern applied as given by

$$\hat{v_{pi}} = \frac{c}{a+0.5c}V_{\rm DC}. \tag{7}$$

III. Power Regulation Using the Digitized Modulation

To highlight how the proposed digitized modulation scheme can be used to regulate the power flow in a primary-side-controlled IPT system, the circuit can be simplified as shown in Fig. 5. In this circuit, the IBMC is represented by a voltage source $v_{\rm pi}$ as described by (6), and the rectifier and the EV battery can be represented by an ac resistor.

Assuming the dc inductor $L_{\rm DC}$ is large enough and the diode rectifier operates in the continuous conduction mode, the average voltage on the left-hand side of $L_{\rm DC}$ must equal to its right-hand side average voltage

$$\int_t^{t+1/f_{sw}} \hat{v}_{\rm rect}\sin(2\pi f_{\rm sw}t) = V_{\rm batt}. \tag{8}$$

This can be rearranged to

$$\frac{4}{\pi}\hat{v}_{\rm rect} = \frac{2\sqrt{2}}{\pi}V_{\rm rect} = V_{\rm batt} \tag{9}$$

where $\hat{v}_{\rm rect}$ and $V_{\rm rect}$ are the peak and rms value of $v_{\rm rect}$, respectively.

To further simplify the diode rectifier behavior, the input power of the diode rectifier is assumed to be equal to the output power as

$$V_{\rm rect}I_{\rm rect} = V_{\rm batt}I_{\rm batt} \tag{10}$$

which yields

$$\frac{\pi}{2\sqrt{2}}I_{\rm rect} = I_{\rm batt}. \tag{11}$$

By combining (9) and (11), the equivalent load ac resistor can be expressed as

$$R_{\rm ac} = \frac{V_{\rm rect}}{I_{\rm rect}} = \frac{\frac{\pi}{2\sqrt{2}}V_{\rm batt}}{\frac{2\sqrt{2}}{\pi}I_{\rm batt}} = \frac{\pi^2}{8}\frac{V_{\rm batt}}{I_{\rm batt}}. \tag{12}$$

Similar to the analysis in [13] and [18], the phasor of the nth harmonic of the ac current sourced by the IBMC can be derived as

$$I_{\text{pi\_}n} = \frac{V_{\text{pi\_}n}}{R_{\text{pi}} + X_{L_{\text{pi}}} + [X_{C_p} // (R_{\text{pt}} + X_{L_{\text{pt}}} + X_{C_{1p}} + Z_{\text{pr}})]} \tag{13}$$

where $V_{\text{pi\_}n}$ is the amplitude of the nth harmonic of (6)

$$V_{\text{pi\_}n} = \frac{4\hat{v_{\text{pi}}}}{n\pi} \sin\left(\frac{n\pi}{2}\right)$$

and

$$Z_{\text{pr}} = \frac{\omega^2 M^2}{X_{L_{\text{st}}} + R_{\text{st}} + X_{C_{1s}} + (X_{C_s} // R_{\text{ac}})}.$$

$X_{L_{\text{pi}}}, X_{C_p}, X_{C_{1p}}, X_{L_{\text{pt}}}, X_{L_{\text{st}}}, X_{C_{1s}}$, and X_{C_s} are the reactances of $L_{\text{pi}}, C_p, C_{1p}\, L_{\text{pt}}, L_{\text{st}}, C_{1s}$, and C_s, respectively, at a frequency $2n\pi f_{\text{sw}}$ (i.e., at each nth harmonic). $R_{\text{pi}}, R_{\text{pt}}$, and R_{st} are the ESR of L_{pi}, L_{pt}, and L_{st}, respectively. M is the mutual inductance between L_{pt} and L_{st} ($M = k\sqrt{L_{\text{pt}} L_{\text{st}}}$, and k is the magnetic coupling factor).

In order to minimize the volt-amp (VA) rating of the converters, both the primary and the secondary compensation networks are typically tuned to the fundamental frequency, f_{sw} of the voltage source v_{pi}, as given by

$$\omega_{\text{sw}} L_{\text{pt\_eff}} = \omega_{\text{sw}} L_{\text{pt}} - \frac{1}{\omega_{\text{sw}} C_{1p}} = \omega_{\text{sw}} L_{\text{pi}} = \frac{1}{\omega_{\text{sw}} C_p} \tag{14}$$

$$\omega_{\text{sw}} L_{\text{st\_eff}} = \omega_{\text{sw}} L_{\text{st}} - \frac{1}{\omega_{\text{sw}} C_{1s}} = \frac{1}{\omega_{\text{sw}} C_s} \tag{15}$$

where $\omega_{\text{sw}} = 2\pi f_{\text{sw}}$. Under tuned conditions, most of the power transfer happens at the fundamental frequency [18], and therefore, the power delivered to the EV battery is given by

$$P = \frac{k\sqrt{L_{\text{pt}} L_{\text{st}}}\, \hat{v_{\text{pi}}} V_{\text{batt}}}{\omega_{\text{sw}} L_{\text{pi}} L_{\text{st\_eff}}}. \tag{16}$$

As seen from (16), in a primary-controlled IPT system, $\hat{v_{\text{pi}}}$ is the only variable that can be controlled to regulate the power flow when operating conditions change (i.e., changes in k and/or V_{batt}). Since the primary focus of this article is to demonstrate the operating principles of the proposed digitized modulation, $\hat{v_{\text{pi}}}$ is derived through an open-loop controller. At each operating point, the required $\hat{v_{\text{pi}}}$ is calculated using (16), and the duty-cycle pattern that is needed to achieve this $\hat{v_{\text{pi}}}$ is determined using (7). The microcontroller is then programmed to operate the SMs at this predetermined duty-cycle pattern using the control algorithm shown in Fig. 6.

When using the digitized modulation scheme, there are a fixed number of voltage steps that can be generated, as shown in Table II. However, these discrete values might not satisfy the finer voltage steps that the controller needs to regulate the power. Therefore, in the prototype system, the input dc bus voltage is also controlled to support the regulation. The input voltage variation considered in this case is 350 V $< V_{\text{DC}} <$ 450 V, which is a reasonable voltage range for a typical single-phase PFC. The full spectrum of $\hat{v_{\text{pi}}}$ that can be generated when varying the duty-cycle pattern applied and the dc bus voltage can be visualized in Fig. 7.

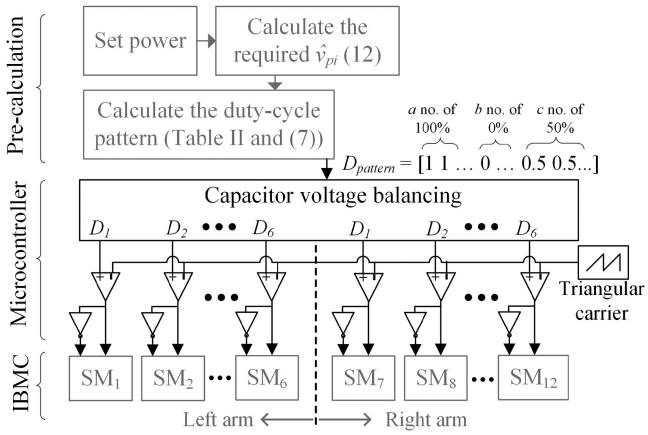


Fig. 6. Block diagram for the open-loop controller for an IBMC with digitized modulation.

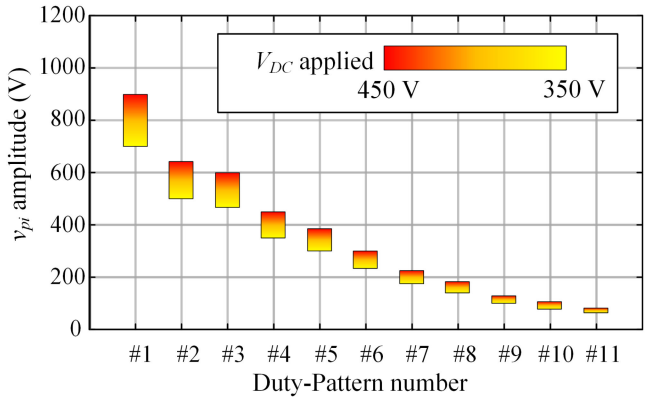


Fig. 7. Varying dc voltage and duty-cycle pattern to achieve finer steps of v_{pi} amplitude.

This article focuses on the operating principles of the digitized modulation scheme under steady-state conditions, and the dynamic response of the IBMC-based system is out of scope. This is because in a stationary wireless EV charging system, no sudden load change is expected, and the loading transient time is considered "slow." As stated in the SAE J2954 standard, when the vehicle side and the ground side negotiates the power flow through high-frequency communication channels such as WiFi or Bluetooth, the power level increases at a rate slower than 2 kW/s. Due to these reasons, this article only demonstrates an open-loop controller for power regulation.

Although the duty-cycle pattern is derived using an open-loop controller, as discussed in the proceeding section, a closed-loop controller was employed to balance the voltages across SMs.

IV. SM Capacitor Voltage Balancing

In this section, the details of the closed-loop capacitor voltage balancing algorithm will be discussed. When using the digitized modulation scheme, during a particular switching period, the amount of the current entering an SM to charge/discharge its storage capacitor depends on the duty cycle the SM is operated at. The change in the voltage across the storage capacitor during

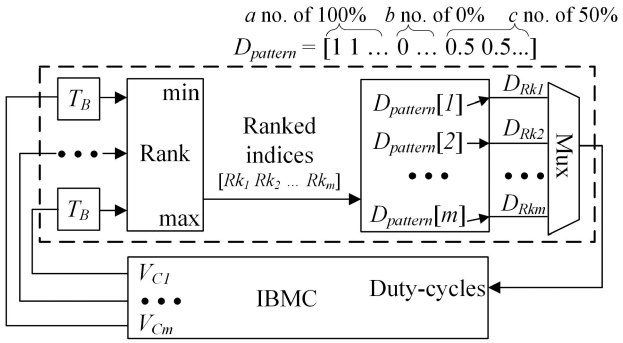


Fig. 8. IBMC voltage-balancing algorithm block diagram.

a switching period can be expressed by

$$\Delta V_{Cm} = \frac{1}{C_{\text{SM}}} \int_0^{D_m T_{\text{sw}}} i_{\text{SM}}(t)dt \quad (m = 1, 2, ...6). \tag{17}$$

Therefore, during one switching period, an SM operating with 100% duty cycle will see an increase in the capacitor voltage because the average of I_{SM} is always positive (i.e., $\bar{I}_{\text{SM}} = \frac{P}{2V_{\text{DC}}}$). $\bar{I}_{\text{SM}}$ can be substituted into (17) to obtain

$$\Delta V_{C\_100\%} = \frac{P}{2V_{\text{DC}} f_{\text{sw}} C_{\text{SM}}}. \tag{18}$$

Because the volt-second product across L_1 should be 0, the average voltage on the left-hand side of L_1 must be equal to V_{DC} and $\sum_{m=1}^{6} \Delta V_{Cm}$ must equal to 0. Therefore, within one switching period, an SM operating with 50% duty cycle will see a decrease in the capacitor voltage, which equals to

$$\Delta V_{C\_50\%} = -\frac{a}{c} \Delta V_{C\_100\%} = -\frac{aP}{2cf_{\text{sw}} V_{\text{DC}} C_{\text{SM}}}. \tag{19}$$

Note, an SM operating with 0% duty cycle will see no change in the voltage across its storage capacitor, since the current is completely bypassed.

To gain an insight on how the capacitor voltage varies, consider an example where the IBMC is controlled using the duty-cycle pattern #6 (i.e., $a = 2, b = 1, c = 3$) shown in Fig. 4(b). According to (18) and (19), the capacitor voltage of the SMs running 100% duty cycle will increase, while the SMs running 50% duty cycle will decrease. If operated in this manner, eventually, the 50% duty cycle SMs will have 0 V, while the voltage across 100% duty cycle SMs will increase to compensate for SMs at 0 V. Therefore, a closed-loop voltage balancing algorithm is implemented to maintain the same average voltage across all SMs. This algorithm rotates the duty cycle of each SM between 100%, 0%, and 50%, while maintaining the duty-cycle pattern (i.e., $a = 2, b = 1, c = 3$ in this example). This algorithm balances SMs in each arm individually and executes at a frequency f_B, which is one Nth of the switching frequency (i.e., $f_B = f_{\text{sw}}/N$). This ensures that within one switching period, the converter output voltage waveform shape stays the same.

A block diagram of the balancing algorithm is shown in Fig. 8. The voltage across each SM in an arm at the end of every T_B period is read ($T_B = 1/f_B$) and ranked from high to low. The indices of the ranked SMs get passed to a rearranging block, where the SMs with the lowest voltages will get assigned to operate with 100% duty cycle while the SMs with the highest voltages will be assigned to operate with 50% duty cycle. The remaining SMs will be assigned to operate with 0% duty cycle as needed to generate a specific duty-cycle pattern. This way, during the next time period T_B, the lowest voltage SMs will see an increase in their voltages, and the highest voltage SMs will see a decrease in their voltages. A higher f_B means the duty cycles of the SMs are rotated more frequently, which results in lower voltage variations since the magnitude of the SM voltage variation with balancing can be expressed by

$$|\Delta V_{Cm}| = \frac{P}{2V_{\text{DC}} f_B C_{\text{SM}}} \quad (m = 1, 2, ..., 6). \tag{20}$$

V. ZVS Operation of the Proposed System

This section explains how the proposed digitized modulation scheme ensures an IBMC operates with ZVS under all conditions. Only the left arm is considered since the right arm operation is identical but phase shifted by 180°. As shown in Fig. 2, the current entering the left arm SMs consists of two parts

$$i_{\text{SM}}(t) = -i_{\text{pi}}(t) + i_{L1}(t). \tag{21}$$

Using (13), i_{pi} can be expressed by

$$i_{\text{pi}}(t) = \sum_{n=1,3,..}^{\infty} [|I_{\text{pi\_}n}| \cos(n\omega_{\text{sw}} t + \angle(I_{\text{pi\_}n}))]. \tag{22}$$

The current in each dc inductor together with the ripple component can be expressed as

$$i_{L1}(t) = \frac{P}{2V_{\text{DC}}} + \frac{1}{L_1} \int_0^{T_{\text{sw}}} [V_{\text{DC}} - v_1(t)]dt. \tag{23}$$

The condition to achieve ZVS operation of a half-bridge is well established and can be found in the literature [19].

To gain a clear understanding of the ZVS operations of an IBMC operating with the proposed modulation scheme, the v_{pi} and i_{SM} waveforms during one switching period are shown in Fig. 9(a). Note that the parameters of the example system considered in this article are in Table I. The voltage and current waveforms of the high-side MOSFET ($S1$) in one of the SMs being inserted at $t = 0$ are depicted in Fig. 9(b). In this switching transition, $S2$ is getting turned OFF during $0 - t_2$. During $t_2 - t_3$, the SM current starts charging and discharging the output capacitance (C_{oss}) of $S2$ and $S1$ (consisting of drain–source capacitor and gate–drain capacitor where $C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$), respectively. This current is indicated in purple. Therefore, only the remaining current I_{ch2} is passing through the $S2$ channel (i.e., $I_{\text{ch2}} = I_{\text{SM}} - I_{\text{Coss1}} - I_{\text{Coss2}}$), indicated in red. During this period, the $S2$ turn-OFF loss is small (indicated in the shaded area) because the majority of the SM current flows through C_{oss}. The $S2$ channel current will decay down to 0 A as the gate–source voltage decreases below the threshold V_{th}, and now i_{SM} starts to flow through the body diode of $S1$, indicated in green. The turn-ON gate signal is applied to $S1$ after its body diode starts conducting, resulting in approximately 0 V across $S1$ drain–source at the instance of turn-ON. Therefore, zero

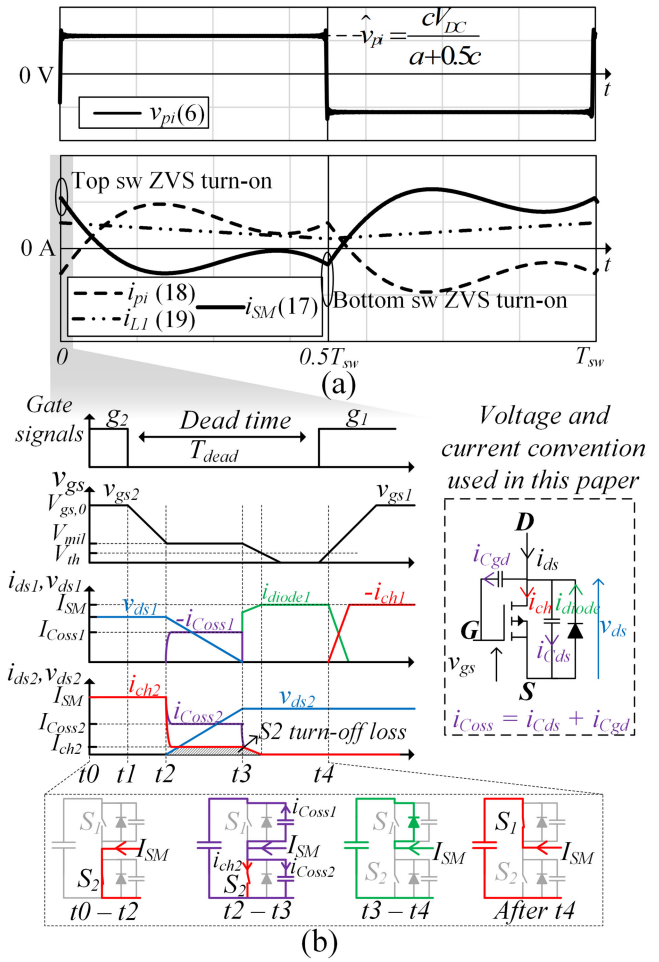


Fig. 9. (a) IBMC voltage and currents during one switching period. (b) SM voltage and currents during top switch turn-ON instance (top switch ZVS).

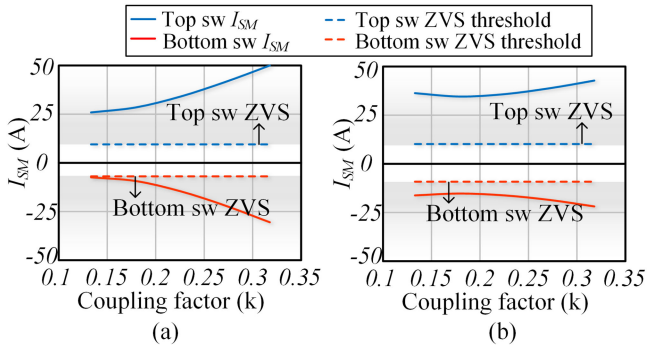


Fig. 10. SM current for top and bottom switch ZVS operations when battery voltage is (a) 280 V and (b) 420 V.

voltage turn-ON is achieved. Similarly, we can also show that at $t = 0.5T_{\text{sw}}$ the $S2$ achieves zero voltage turn-ON.

By substituting $t = 0$ and $t = 0.5T_{\text{sw}}$ into (21) and using the parameters presented in Table I, the SM currents at turn-ON events of S1 and S2, respectively, are calculated under all operating conditions. The results are shown in Fig. 10, where the solid lines represent the i_{SM} at the switching instances. The dotted lines represent the i_{SM} threshold to ensure ZVS operation,

TABLE III
PARAMETERS OF STATE-OF-THE-ART GaN Si SiC SWITCHES

		GaN	Si	SiC
Per switch	Name	EPC2034	IPP110N20N	C2M0025120D
	VdsMAX (V)	200	200	1200
	Rds (mΩ)	6	10	25
	Qoss (nC)	96	162	242
	Qrr (nC)	0	640	406
	Qg (nC)	11	65	161
	Cost (USD)	6.2	5.6	70
Per arm	No. of switches	6	6	1
	Total Rds (mΩ)	36	60	25
	Total Eon (μJ)	88.8*	283.2*	434*
	Total Eoff (μJ)	34.2*	60.6*	92.3*
	Total cost (USD)	37.2	33.6	70.0

*Note: The switching losses are measured at 900 V 10 A.

which is calculated by

$$|I_{\text{SM(ZVS)}}| > 2Q_{\text{oss}} * (a + c)/T_{\text{dead}}. \tag{24}$$

Note that the deadtime implemented is 200 ns, and the Q_{oss} of the MOSFET used is 160 nC. Fig. 10 demonstrates that an IBMC with the digitized modulation can achieve ZVS operation across the entire SAE J2954 WPT2/Z2 operating range while also transferring rated power.

VI. CONVERTER DESIGN CONSIDERATIONS

One of the advantages of using a multilevel converter design is the ability to share the high-voltage stress across a number of low-voltage switches. The study in [20] shows that stacking up a number of low-voltage switches can result in an equivalent switch with a significantly higher figure of merit than a single high-voltage switch. Therefore, multilevel converters can achieve lower losses, resulting in a higher converter efficiency and a smaller heatsink size.

In this article, the state-of-the-art Si, GaN, and SiC switches were considered as options to implement the IBMC. Their properties are summarized in Table III. The switching losses of the switches are derived using the SPICE model provided by the manufacturers. In the case of the 1200-V SiC switch, it is assumed to be used in a traditional FB converter, and therefore, the properties of a single switch are considered. The 200-V Si and GaN switches are assumed to be used in the IBMC in Fig. 2, and therefore, the properties of an equivalent switch made from six of them are considered to make a fair comparison with the high-voltage SiC switch. Although the SiC switch has the lowest conduction loss, both low-voltage Si- and GaN-based solutions provide better switching properties. GaN switches, in particular, have the best switching performance due to their low Q_g and no reverse recovery charge. However, the drawback of GaN switches is heat management because of their small package. Given the operating range required in a primary-controlled IPT converter, even with superior switching properties, each GaN switch could experience up to 8 W of loss, which would result in an unsafe junction temperature. Although custom-made heatsink

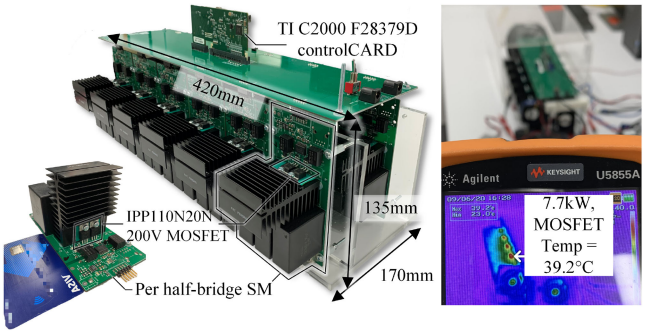


Fig. 11. 7.7-kW prototype IBMC utilizing 200-V Si MOSFETs.

or liquid cooling solutions could be employed [21], the thermal design complexity significantly increases for such systems.

On the other hand, the Si-based solution is the cheapest and allows a simpler thermal design. The main drawback of a Si MOSFET is its body diode's high reverse recovery charge, which often results in high switching losses when hard switching. However, the proposed modulation ensures ZVS operation across the entire operating range, which reduces the switching loss in the Si MOSFETs significantly, making them suitable for a 7.7-kW 85-kHz wireless EV charger. Thus, the prototype of the IBMC presented in this article, shown in Fig. 11, was built using the Infineon IPP110N20 N 200-V MOSFETs. The size of each SM is comparable to a standard credit card, and the multilevel design allows distributing the thermal load across multiple small heatsinks. The dimension of each SM is 134 mm × 65 mm × 65 mm ($L \times H \times W$), and the dimension of the IBMC prototype is 420 mm×170 mm × 135 mm($L \times H \times W$). As a proof of concept prototype, it was designed to have sufficient space for debugging. The volume of the design can be greatly reduced if refined to a production-ready design. As captured by the thermal camera, when transferring 7.7 kW at the worst-case operating point (i.e., $k = 0.31$), the switches operate at about 39.2° C. In this design, a UCC20520 isolated half-bridge gate driver is used in each SM, which generates a 100-ns dead-time ensuring shoot-through protection of the two switches. TI F28379D controlCARD is used as the control unit that implements the open-loop controller mentioned in Fig. 6 and the voltage-balancing algorithm mentioned in Fig. 8. As discussed previously, the control algorithm ensures the voltage stresses are balanced across all SMs, hence, avoiding issues due to timing mismatch between the SMs.

VII. Experiment Results

To highlight the benefits offered by an IBMC using the proposed digitized modulation scheme, a prototype of the primary-side controlled IPT system shown in Fig. 2 is designed and built. The system parameters are shown in Table I. This design employs DD magnetic couplers on both the primary and secondary sides, which were built according to the specifications in the SAE J2954 WPT2/Z2 Test Stand. The dimensions of the couplers are also shown in Fig. 12.

To comply with the SAE J2954 WPT2/Z2 specifications, the prototype is designed to maintain power transfer at 7.7 kW

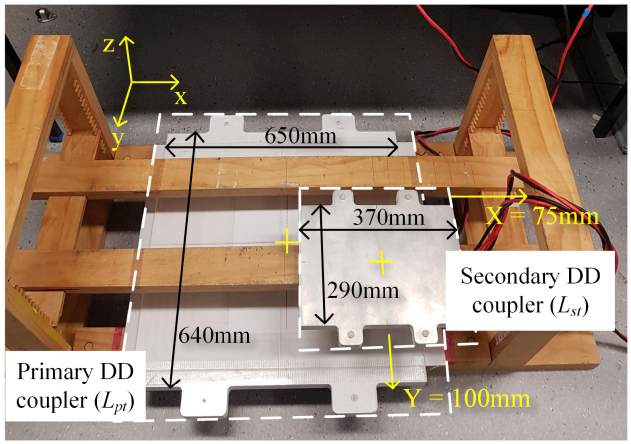
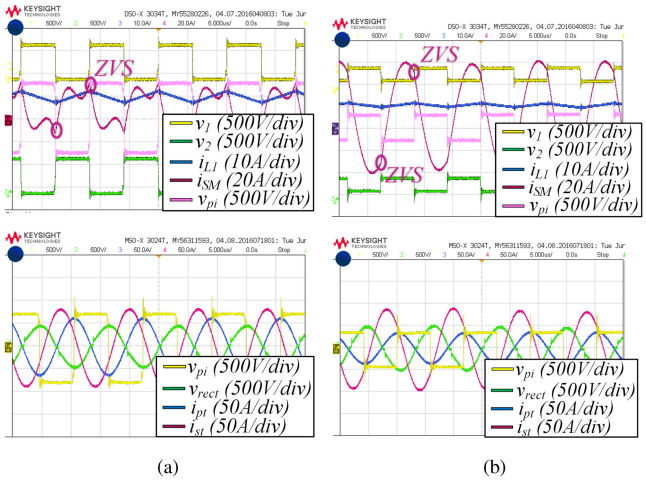


Fig. 12. SAE J2954 WP2/Z2 compliant DD magnetic couplers.



(a) (b)

Fig. 13. Waveforms when transferring 7.7 kW at two extreme cases: (a) the most misaligned position, $k = 0.138$, $V_{\text{batt}=280V}$, the system is running duty-cycle pattern #1 to produce the highest $\hat{v_{\text{pi}}}$, (b) the most aligned position $k = 0.31$, $V_{\text{batt}=420V}$, system is running duty-cycle pattern #6 to produce lower $\hat{v_{\text{pi}}}$.

under a vertical (Z) misalignment of 140–210 mm, a longitudinal (X) misalignment of 75 mm, and a lateral (Y) misalignment of 100 mm. The misalignments in (X, Y, Z) directions are measured from the center of the primary DD coupler to the center of the secondary DD coupler, as shown in Fig. 12. Misalignment leads to variations in the coupling factor, k, and to a lesser extent, the self-inductances of the couplers. When the secondary coupler is at (75 100 210), k is measured as the lowest at 0.138. When the secondary coupler is perfectly aligned with the primary and is at its lowest Z position, i.e., (0,0140), k reaches its highest, which is 0.31.

When transferring the rated power (i.e., 7.7 kW), the key waveforms of the IBMC-based IPT system operating at the most extreme conditions are shown in Fig. 13. Fig. 13(a) depicts the operation of the IBMC when the secondary magnetic coupler is at the most misaligned position ($X = 75$, $Y = 100$, and $Z = 210$) and the EV battery voltage is the lowest (i.e., 280 V). In this operating point, the IBMC needs to generate $\hat{v_{\text{pi}}}$ with the highest amplitude to drive the primary magnetic coupler at a higher current. Therefore, the duty-cycle pattern applied in

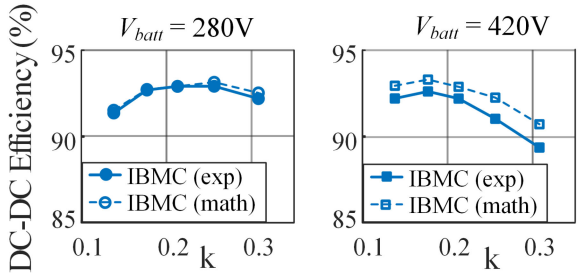


Fig. 14. DC–DC efficiency of the proposed prototype system.

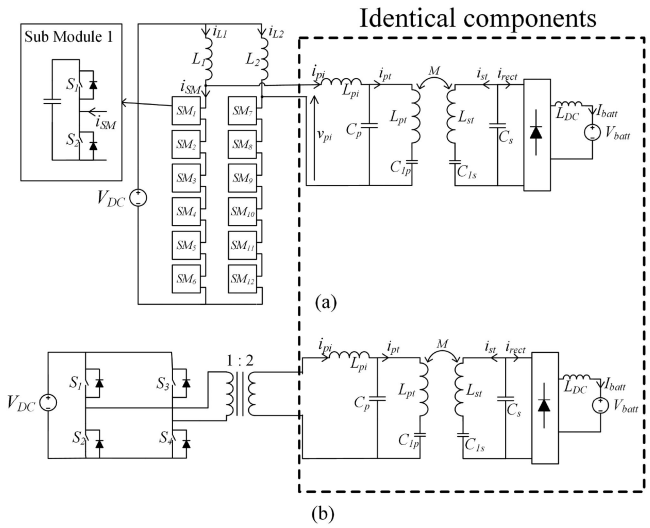


Fig. 15. Circuit diagrams of the comparison between (a) IBMC-based and (b) FB-based IPT systems.

this case is #1. Fig. 13(b) depicts the operation of the IBMC when the secondary magnetic coupler is in the perfectly aligned position (X=0, Y=0, Z=140) and the load battery voltage is at its highest (i.e., 420 V). In this operating point, the IBMC needs to generate $\hat{v_{\rm pi}}$ with the lowest amplitude to reduce the current in the primary magnetic coupler. Therefore, the duty-cycle pattern applied in this case is #6. The SM gating signals are shown at the top in Fig. 13(a) and (b).

The efficiencies of this prototype system at different alignment positions are plotted in Fig. 14. In the same plot, the theoretical efficiency is plotted too, the theoretical mathematical model uses the same component value as shown in Table I, and uses Infenion datasheet for the MOSFET conduction loss and switching losses. The theoretical efficiency matches closely with the experimental efficiency, which proves the accuracy of the mathematical model. Note, the higher deviation at higher battery voltage is due to the nonlinearity of the losses in the system with respect to temperature (e.g., coupler copper losses increases with higher temperature, but ferrite loss reduces with higher temperature).

Two IPT systems shown in Fig. 15 are used to conduct a comparison between the IBMC with a digitized modulation scheme and a traditional FB with phase-shift modulation. In order to ensure a fair comparison, in these two systems, the compensation networks and the secondary-side electronics are identical. The FB utilizes a 1:2 step-up transformer to match the

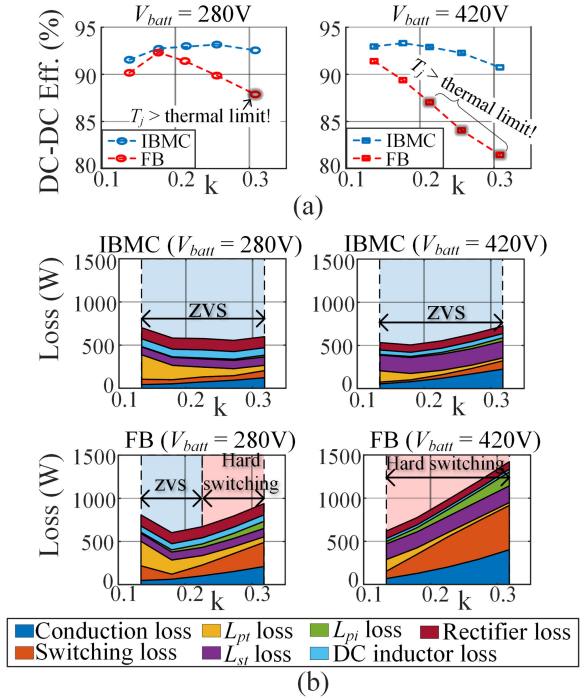


Fig. 16. (a) Efficiency and (b) loss breakdown between IBMC- and FB-based IPT systems.

output voltage with that of the proposed IBMC. The IBMC uses 200-V Si switches, whereas the FB uses the 1200-V SiC switches mentioned in Table III. The IBMC utilizes digitized modulation, and the FB uses phase-shift modulation. The efficiency of this comparison is shown in Fig. 16, and the loss breakdown of the two systems is shown in Fig. 16(b). The FB converter operating at a very low duty-cycle at high coupling positions or high battery voltages leads to high loss due to hard switching. On the other hand, the IBMC with digitized modulation benefits from the ZVS operation, leading to higher efficiency.

A high-level cost comparison of the IBMC and the FB (shown in Fig. 15) is provided in Table IV. It can be found the FB costs less than the IBMC with 12 SMs. However, since the PFC stage has a limited output voltage range, the FB needs to handle a large modulation depth, the FB switching conditions will suffer significantly. As predicted by the efficiency curve shown in Fig. 16, at the operating points highlighted in dark red, each switch in the FB will have higher than 100 W loss, which results in unsafe junction temperature in the device. In this case, multiple parallel-connected switches are needed to share the stress. If implemented in this manner, the number of switches needed to build an FB will be eight instead of four, increasing its price from $471 to $751.

VIII. Comparison With Existing Solutions

To highlight the benefits of the digitized modulation scheme used in an IBMC, the proposed IBMC-based IPT system is compared with state-of-the-art prototype systems from other research institutes at similar power levels. This comparison is shown in Table V. When considering the cost of the system, only the inverter semiconductor cost is compared. This is because

TABLE IV
COST COMPARISON BETWEEN THE PROPOSED IBMC AND THE FB DESIGNS

	IBMC				Full-bridge			
	Description	Unit price (USD)	Quantity	Cost (USD)	Description	Unit price (USD)	Quantity	Cost (USD)
Switches	Si MOSFET	5.6	24	134	SiC MOSFET	70	4	280
Drivers	Half-bridge drivers	8	12	96	Single MOSFET driver	10	4	40
Storage Capacitor	200V film capictor	6.4	36	229	630V DC bus capcitor	20	2	40
Sensing & Protection	Isolated ADC	3	12	36	Isolated ADC	3	1	3
Heatsink	Modular heatsink	4	12	48	Centralised heatsink	108	1	108
Total Cost (USD)				**543**				**471**

TABLE V
COMPARISON BETWEEN PROPOSED IBMC AND THE STATE-OF-THE-ART SOLUTIONS FROM OTHER RESEARCH INSTITUTES

Converter Type	Power	Coupling Range	Frequency	Efficiency	Modulation Scheme	Inverter Devices	Inverter Semiconductor Cost (USD)
The proposed IBMC	7.7 kW	k = 0.138 - 0.31	85 kHz	90% - 93%	Digitized modulation + capacitor balancing	Si MOSFET IPP110N20N * 24	134
Full-bridge [10]	7 kW	k = 0.2 - 0.3	20-26 kHz	80% - 89.5%	Phase shift/duty-cycle modulation	Si power module PM600DV1A060 * 2	516
Full-bridge [22]	7.7 kW	k = 0.28	85 kHz	95.20%	Phase shift/duty-cycle modulation	SiC MOSFET C2M0025120D * 4	280

TABLE VI
COMPARISON BETWEEN THE PROPOSED IBMC-BASED IPT SYSTEM WITH EXISTING INDUSTRIAL SOLUTIONS

Name	Power	Charging Height	Frequency	Efficiency	Control/Modulation Technique
The proposed IBMC	7.7 kW	140-210mm	85 kHz	90-93%	Primary-side digitized modulation
Witricity [23]	3 - 11 kW	100-250mm	85 kHz	90-93%	PFC + Tuneable matching network
Qualcomm Halo [24]	7 kW	N/A	20 kHz	N/A	Primary-side full-bridge phase shift modulation
Conductix-Wampler [25]	60-180 kW	40mm	N/A	>90%	N/A
Momentum Dynamics [26]	3.3 - 0 kW	610mm	N/A	92%	N/A
HEVO Power [27]	1-10 kW	305mm	85 kHz	>85%	N/A
ETH Zurich + ABB [28]	50 kW	100-200mm	85 kHz	up to 95.8%	Extra DC/DC stage for power regulation

the power semiconductors typically account for a significant portion of the overall system cost, and the existing solutions did not provide information on other components such as drivers, controllers, and heatsinks. As can be seen from Table V, the proposed system can handle a significantly larger coupling range while costing less than solutions proposed by other research groups. Note, the prices of the semiconductor devices are from Digikey in February 2021.

The proposed IBMC with the new digitized modulation scheme is also compared with existing industrial solutions, as shown in Table VI. A lot of commercially sensitive information cannot be obtained in this comparison. As such, these fields are left as "N/A." Most industry solutions utilize phase-shift control for the FB inverter or utilize the PFC stage to lower the stress on the inverter stage. Although these solutions may not be the most efficient or advanced techniques, they are relatively simpler to design and implement, thus usually preferred by the industry. This article, however, introduces a new direction for the researchers and the industry to consider. The advantages of the IBMC with the digitized modulation scheme include the wide operating range and the ZVS operation under all conditions, which may overweight its disadvantages (mainly component counts and control complexity). Especially when the industry is pushing for higher power levels, the IBMC with digitized modulation could become an enabling technology for extremely fast wireless charging applications in the future.

IX. CONCLUSION

This article proposes a new digitized modulation scheme that can be used in an IBMC to realize a large operating range and ZVS operation. The key advantage of the digitized modulation scheme is its ability to generate a boosted square-wave-shaped ac waveform with a controllable amplitude, which can guarantee ZVS operation of all switches across the entire operating range. The controllable amplitude is achieved by making sure the operating duty cycle of each SM in the IBMC is either 0%, 50%, or 100%. The operation of an IBMC with 12 SMs, which are controlled using the digitized modulation scheme, is discussed in detail. After comparing the properties of state-of-the-art switches, the use of 200-V Si MOSFET is justified. An SAE J2954 WPT2/Z2 compliant prototype IPT system is then implemented using an Si MOSFET-based IBMC on its primary side. Using the digitized modulation scheme to control the IBMC, the power

transfer is regulated at 7.7 kW under a coupling variation of over 220% (from 0.14 to 0.31) and an EV battery voltage variation of over 150% (280–420 V), while maintaining 90–93% efficiency.

APPENDIX
ONLINE MULTIMEDIA OF THE PROTOTYPE SYSTEM

A video demonstration of the prototype system can be accessed through https://youtu.be/nDifqDISVzA.

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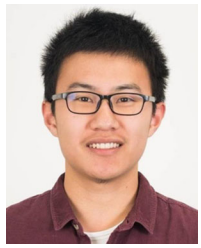

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