

A Review of Architectural Design and System Compatibility of Power Modules and Their Impacts on Power Electronics Systems

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Abstract—The architectural design of a power module determines its application. And the efficacy of a power module layout appears in the system performance by assisting low-inductive busbar design. In this article, some of the previously proposed power modules are reviewed and analyzed considering their system-level applications and their impacts on the architectural design approach. A codesign methodology is then described that accounts for power module system compatibility. The resultant module designs improve the performance of widebandgap (WBG) power semiconductor devices with respect to their interaction with the rest of the power electronics system, such as gate drivers and dc-link capacitor bank. A few common power modules are categorized by architecture and layout; the interdependency of the power modules to each other in a multiphase system and the impact of the power module layout on the busbar and system design are investigated using ANSYS Q3D to elaborate the effectiveness of the proposed power module design methodology.

Index Terms—Double-sided power module, module packaging architectures, power electronic system applications, widebandgap (WBG) power modules.

I. INTRODUCTION

WITH the advancement of widebandgap (WBG) devices, the main goal is to design high power density power electronic systems with improved electrical and thermal performances. However, the components surrounding the WBG devices should also be capable of operating at high temperatures, high breakdown voltages, and high switching frequencies that are afforded by the WBG devices [1]. The closer the parts to each other, the more likely that they are heating each other in a small confine of a compact high-power density system. Hence, higher power density can degrade the thermal performance unless innovative thermal management methods are utilized. Switch

losses, passive control methods such as dc-link capacitor voltage/current control, thermal management, and system design/integration methodology are all critical barriers that must be carefully considered for increasing the system power density [2].

Lee *et al.* [3] reviewed the challenges arising from power module packaging limitations for WBG devices and described some solutions for high switching frequency, thermal management, and high voltage operation. Chen *et al.* [4] reviewed the layouts, packaging materials, and integration trends of the power modules. These are important design considerations for power module packaging. However, the interactions between the power modules and the power electronic system components that fall into the system-level design/integration category are usually neglected. These interactions impact the entire power electronic system as much as the internal electrical and thermal characteristics of the power modules.

The power module architecture affects its mechanical, thermal, and electrical performances [1]. The integration level of the power modules influences the module and system-level parasitic inductances that are critical limiting factors in achieving enhanced system performance. The first two sections of this article review a few of the previously proposed power module architectures and study how their integration level and system characteristics had an impact on the overall power module design. Then, a power module design methodology considering its system compatibility is proposed in the third section of the article. The power module system compatibility determines the interactions between the power module and the power electronic system that directly affect the electrical and thermal characteristics of the system.

Section II of this article reviews the power module architectures and how the power module application goals can change the basics of a power module architecture. The integration level of these power modules is also explored in this section. Section III includes the main contributions of this article, analyzing the system compatibility of both single-sided and double-sided power modules and providing a codesign methodology to design power modules to achieve better compatibility with high-density power electronic systems. It is shown that improving the power module layout can decrease the internal inductance of busbars by 75%. Also, the orientation of the power modules in a multiphase system can affect the system power density.

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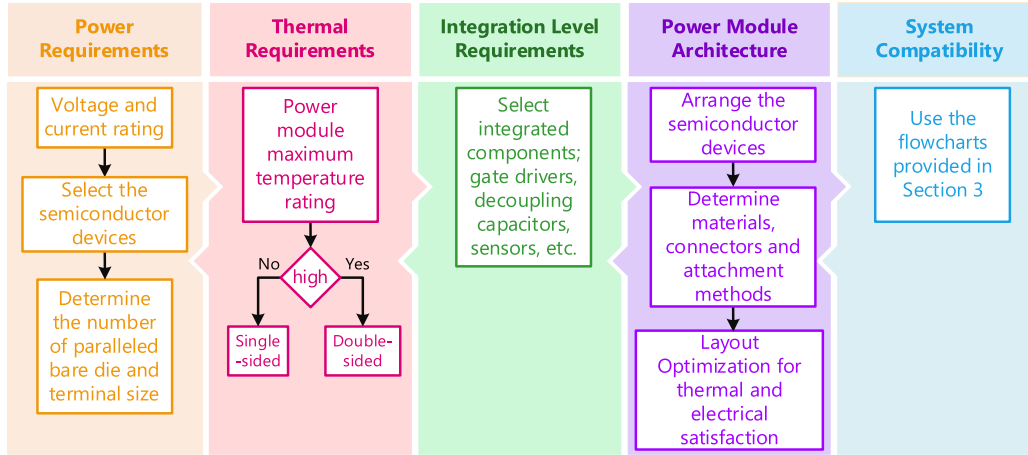


Fig. 1. Power module design flow.

II. POWER MODULE ARCHITECTURE

Power module architecture design starts with determining the breakdown voltage, current handling, and thermal requirements. As shown in Fig. 1, the first step is the selection of WBG bare die to satisfy the breakdown voltage, peak current, and power handling specifications. In most instances, multiple paralleled WBG devices are needed per switching position. If the maximum temperature capability of a power module is required to be close to the bare die maximum junction temperature, either an innovative cooling method or a double-sided cooling architecture may be a necessity instead of a conventional single-sided architecture. This is because the thermal resistance from the die to the module case, R_{th} , can be lower in a double-sided power module since the power module is cooled down from both sides. According to the thermal power formula, $P_{th} = \frac{\Delta T}{R_{th}}$, to use the maximum current capability of bare die devices, the modules with operating temperature close to the junction temperature that has smaller ΔT should have smaller R_{th} as well to be able to keep the required P_{th} .

At this point, the required electrical performance quality of the power module should be considered. If the power module is aimed to be used for high switching frequencies, especially in the case of WBG devices, the integration of more devices inside the power module such as gate drivers can significantly improve its performance. The power module layout and bare die arrangement are designed as the next steps after the selection of the WBG die and deciding upon the power module integration level. Partial discharge (PD) [5] should be carefully taken into account in the power module layer structure for high breakdown voltages. The bare die arrangement and the attachment methods between the top and bottom power substrates should satisfy the PD requirements. The interconnections for a power module, die-attach, power substrate attachment, and electrical interconnections affect the reliability and thermal and electrical performance of the power modules.

Reliability studies can be performed after initial power module fabrication. Most module failures are related to die-attach and electrical interconnections. Various

interconnection methods are studied in [6]–[10] considering thermal performance, fatigue, thermal resistance, conductivity, reliability, and mechanical strength. For instance, a higher aspect ratio, α , that is the ratio between bond loop height and distance of bonding stitches results in a higher power cycling lifetime [11]. Also, the self-inductance of a wire bond is related to its diameter and length [12]. The following equation provides the self-inductance equation for a wire:

$$L_{self} = 2l \cdot \left(\ln \left(\frac{4l}{d} \right) - 0.75 \right) \text{ (nH)} \quad (1)$$

where l and d are, respectively, the length and diameter in centimeters. Using this equation, for a 1 cm wire with 0.03 cm (12 mil) diameter, the self-inductance value is 8.3 nH. For a 1 cm wire with twice that diameter, 0.06 cm, the self-inductance value is 6.7 nH, which is only slightly lower than 8.3 nH. However, twice the wire length, 2 cm, and the same diameter, 0.03 cm, the self-inductance value is 19.3 nH, that is, even more than twice the inductance value of a 1 cm wire. Hence, the length of a wire has the highest impact on its stray inductance [13], [14]. The distance between wire bonding stitches is related to the module layout and cannot change much, so to increase α , the wire bond loop might increase, that is, in controversy with the wire bond self-inductance optimization. The requirements for low inductive current paths in WBG modules, high current capability, and more importantly, the reliability issues of aluminum wire bonding implore better electrical interconnection methods.

A. Power Modules Without Additional Integrated Components

The power module architecture is defined as the layer-to-layer structure from the base plate to the die and housing, the material selection, and the attachment strategy. A few significant double-sided and stacked power module architectures and their system compatibility are described as follows.

1) *Double-Sided Power Modules:* Double-sided modules have more design flexibility, especially in the z-direction. Hence, sometimes a custom-made power module is preferred to meet the system requirements. Fig. 2 shows a double-sided power module

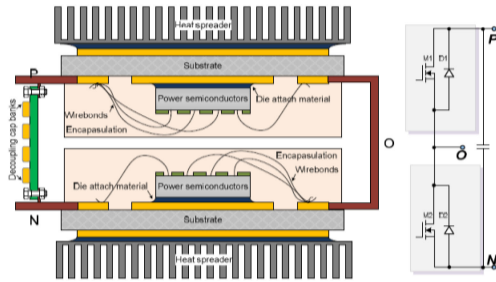


Fig. 2. Packaging structure of power module proposed in [15], ©[2018] IEEE.

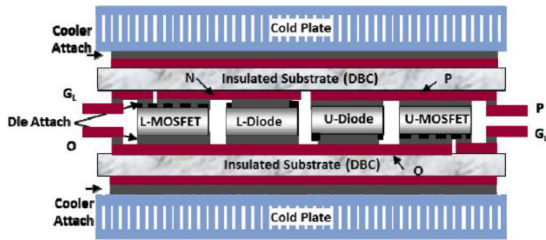


Fig. 3. Planar-bond-all power module [16], ©[2015] IEEE.

constructed using two direct-bond copper (DBC) substrates with wire-bonded bare die attached top-to-top from each other [15]. This module is specifically designed for an air-cooled system where the air can flow through the top and bottom switches. The wire bonds and the distance between the two switches have increased the power module thickness. Such design requires a meticulous mechanical analysis to mitigate the stress that might be applied to the single attachments on the substrates or terminals.

The planar-bond-all power module [16] had a completely different strategy with creating a compact power module, concerning the size and fabrication strategy to make mass production possible. In the planar-bond-all power module, both the drain and source pads are connected to the top and bottom DBC substrates using a planar connection, as shown in Fig. 3. The WBG devices are processed from the wafer level to have the desired pad metallization [16] that is the best solution for reliable solder-based connection of the die to the substrates, especially on gate and source signal pads [17]. The diodes and MOSFETs have different thicknesses, as do their connection pads. However, both the top- and bottom-switching positions are symmetrical regarding the top and bottom thermal management systems and can be cooled down equally and simultaneously from both sides. It is important to note that although not possible with all the power module design architectures, such symmetry is desired for electrical performance of the switching legs or switching positions, thermal and current capability, parasitic performance, and overall module performance.

2) *Stacked Power Modules*: Stacked power module architectures enable the three dimensionality of the current paths and/or cooling paths. Such power modules usually have a small footprint, are lightweight, and possess a low parasitic inductance enabled by magnetic field cancellation.

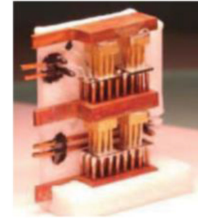


Fig. 4. Stacked power module with thermally improved LTCC interposer [20], ©[2016] IEEE.

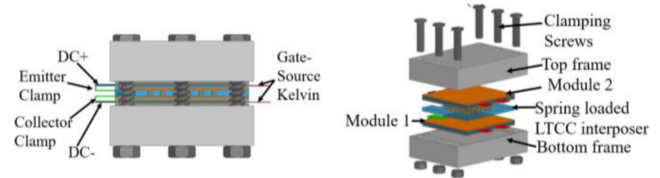


Fig. 5. Some of the previously proposed single-sided, double-sided, and stacked power module architectures.

Most stacked power modules are double-sided but some of them do not enable double-sided cooling since their power devices are usually cooled from one side as they are “stacked” on top of each other. Hence, although these power modules have better power density at the module level, they might not be able to increase system power density simply with smaller volume because the power density is also defined by the power handling capability that can degrade because of lower thermal performance.

New double-sided cooling methods for stacked power modules are reported in [18]–[21]. Fig. 4 shows a stacked power module to mitigate wire bond reliability and large area soldering [18] and improve thermal performance. The wire bonds of the power pads are replaced with a gold-plated pin-fin-based copper connector that improves reliability and eliminates voids and cracking that happens with large-area soldering.

In this power module architecture, the bare die can be cooled down directly with an isolated cooling fluid rotating inside the power module structure through the connecting pin-fins. The power module housing requires cautious design since it has to be completely sealed to prevent any fluid leakage. An accurate alignment system, fixture design, and unconventional vertical wire bonding from the gate/source pads to the pins on the housing may present potential manufacturing issues.

Fig. 5 shows a stacked power module for a half-bridge (HB) topology using a low-temperature cofired ceramic (LTCC) interposer with spring-loaded electrical terminals [22]. The LTCC interposer serves not only to enhance the mechanical integrity of the spring-loaded electrical connectors but also to enable electrical routing. This stacked power module architecture is conducive to high-voltage applications by vertical stacking of many of these modules similar to the high-voltage valve architecture [23] for ultrahigh-voltage dc-dc transmission systems. Low parasitic inductance is achieved due to its wire bondless interconnections.

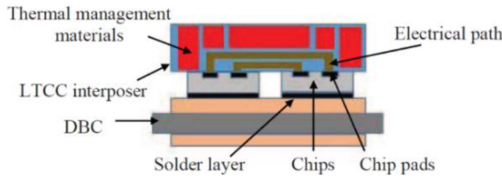


Fig. 6. HB stacked power module structure [18], ©[2017] IEEE.

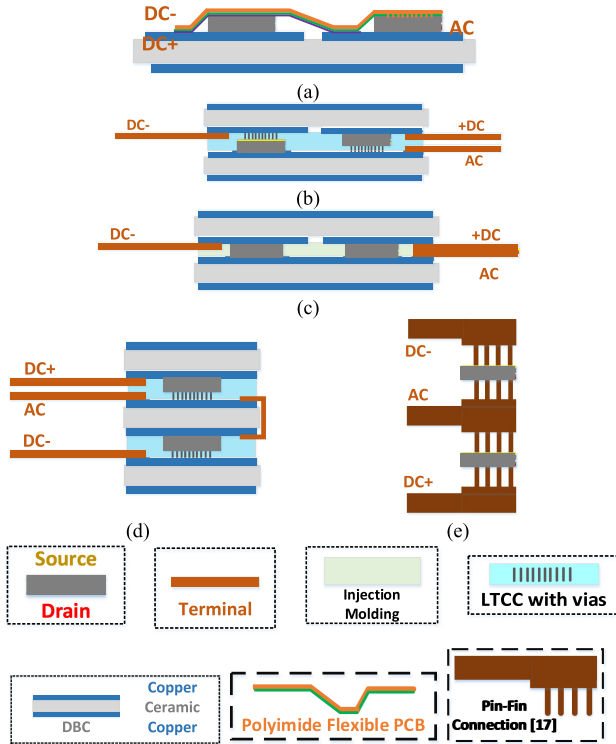


Fig. 7. Spring-interconnected stacked power module [22], ©[2019] IEEE.

Fig. 6 shows an LTCC interposer embedded into a stacked power module structure for electrical and thermal routing [20]. For most stacked architectures, localized heating usually occurs within the confine of the back-side cooled power devices. To remove the heat generated from the stacked devices, the LTCC interposer is loaded with heat spreading materials such as nanodiamond, graphene, and pyrolytic graphite sheets on the surface and inside the through-hole thermal vias to facilitate heat spreading to the sides of the stacked module to afford side cooling. The conducting vias of the LTCC interposer serve as the electrical interconnections between the power devices on the top and bottom DBC substrates. The CTE mismatch between the copper baseplate, attachment layer, and ceramic power substrate presents a reliability issue. As shown in the previous examples, some power module architectures eliminate the base plate [24] and use housing or interposers to improve their mechanical strength.

Fig. 7 summarizes some of the previously proposed single-sided, double-sided, and stacked power module architectures. Fig. 7(a) shows SKiN technology where a flexible PCB is sintered on top of the devices to create the current paths from the

TABLE I
COMPARISON OF POWER MODULE ARCHITECTURES WITHOUT ADDITIONAL INTEGRATED COMPONENTS

Fig.	Pros	Cons
7(a)	<ul style="list-style-type: none"> • Suitable for SMD components integration in proximity with the power devices • Better reliability, thermal management, and electrical performance [25] 	<ul style="list-style-type: none"> • More complicated fabrication • Polyimide PCB is prone to high moisture absorption
7(b)	<ul style="list-style-type: none"> • High-temperature capability especially by adding thermal dissipation material inside the LTCC • Flexible LTCC design [26] 	<ul style="list-style-type: none"> • Expensive [26] • Complicated fabrication process • Difficult to make attachments on LTCC
7(c)	<ul style="list-style-type: none"> • Repeatable manufacturing process • Faster for mass production • Low-cost repeatability 	<ul style="list-style-type: none"> • High initial cost • Not possible for complicated module designs
7(d)	<ul style="list-style-type: none"> • Small module footprint • Possibility of designing low-inductive modules • Can have high breakdown voltage capability [22] 	<ul style="list-style-type: none"> • Without innovative methods, the thermal performance is not as good as the double-sided modules • Expensive [26] • Difficult to make attachments on LTCC • Complicated fabrication process • Limited current capability
7(e)	<ul style="list-style-type: none"> • Improved thermal performance • Higher reliability because of smaller attachment area [18] 	<ul style="list-style-type: none"> • Complicated fixturing and fabrication process • Complicated housing design for coolant liquid rotation inside the module • Difficult to attach the G/S pins • Complicated system-level attachment especially considering the vertical nature, and a coolant rotation inside the module

top side of the devices [25]. In this technology, both sides of the power devices are sintered to the DBC and flexible PCB. The electrical, thermal, and reliability of the proposed module architecture are improved because instead of wire bonds, wide current patterns are directly connected to the devices that provide low inductive paths, as explained in (1), and better heat dissipation, especially along with a pin-fin base sintered to the substrate. Fig. 7(b) shows a double-sided module architecture with an LTCC interposer between its two substrates. The interposer consists of vias to create electrical connections from the source and gate pads. Vias can be eliminated from this design by using simple connection blocks. This interposer does not necessarily need to be out of LTCC material. Another candidate for such interposer is 3-D printed ceramic that is cheaper, lighter, but also more fragile [26]. Fig. 7(c) shows a double-sided module with injection molding. Fig. 7(d)–(e) shows stacked modules, one using LTCC interposers [22] and the other using pin-fin connectors [18]. The pros and cons of these modules are tabulated in Table I.

B. Highly Integrated Power Modules

In some power module architectures, passive circuit components and gate drivers are integrated with the module. The integration of additional components into a power module presents both merits and demerits that should be carefully considered according to power module requirements. Any components that

can be integrated into a module reduce the dead space that could have been created between the power module and the same components in a system-level design [27]. The parasitic inductance mitigation using decoupling capacitors, high-quality gate drive signals, and lower electromagnetic interference (EMI) emissions is the electrical performance enhancement desired in highly integrated power modules. More importantly, the gate parasitic inductance mitigation enables a high switching frequency. However, the integrated passive components and their attachment material must be selected carefully to avoid thermal limitation [28] and cracks along the attachment bonds [1]. For the gate driver integration, the symmetry of the gate driver to the paralleled WBG devices and crosstalk between the signal pad and power pads inside the power module are critical architectural issues that if not considered accurately can result in false switch turn-ON and even system failure. In [29], the power switch false turn-ON caused by the parasitic between the power and driver circuitry is studied. Three mitigation methods were introduced:

- 1) adding a capacitor on the control stage that ended up reducing the switching speed;
- 2) minimizing the capacitance on the DBC layout that required more advanced soldering equipment or accurate DBC design and etching process;
- 3) using an additional shielding layer in which the driver circuit was not at the same level as the power circuit.

To study power module architectures possible for integrating surface mount devices (SMD), Fig. 8(a)–(f) provides a survey of several highly integrated power module architectures. These illustrate architectures that overcome one or more shortcomings when attempting high levels of integration but serve to identify many of the key issues to be considered. Fig. 8(a) shows a power module structure with an LTCC integrated with the DBC power substrate. The LTCC substrate is used for the SMD components such as capacitors and gate drivers, while the DBC is for bare die attachments. Fig. 8(b) shows a power module structure that uses a multilayer copper thick film for the integration of the SMD components. Fig. 8(c) is a single-sided power module with the PCBs mounted on the DBC power substrate to ease the soldering of the SMD components. Fig. 8(d) shows a double-sided power module without a DBC power substrate. To achieve a high-current handling capability, busbar-integrated PCBs are used. These PCBs have limitations in the number of paralleled internal busbars and their thickness as well as a high fabrication cost. Fig. 8(e) shows the same integration method without stacking the power devices. This creates additional issues on the PCB as the two busbars are integrated into one PCB that further limits its thickness and current handling capability. Fig. 8(f) shows a power module that combines both the DBC and PCB. Although easy for integration as shown in the simulations, the PCB mounted on the bare die presents a CTE mismatch problem. The advantages and disadvantages of these power module architectures are tabulated in Table II.

1) *Non-PCB-Based Architectures*: Fig. 9 shows a power module using multilayer copper thick film that provides a fine-pitched surface to easily attach the gate drivers and decoupling capacitors on it [30].

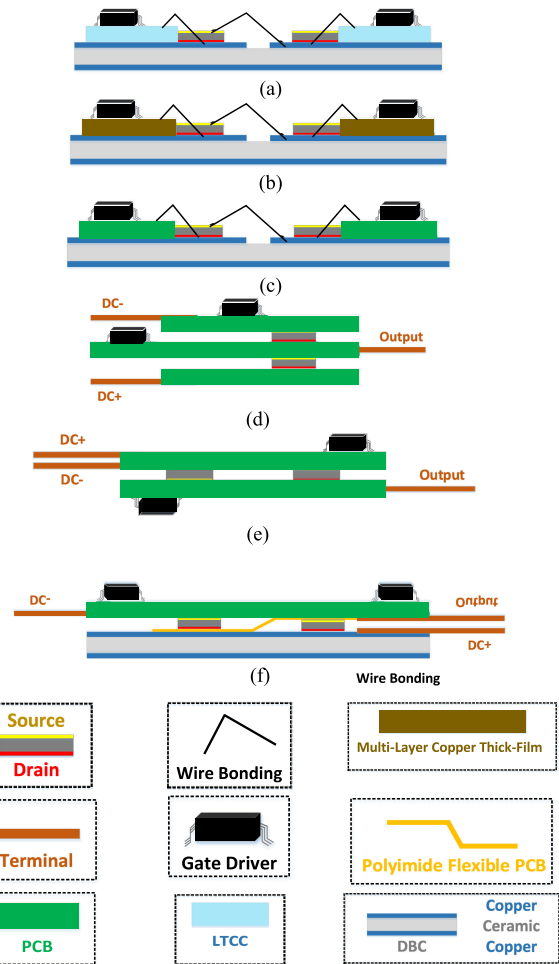


Fig. 8. Possible structures for highly integrated power modules.

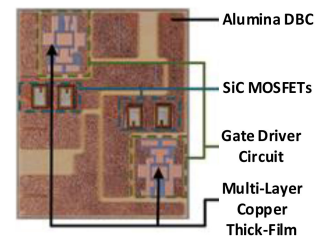


Fig. 9. Integrated power module using multilayer copper thick film proposed in [30], ©[2018] IEEE.

Decoupling capacitors were integrated in the power modules to mitigate the effects of internal parasitic inductance on voltage overshoot and ringing [30]–[36]. In [37], a stacked power module with integrated gate driver ICs is proposed. A flexible epoxy-resin substrate is used instead of ceramic substrates because of its matching CTE and better thermal properties.

2) *PCB-Based Architectures*: Fig. 10 shows a power module with a separate substrate for the gate drivers and the power circuits to mitigate the crosstalk issue [38]. Both the power substrate and the PCB are wire-bonded next to each other inside the power module package. This additional PCB for the gate drivers makes the module assembly process much easier.

TABLE II
COMPARISON OF HIGHLY INTEGRATED POWER MODULE STRUCTURES

Fig.	Pros	Cons
8(a)	<ul style="list-style-type: none"> High-temperature capability 	<ul style="list-style-type: none"> One-sided power module Difficult to solder on the LTCC substrate
8(b)	<ul style="list-style-type: none"> Good thermal performance Suitable for SMD components integration 	<ul style="list-style-type: none"> Not cost-efficient
8(c)	<ul style="list-style-type: none"> Simple to fabricate and low cost Easy of gate driver integration 	<ul style="list-style-type: none"> One-sided power module Increase in power module size A high-temperature PCB is required to solder on DBC. Polyimide PCB is prone to high moisture absorption CTE mismatch between the DBC and PCB
8(d)	<ul style="list-style-type: none"> Minimum mutual inductance layout possible Double-sided power module Ease of gate driver integration 	<ul style="list-style-type: none"> Require to underfill between bare die to reduce mechanical stress High fabrication cost (expensive) Low Tg (140°C) of the PCBs Difficult attachment process because of the difference in the thicknesses of the components
8(e)	<ul style="list-style-type: none"> Minimum mutual inductance layout possible Double-sided power module Easy of gate driver integration 	<ul style="list-style-type: none"> Require to underfill between bare die to reduce mechanical stress High fabrication cost (expensive) Low Tg (140°C) of the PCBs The DC+ and DC- terminals cannot be thicker than 0.8 mm
8(f)	<ul style="list-style-type: none"> Double-sided power module Minimum mutual inductance layout possible Easy of gate driver integration 	<ul style="list-style-type: none"> More complicated fabrication Polyimide PCB is prone to high moisture absorption CTE mismatch

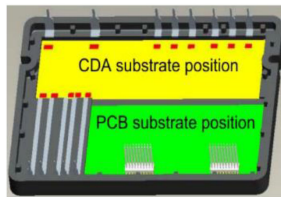


Fig. 10. Three-dimensional model of full-integrated power module [38], ©[2017] IEEE.

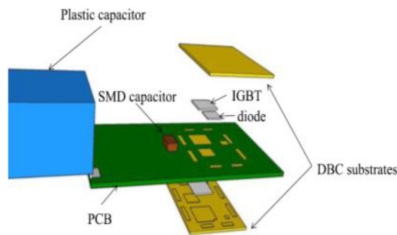


Fig. 11. Power module with a combined DBC and PCB [40], ©[2017] IEEE.

A polyimide flexible interconnect with SMD components in a single-sided power module is proposed in [39]. Such an architecture enhances the electrical performance due to the small stray inductance between the driver and the bare die but limits the power module to a single-sided structure.

Fig. 11 shows a double-sided power module using a DBC+PCB+DBC structure with its IGBT bare die stacked

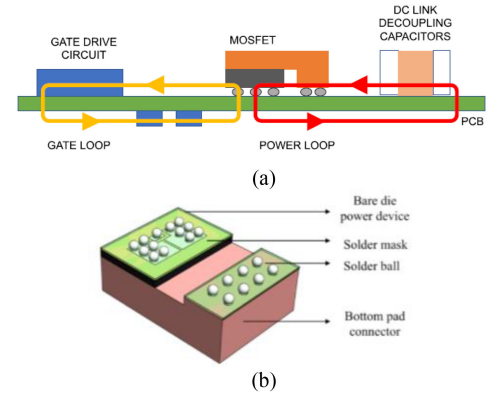


Fig. 12. (a) PCB-based power module with an integrated gate driver board [41], ©[2018] IEEE, and (b) copper pieces for flip-chip connection of all three pads of the semiconductor devices [42], ©[2020] IEEE.

on both sides of the middle PCB [40]. In this power module structure, the bare die devices are soldered on the DBCs, but conductive glues are used to connect them to the PCB. This structure is simple and has a small parasitic inductance. The SMD components for parasitic mitigation and gate driver board are soldered on the same PCB to improve the overall performance of the power module. However, this structure is sensitive to CTE mismatches of different materials. Although the power module has a double-sided architecture, the semiconductor devices are cooled only from their respective DBC substrates. The conductive glue interconnections of the bare die to the PCB deserve more investigation, especially in high-current applications. Conductive glue has a high thermal and electrical resistance that increases the losses and is detrimental to power module reliability.

In Fig. 12(a), a PCB-based power module with an integrated gate driver board is shown [41], [42]. The bare die semiconductor devices are placed on the same board as the gate drivers along with their dc-dc power supplies. The great advantage of this structure is the elimination of the wire bonds and innovative copper pieces that are used to flip-chip bond all three gate, source, and drain pads of the die to the PCB at the same level [see Fig. 12(b)]. These copper pieces reduce the equivalent parasitic inductance of the connection bonds, compensate for the different thicknesses of bare die devices, and cool them down like a small heatsink directly connected to the device. CTE mismatch between the PCB board, semiconductor bare die devices, and the copper, PCB current limitation, as explained in Table II, and accurate milling of the copper pieces with the high-tolerance machine are the fabrication concerns of this architecture.

Fig. 13 shows a power module using a DBC substrate for the power loop and PCB for both the power and driver loops [43]. In this structure, the PCB has small cavities where the bare die devices are attached to the DBC without touching the PCB. Then, the gate and source pads are wire-bonded to the PCB, creating low-inductive gate driver paths with an integrated gate driver. This is one of the ways of utilizing a PCB for integrating SMD components inside the power module without degrading the reliability of the power module as a result of the CTE

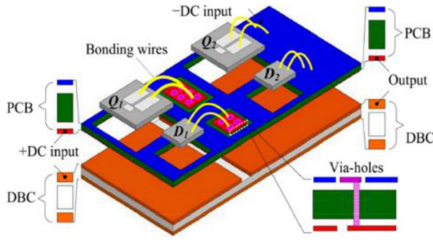


Fig. 13. Power chip-on-chip with PCB-DBC; exploded view of 3-D rendition [43], ©[2017] IEEE.

TABLE III
MATERIAL PROPERTIES USED IN THE SOLIDWORKS SIMULATION

	Poisson's Ratio	Tensile Strength (N/m ²)	Mass Density (kg/m ³)	CTE (1/°K)
SiC	0.36	300e+6	3200	3.8e-6
AlN	0.23	197e+6	2920	4.3e-6
AlSiC	0.292	500e+6	2784	6.5e-6

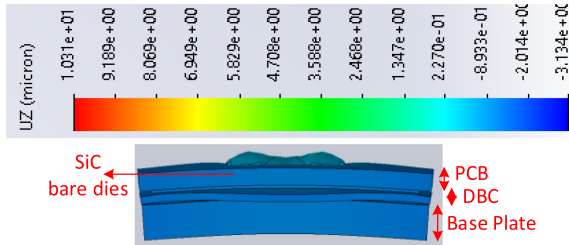


Fig. 14. Warpage simulation of the power module reported in [43] using two CREE SiC MOSFETS.

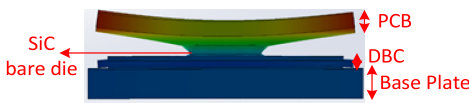


Fig. 15. Warpage simulation of a PCB + die attachment architecture reported in [44] using two CREE SiC MOSFETS.

mismatch between the PCB and the bare power semiconductor die. To investigate the effects of CTE mismatch, two SolidWorks simulations were designed to show the difference between the power module mechanical displacements of a PCB + DBC [43] versus the PCB + die attachment architecture [44]. Table III provides the material properties of the PCB, DBC, and SiC used for the simulations [45]–[47]. For consistency, Cree's 1200 V, 112 A SiC MOSFET bare die (CPM3-1200-0016A) is used. As shown in Figs. 14 and 15, the z -direction warpage caused by the CTE mismatch for the PCB on DBC architecture is 1.4 μm . This is much smaller than the 10.3 μm warpage, where the PCB is directly attached to the bare die. Note that the convex warpage shown in Fig. 14 can also be solved by prebending the base plate. The effects of such warpage solutions are not considered in these simulations.

III. POWER MODULE SYSTEM COMPATIBILITY

WBG-based power modules offer significant advantages in many power electronics applications. In the traction inverter

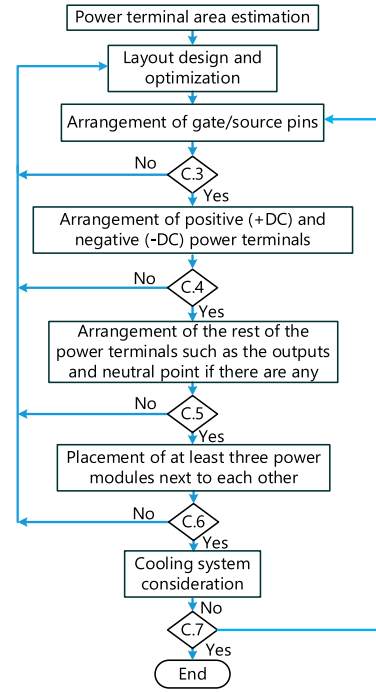


Fig. 16. Proposed design flowchart for system compatibility of single-sided power modules in the absence of a mathematics-based optimization algorithm, such as PowerSynth [54].

and charger systems for transportation applications [48], these modules help to reduce the system volume and weight, fuel consumption, and improve the system overall efficiency by having variable frequency drives [1]. In power grid applications, such as high-voltage direct current transmission lines, renewable energy generation systems [49], and flexible alternating current transmission systems, the traditional combiner boxes can be replaced with high-efficiency WBG-based power conversion units [50]. As mentioned previously, the great features of SiC devices cannot be fully utilized without a good power module design. A low-inductive power module design alone does not guarantee that the power electronic system can achieve all the great features afforded by the WBG devices. This is because the interaction of the power module with the rest of the power electronic system has a great influence on the overall system performance [51], [52]. The busbar design to connect the power module to the dc-link capacitors plays an important role in the system parasitic inductance, ringing, voltage overshoot, and the EMI filter size [53]. The busbars should be carefully designed, not only during the system design but also during the power module design stage. The power module can either promote a low-inductive busbar or can make it very challenging to achieve a high-performance and high-power-density power electronic system. In this section, the system compatibility of both single-sided and double-sided power modules is studied. The proposed design methodology for single-sided power modules considering their system compatibility is shown as a flowchart in Fig. 16. The blocks C.3–C.7, in the flowchart, are the design conditions in the proposed flowchart.

TABLE IV
INFLUENCE OF POWER MODULE LAYOUT AND TERMINAL ARRANGEMENT ON THE POWER ELECTRONICS SYSTEM DESIGN

		(a)	(b)	(c)	(d)	(e)	(f)
Module Packaging methodology	S.1: Terminal Area	S.1: -	S.1: -	S.1: -	S.1: -	S.1: -	S.1: -
	S.2: Layout	S.2: ✗	S.2: ✗	S.2: ✓	S.2: ✗	S.2: ✗	S.2: ✓
	S.3: G/S pins	S.3: ✗	S.3: ✗	S.3: ✓	S.3: ✓	S.3: ✓	S.3: ✓
	S.4: +/- DC	S.4: ✗	S.4: ✗	S.4: ✗	S.4: ✓	S.4: ✓	S.4: ✓
	S.5: Rest of terminals	S.5: -	S.5: -	S.5: -	S.5: -	S.5: -	S.5: -
	S.6: Three-Phase	S.6: ✗	S.6: ✓	S.6: ✓	S.6: ✓	S.6: ✓	S.6: ✓
	S.7: Cooling	S.7: -	S.7: -	S.7: -	S.7: -	S.7: -	S.7: -
Module Size (mm³)		27 × 70 × 10	33 × 55 × 10	40 × 51 × 10	40 × 51 × 10	40 × 51 × 10	40 × 47 × 10
Module Inductance (nH)		11.1 nH	13.5 nH	12.75 nH	14.8 nH	11.4 nH	5 nH
Busbar Inductance (nH)		13.6 nH	19 nH	21.7 nH	9 nH	14.5 nH	7.6 nH
System Power Density (kW/L)		32 kW/L	40 kW/L	42 kW/L	42 kW/L	42 kW/L	43 kW/L

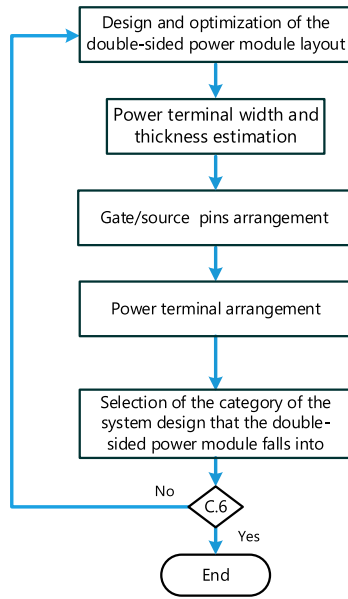


Fig. 17. Proposed design flowchart for system compatibility of double-sided power modules in the absence of a mathematics-based optimization algorithm, such as PowerSynth [54].

The proposed codesign methodology is trimmed for the double-sided power modules as well. Double-sided power modules have two of their larger sides occupied by the cooling systems, and as such, the only space available is the edges of the power module. Hence, it is desirable to specify which sides of the double-sided power module are for the dc-link capacitor, the input power supply, the output load, and the gate driver board during the first design stage. The flowchart in Fig. 17 provides the codesign methodology to design double-sided power modules.

Six different power module design examples along with their system-level inclusion in a conventional inverter are provided in Fig. 18(a)–(f). For the sake of comparison, all six power modules have an HB switching arrangement and two paralleled CREE’s CPM3-1200-0013A SiC bare die per switching position. The gate/source pins and power terminals have the same size in all six modules and the clearance distance between the terminals is kept at a minimum of 9 mm according to the UL-840 standard. The distance between the paralleled bare die is 3 mm. Table IV

compares the design methodology of the power modules, the codesign steps from the flowchart of Fig. 15 that each power module has missed, and its influence on the module internal parasitic inductance, system-level busbar inductance, and system power density. It is shown that minimizing the module internal inductance cannot always guarantee the best system performance as the module layout and terminal arrangement may not allow for low-inductance busbar design. Each power module is used in a conventional three-phase inverter system with a similar SBE’s 906A13799-104 dc-link capacitor that is 135 μ F, 900 V with DuPont Teijin PEN HVTM film. The cold plates are all custom-designed according to the power module size. The distance between the modules is kept 3 mm in all three-phase systems and the distance from the outer edges of the modules to the edges of the cold plates is considered 10 mm in all six systems. Such module arrangement is shown in Fig. 29. The system power densities are compared in Table IV for a dc-link voltage of 700 V and module current capability of 170 A @ $T_j = 160$ °C. It must be pointed out that no specific form factor requirements are considered for these system designs. Of course, any specific system form factor can change the decisions upon the system part selections such as capacitors and thermal management systems. But it still does not significantly change the power module attachment method to the rest of the system components. The details of these designs are described in the following along with the power module codesign methodology steps to clarify how each step can affect the system-level design.

1) *Power terminal cross-sectional area estimation*: The power terminals introduce a large percentage of the overall module parasitic. As the first step of a power module design, the required power terminal cross-sectional area must be estimated accurately to ensure the current handling capability without overheating. The desired current density determines the minimum cross-sectional area of the terminal. Equation (2) calculates the minimum cross-sectional area for current flow. Moreover, the layout symmetry of parallel power die affects the placement of the power terminals [55]. The size and number of the terminals affect the overall parasitic inductance of the power module and the symmetric current distribution along with the bare die devices. Hence, the current capability determines the minimum cross-sectional area of the power terminals but, as mentioned

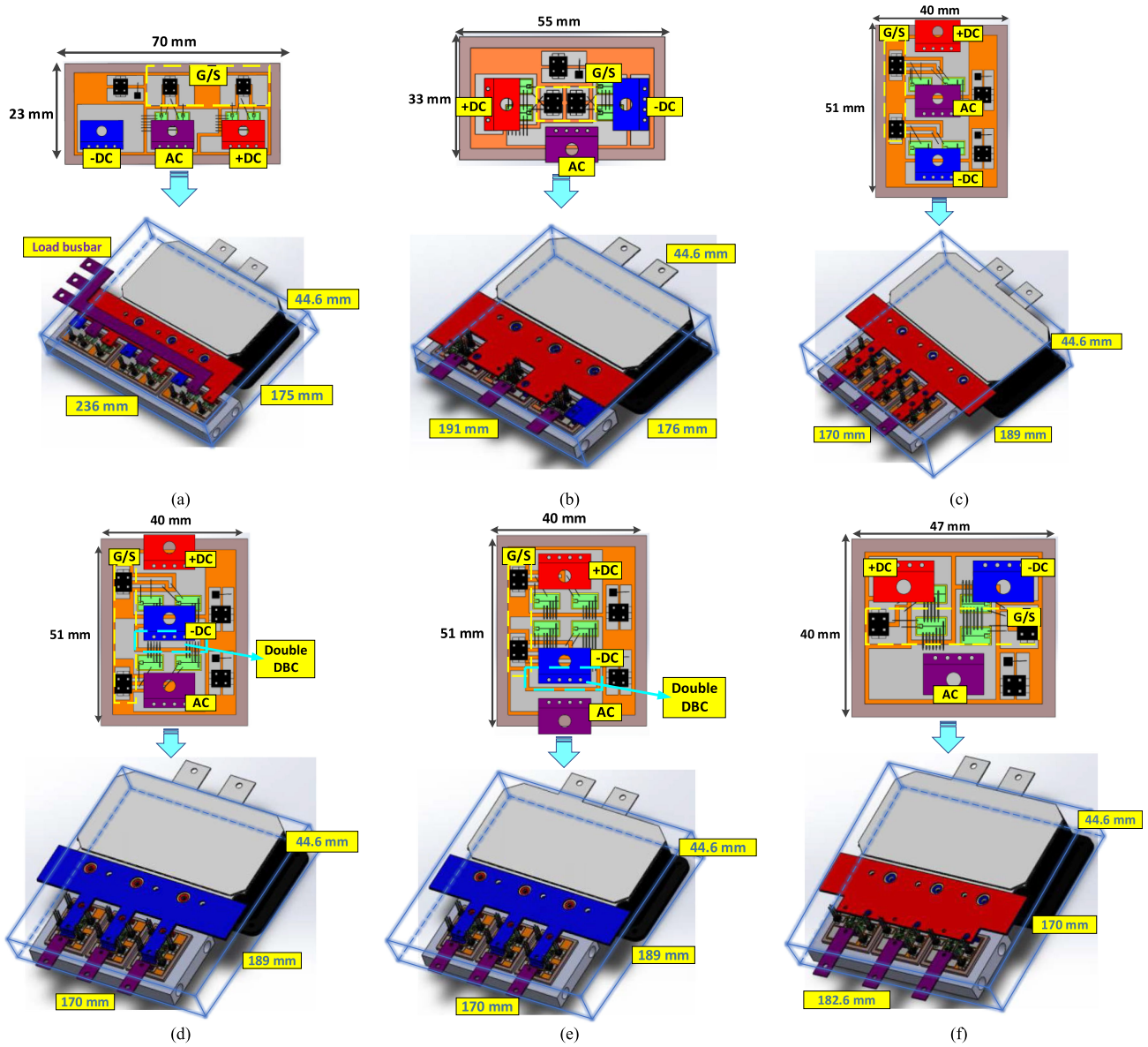


Fig. 18. Examples of power module designs and their impact on the power electronics system design.

above, even larger terminals might be selected to meet other requirements of the module, such as current distribution between devices or internal inductance. In [56], two power modules, one with one set of power terminals and the other with two sets of the same power terminals, are compared in terms of parasitic inductance and current distribution. It is shown that the power module with a higher number of terminals has lower power loop parasitic inductance and better current distribution with fewer hot spots.

In a double-sided power module, the width of the power terminals is usually dependent on the layout, but its thickness can be changed according to the current capability of the power module

$$A = 400 \cdot I \times 0.785 \times 10^{-6} \text{ in}^2. \quad (2)$$

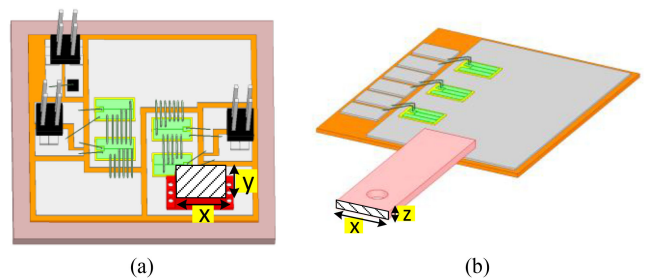


Fig. 19. Cross-sectional area for (a) single-sided and (b) double-sided power modules.

Fig. 19 shows the power terminal cross-sectional area definition in single-side and double-side power modules.

2) *Layout design*: The power module layout optimization is considered the second step. In a classic power module design, this is an iterative procedure that must be repeated after every design step to achieve the desired power module characteristics.

To eliminate or reduce iterations, a proper mathematics-based optimization tool, such as PowerSynth, described in [54], can also be used which facilitates a rapid design procedure. PowerSynth [54] can automate the layout design box of the flowchart shown in Fig. 16 but in the future, it may also eliminate the iterative process and consider the conditions as its optimization function constraints.

The layout design is basically the primary stage to consider the power module switching configuration, DBC-to-DBC, and die-to-DBC connection and deciding upon any innovative methods, such as using separate DBCs, for each switching arrangement for better thermal performance by reducing heat transfer [57]. The layout can be affected and adjusted in the following design stages during power terminal and signal pins placement.

The layout design of a double-sided power module, however, can be more complicated because stray inductance cancelation using the mutual inductance is one of the important features that double-sided power modules offer.

3) *Arrangement of gate/source pins*: The signal pins should not be surrounded by the power terminals since it will be very difficult to prevent them from proximity noise interference. Also, it might limit the system busbar width which creates highly inductive power paths. For the same reasons, the power terminals shall not be surrounded by the signal terminals. Also, the gate/source and control pins are better to be placed at two different sides or in two rows to increase the mounting stability of the gate driver board on the power module. This is the decision condition C.3 in the flowchart of Fig. 16.

The arrangement of Fig. 18(a) shows a power module with G/S pins all in one row. Such design is mechanically more problematic if the gate driver boards are only going to rely on pin headers for attachment on the module as the stability of the gate driver board becomes dependent on one row of pins. Fig. 18(b) shows a power module design with G/S pins closely surrounded by the power terminals. As can be seen from its system design, such a design will limit the connection busbar expansion throughout all the terminals of three adjacent power modules in a three-phase system. Moreover, the gate–source pins are located at the middle of the power module, almost inside the switching loop has the most concentrated EMI field due to switching noises [58].

In a double-sided module, all gate pins can be located on one side of the power module. Alternatively, gate pins can be placed on both sides of the power module, but the system will need separate gate driver boards for each switching position.

4) *Arrangement of positive (+dc) and negative (–dc) power Terminals*: The placement of the positive (+dc) and negative (–dc) terminals in the power module is a crucial consideration. This is the decision condition C.4 in the flowchart of Fig. 16. The positive and negative busbars introduce large parasitic inductances to the system if they are not carefully designed. Hence, the power module terminal arrangement should be optimized carefully. The typical method to prevent high stray inductances

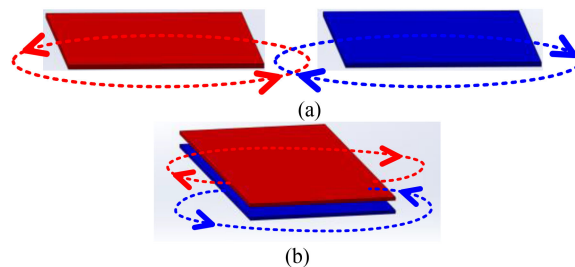


Fig. 20. (a) Planar busbars and (b) laminated busbars.

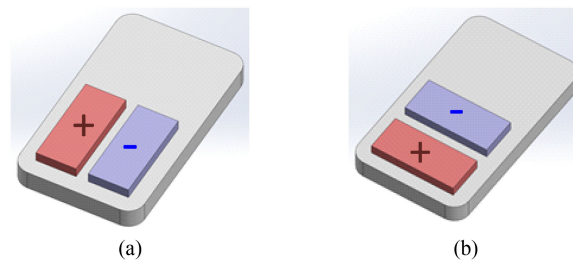


Fig. 21. Arrangement of positive and negative power terminals: (a) side-by-side and (b) along the longer edge of the power module.

in the positive and negative power paths is to create a large negative mutual inductance between them. The positive and negative busbars can either be placed in a planar mode or laminated on top of each other, as shown in Fig. 20(a) and (b), respectively. In the planar mode, the electromagnetic fields of the two planes can only partially interact with each other. To ensure a high mutual inductance in the laminated busbar design, the positive and negative power terminals should be placed as close as possible to each other after considering the creepage and clearance distances.

The positive and negative power terminals can be placed side-by-side along the shorter edge of the power module, as shown in Fig. 21(a), or along the longer edge of the power module, as shown in Fig. 21(b). Both these arrangements facilitate a laminated busbar design as far as the two power terminals are placed next to each other. However, the difference between these two designs is that in the case of Fig. 21(a), either planar or laminated busbar design is possible. But in the power module with the terminals arranged along the longer edges [see Fig. 21(b)], the system designer has no other choice but to adopt the laminated busbar design. The cost of a busbar is significantly related to its design and it rises as the number of holes and bending increases. The busbar design can be flexible, but the cost might be a limiting factor. Hence, in a system design, there is a compromise between the price of a busbar, system electrical performance, power density, form factor, and mechanical robustness.

It is not always possible to place the positive and negative terminals next to each other without having the ac terminal in between them. This is even more complicated for power modules with the power terminals along the longer edge. Fig. 18(a)–(c) shows three different power module layout examples in which the ac terminal is placed in between the +dc and –dc terminals. These power modules follow a straightforward source-to-drain

connection to achieve an HB switching arrangement. Such module design sacrifices the system busbar inductance to the module simplicity and internal inductance. As given in Table IV, the busbar inductance is high in the modules of Fig. 18(a)–(c). The module in (a) has lower busbar inductance in comparison with (b) and (c) because of the proximity of its power terminals to the power module edges and the dc-link capacitor. Its load busbar, ac, however, is more complicated because of the placement of all the control and G/S signal pins at the opposite side of the input terminals. The busbar inductance in module (b) is smaller than the busbar inductance of module (c) because of the width of the busbar and the mutual inductance between the positive and negative terminals of two adjacent modules. The module in (c) has the highest busbar inductance because of the long distance between the positive and negative terminals and the ac terminal in between that hinders from increasing the mutual inductance between positive and negative attachments. As can be seen from Fig. 18, it might be required to reroute the terminal paths to be able to place the positive and negative terminals next to each other. This will result in a compromise between the module internal inductance and the busbar stray inductance. Ignoring one of these over the other might result in optimum local result, in a module or busbar, but will not provide the optimum result from the overall system-level point of view.

An interesting power module layout method to place the positive and negative terminals alongside each other is reported in [59]. The authors use two substrates instead of one that are soldered on top of each other and are connected by wire bonds. Hence, the negative power terminal is extended next to the positive terminal using the bottom power substrate. Such a power module architecture automatically creates canceling magnetic fields that eliminate the high internal parasitic inductance of the power module and results in an ultralow inductive external busbar because of the laminated structure.

Fig. 18(d)–(f) provides three module designs with positive and negative terminals next to each other. In the power modules (d) and (e), a second DBC is used for placing the negative terminals between the positive and ac terminals. In module (e), the layout of module (d) is changed to bring both switching positions close to each other and, consequently, reduce the module's internal inductance. Per Table IV, as much as the internal inductance is reduced, the busbar inductance is increased in this design that is because the terminals got further away from each other and eventually resulted in lower mutual inductance. The change of the module internal inductance and the busbar inductance is quite clear comparing these two modules and their resultant simulations from ANSYS Q3D that is provided in Table IV. Having seen the inductance values of the modules in Fig. 18(d) and (e), their layout is further optimized to be able to bring both module and busbar inductance to more acceptable values. This module is shown in Fig. 18(f).

For double-sided power modules, Fig. 22(a) and (b) shows two common designs. These power modules are designed with different system-level requirements. The double-sided power module in Fig. 22(a) can be used either horizontally or vertically inside a stack cooling system connected to a power source and load from one side and the gate driver board from the opposite

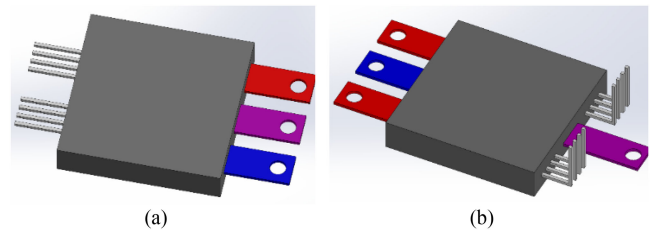


Fig. 22. Power terminals and signal pins arrangement for most of the double-sided power modules.

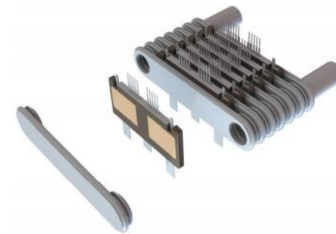


Fig. 23. Double-sided power module in a stack cooling system, [60], ©[2019] IEEE.

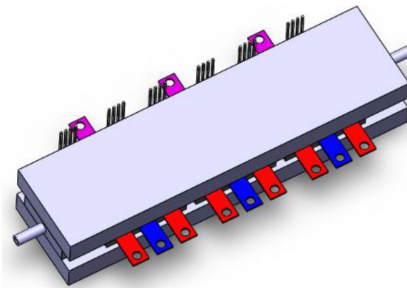


Fig. 24. Double-sided power modules placed horizontally between two cooling systems [63], [64].

side, considering an entire side for the input/output channels of the cooling system. Fig. 23 shows such a system design with a heat exchanger stack [60], [61]. The commercial module reported in [62] employs this cooling scheme.

The power module, as shown in Fig. 22(b), has its power and load terminals on opposite sides. In this case, the gate driver should be placed on top of the cooling system on the upper side of the power module while the ac busbar will go outwards. The gate driver pins are bent upwards in such a power module design but the length of the pins limits the overall thickness of the cooling system. Fig. 24 shows a horizontal system design with double-sided power modules [63], [64]. Commercial modules reported in [60] and [65] employ such a cooling scheme. Other compact commercial double-sided power modules are reported in [66] and [67].

In some double-sided power modules, the orientation of the power terminals and the gate driver pins creates additional system design constraints. As shown in Fig. 4, the power and gate terminals are on the same side of the compact double-sided module that limits the system design options and results in a complicated PCB design for the gate driver board [18], [68].

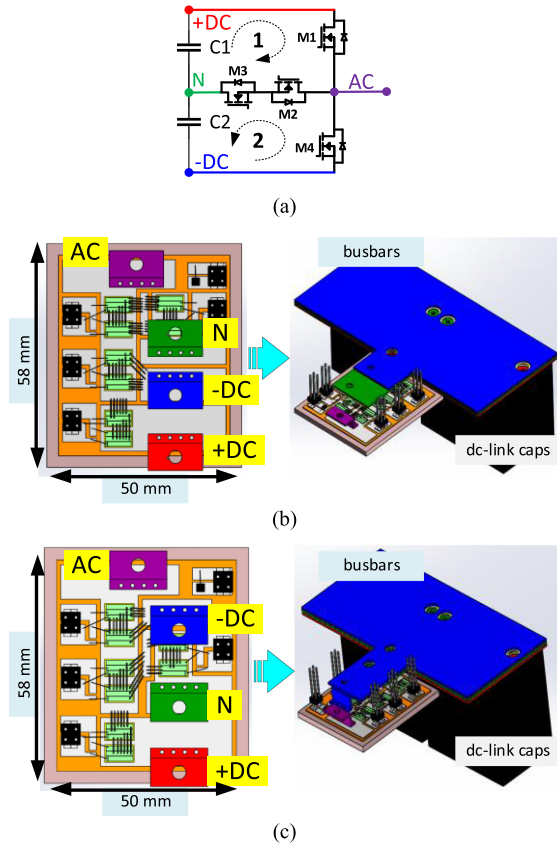


Fig. 25. T-inverter phase-leg: (a) current loops, (b) design I, and (c) design II.

5) *Arrangement of the rest of the power terminals such as outputs and neutral point if there are any:* In case the power module has a different switching arrangement than an HB, such as neutral point clamp or T-inverter, there will be more power terminals to arrange on the module such as the neutral power terminal in a phase-leg T-inverter, as shown in Fig. 25(a)–(c). In this case, the switching analysis is required to understand the current loops and power paths in the module to be able to correctly predict the minimizing mutual inductances and, hence, the correct placement of the terminals. For instance, in a T-inverter, two current loops exist [see Fig. 25(a)], one between the positive and neutral point and the other between the negative and neutral point [69]. In this module, the neutral power terminal will be connected to the neutral point of the dc-link capacitor bank, i.e., the input side. So, not only the path stray inductance minimization but also symmetrical current loops are critical for an efficient power electronics system performance. Fig. 25(b) and (c) compare two different arrangements for T-inverter phase-leg power modules. In the system design of these power modules, two 60 μF TDK film capacitors are utilized. The power module internal inductance and the busbar inductance are simulated for both current loops 1 and 2 in ANSYS Q3D. The total loop inductance is calculated as follows:

$$L_{\text{loop}} = L_{\text{cap}} + L_{\text{busbar}} + L_{\text{module}} \quad (3)$$

where L_{cap} is the internal inductance of the dc-link capacitor that is similar for both systems in Fig. 25 so is not considered in the

TABLE V
INDUCTANCE COMPARISON BETWEEN T-INVERTER PHASE-LEGS OF DESIGN I AND II

	Current Loop 1		Current Loop 2	
	Module Inductance (nH)	Busbar Inductance (nH)	Module Inductance (nH)	Busbar Inductance (nH)
Design I	10.5	29.5	5.5	24
	Total = 40		Total = 29.5	
Design II	8.3	25	7.7	22
	Total = 33.3		Total = 29.7	

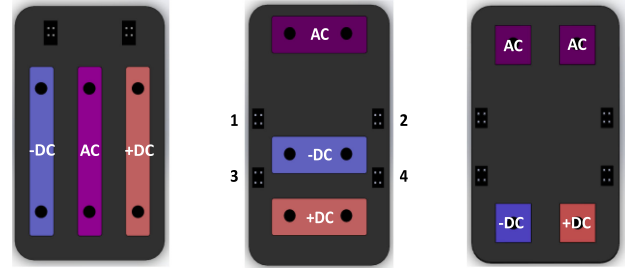


Fig. 26. Three power modules with different terminal arrangements.

calculations of Table V, L_{busbar} is the loop busbar inductance, and L_{module} is the module inductance in the current loop path. As it is given in Table V, in design I, the total inductance of the loops is neither low nor symmetrical. In the second design, however, with rearranging the power terminals accordingly, both loop inductance values are lower and symmetrical.

This is the decision condition C.5 in the flowchart of Fig. 16. The length of the ac terminal is not as important since large inductive filters are often connected to its busbar in many system applications. As such, the ac terminal can be placed anywhere in the power module as long as the capacitance between the ac layout and the base plate does not create a high conductive EMI [70]. In the system design, however, as the number of the paralleled power modules increases, the shape and position of the output terminal busbar take on an added importance. The design of the output busbars needs to be symmetrical for parallel power modules. Then, the current can distribute uniformly among the power modules [34], [71], [72].

Consider the power modules shown in Fig. 26(a)–(c). In Fig. 26(a), the wide terminals in the power module facilitate symmetrical current distribution if all the parallel SiC MOSFETs are alongside the power terminal. This is because the parasitic distribution of the current traces will be equal for all the paralleled bare die [73]. However, the arrangement of the power terminals on the power module suggests a finger design for the system busbars. Since the output ac power terminal is between the positive and negative power terminals, it is more difficult to design a laminated busbar structure for this power module since the output or ac busbar path is independent of the laminated positive/negative power busbars [13]. Fig. 27(a) and (b) shows the possible busbar designs for this power module with the same SBE dc-link capacitor used for the modules of Fig. 18.

In the power module shown in Fig. 26(b), the positive and negative power terminals are positioned alongside each other.

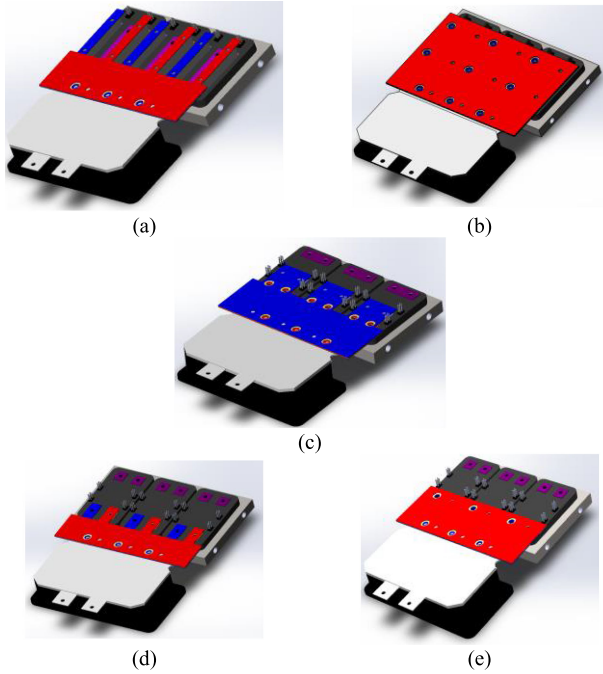


Fig. 27. (a) Finger busbar design and (b) planar busbar design for power modules with side-by-side terminals; (c) planar busbar design for power modules with terminals along the longer edge, (d) finger busbar design, and (e) planar busbar design for power modules with terminals along the shorter edge.

Hence, the power module design requires lamination of the positive and negative power busbars, as shown in Fig. 27(c). Having the ac terminal at the other end of the power module eases the design of the output busbar as well.

The power module shown in Fig. 26(c) has the positive and negative power terminals next to each other on the short edge of the power module. These terminals create short-distance busbars that if designed correctly can have better inductive performance. In Fig. 27(d) and (e), two busbar designs are shown for this power module. These busbar designs are simulated in ANSYS Q3D. In Fig. 28(a), the self-inductance and mutual inductance values of the busbars shown in Fig. 27(a)–(e) are compared. The left bars provide the total self-inductance values (L_1+L_2) and the right bars show the mutual inductance between the two busbars at a frequency of 12 MHz, which considers the switch rise/fall time [57]. The total inductance values that are calculated by L_1+L_2-2M are compared for all these busbar designs in Fig. 28(b).

The inductance value plots show that there is a 75% difference between the inductance values of the system (a) and (e). The power modules with laminated structures can provide the lowest possible inductance because of the short path between the terminals and the dc-link capacitor. The size of the power terminals, however, might be a limiting factor for the power module current capability or the module internal inductance.

6) *Arrangement/placement of power modules next to each other:* The design of power modules should consider the requirements of multiphase power electronics systems. For instance, typically three HB power modules are needed for a three-phase power electronics system. Hence, the design of a

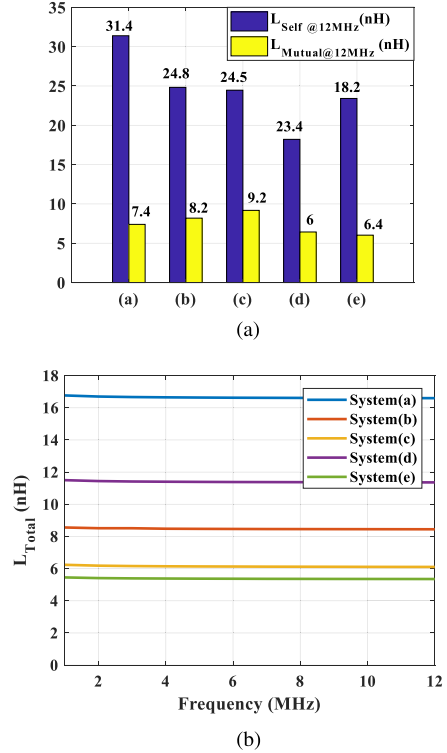


Fig. 28. Inductance value comparison for the busbars shown in Fig. 27(a)–(e). (a) Comparison of the total self-inductance (L_1+L_2) and mutual inductance (M) values at 12 MHz. (b) Comparison of the total inductance values (L_1+L_2-2M) versus frequency.

power module needs to consider the placement of three power modules either next to each other on a cold plate for single-sided power modules or stacked on top of each other on a stack cooling system for double-sided power modules. The positives and negatives shall be able to be connected with wide busbar planes without interfering with the ac busbars and gate driver pins as in the modules shown in Fig. 18(a)–(e) because such designs will somehow compromise the cost-effective, simple, and well-performance busbars. This is the decision condition C.6 in the flowchart of Fig. 16. Fig. 29(a) and (b) shows a single-sided power module with two different arrangements on two cold plates. Considering the spacing between the modules, there is a system volumetric difference between these two power module arrangements. Consider a standard HB power module with a $62 \times L$ mm² area, where L is the length of the power module. Having a system thickness of h , 3 mm spacing between the three modules, and 10 mm spacing between the module and cold plate edges, the arrangement in Fig. 29(a) results in a volume of $h[2.12L + 42.40]$ cm³. From the arrangement shown in Fig. 29(b), a volume of $h[2.46L + 21.32]$ cm³ results. A volume comparison is provided in Fig. 29(c) for a system with a 50 mm height. If L is larger than 62 mm, the second arrangement results in a higher volume. More importantly, the smaller volume arrangement in Fig. 29(a) leads to a smaller cold plate or cooling system with better performance, a lower pressure drop, and a lower price. The power density comparison between the six power modules in Fig. 18 shows that the dependence of the

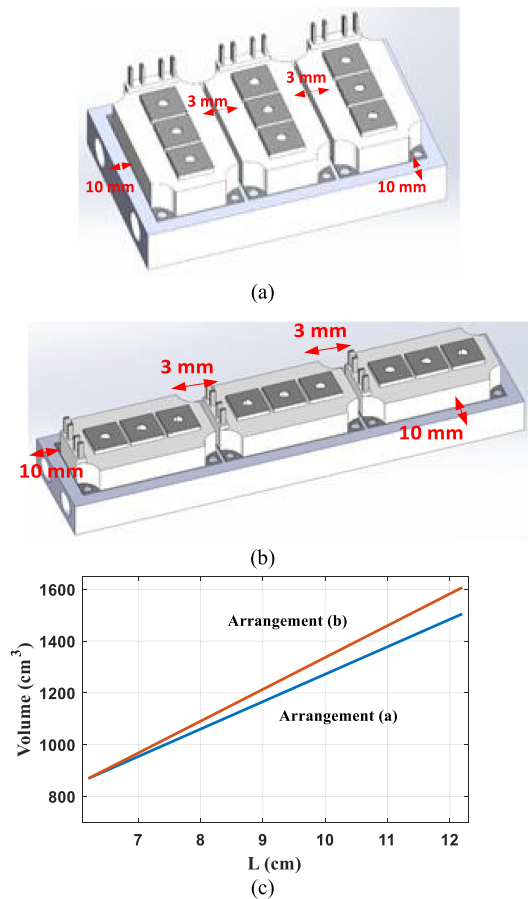


Fig. 29. Single-sided power module with two different arrangements on two cold plates. (a) $[2.12L + 42.40] \text{ mm}^3$, (b) $h[2.46L + 21.32] \text{ mm}^3$, (c) volume comparison between the arrangement (a) and (b) when h is 50 mm.

system power density is not only on its size but also its power and signal terminal arrangements, which will eventually affect the way the modules are arranged next to each other in a multiphase system. Note that the system for the module design of Fig. 18(a), which has long edges higher than 62 mm, that needed to be arranged along the longer edges of the modules to achieve a wide low-inductance busbar has the lowest power density because of its overall design and terminal arrangement deficiency. Of course, one should consider the required form factor by the system application that can lead to different orientations of the modules such as the circular orientation of modules integrated inside a motor. This does not change the fact that the placement of power and signal terminals should accommodate the orientation of the modules, making it more convenient to attach different terminals of the modules to each other accordingly.

7) *Considering the cooling system in a single-sided module and selection of the system design category for the double-sided power module:* The power and gate terminals should be arranged considering the cooling system and gate driver board. This is the decision condition C.7 in the flowchart of Fig. 16.

In a double-sided power module, having considered three power modules (in the case of a three-phase system), it is critical to know whether the double-sided power modules are suitable

for a vertical stack cooling system, as shown in Fig. 23, or it is easier to place them horizontally on a cold plate and put another cold plate on its top layer, as shown in Fig. 24. Hence, it is possible to learn if the power module is designed appropriately to be located inside a system to easily attach to the control and gate driver board, dc-link capacitor bank, load, and supply.

If, for instance, the output terminal gets in the way of the gate driver board or there is not enough space, i.e., an empty side on the system to place the dc-link capacitor bank and connect it to the positive/negative power terminals in either vertical or horizontal design, the terminals of double-sided power module layout should be rerouted as shown in the decision condition box of C.6 in the flowchart of Fig. 17.

III. CONCLUSION

The architecture, integration level, and system compatibility of power modules were reviewed and analyzed in this article. The full utilization of the superior electrical and thermal performances of the WBG semiconductors requires an advanced packaging architecture solution. The integration of power devices with gate drivers and passive components inside the power modules is also desired to take advantage of the WBG power devices. However, a novel low-inductance power module package is still not good enough to achieve the goals of a high-power-density power electronic system. A small, ultralow inductive power module requires a power electronic system designed using the same design strategy around the power module, such as the cooling system, the dc-link capacitors, and busbars, to enable a high power density and high-performance power electronic system. System designers and power module packaging designers do not always mitigate each other's needs to achieve the highest power densities in a power electronic system. Although completely independent of each other, these two design aspects are intertwined. For this reason, a complete analysis of the system compatibility of a power module design for both single-sided and double-sided power modules was described in this article. Commercially available and laboratory prototype power module designs were compared to each other, and their merits and demerits from a system-designer point of view were studied. Finally, a methodology for designing an optimized power module considering its system compatibility was proposed.

REFERENCES

- [1] H. A. Mantooh, M. D. Glover, and P. Shepherd, "Wide bandgap technologies and their implications on miniaturizing power electronic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014.
- [2] J. Morroni and P. Shenoy, "Understanding the trade-offs and technologies to increase power density," Texas Instruments, Dallas, TX, USA, 2020.
- [3] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020.
- [4] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, 2017.
- [5] C. M. DiMarino, B. Mouawad, C. M. Johnson, D. Boroyevich, and R. Burgos, "10-kV SiC MOSFET power module with reduced common-mode noise and electric field," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6050–6060, Jun. 2020.

- [6] T. Gongyue, L. J. Bum, and C. T. Chong, "Thermal design and analysis of high power SiC module with low profile and enhanced thermal performance," in *Proc. IEEE 18th Electron. Packag. Technol. Conf.*, Singapore, 2016, pp. 823–828.
- [7] H. Niu, "A review of power cycle driven fatigue, aging, and failure modes for semiconductor power modules," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, Miami, FL, USA, 2017, pp. 1–7.
- [8] M. Kwak, M. Joung, and K. H. Kim, "The thermal and mechanical properties of reinforced AlN with metal bonding types," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, pp. 978–981, 2019.
- [9] H. Zhang *et al.*, "Effects of sintering pressure on the densification and mechanical properties of nanosilver double-side sintered power module," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 5, pp. 963–972, May 2019.
- [10] Y. Zhang, H. Nee, T. Hammam, I. Belov, P. Ranstad, and M. Bakowski, "Multiphysics characterization of a novel SiC power module," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 3, pp. 489–501, Mar. 2019.
- [11] U. Scheuermann, "Reliability of planar SKiN interconnect technology (invited)," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, pp. 1–8, 2012.
- [12] K. K. Lwin, C. E. Tubillo, T. J. Dimaano Panumard, N. Suthiwongsunthorn, and S. Sirinorakul, "Copper clip package for high performance MOSFETs and its optimization," in *Proc. IEEE 18th Electron. Packag. Technol. Conf.*, Singapore, 2016, pp. 123–128.
- [13] R. Alizadeh *et al.*, "Busbar design for distributed DC-link capacitor banks for traction applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Portland, OR, USA, 2018, pp. 4810–4815.
- [14] A. D. Callegaro *et al.*, "Bus bar design for high-power inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2354–2367, Mar. 2018.
- [15] M. Chinthavali, Z. J. Wang, S. Campbell, T. Wu, and B. Ozpineci, "50-kW 1kV DC bus air-cooled inverter with 1.7 kV SiC MOSFETs and 3D-printed novel power module packaging structure for grid applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 133–140.
- [16] Z. Liang, "Planar-bond-all: A technology for three-dimensional integration of multiple packaging functions into advanced power modules," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Chicago, IL, USA, 2015, pp. 115–118.
- [17] N.-C. Sintamarean, "Automotive MOSFETs current handling in," Infineon Appl. Note, Munich, Germany, 2015.
- [18] L. M. Boteler, V. A. Niemann, D. P. Urciuoli, and S. M. Miner, "Stacked power module with integrated thermal management," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Delft, The Netherlands, 2017, pp. 1–5.
- [19] R. C. Burns, "Power stack—Advantages and reliability of an aluminum," in *Proc. Power Convers. Intell. Motion*, Nuremberg, Germany, 2016, pp. 969–975.
- [20] S. Huang, Z. Xu, F. Yu, and S. S. Ang, "Impact of nano-diamond composites on low-temperature co-fired ceramic interposer for wide bandgap power electronic module packages," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, Fayetteville, AR, USA, 2016, pp. 314–318.
- [21] S. Huang and S. S. Ang, "Investigations of low temperature co-fired ceramic heat spreading interposer for the thermal management of three-dimensional packages," in *Proc. IEEE Thermal Meas., Model. Manage. Symp.*, San Jose, CA, USA, 2018, pp. 8–12.
- [22] A. Dutta and S. S. Ang, "A module-level spring-interconnected stack power module," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 9, no. 1, pp. 88–95, Jan. 2019.
- [23] H. Stomberg, B. Abrahamsson, and O. Saksvik, "Modern HVDC thyristor valves," ABB Power Syst.
- [24] F. D. Barlow and A. Elshabini, "High-temperature high-power packaging techniques for HEV traction applications," Oak Ridge Nat. Lab., Moscow, ID, USA, 2006.
- [25] T. Stockmeier, P. Beckedahl, C. Göbl, and T. Malzer, "SKiN: Double side sintering technology for new packages," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, San Diego, CA, USA, pp. 324–327, 2011.
- [26] R. Alizadeh, K. U. Porter, T. Cannon, and S. Ang, "Fabrication of ceramic interposers for module packaging," *J. Microelectron. Electron. Packag.*, vol. 17, no. 2, pp. 67–72, 2020.
- [27] R. Alizadeh, T. Adamson, J. C. Balda, Y. Zhao, M. Asheghi, and K. E. Goodson, "A compact 50-kW traction inverter design using Off-the-Shelf components," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, 2019.
- [28] P. K. Ghosh *et al.*, "High temperature capacitors using AlN grown by MBE as the dielectric," *J. Vac. Sci. Technol.*, vol. 36, no. 4, pp. 2166–2174, 2018.
- [29] Z. Dong, X. Wu, and K. Sheng, "Suppressing methods of parasitic capacitance caused interference in a SiC MOSFET integrated power module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 745–752, Jun. 2019.
- [30] B. N. An *et al.*, "A highly integrated copper sintered SiC power module for fast switching operation," in *Proc. IEEE Int. Conf. Electron. Packag. iMAPS All Asia Conf.*, Mie, 2018, pp. 375–380.
- [31] B. Mouawad, J. Espina, J. Li, L. Empringham, and C. M. Johnson, "Novel silicon carbide integrated power module for EV application," in *Proc. Workshop Wide Bandgap Power Devices Appl. Asia*, Xi'an, China, 2018, pp. 176–180.
- [32] Z. Huang *et al.*, "A novel low inductive 3D SiC power module based on hybrid packaging and integration method," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 3995–4002.
- [33] A. Stippich *et al.*, "A highly-integrated SiC power module for fast switching DC-DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, USA, pp. 5329–5336, 2019.
- [34] T. Hirao, K. Wada, and T. Shimizu, "Circulating resonant current between integrated half-bridge modules with capacitor for inverter circuit using SiC-MOSFET," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1555–1562, Mar./Apr. 2018.
- [35] M. Schmenger *et al.*, "Highly integrated power modules based on copper thick-film-on-DCB for high frequency operation of SiC semiconductors—Design and manufacture," in *Proc. Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–8.
- [36] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 1886–1893.
- [37] X. Zhao *et al.*, "Flexible epoxy-resin substrate based 1.2 kV SiC half bridge module with ultra-low parasitics and high functionality," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 4011–4018.
- [38] Q. Hua *et al.*, "Full-integrated power module for motor drive applications," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, Kanazawa, Japan, 2013, pp. 289–292.
- [39] H. N. Shah *et al.*, "Power electronics modules for inverter applications using flip-chip on flex-circuit technology," in *Proc. IEEE Ind. Appl. Conf.*, Seattle, WA, USA, 2004, pp. 1526–1533.
- [40] J. L. Marchesini, P. O. Jeannin, Y. Avenas, J. Delaine, C. Buttay, and R. Riva, "Implementation and switching behavior of a PCB-DBC IGBT module based on the power chip-on-chip 3-D concept," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 362–370, Jan./Feb. 2017.
- [41] S. Seal, M. D. Glover, and H. A. Mantooth, "3-D wire bondless switching cell using flip-chip-bonded silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8553–8564, Oct. 2018.
- [42] S. Seal, A. K. Wallace, A. M. Dearien, C. Farnell, and H. A. Mantooth, "A wire bondless SiC switching cell with a vertically integrated gate driver," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9690–9699, Sep. 2020.
- [43] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An SiC-based half-bridge module with an improved hybrid packaging method for high power density applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8980–8991, Nov. 2017.
- [44] A. E. Risseh, H. Nee, and K. Kostov, "Realization of a planar power circuit with silicon carbide MOSFETs on printed circuit board," in *Proc. Int. Symp. Power Electron., Elect. Drives, Automat. Motion Drives, Automat. Motion*, Amalfi, 2018, pp. 1079–1083.
- [45] Rogers Corporation. Ziamen Powerway Advanced Material Co., Ltd. [Online]. Available: <https://blog.rogerscorp.com/2011/08/12/modeling-a-pcb%E2%80%99s-thermal-behavior/>
- [46] G. Lefranc, H. P. Degischer, K. H. Sommer, and G. Mitic, "Al-SiC improves reliability of IGBT power modules," 1998.
- [47] Ziamen Powerway Advanced Material Co., Ltd., [Online]. Available: https://www.qualitymaterial.net/news_list85.html
- [48] H. Shayeghi, S. Pourjafar, M. Maaandish, and S. Nouri, "Non-isolated DC-DC converter with a high-voltage conversion ratio," *IET Power Electron.*, vol. 13, no. 16, pp. 3797–3806, 2020.
- [49] S. Nouri, E. Babaei, and S. H. Hosseini, "A new AC/DC converter for the interconnections between wind farms and HVDC transmission lines," *J. Power Electron.*, vol. 14, no. 3, pp. 592–597, 2014.
- [50] I. C. Kizilyalli, E. P. Carlson, D. W. Cunningham, J. S. Manser, Y. Xu, and A. Y. Liu, "Wide band-gap semiconductor based power electronics for energy efficiency," ARPA.E, Washington, DC, USA, 2018.
- [51] T. McNutt *et al.*, "Module and system considerations to maximize performance," *Mater. Sci. Eng.*, vol. 924, pp. 883–886, 2018.

- [52] S. Buschhorn and C. R. Müller, "Performance of power semiconductor devices and the impact on system level," in *Proc. Power Convers. Intell. Motion*, Nuremberg, Germany, pp. 1474–1481, 2015.
- [53] N. Nourani Esfetanaj, Y. Peng, H. Wang, F. Blaabjerg, and P. Davari, "Analytical modeling of 9–150 kHz EMI in three-phase active rectifiers," in *Proc. IEEE Workshop Control Model. Power Electron.*, pp. 1–6, 2020.
- [54] T. M. Evans *et al.*, "PowerSynth: A power module layout generation tool," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5063–5078, Jun. 2019.
- [55] A. J. Morgan, Y. Xu, D. C. Hopkins, I. Husain, and W. Yu, "Decomposition and electro-physical model creation of the CREE 1200V, 50A 3-Ph SiC module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, pp. 2141–2146, 2016.
- [56] G. Borghoff, "Implementation of low inductive strip line concept for symmetric switching in a new high power module," in *Proc. Int. Exhib. Conf. Power Electron. Appl.*, Berlin, Germany, pp. 1–7, 2013.
- [57] J. Ke *et al.*, "Investigation of low-profile, high-performance 62-mm SiC power module package," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, 2020.
- [58] A. Dutta and S. S. Ang, "Effects of parasitic parameters on electromagnetic interference of power electronic modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 2706–2710.
- [59] S. Sato *et al.*, "Development of high temperature operation SiC power module," *ECS Trans.*, vol. 86, no. 12, pp. 83–90, 2018.
- [60] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive traction inverters: Current status and future trends," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3337–3350, Apr. 2019.
- [61] S. Nozawa, T. Maekawa, E. Yagi, Y. Terao, and H. Kohno, "Development of new power control unit for compact-class vehicle," in *Proc. Int. Symp. Power Semicond. Devices IC's*, Hiroshima, Japan, pp. 43–45, 2010.
- [62] S. W. Yoon, K. Shiozaki, and T. Kato, "Double-sided nickel-tin transient liquid phase bonding for double-sided cooling," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, pp. 527–530, 2014.
- [63] J. Marcinkowski *et al.*, "Dual-sided cooling for automotive inverters - Practical Implementation with power module," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, pp. 1212–1219, 2015.
- [64] "Design case study double sided cooling for hybrid vehicle," Aavid Thermal Div. Boyd Corp., Taipei, Taiwan, 2017.
- [65] M. Anwar, S. M. N. Hasan, M. Teimor, M. Korich, and M. B. Hayes, "Development of a power dense and environmentally robust traction power inverter for the second-generation chevrolet VOLT extended-range eV," in *Proc. IEEE Energy Convers. Congr. Expo.*, Montreal, QC, Canada, pp. 6006–6013, 2015.
- [66] Danfoss. [Online]. Available: <https://www.danfoss.com/en-us/about-danfoss/our-businesses/silicon-power/danfoss-dcm-1000-power-module-technology-platform/>
- [67] Infineon. [Online]. Available: <https://www.autonomousvehicletech.com/articles/1497-infineons-dual-sided-power-module-for-electric-vehicle-systems>
- [68] S. Kaplan, "Broadband model of a stacked power switching module for parasitic inductance extraction," U.S. Army Res. Lab., Adelphi, MD, USA, 2018.
- [69] Z. Wang, Y. Wu, M. H. Mahmud, Z. Yuan, Y. Zhao, and H. A. Mantooth, "Busbar design and optimization for voltage overshoot mitigation of a silicon carbide high-power three-phase T-Type inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 204–214, Jan. 2021.
- [70] Y. Xie, Z. Huang, C. Chen, and Y. Kang, "An EMI performance improved stacked substrate packaging structure with ultra-low parasitics for SiC half-bridge power module," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, pp. 170–186, 2019.
- [71] J. Wang, R. Burgos, D. Boroyevich, and Z. Liu, "Design and testing of 1 kV H-bridge power electronics building block based on 1.7 kV SiC MOSFET module," in *Proc. Int. Power Electron. Conf.*, Niigata, pp. 3749–3756, 2018.
- [72] J. Weigel, J. Boehmer, E. Wahl, A. Nagel, and E. U. Krafft, "Paralleling of high power dual modules: Standard building block design for evaluation of module related current mismatch," in *Proc. Eur. Conf. Power Electron. Appl.*, Riga, pp. 1–10, 2018.
- [73] F. Yang, "Design considerations for paralleling multiple chips in SiC power modules," M.S. thesis, Dept. Elect. Eng., Univ. Tennessee, Knoxville, TN, USA, 2017.