A Pulsed Power Supply Based on an Optimized SFPFN Scheme Producing Large Currents With a Flat Top on a Heavily Inductive Load

Peng E, Wenbin Ling, Aaohua Mao, Jian Guan, Xun Ma, Hongtao Li, Zhiguo Yu, and Mingjun Ding

***Abstract*—A power supply able to generate a pulsed large current (∼26 kA) with a flattop period > 10 ms for a heavily inductive load was designed based on the sequentially fired pulse forming network (SFPFN) scheme with high-energy-transfer efficiency. To overcome the high voltage stress on switching devices due to the SFPFN scheme, a novel electrical circuit topology was developed. In particular, the current changing rate (*di/dt*) on switching devices is limited by new designs of crowbar branch and pulse-forming unit (PFU). The assembled power supply is shown to provide an output current of a flattop of 26 kA and 12 ms on a load of 40 μH and 4.24 mΩ with the predicted improvement in energy transfer efficiency.**

***Index Terms*—Crowbar branch, flattop current, pulse-forming unit (PFU), pulsed power supply, sequentially fired pulse forming network (SFPFN).**

I. Introduction

THE pulsed magnetic window is a novel technique to mitigate the spacecraft communication blackout. To achieve the goal, a pulsed magnetic field with a high-intensity flattop in a large space is needed. For the power supply to generate such a field, a large space means that the load has a large inductance, and a strong field means a large output current. Thus, it is critical to investigate a pulsed power supply that can output a flattop current with a high magnitude on a heavily inductive load [1].

A pulsed power supply with a current flattop can be achieved in two ways, one with an open-loop control [2]–[14] and another with a closed-loop control [15]–[24]. Even though the power supply using a closed-loop control has good characteristics such as high dynamic performance and low current ripple, its achievable current level is limited by the high switching frequency of the power electronic devices. In addition, its structure and control are more complex than that with the open-loop control. Pulsed generators [15], [16], multistage pulsed current sources [17]–[19], and power supplies achieved with the switched-mode converters [20]–[24] are typical examples of closed-loop control power supplies. On the other hand, an open-loop power supply can provide current with higher magnitude [2]–[14]. Furthermore, it has simpler structure and control strategy, which makes electromagnetic interference less a problem. As a result, we determined to use the open-loop control for our power supply.

Traditionally, the capacitor bank [2]–[6] or lumped pulse forming network (PFN) [7], [8] controlled in an open-loop way has been used to generate pulsed flattop current with large amplitude. However, these two schemes have an extremely low energy transfer efficiency, which is defined as the ratio of the effective energy possessed by the load during the flattop to the energy storage of the power supply. Particularly, the bottom width of the waveform driven by the capacitor bank is rather large, which extremely limits the effective energy delivered to the load. Whereas for the lumped PFN, a large amount of energy is wasted on the auxiliary resistor, that is essential to the formation of the rectangular current waveform. Thus, the capacitor bank and lumped PFN are not preferable to generate the pulsed current flattop due to their low energy transfer efficiency.

With the advancement of high power electronics, the sequentially fired pulse forming network (SFPFN) has been developed to generate high-level pulsed current flattops [9]–[14], and the energy transfer efficiency has been improved considerably. So far, the SFPFN has mainly been applied to resistive loads, where the *di/dt* of the switching elements is relatively low, leading to a low reverse overvoltage and high threshold of the dynamic avalanche. In addition, the switching loss is also small and the thermal burden is low. As a result, the stresses of the switching elements and their risks of destruction are low with a resistive load.

However, applying the SFPFN to a heavily inductive load remains a challenge, since the stresses on the switching elements increase dramatically. The di_r/dt (descending rate of current) of the switching elements during the turn-OFF process will rise substantially to boost the overshoot of the reverse voltage [25], [26]. Furthermore, the increased di_r/dt will intensify the reverse current peak [27], causing a lower threshold of dynamic avalanche [28]–[30]. Thus, the risk of overvoltage breakdown

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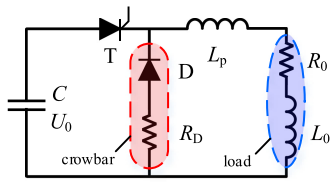

Fig. 1. Capacitor bank scheme.

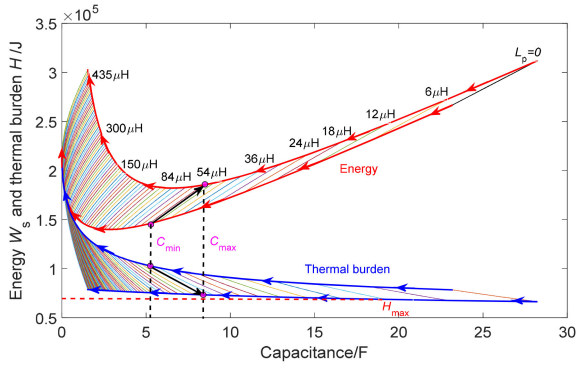

Fig. 2. Energy (W_s) and thermal burden (H) versus C and L_p for the capacitor bank.

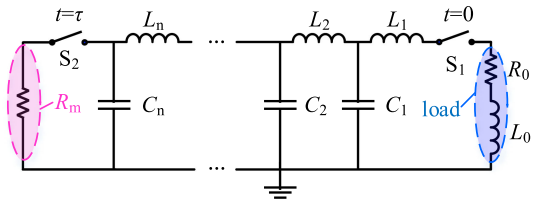

Fig. 3. Lumped PFN scheme.

increases significantly, which is further raised by the temperature rise attributed to the increased switching loss [31], [32]. Meanwhile, for thyristors of the SFPFN, the risk of thermal breakdown due to a high rising rate of the turn-ON current and the risk of spurious triggering are also increased with a heavily inductive load.

To overcome these issues, a novel power supply based on an optimized SFPFN scheme was designed. The detailed design and initial test results will be presented in this article. It is organized as follows. In Section II, the traditional schemes for achieving the design goal are analyzed with critical problems emphasized. In Section III, the design of the novel power supply is presented with details in addressing issues arising from a heavily inductive load. Test results of the power supply are shown and analyzed in Section IV. Finally, Section V concludes this article.

II. Traditional Schemes to Generate a Flattop Current

A pulsed current with amplitude and flattop time larger than 26.6 kA and 10 ms, respectively, on a heavily inductive load (40 μH, 4.24 mΩ) is needed. In this section, the conventional schemes to attain the target are introduced and analyzed.

A. Capacitor Bank

The capacitor bank is the simplest way to achieve the goal. Fig. 1 shows its circuit schematic, where C and U_0 are the capacitance and voltage of the capacitor bank, T and D represent the thyristor and diode, respectively, R_D is the resistance of the crowbar, L_p denotes the pulse forming inductor, and R_0 and L_0 are the load resistance and inductance, respectively. In the crowbar, a resistor R_D is used to dampen current resistively. The capacitor begins to discharge into the load when the thyristor turns ON. When the voltage of the capacitor starts to reverse, the load current flows through the crowbar. The time interval during which the current remains larger than 90% of its peak is defined as the flattop width t_{flat}. Thus, the flattop is not strictly flat and has a ripple of 10%.

It is necessary to find the optimized C, U_0, L_p, and R_D to minimize the storage energy W_s ($= 1/2CU_0^2$) of the power supply. There are three constraints imposed on the optimization problem. First, t_{flat} must be equal to the required flattop time. Then, the current peak I_p should be equal to the target value. At last, the thermal burden $H = \int i(t)^2 R_0 dt$ of the load, where $i(t)$ is the current through it, should be smaller than its allowed maximum H_m(=68.7 kJ).

To perform the optimization, the W_s and H as functions of the capacitance (C) and pulse forming inductance (L_p) are computed and shown in Fig. 2. For any L_p, C can be in a range of [C_{min}, C_{max}] to comply with the first and second constraints by adjusting the value of R_D. Meanwhile, with C increasing from C_{min} to C_{max}, H decreases but W_s increases. H is smaller than H_m only for $L_p < 12$ μH, but the corresponding W_s as well as the capacitance (C) is too large to be acceptable, whereas if W_s reaches the minimum, the thermal burden would be larger than the value allowed for the load. In this situation, $(W_s)_{min} = 144$ kJ for $L_p = 100$ μH and $C = 2.8$ F. However, the capacitance is still too large to be unfeasible. Considering the various factors, a workable design is $C = 18$ mF, $U_0 = 20$ kV, $L_p = 8$ mH, and $R_D = 200$ mΩ with the stored energy of $W_s = 3.6$ MJ. The effective energy transferred to the load is about 18 kJ; thus, the energy transfer efficiency is only about 0.5%, which is extremely low.

B. PFN

The lumped PFN, as shown in Fig. 3, can be used to generate a long rectangular pulse. L_n and C_n are the inductors and capacitors, respectively. To restrain the oscillation of the load current, a matched resistor (R_m) is connected to the main circuit and switched ON at a certain time τ. A possible design is that $L_n = 215$ μH and $C_n = 560$ μF, the discharge voltage $U_0 = 20$ kV, the number of modules $n = 18$, and $\tau = 6$ ms. The simulated current under the abovementioned parameters is shown in Fig. 4. The total energy needed for the PFN is 2 MJ, whereas the effective energy coupled to the load is 20 kJ, and thus, the energy transfer efficiency is very low (only 1%) since most of the energy is dissipated on the R_m.

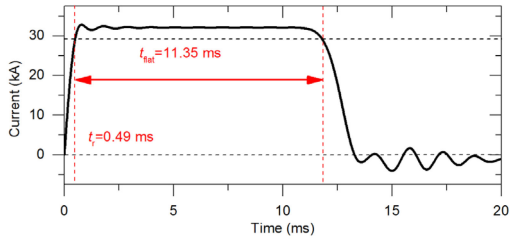

Fig. 4. Simulated current of the lumped PFN.

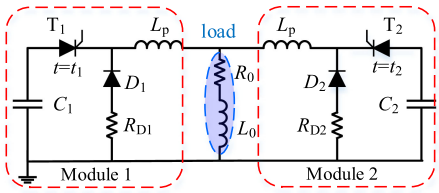

Fig. 5. SFPFN scheme with two modules.

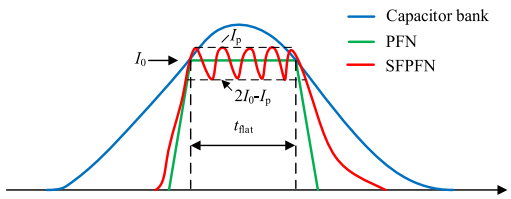

Fig. 6. Flattop current of the capacitor bank, PFN, and SFPFN.

C. SFPFN

Fig. 5 depicts an SFPFN with two modules. C_1 and C_2 are the capacitors with charging voltages U_1 and U_2, respectively. T_1 and T_2 are the thyristors with trigger times t_1 and t_2, respectively. D_1 and D_2 are the crowbar diodes, while R_{D1} and R_{D2} are the resistors in the crowbar branches with the same resistance as $R_{D1} = R_{D2} = R_D$. L_{p1} and L_{p2} are the pulse forming inductors with the same inductance as $L_{p1} = L_{p2} = L_p$. R_0 and L_0 are, respectively, the resistance and the inductance of the load.

The current waveform of the SFPFN is shown in Fig. 6, with that for the capacitor bank and PFN as a comparison. The load current is driven to reach the peak I_p by the Module 1, after which it descends flowing through the crowbar. When it decreases to $2I_0 - I_p$, the Module 2 is triggered to make it reach I_p again. Afterwards, it begins to flow through the crowbar again. To sustain a flattop width of t_{flat}, more modules should be used to repeat the process of the Module 2.

As seen from Fig. 6, the area of the current waveform for the capacitor bank is extremely large. Thus, a large amount of energy is wasted on the load, leading to a low energy transfer efficiency, whereas for the PFN and SFPFN, the energy dissipated on the load is small and basically equivalent. In addition, since a matched resistor of the PFN is not needed in the SPFFN, the energy efficiency of the SFPFN is significantly high compared with the capacitor bank and PFN.

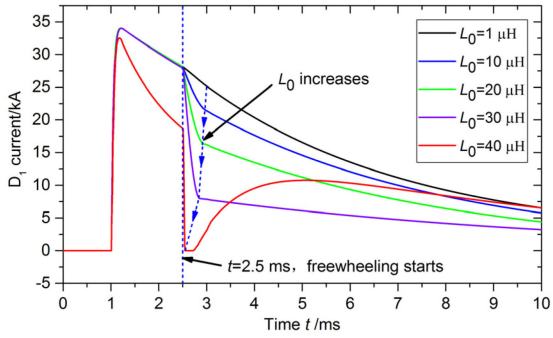

Fig. 7. Current waveforms of D_1 with L_0 as a parameter.

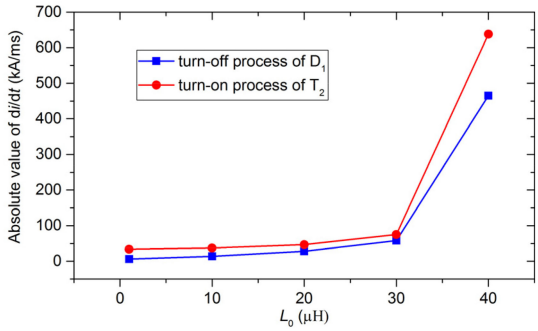

Fig. 8. *DI/DT* of D_1 and T_2 versus L_0.

However, the SFPFN has been mainly applied in the short-circuited or slightly inductive load with low stress on the switching devices, which rapidly increases with the larger inductivity of the load. The loads with $L_0 >> L_p$ are defined as slightly inductive, while the loads with $L_0 << L_p$ are heavily inductive. The performance will be demonstrated by the circuit simulation as follows. To obtain the target flattop, it is necessary to adapt L_{p1} and L_{p2} to match the load. Namely, when the parameters of capacitors and the load are given, the sum of the L_p and L_0 must be a constant. In accordance with our power supply, the parameters of the SFPFN are set as follows in the simulation: $C_1 = 9.6$ mF, $C_2 = 2.4$ mF, $U_1 = U_2 = 2.5$ kV, $t_1 = 0$, $t_2 = 2.5$ ms, $R_D = 1$ mΩ, $L_p + L_0 = 42$ μH, and $R_0 = 4.24$ mΩ.

Fig. 7 shows how the current of diode D_1 varies with L_0. When t equals 1 ms or so, the diode D_1 switches, and the freewheeling begins. Until $t = 2.5$ ms, the T_2 is triggered and D_1 goes into the turn-OFF process. For the slightly inductive load, such as $L_0 = 1$ μH, the D_1 does not reversely recover when reenters the freewheeling period. While for the heavily inductive load, such as $L_0 = 40$ μH, the D_1 turns OFF before starting freewheeling again. Remarkably, the current changing rate *di/dt* of the D_1 current in the turn-OFF process increases sharply with an increase in L_0. Fig. 8 plots the dependence of the *di/dt* on L_0. Thus, we can conclude that a heavily inductive load is detrimental to the power supply. An L_0 beyond a certain threshold would lead a large increase in the current changing rate, and as a result, the reverse voltage overshoot of the diode will increase considerably, which would damage the diode. In addition, a high d*i*/d*t* also increases

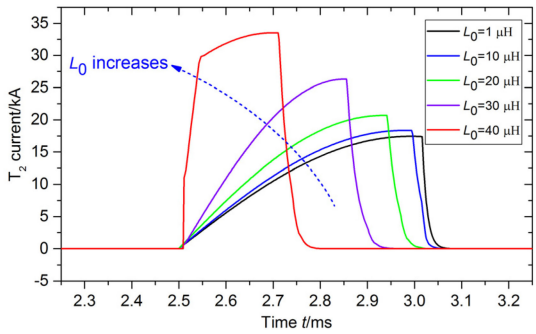

Fig. 9. Current waveform of T_2 with L_0 as a parameter.

the switching loss, which also may damage the freewheeling diode.

Another risk relevant to the high voltage stress of the diode D_1 is as follows. For a heavily inductive load, the high voltage on the D_1 during the turn-OFF process will be exerted on the cathodes of the thyristors. Before discharging, the anodes of the thyristors have the same voltages as the charging levels of the capacitors. Thus, the high forward voltage exerted in the thyristors may increase their risks of erroneous triggering.

Fig. 9 shows the current waveform of the thyristor T_2 as L_0 increases. It can be clearly seen that when T_2 is triggered, its current rising rate and the current magnitude increase significantly as the load becomes more inductive. It is known that when the current rising rate *di/dt* surpasses a certain threshold, the thyristor could be damaged by local thermal concentration. On the other hand, it can be also seen in Fig. 9 that the descending time of the T_2 current is basically constant with respect to different L_0. Thus, the *di/dt* of T_2 during its turn-OFF increases as L_0 increases, and there will be a larger overvoltage during its reverse recovery. Therefore, we can see that its *di/dt*, voltage, and thermal stresses increase substantially as the load is more inductive.

In addition, under the condition of the heavily inductive load, if the electric insulation of the thyristor T_1 did not recover when the T_2 is fired, the capacitor of the second module would discharge into the capacitor of the first module, resulting in a failure to form a pulsed current flattop. Thus, it is urgent to use the thyristor with fast recovery in the case of a heavily inductive load.

In summary, when the SFPFN works under the condition of a heavily inductive load, the stresses of the switching devices heighten considerably, and further improvement of the scheme is needed in order to incorporate it in the power supply design.

III. Structure and Key Technology of the Pulsed Power Supply

A. Structure and Principle of the Pulsed Power Supply

The structure of the novel power supply based on the SFPFN scheme is shown in Fig. 10. The pulsed power supply consists of n modules discharging successively. The nth module with capacitance C_n discharges at the time t_n. Different from the

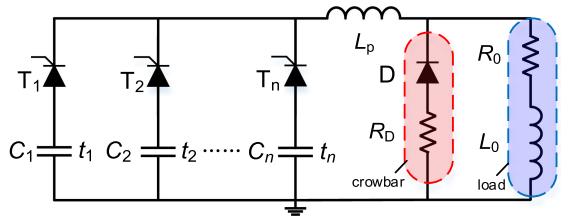

Fig. 10. Structure of the proposed pulsed power supply.

SFPFN in Fig. 5, all modules share one pulse forming inductor L_p and one crowbar branch (D and R_D), making the power supply more cost-effective and compact.

Without considering the resistances for simplification, the parameters of the flattop current can be derived from the energy conservation equations as follows:

$$\frac{1}{2}C_1U_0^2 = \frac{1}{2}(L_p + L_0)(I_{av} + \Delta I)^2 \tag{1}$$

$$\frac{1}{2}C_nU_0^2 = \frac{1}{2}(L_p + L_0)(I_{av} + \Delta I)^2 - \frac{1}{2}L_0(I_{av} - \Delta I)^2 \tag{2}$$

where I_{av} is the mean of the maximum and minimum of the flattop current, and ΔI is the difference of the maximum and the mean. Through (1) and (2), I_{av} and ΔI can be expressed as follows:

$$I_{av}, \Delta I = \frac{1}{2}U_0\left(\sqrt{\frac{C_1}{L_p + L_0}} \pm \sqrt{\frac{C_1 - C_n}{L_0}}\right). \tag{3}$$

For the first and nth (n>1) module, the time of the current increasing from I_{av}-ΔI to I_{av}+ΔI can be obtained through

$$T_1 = \sqrt{(L_0 + L_p)C_1}\arcsin\left(\frac{I_0 - \Delta I}{I_0 + \Delta I}\right) \tag{4}$$

$$T_n = \sqrt{(L_0 + L_p)C_n}\left(\frac{\pi}{2} - \theta\right) \tag{5}$$

$$\theta = \arctan\left[\frac{I_0 - \Delta I}{U_0\sqrt{C_n(L_0 + L_p)}}\right]. \tag{6}$$

It assumes that the current commutates from the thyristor to the crowbar transiently, and the time of the current decreasing from I_{av}+ΔI to I_{av}−ΔI in the freewheeling period satisfies

$$T_3 = \ln\left(\frac{I_{av} + \Delta I}{I_{av} - \Delta I}\right)\frac{L_0}{R_0 + R_D}. \tag{7}$$

Thus, to achieve a flattop current with the width of t_{flat}, the number n of the modules should be

$$n > \frac{t_{flat} - T_1 + T_2}{T_2 + T_3}. \tag{8}$$

And, the trigger time of the modules should be

$$t_1 = 0, t_n = t_r + T_3 + (n-2)(T_2 + T_3), n > 2 \tag{9}$$

where t_r is the peak time of the current driven by the first module. Then, the parameters of the power supply, namely C_n, n, and t_n, can be obtained through (1), (2), and (4)–(9). Since the stray parameters are neglected, C_n and n may be lower than that are

really needed, which can be corrected through the experiments. The parameters of the power supply are finally identified as the capacitance $C_1 = 9.6$ mF, $C_2 = \cdots = C_n = 2.4$ mF, the module number $n = 6$, the discharge voltage $U_0 = 2.6$ kV. The trigger time of the first module is set to be $t_1 = 0$ and other modules are triggered at $t_n = [2.5{+}2.1(n{-}2)]$ ms.

To predict the *di/dt* of the thyristor and the crowbar diode during the turn-OFF process, the turn-OFF current i_c is assumed to linearly decrease from I_{av} to zero and the current of the load is supposed to be constant. Thus, the fall time $T_{T,\,D}$ (T and D means the thyristor and diode) of the current should satisfy the following:

$$\frac{1}{2}C\left(U_{c0} - \frac{1}{C}\int_0^{T_{T,D}} i_c dt\right)^2 - \frac{1}{2}CU_{c0}^2 + (R_c + R_D)\int_0^{T_{T,D}} {i_c}^2 dt \pm \frac{1}{2}L_p I_{av}^2 = 0 \quad (10)$$

where the final term is added for the thyristor and subtracted for the crowbar diode. R_c is the stray resistance of the turn-OFF loop except for the crowbar branch. U_{c0} is the voltage of the capacitor when the switch begins to turn OFF. For the thyristor and the crowbar diode, U_{c0} is expresses as follows:

$$U_{c0T} = I_{av}\left(R_c - \frac{L_p}{L_0}R_0\right) \quad (11)$$

$$U_{c0D} = U_0. \quad (12)$$

Through solving (10), the descending rate of the current is

$$\left(\frac{di_r}{dt}\right)_{T,D} = \frac{I_{av}}{T_{T,D}} \quad (13)$$

$$T_{T,D} = -4C\left(\frac{R_C + R_D}{3} - \frac{U_{c0T}}{2I_0}\right) \pm 2\sqrt{\left[2C\left(\frac{R_C + R_D}{3} - \frac{U_{c0T}}{2I_0}\right)\right]^2 \pm L_p C}. \quad (14)$$

And the voltage of the capacitors when the turn-OFF current of the thyristor or the diode reduces to zero is

$$U_{c1T,D} = U_{c0T,D} - \frac{I_{av}T_{T,D}}{2C}. \quad (15)$$

Then, the revere overshoot voltage of the thyristor and the diode can be approximated as follows:

$$U_{rpT,D} = c_{T,D}L_p\left(\frac{di_r}{dt}\right)_{T,D} \pm U_{c1T,D} \quad (16)$$

where c_T and c_D are the ratios of the maximum *di/dt* in the second portion of the reverse recovery to that in the first portion for the thyristor and diode, respectively. The zero *di/dt* is used to distinguish two portions of the reverse recovery. Before the time at *di/dt* = 0, the current is in the first portion and its slope is negative, while after the time, the current is in the second portion and its slope is positive.

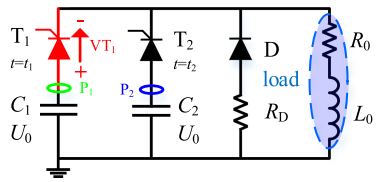

Fig. 11. Circuit to test the recovery time of the thyristor.

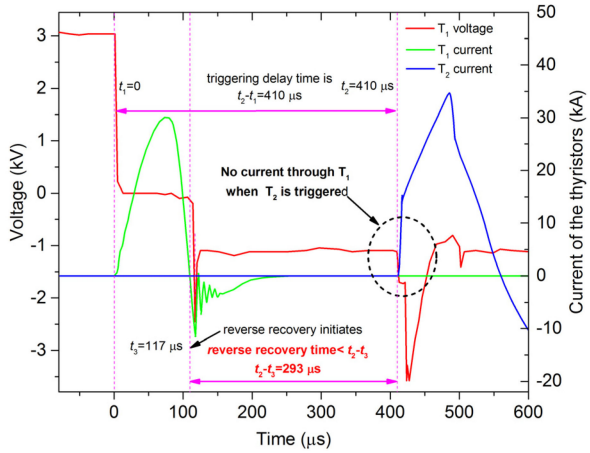

Fig. 12. Test result of the recovery time of the thyristor.

B. Reliable Operation of the Thyristors

During the successive discharging of the modules, it is very critical to isolate the subsequent modules from the former discharged module. The key point for the safe isolation is that the thyristor of the prior module must recover to the reverse blocking state before the subsequent module discharges. Otherwise, the subsequent module would discharge through the prior module, and the current may be extremely large to destruct the thyristors. Therefore, thyristors that recover fast must be used in the power supply. Furthermore, the triggering time delay between the modules should be larger than the sum of the thyristor recovery time and its time of forward conduction.

The recovery time of the thyristors has been tested under the condition of the proposed power supply with $C_1 = C_2 = 300\ \mu$F, $U_0 = 3$ kV, $R_D = 1\ \text{m}\Omega$, $L_0 = 2\ \mu$H, and $R_0 = 2\ \text{m}\Omega$. The test circuit is shown in Fig. 11. T_1 and T_2 are the same thyristors and T_1 is the thyristor being tested. The trigger time of the two modules t_1, t_2 is set to be 0 and 410 μs, respectively. Fig. 12 shows the voltage and current waveforms measured in the test. Note that when T_2 is triggered, there is no current injected into T_1, meaning that T_1 must have recovered before T_2 starts work. Since T_1 begins reverse recovery at time t_3 (117 μs), its time of recovery must be less than t_2–t_3 (293 μs). For the proposed power supply, the recovery time of the thyristor should be much shorter than 1.3 ms, which is the span between the time at which the turn-off current of the former thyristor reaches zero and the triggering time of the next thyristor. So, the tested thyristors satisfy the requirement and can be applied.

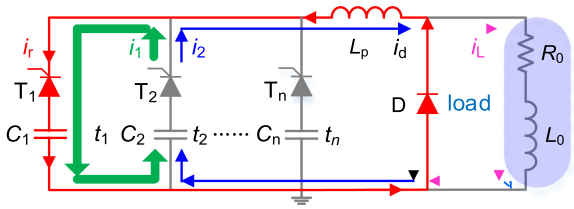

Fig. 13. Turn-OFF loop of the thyristor and current paths when it is broken down or fails to recover electric isolation.

In addition, it is of great importance to ensure that the thyristors do not break down during its turn-OFF phase. Fig. 13 shows the turn-OFF loop of the thyristor and current paths in its failure mode, i.e., when it is broken down or fails to recover electric isolation. The turn-OFF loop is highlighted with the red line, while the fault current paths are marked in green and blue. When the voltage of C_1 reverses, the crowbar diode starts freewheeling and the current of thyristor T_1 begins to decrease. After the current approaches zero, it reverses to continue to sweep out the minority carriers and the thyristor enters the process of reverse recovery [33]. When *di/dt* reaches a maximum on the second stage of the reverse recovery, an intensive voltage overshoot occurs on the thyristor due to inductance. This large reverse voltage spike may damage the thyristor T_1 and make it short-circuited. If this situation were to occur, the electric isolation between the first module and other modules would be broken. As a result, when the another module (for instance the second module) starts to discharge, the first module with extremely low impedance relative to the load would have a large discharge current from the second module flowing into it, while depleting the current needed in the load. Note that the current i_1 may be large enough to damage the thyristor of the second module.

It has been shown that if the di_r/dt of the turn-OFF current of the thyristor is large, the overshoot of the reverse voltage that it can endure would decline dramatically [28], [29]. The reason is that the high di_r/dt would decrease the voltage threshold (V_{av}) of the dynamic avalanche of the thyristor considerably.

It is found that V_{av} satisfies

$$V_{av} = \frac{1}{2}\left(\frac{8}{M}\right)^{\frac{1}{4}}\left(\frac{eN_{eff}}{\varepsilon}\right)^{-\frac{3}{4}} \tag{17}$$

where M is the constant for the ionization coefficient as a function of an electric field, and $M = 1.8 \times 10^{-35}$ cm^6·V^{-7} for the Si semiconductor at the room temperature. e is the electron charge. ε is the permittivity of silicon. N_{eff} is the effective density of the space charge in the N region of the thyristor, and

$$N_{eff} = N_D + p_{ex} \tag{18}$$

where N_D is the doping concentration, p_{ex} is the density of the holes and is written as follows:

$$p_{ex} = \frac{I_{rp}/A_j}{ev_{sat}(p)} \tag{19}$$

where A_j is the conducting area of the thyristor, and $v_{sat}(p)$ is the saturation velocity of the hole.

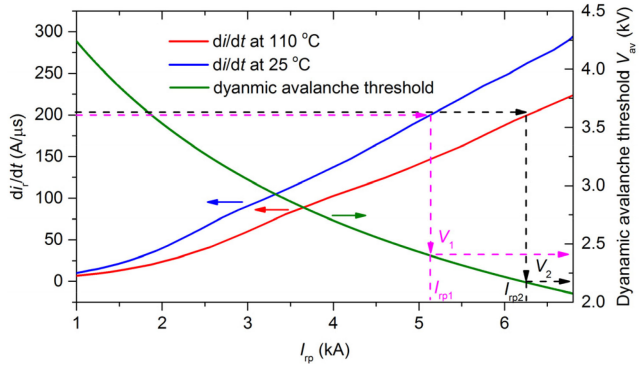

Fig. 14. Relationship between di_r/dt, I_{rp} and dynamic avalanche threshold.

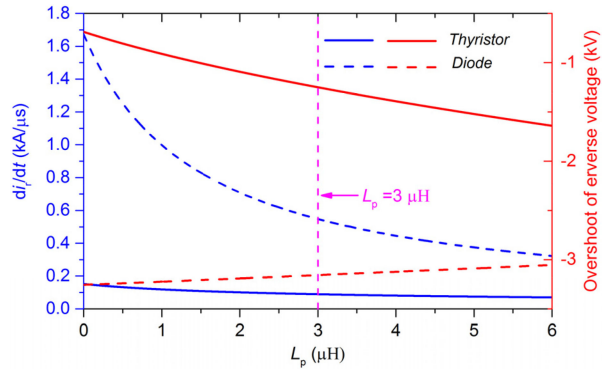

Fig. 15. DI_r/DT, overshoot of reverse voltage versus pulse forming inductor L_p.

A large di_r/dt would lead to a high reverse current peak I_{rp}, and their relationship can be expressed as follows:

$$I_{rp} \approx \sqrt{\frac{2\tau I_F(di_r/dt)}{S+1}} \tag{20}$$

where τ is the lifetime of the carrier, I_F is the forward current, and S is the snappiness. Thus, according to (17)–(20), the voltage threshold V_{av} of the dynamic avalanche decreases remarkably [28], [29] for the proposed power supply with a large di_r/dt and a high forward current.

For the supply, the thyristor H100KMR from TECHSEM is used. Based on the parameters of Lutz *et al.* [28], the relationship of V_{av} and I_{rp} is shown in Fig. 14 with the curves of di_r/dt versus I_{rp} from the user manual. It is seen that if di_r/dt of the reverse current is larger than 0.2 kA/μs, V_{av} is smaller than 2.5 kV. Higher temperature causes a larger I_{rp}, further reducing V_{av}. Since the voltage of the proposed power supply is 2.6 kV, it is extremely important to increase V_{av} by decreasing di_r/dt to avoid overvoltage destruction.

A pulse forming inductor L_p is used [34] to reduce di_r/dt,. According to (13)–(16), the di_r/dt and the reverse voltage overshoot can be obtained for the thyristor and the diode, as shown in Fig. 15. The coefficients c_T and c_D in (16) are determined experimentally, as introduced in Section IV. For the thyristor, with L_p increasing, di_r/dt decreases but the overshoot of reverse voltage increases. For $L_p = 3$ μH, di_r/dt is about 0.09 kA/μs.

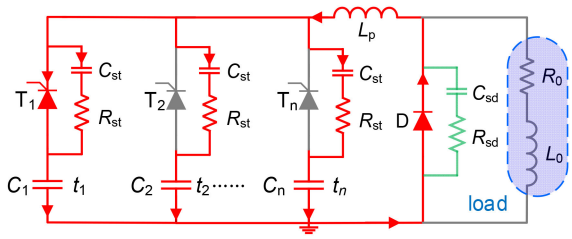

Fig. 16. Turn-OFF loop of thyristor T_1 with snubber circuit.

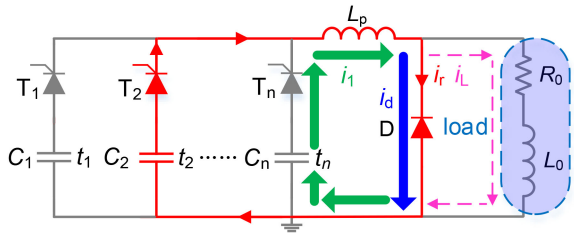

Fig. 17. Turn-OFF loop of the diode and current paths when it fails to turn OFF.

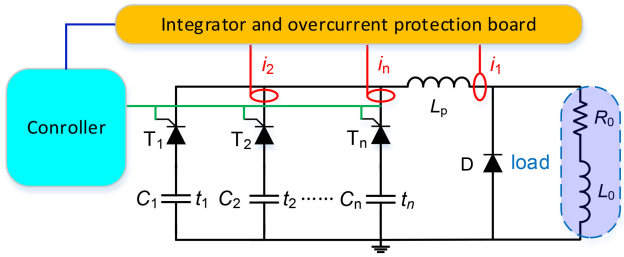

Fig. 18. Control and protection of the pulsed power supply.

Thus, according to Fig. 14, the threshold voltage of the dynamic avalanche is about 2.8 kV, which is larger than the voltage overshoot (1.2 kV). It is noteworthy that the actual allowable voltage may be much lower than the theoretical limit for the voltage since the thyristor was destructed under the reverse voltage spike as about 1 kV in one test. The reason for the destruction may be the inner defect and the inhomogeneity of the thyristor, which would result in a local intensive current density. Thus, the voltage stress must be further mitigated through increasing the dynamic avalanche threshold or reducing the voltage overshoot. However, L_p cannot be increased too much to increase the dynamic avalanche threshold due to the increasing energy of the power supply. So, other measures must be adopted to reduce the overvoltage.

Then, two thyristors are connected in series to alleviate the reverse overvoltage imposed on them. The characteristics of the voltage sharing are tested and given in Section IV. In addition, the snubber circuits paralleled to all the thyristors are applied to reduce the overvoltage. The snubber circuits and the current paths when the thyristor T_1 starts to support a reverse voltage are shown in Fig. 16. Remarkably, when any thyristor turns OFF, all the snubbers start to work in parallel. So, the parameters for each snubber are $C_s = nC_{st}$, $R_s = R_{st}/n$ as $C_{st} = 1\ \mu$F and $R_{st} = 10\ \Omega$. When the thyristor is in the second portion of the reverse recovery, the *di/dt* of L_p is decreased effectively by the snubbers. Then, the voltage spike of the thyristor is weakened. Since only a small amount of energy is absorbed by the snubbers compared to the energy of the power supply, the energy transfer efficiency is not influenced. In addition, the turn-OFF loss of the thyristor is also decreased. Thus, the increase of di_r/dt due to the rising temperature is also prevented.

Furthermore, L_p can also limit the ascending rate of the turn-ON current of the thyristor. When the thyristor turns ON, the current commutates from the diode to the thyristor transiently, with the load current being a constant. Thus, the current ascending rate of the thyristor is the same as the descending rate of the turn-OFF current of the diode. It can be seen from Fig. 15 that the ascending rate of the turn-ON current is reduced with L_p increasing. For $L_p = 3\ \mu$H, the ascending rate is about 0.55 kA/μs, which is much smaller than the allowable maximum 3 kA/μs. Thus, the thermal breakdown due to the local current concentration is avoided.

In addition, to avoid the spurious triggering of the thyristors due to the high forward voltages caused by the reverse overvoltage of the crowbar diode in the turn-OFF process, the pulse forming inductor L_p is designed to isolate the thyristors from the crowbar diode. Meanwhile, the inductance should be small enough to do not influence the load current. In our design, an inductance of 3 μH is applied.

Moreover, there is a high magnetic field around the pulse forming inductor, thyristors, and diode assembly. Since the flat-top width of the current is about 12 ms and the rise time is about 1ms, the field mainly contains the low-frequency components. The strong magnetic field may interfere with the trigger circuits. If the interference occurs, the thyristors may be erroneously triggered. Then, all the capacitors of the modules with spurious triggered thyristors discharge into the regularly working module. Thus, the current through the module becomes extremely large and the thyristor in the module may be damaged. So, the electromagnetic interference must be restrained. The most effective measure is to reduce the distance between the object and the interference source to decrease the magnetic field. So, the layouts of the thyristors and their trigger circuits are optimized. The key point is that the trigger circuits cannot be assembled with the thyristors or close to the pulse forming inductor and the diode assembly. The power supply is organized into a rack with three layers. The pulse forming inductor and the diode are located on the left half of the middle layer, and the trigger circuits are placed on the right-hand side of the top layer, as shown in Fig. 19. The distances between them are more than 1.5 m. A series of tests validated the design of the electromagnetic compatibility of the power supply.

C. Reliable Operation of the Crowbar Diode

The crowbar diode is working under a complex and harsh condition. As one module starts to discharge, the crowbar diode enters the turn-OFF process. Fig. 17 shows the turn-OFF loop (marked in red) and the current paths when the diode fails to turn OFF. When the diode is in the failure mode, the current of

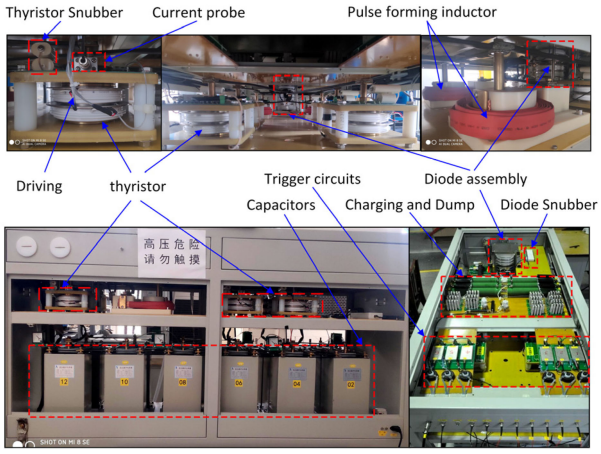

Fig. 19. Practical pictures of the power supply and its components.

the module is labeled as i_1 and the currents through the short-circuited diode and load are labeled as i_d and i_L, respectively. A huge reverse voltage overshoot may occur on the diode due to the stray inductance in the turn-OFF loop. Meanwhile, a large di_r/dt of the turn-OFF current may weaken the ability of the diode to sustain the reverse overvoltage. Once the diode is broken down due to the overvoltage, the current of the later module (i_1) will mainly flow through the crowbar diode (i_d) rather than the load (i_L), leading to the sharp decrease of the load current.

Another challenge to the diode is the high repetition rate of the turn-ON and turn-OFF operations with a frequency of 1 kHz. The diode conducts a large forward current, leading to a great conduction loss and sustains an intensive reverse voltage during the turn-OFF process, resulting in a great turn-OFF loss. Due to the high repetition rate, the heat deposited on the diode cannot dissipate into the environment in time and is accumulated, then makes the temperature of the diode rise rapidly, which increases the lifetime of minority carriers leading to the increased reverse current peak [34] and the reduced threshold of the dynamic avalanche. Then, the ability of the diode to support the reverse voltage is also significantly weakened.

Several measures have been taken to reduce the stresses on the diodes. A pulse forming inductor L_p is used to limit di_r/dt of the turn-OFF current of the diode, and the di_r/dt is decreased to about 0.55 kA/μs for $L_p = 3$ μH, as shown in Fig. 15. Furthermore, the diode assembly is applied, which consists of two parallel branches with three diodes connected in series in each one. The current through the diode assembly is divided equally into two parallel branches; thus, the reverse current through each diode is reduced by half. Therefore, the current rate di_r/dt is also reduced by half, and then the reverse voltage spike is weakened. Meanwhile, the diodes with same characteristics in each branch equally share the reverse voltage, leading to the decreased voltage stress on each diode. In addition, a snubber circuit with $C_{sd} = 10$ μF and $R_{sd} = 1$ Ω is designed for the diode assembly to further limit the reverse overvoltage. Thus, the turn-OFF loss of each diode is also decreased due to the reduced reverse voltage and current. Meanwhile, the conduction loss is also decreased by the parallel connection. In summary, adopting a diode assembly with the snubber circuit can reduce the di_r/dt and switching loss, and limit the reverse overvoltage effectively.

D. Control and Protection of the Pulsed Power Supply

The pulsed power supply uses an open-loop control. A series of trigger pulses for the thyristors generated by a field-programmable gate array (FPGA) are converted to the light pulses, which is transmitted to the trigger circuits of the thyristors through the optical fibers, and then are converted back to the electric pulses before triggering the thyristors. So, the conduction interference can be eliminated by the optical isolation. Meanwhile, an isolation transformer is used for the triggering circuit to isolate the primary terminals of weak signal from the secondary terminals of the strong driving current. The primary weak signal is converted from the light pulses and the secondary terminals are connected to the triggering electrode and cathode of the thyristor. The time intervals between the trigger pulses can be adjusted to obtain the required waveform of the output current. In addition, the controller is put in a shielding aluminum box to reduce the spatial high-frequency electromagnetic interference.

Moreover, a protection circuit is adopted to prevent the failure expanding, which is manifested by the intensive overcurrent. The overcurrent of the thyristor may occur when the diode assembly is broken down, the load is short-circuited, one of the other thyristors is short-circuited or fails to turn OFF, and so on. And if the thyristor is short-circuited or fails to turn OFF, its current would exceed the negative threshold. If the thyristors are triggered spuriously leading to more than one module discharging simultaneously, the current of the pulse forming inductor surges. In addition, if the diode assembly breaks down or the load is short-circuited, the current of the pulse forming inductor also exceeds the normal value.

In the proposed power supply, the positive and negative current thresholds of the protection circuit are 35 and 2 kA, respectively. As shown in Fig. 18, six current probes are used to monitor the current through the thyristors of No. 2–6 and the pulse forming inductor. The current through the thyristor of No. 1 can be monitored by the probe for the pulse forming inductor. If an overcurrent occurs, the corresponding channel of the protection circuit will output logic 1, and logic 0 otherwise. The results of the "or logic" of all channels is sent to the controller. Once the current of any channel surpasses the threshold, the controller receives logic 1 from the protection circuit and stops triggering the subsequent thyristors to reduce the risk.

IV. Test Results

The pulsed power supply based on the abovementioned designs has been constructed and tested. The practical pictures of the power supply and its components are shown in Fig. 19. In the test, the voltage and current are measured by the high-voltage probe of Tektronix P6015A, the Pearson current transducer, respectively.

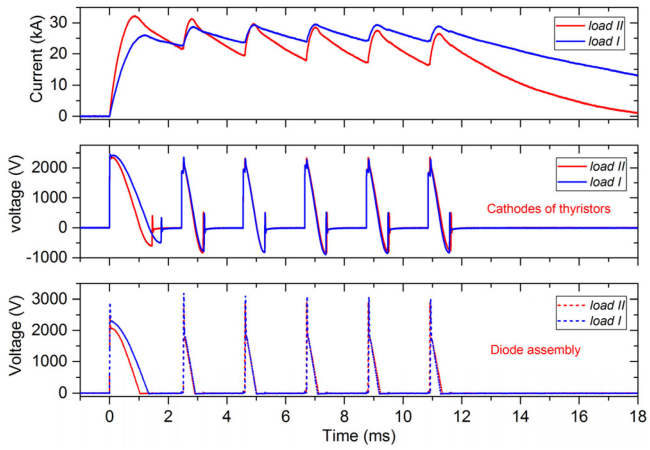

Fig. 20. Output current, the voltage of the cathodes of the thyristors, and the voltage of the diode assembly for two loads.

A. Characteristics of the Output Current and Voltage

The power supply has been tested on two loads, labeled load I with $R_0 = 4.2$ mΩ, $L_0 = 40$ μH and load II with $R_0 = 6.5$ mΩ, $L_0 = 32$ μH. The operating voltage is 2.6 kV. Fig. 20 shows the waveforms of the output current, the voltage of the cathodes of the thyristors, and the voltage of the diode assembly. For the load I, the minimum and maximum of the flattop current are 23.8 and 27.8 kA, respectively. Thus, the mean current is about 26 kA, which is slightly lower than the required 26.6 kA due to the stray parameters in the power supply. The flattop width is about 12 ms, which meets the design requirements.

For the load II with a smaller inductance, the current excited by the first module rises more sharply and reaches a higher level. Meanwhile, the voltages of the cathodes of the thyristors and the diode assembly also descend faster. However, since the resistance of load II is larger, the current in the period of the freewheeling through the diode assembly decays more rapidly, and the peak value of the current successively excited by each module declines gradually. In fact, the descending rate of the current in the freewheeling period depends on the characteristic time of the freewheeling loop, which has a negative correlation with the ratio of the loop inductance to loop resistance. Thus, the output current is rather sensitive to the load resistance and the layout of the diode assembly has been optimized to reduce the resistance of the freewheeling loop as much as possible.

It can be seen from Fig. 20 that the voltages of the cathodes of thyristors and the diode assembly are almost the same for the load I and II after the first module is discharged. It is because that the voltages mainly depend on the period of current ascent, which is less sensitive to the load parameters. The reverse voltage overshoot of the thyristors and the diode assembly are 1.33 and 3.1 kV, respectively, as a result of different di_r/dt and different voltages of the capacitors when they are in the second period of the reverse recovery.

Fig. 21 shows the current through the switching devices and the corresponding *di/dt* during the turn-OFF process of the thyristor and the diode assembly with the operating voltage of

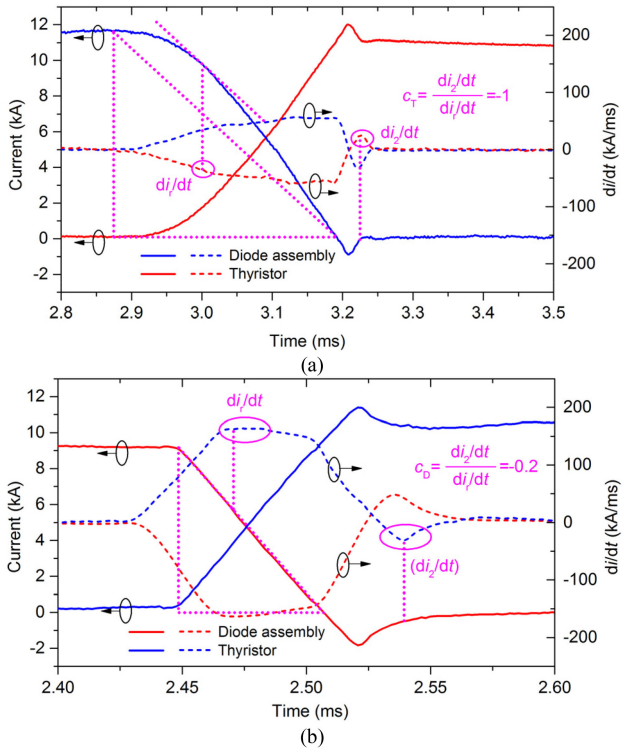

Fig. 21. Current and *di/dt* of the thyristor and diode assembly in the turn-OFF process of the (a) thyristor and (b) diode assembly.

1 kV. The descending rate di_r/dt of the thyristor and the diode assembly is about 0.034 and 0.16 kA/μs. And for the operating voltage of 2.6 kV, the descending rates di_r/dt are about 0.088 and 0.42 kA/μs obtained by multiplying a coefficient of 2.6, which agrees well with the predicted values of 0.088 and 0.55 kA/μs, as shown in Fig. 15.

To obtain the coefficients c_T and c_D in (16), it is noteworthy that the *di/dt* through L_p during the turn-OFF process of the thyristor (diode assembly) is *di/dt* during the turn-ON process of the diode assembly (thyristor). So, c_T for the thyristor can be obtained according to the current through the diode assembly and vice versa for c_D. Through calculations, it is found that $c_T = 1$ and $c_D = 0.2$, and the voltage overshoot can be obtained through (16), as shown in Fig. 15. For the thyristor and the diode assembly, the overvoltage is 1.25 and 3.16 kV, respectively, with the operating voltage of 2.6 kV, which conforms with the estimated result. Thus, the method to calculate the di_r/dt and the reverser voltage spike is applicable.

B. Voltage Sharing of the Thyristors Connected in Series

The characteristic of the voltage sharing of two thyristors connected in series has been tested. The power supply with three modules has been applied to test the thyristors with an operating voltage of 500 V. Fig. 22 shows the voltage of the thyristors and the current through the load. The reference direction of the voltage is from the cathode to the anode. The typical times of the voltage waveforms are as follows.

t_1: The second module starts discharging.

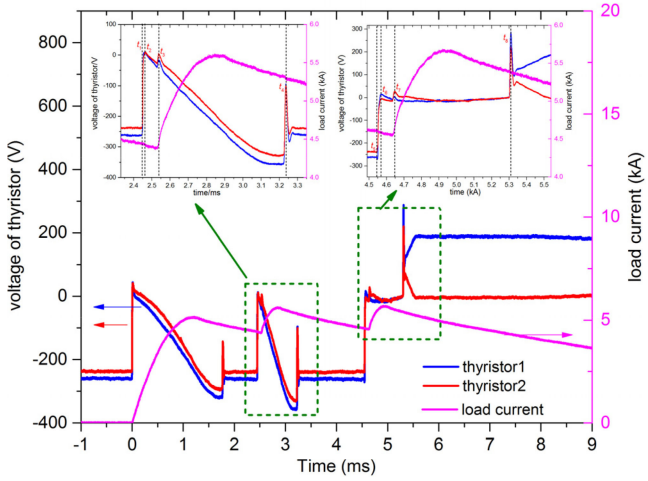

Fig. 22. Voltage waveforms of the two thyristors connected in series.

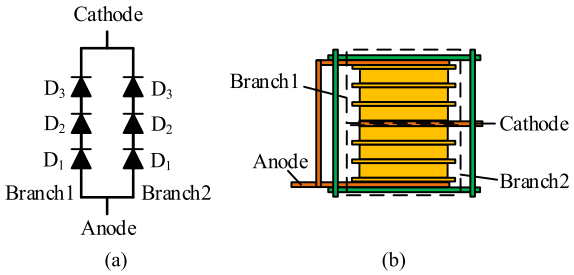

Fig. 23. (a) Circuit model and (b) layout of the diode assembly.

t_2: The turn-ON transient of the thyristors in the second module causes the voltage overshoot.

t_3: The voltage spike of the diode assembly during the reverse recovery is exerted on the thyristors.

t_4: The thyristors of second module turns OFF with a voltage overshoot.

The $[t_5–t_8]$ is the same procedure during the third module discharging as the $[t_1–t_4]$ of the second module. The inactive thyristors share a static voltage, while working thyristors share a dynamic voltage. For the static voltage and the dynamic voltage overshoot, the deviations from the average voltage of the thyristors are within 6.8% and 16.7%, respectively. Therefore, the voltage stress of one thyristor can be reduced by half through using two thyristors connected in series.

C. Current Through the Diode Assembly and the Voltage Sharing

The performance of the diode assembly consisting of two branches connected in parallel with three diodes in each branch has been tested with the operating voltage of 1 kV. Fig. 23 shows the diode assembly. The three diodes are labeled as D_1, D_2, and D_3 from the anode up. Figs. 24 and 25 show the waveforms of the current through the diode assembly and the voltage of each diode. The reference direction of the voltage is from the cathode to the anode. The currents through the two branches of the diode

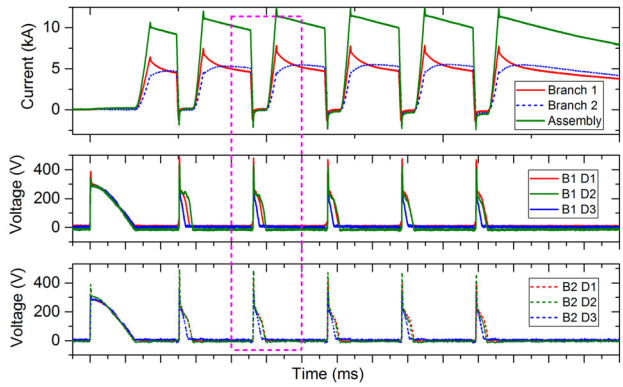

Fig. 24. Waveforms of the current through the diode assembly and the voltage of each diode.

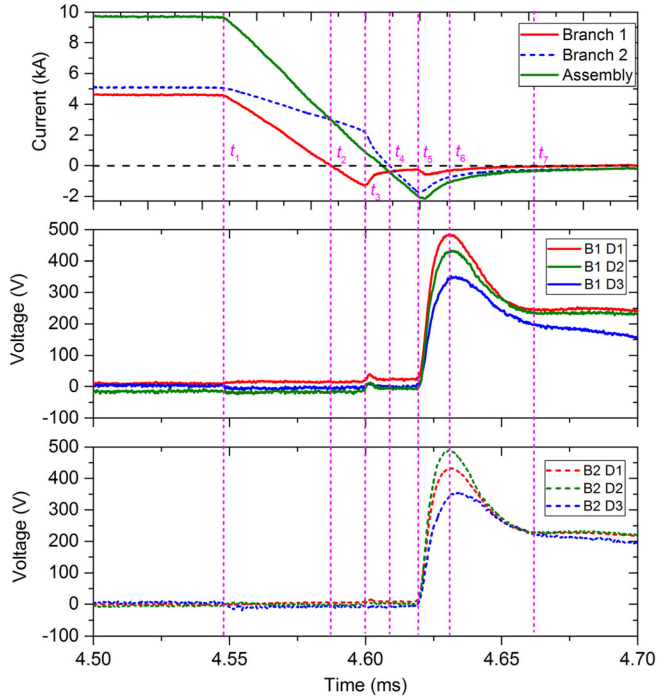

Fig. 25. Waveforms of the current through the diode assembly and the voltage of each diode (local zoom of Fig. 24).

assembly are different due to the different impedance of the two branches. The current through the first branch rises sharply compared to the second branch when the diode assembly begins freewheeling. Also, the current of the first branch descends more rapidly than the second branch while the crowbar begins to turn OFF. However, during the forward conduction, the currents through two branches tend to approach the same. The current is basically shared by two branches, and the conduction losses of them are almost equivalent.

The overshoot of the reverse voltage on the diode assembly is about 1265 V. For the diodes of the first branch, the overshoot voltages are 484 V for D_1, 431 V for D_2, and 350 V for D_3. As to the second branch, the overshoots are 431 V for D_1, 487 V for D_2, and 350 V for D_3. The voltage overshoot of the diode

TABLE I
COMPARISON WITH RELEVANT PULSED POWER SUPPLY

Scheme	Load	*I*/kA	*V*/kV	Flattop/ms	Energy/kJ	η	Element number	Control	Application	reference
Multistage Converter	1 mH	2	2.5	2	7.86	12.7 %	>20	Closed-loop	Particle accelerator	[17]
Switched-mode converter (conceptual)	Resistive or highly inductive	30	10	unlimited	-	-	>90 per module 20 modules	Closed-loop	Particle accelerator, MRI and HVDC circuit breaker	[24]
Pulsed generator	4.16mH, 13.2mΩ	13	6.9	100	20×10^3	5.1%	>17	Closed-loop	Pulsed magnet	[15]
Capacitor bank	2.06mH, 177mΩ	0.68	0.45	10	6.19	7.7%	>37	Closed-loop	Pulsed magnet	[5]
SFPFN	3.2μH, 8.5mΩ	150	10	1.5	1.2×10^3	3%	7 per module 24 modules	Open-loop	Electric gun	[9]
SFPFN	15.6μH, 11mΩ	5	0.3	8	14	1.4%	>20 per module 8 modules	Open-loop	electromagnetic launcher	[10]
Proposed	40 μH, 4mΩ	30	2.6	12	110	12.3%	32	Open-loop	Pulsed magnet	

assembly is basically shared by the three diodes in each branch with a deviation less than 17%. Therefore, the voltage stress on one diode is considerably decreased.

From t_1, the diode assembly enters the turn-OFF process, and the current through the first branch reverses at t_2 and the diodes in the first branch start reverse recovery. Until t_3, the carriers at the ends of the N^- region of the diodes in the first branch are depleted and the reverse current starts to descend. After t_3, the di_1/dt of the first branch becomes positive abruptly. Since the voltage of the capacitor in the turn-OFF loop (see Fig. 17) cannot vary discontinuously, the voltage and *di/dt* of the $L_{\rm p}$ also cannot change suddenly. Then, the total *di/dt* of the diode assembly should change continuously, leading to the magnitude of the DI_2/DT of the second branch increasing instantly. Until t_4, the diodes in the second branch go into reverse recovery. With the carriers swept out as the increasing reverse current, the diode assembly begins to sustain a reverse voltage after time t_5. Then, the *di/dt* of the second branch in the second portion of the reverse recovery reaches the maximum at t_6, when the voltage overshoot occurs. At last, the diodes in the diode assembly recover to the reverse blocking states after time t_7. It is noteworthy that the time to sustain a reverse voltage is determined by the branch that has a smaller di_r/dt. Before the slower branch starts to burden a reverse voltage, the voltage of the assembly is clamped to the sum of the conduction voltage of the diodes in the second branch; however, the current through the first branch changes.

D. Comparison With Other Relevant Pulsed Power Supplies

The total stored energy of the proposed pulsed power supply is about 110 kJ. The effective energy that is coupled to the load is just 12 kJ, leading to an energy transfer efficiency of about 12.3%. Comparison with other relevant power supplies reported in [5], [9], [10], [15], [17], and [24] is tabulated in Table I including the load characteristics, the current, the operating voltage, the flattop, the stored energy, the energy transfer efficiency, the number of elements, the control method, and the application fields. Even though the power supplies with a closed-loop control have a higher energy-transfer efficiency, their current capabilities are limited and structures are more complex. This is especially true for the power supplies achieved by the power electronic converters. The power supplies with an open control can overcome the shortcomings. Remarkably, compared with the capacitor bank, the pulsed generator, and the two SFPFNs, the energy transfer efficiency of our proposed power supply is obviously improved, which implies that the stored energy can be considerably reduced. In addition, from Table I, it is shown that the inductance of the load used in previous SFPFNs are obviously smaller than that used in our pulsed power supply, which reduces the difficulty to realizing the flattop current analyzed in Part C of Section II. Therefore, our pulsed power supply has obvious advantages for the heavily inductive load. Besides, the flattop current sources with a heavily inductive load are extensively applied in the fields, such as pulsed magnet, particle accelerator, high-voltage direct current (HVDC) circuit breaker, magnetic resonance imaging (MRI), and electric gun.

V. CONCLUSION

A pulsed current with a flattop (~26 kA, 12 ms) has successfully realized in a heavily inductive load by a pulsed power supply based on an optimized SFPFN scheme. The crowbar branches and the inductors in each pulse-forming unit (PFU) are removed, and a new crowbar branch and an inductor placed between the new crowbar branch and the modified PFU to limit the maximum current capability of the switches are shared by all modified PFUs. The structure and the key technologies of the proposed power supply based on the optimized SFPFN scheme are introduced. Furthermore, the models to predict the *di/dt* and the reverse voltage overshoot of the switching devices are presented. To make the power supply operate reliably, some key technologies are taken.

1) The thyristors with fast recovery are used to ensure the electric isolation between the modules. A pulse-forming inductor is used to limit *di/dt* of the turn-OFF and turn-ON currents of the thyristors to avoid the breakdown caused by the dynamic avalanche and the local current concentration. Also, the thyristor assembly with a snubber circuit is adopted to further reduce the reverse voltage spike. The thyristors are isolated from the diodes to prevent the erroneous triggering. In addition, the layout of the trigger circuit of the thyristor is optimized to reduce the interference of low-frequency magnetic field.
2) A pulse-forming inductor is utilized to limit the *di/dt* of the diode to reduce the risk of dynamic avalanche. Meanwhile, a diode assembly with a snubber circuit is applied to restrain the voltage stress and the thermal stress exerted on each diode.
3) An open-loop control with optical isolation based on FPGA is used to reduce the electromagnetic interference.

An overcurrent protection circuit is designed to monitor the failure and protect the power supply.

The proposed power supply is tested and the results indicate the availability. Compared with other relevant power supplies, the number of the pulse forming inductor is reduced to get a more compact power supply, and the energy transfer efficiency is improved remarkably.

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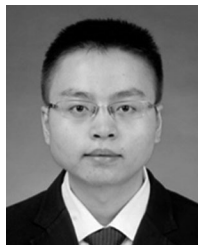

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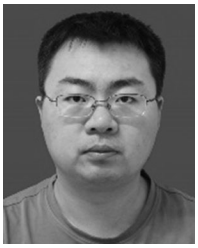

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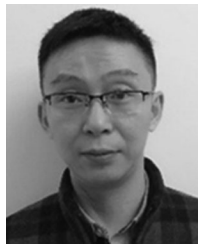

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