A Modified RC Snubber With Coupled Inductor for Active Voltage Balancing of Series-Connected SiC MOSFETs

Chengmin Li, *Member, IEEE*, Saizhen Chen, *Student Member, IEEE*, Haoze Luo, *Member, IEEE*, Chushan Li, *Member, IEEE*, Wuhua Li, *Member, IEEE*, and Xiangning He, *Fellow, IEEE*

***Abstract*—Series connection of SiC power MOSFET is an attractive approach to expand the blocking voltage of SiC devices, whereas the dynamic voltage balancing among the series-connected devices is the most critical challenge of the technique. In this article, a simple, fast, and cost-effective dynamic voltage balancing circuit of the series-connected SiC MOSFETs is proposed to suppress the voltage imbalance among the devices. The proposed circuit is composed of a resistor-capacitor (RC) snubber with a coupled inductor to effectively sense the voltage imbalance and add a compensated signal to the gate driving voltage. In the article, the operation principle of the proposed method is described in detail and the parameter selection of the circuit is given. Then the optimized layout of the circuit in a typical half-bridge SiC power module is proposed to reduce the stray parameters introduced by the coupled inductor effectively. The proposed method is verified by experiments under different conditions. Compared with a purely RC snubber balancing strategy, the capacitor can be significantly reduced. Since only passive components are required in the feedback loop, the proposed method demonstrates a reliable and straightforward approach to achieve equal voltage sharing of the series-connected devices.**

***Index Terms*—Medium-voltage converters, series connection, SiC MOSFETs, SiC power module.**

I. Introduction

MEDIUM voltage (MV) high power converters are widely adopted in worldwide renewable energy generation, variable frequency motor drive, supercharging stations, data centers, and various applications. For the next-generation MV converters, high efficiency, high performance, and high power are generally demanded in a wide range of applications. In special applications, the power density or footprint is also constrained, which are not commonly stressed in conventional MV converters. To meet these requirements, SiC MOSFETs have high switching frequency, high-temperature operation, and low switching loss, which are hoping to significantly improve the performance of the MV converters [1].

Currently, the technology of SiC power MOSFETs is improving and the application in relatively low voltage classes, such as 1200 and 650 V, is booming in electric vehicles and other applications [2]. However, there is still a lack of commercial high-power devices comparable to Si-based high voltage high power devices. Nowadays, although 10 and 15 kV SiC power devices from companies are offered as samples [3], [4], there still exists a series of challenges in the field application of the high voltage high power devices [5], [6], such as the gate electrode reliability, the dramatically increased specific on-state resistance, etc.

Series connection of the SiC power MOSFETs is viewed as one of the effective methods to increase the voltage of SiC MOSFETs-based power converters, which has benefits such as low cost, high-power handling capability, and simple driving from the upper level [5]. However, the critical challenge is the dynamic voltage balancing among the devices, which is essential to ensure the safe operation and the power loss balance. Compared with the widely adopted series connection of Si IGBTs [7], the series connection of SiC MOSFETs is more difficult due to the extremely fast switching speed, which makes the voltage sharing more sensitive to the uneven parameters or gate driving signals mismatch among the devices. Besides, it is also reported that the gate driver architectures and parasitic capacitors in the package have influences on the voltage imbalance [8], [9].

Typically, passive snubbers such as parallel resistor-capacitor (RC) snubber or improved snubbers are adopted in the series-connected devices [10], [11]. The primary purpose is to reduce the voltage slew rate or clamp the drain source voltage to avoid overvoltage of the devices. Adopting the voltage clamping strategy, a power module is proposed in [13] to realize a 3600 V/80 A power module based on the series connection of 1200 V devices, and the overvoltage is limited by the resistor-capacitor-diode (RCD) clamping circuit. In some research works, the high voltage fast speed switch is realized by series-connected SiC

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Chengmin Li, Saizhen Chen, Haoze Luo, Wuhua Li, and Xiangning He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: chengmin.li@epfl.ch; chensaizhen@zju.edu.cn; haozeluo@zju.edu.cn; woohualee@zju.edu.cn; hxn@zju.edu.cn).

Chushan Li is with the Zhejiang University-University of Illinois at Urbana-Champaign Institute, Zhejiang University, Hangzhou 310027, China (e-mail: lichushan@hotmail.com).

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MOSFETs with only one gate driving signal [14], [15]. The blocking voltage is balanced by a relatively complex clamping circuit. However, in the aforementioned methods, the parallel snubber introduces extra switching loss. In [16], a voltage balancing scheme based on energy recovery snubber circuits is proposed. The close loop control over the snubber capacitor voltage is required. Another type of series connection is adopting the super cascade structure [6], [17], which utilizes a SiC MOSFET with the SiC JFET to realize high blocking voltage devices effectively. The drawback is that the turnon or turnoff of the devices is determined by the load current and the switching loss increases in light load conditions. In general, only adding snubbers in the power loop requires a relatively large value of the RC value, which has a significant influence on the original switching trajectory of the SiC MOSFETs. Ideally, it is desired that the behaviors of the series-connected device are the same as the single device. Therefore, such influences should be reduced as small as possible.

In contrast, considering the fact that SiC MOSFETs are fully controllable power devices, it is capable of actively adjusting the voltage imbalance by changing the gate driving voltages. To begin with, the active gate driving time delay method is to utilize the delayed time to adjust the voltage sharing during the turnoff [18]. Typically, a voltage sensing circuit to measure the blocking voltage and a central controller are required to handle the delayed time [19]. Based on this strategy, the mechanism of voltage balancing using driving signal time delay under extremely fast switching conditions is giving and a lookup table is adopted to generate the delayed time in [20]. Compared with passive methods, this method does not bring extra power loss to the power circuit. However, an extra central controller and high-speed communication block in the gate driver are required, which adds complexity and increases the cost.

Another type of solution is to adjust dv/dt during the turnoff of the power device. With the certain strategy, it is realistic to shape the voltage rising waveform by actively changing the gate driving voltage [21]. In [22] and [23], changing the gate driving resistance during different stages of the switching is adopted. In [24], the active gate driving method is adopted to control the voltage imbalance. In [25] and [26], the voltage imbalance is found to be influenced by the parasitic capacitance of the gate driver to the ground. Thus, an active compensation method is adopted to compensate for the voltage imbalance. However, the technique requires a high-speed sampling circuit due to the fast switching speed, and it is challenging to tune the close loop parameters.

Generally speaking, a preferred method to adjust the dv/dt to balance the voltage among the devices should satisfy two conditions. First, if the voltage sharing is ideally balanced, the voltage balancing circuit should not impact the switching speed of the devices. Second, the feedback loop must have sufficient response speed [27]. For example, if the turnoff voltage rising time of SiC MOSFET is 50 ns, the feedback loop should allow such a high-speed signal to pass through the control loop. By engineering experience, the bandwidth of the control loop should be as high as 7 MHz (0.35/50 ns) [28], which brings a very challenging issue on the control loop components, especially in MV operation.

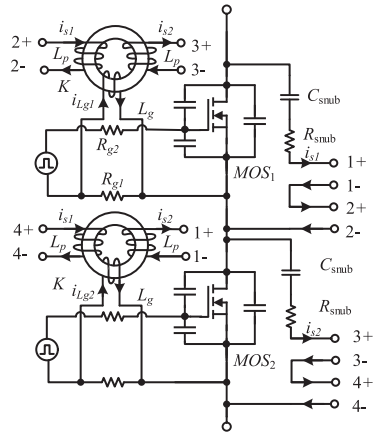


Fig. 1. Proposed voltage balancing circuit based on coupled inductor.

Considering these challenges, this article proposes a modified RC snubber with the coupled inductor circuit to achieve the dynamic voltage balancing [29]. On the basis of the conventional RC snubber, a coupled inductor choke is adopted to sensing the voltage imbalance and realize isolation at the same time. Then the output of the auxiliary winding of the coupled inductor is introduced to the driving voltage of the device to adjust the voltage slew rate accordingly. The proposed method is purely passive and with the proposed optimized design method, the extremely fast response speed can be ensured.

The rest of this article is organized as follows. Section II gives the topology of the proposed method and the operation principle. Section III discusses the parameters design and optimized layout of the proposed method. Section IV gives experimental results. Finally, Section V presents the conclusion.

II. Proposed Circuit and Operating Principle

In an ideal voltage balancing scheme for series connection of the SiC MOSFETs, the fast response speed and limited negative influence on the normal driving of the devices are highly demanded.

So far, compared with other types of voltage balancing circuits, the successfully industrial-applied voltage balancing circuit in the continuous switching scenarios (such as HVDC and MV drive) is the RC snubber, attributing to its simple and reliable structure. In the power circuit that comprises two series-connected SiC power MOSFETs, a parallel RC snubber is always added to achieve dynamic voltage balancing, whereas the snubber capacitance preventing the fast switching speed of the SiC MOSFETs [10].

Considering these facts, to reduce the demanded capacitance in RC snubber, a coupled inductor is added with RC snubber for isolation and sense of the voltage deviation. The proposed circuit is demonstrated in Fig. 1.

In the proposed scheme, an extra three-port coupled inductor links the two snubber circuits of the series-connected devices together. Taking MOS_1 for example, the terminals of the two snubbers $1+$, $1-$ and $2+$, and $2-$ are connected to the two windings of the coupled inductor and then parallel link back to the source electrode of the power MOSFETs. The two windings,

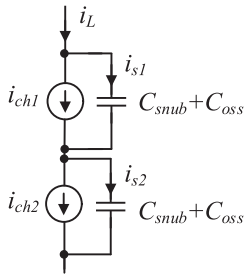


Fig. 2. Equivalent circuit of the series-connected SiC MOSFETs during drain voltage rising period.

termed primary windings, have the same number of turns N_1. The currents flow through the two snubbers are i_{s1} and i_{s2} accordingly. The polarity of the current is arranged as that the magnetic fields caused by i_{s1} and i_{s2} are in the opposite direction. Another winding, called the secondary winding, is connected in parallel to the gate driving resistor R_{g1}. The number of secondary turns is N_2. The total gate driver resistor is divided into R_{g1} and R_{g2}. Typically, R_{g2} is the internal gate resistance of the SiC power module. The magnetic inductance of the coupling inductor is L_p and L_g accordingly.

In the following section, the functionality of the proposed circuit under the unbalanced condition and ideal balanced condition will be discussed separately.

A. *Functionality Under Unbalanced Voltage Condition*

The voltage unbalance is caused by various factors. Apart from the gate driving signals mismatch and the parameter variation of the power devices, there are also reports on the influence of the parasitic capacitors in the circuit [8], [9]. In the analysis, the gate driving time delay mismatch is taken as the example in the following analysis. To begin with, assuming the time delay among the two devices is Δt and the device parameters are the same. The equivalent circuit of the series-connected device is demonstrated in Fig. 2 and the approximation of the turnoff waveform is demonstrated in Fig. 3. In the figure, a linearized approximation of the waveforms is adopted to demonstrate the operating principle [30]. It should be pointed out that the approximated waveform ignores the fast-dynamic transition of the SiC MOSFET and a constant Miller plateau is adopted. Further advanced modeling of the Miller stage transition can improve the accuracy of the analysis, which is ignored here for simplicity. Generally, during the fast voltage rising period, the device can be viewed as the gate voltage-controlled current source. The load current i_L is split into the channel current of the MOSFET and the charging current of the parallel capacitance in this process.

Assuming Δt time delay among the two devices, as shown in Fig. 3, after turn-OFF of the MOS_1 at t_1, the gate source voltage of MOS_1 decreases to the Miller plateau voltage V_{miller}. At t_2, when the channel current cannot support the total output current due to the decreasing gate source voltage, the device channel current i_{ch1} starts to decrease, and the equivalent parallel capacitors, including the output capacitor of the devices and the snubber capacitor, are charged by the partial load current. As a result, the drain source voltage v_{ds_H} of MOS_1 rises first. The

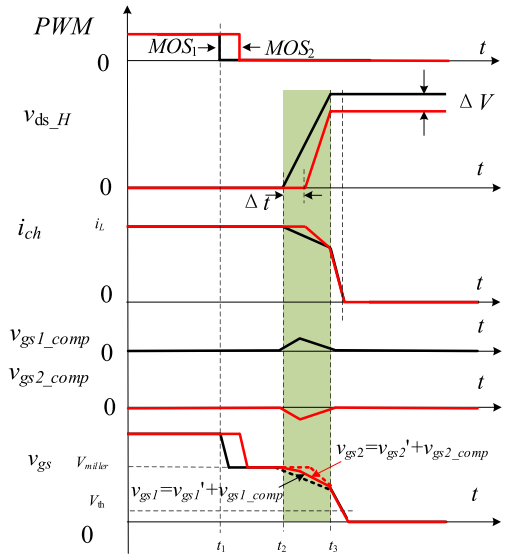


Fig. 3. Turn OFF waveform of the proposed circuit.

voltage change across the snubber induces the capacitor current i_{s1}. After Δt, the voltage of MOS_2 starts to rise and induces i_{s2}. When the total drain source voltage increases to the dc bus voltage at t_3, the drain source voltage starts to oscillate and do not illustrated in Fig. 3.

Since $i_{s1} \neq i_{s2}$, during the voltage transition of the drain source voltage, the differential current generates the magnetic field inside the magnetic core. And consequently, there is an output current induced on the secondary winding of the coupled inductor. The value of the output current i_{g_comp} is proportional to the deviation of the snubber current, namely

$$i_{g\_comp} = \frac{N_1}{N_2}\left(i_{s1} - i_{s2}\right). \tag{1}$$

In this sense, the coupled inductor can be viewed as a differentiate current transducer. The output current introduces an extra compensation voltage v_{gs1_comp} across the R_{g1}. The value is

$$v_{gs1\_comp} = R_{g1}\frac{N_1}{N_2}\left(i_{s1} - i_{s2}\right). \tag{2}$$

The value of the compensation voltage directly reflects the snubber current deviation. Considering that the snubber current is determined by the drain source voltage, the compensated voltage represents the deviation of the drain source voltage of the MOSFETs indirectly. Since R_{g1} is in series with the gate source capacitor of the MOSFET, the compensation voltage caused by the injected current is directly added to the gate voltage. As demonstrated in Fig. 3, there is a positive signal v_{gs1_comp} added to the original gate voltage of MOS_1 v_{gs1}'. As a result, the device current decreases slower compared with no compensation conditions. Therefore, the charging current of the MOS_1 snubber will decrease and the drain voltage rising slew rate is reduced to help the drain voltage of MOS_1 "waiting for" the drain voltage of the MOS_2. A similar process happens to MOS_2, where a negative compensation voltage is added to the gate voltage and consequently, the voltage rising speed is increased to "catch up

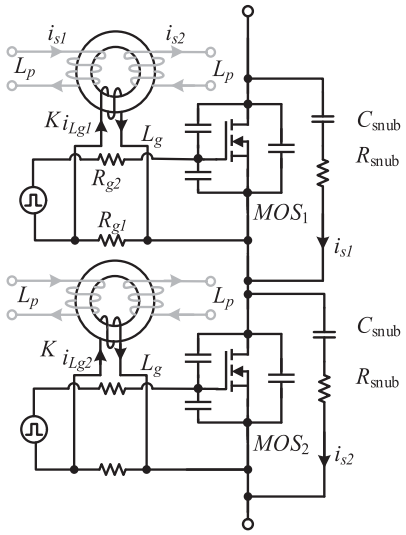


Fig. 4. Equivalent circuit under ideal balanced conditions.

with" MOS_1. Hence, the voltage imbalance between the two devices is reduced.

B. Functionality Under Ideal Balanced Voltage Condition

When the voltage is balanced among the two devices, the proposed circuit should not influence the switching trajectory of the single device. According to the proposed scheme, this contains two aspects, the influence on the gate driving and the influence on the snubber circuit should be reduced with proper design consideration.

The equivalent circuit under ideal balanced condition is given in Fig. 4. Taking MOS_1 for example, with the above-mentioned circuit configuration, under ideal balanced voltage conditions, $i_{s1} = i_{s2}$. As a result, there is no magnetic field exists inside the magnetic core and consequently, there is no voltage drop over the primary winding of the coupled inductor. The coupled inductor can be viewed as short-circuited in the loop. The snubber circuit degrades to the simple RC snubber.

On the gate driver side, when $i_{s1} = i_{s2}$ satisfies, there is no output current of the secondary side turn of the coupled inductor. As demonstrated in Fig. 4, the equivalent circuit contains the magnetic inductor L_g in parallel with the gate resistor R_{g1}. If R_{g1} and L_g are properly selected, the influence of extra parallel-connected L_g on the gate driving circuit can be handled and the extra parallel inductor has little influence on the normal switching of the device. The detailed parameter selection will be discussed in the parameter design section.

C. Circuit for Multiple Devices in Series

The aforementioned analysis is based on two devices in series. Furthermore, the proposed method is still valid for multiple devices in series. The circuit is demonstrated in Fig. 5. The main difference is that the coupled inductor of the first device is connected to the first and second device snubbers. For the *n*th power device, the coupled inductor is connected to the *n*th and $n+1$th power device snubbers. With such configuration, the

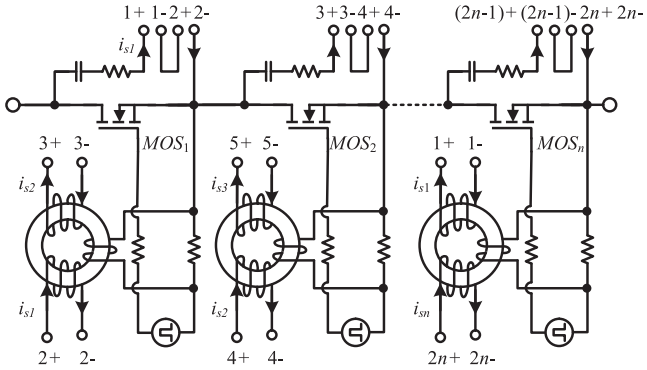


Fig. 5. Circuit diagram for multiple devices in series.

gate source voltage of *n*th power device is adjusted to balance the voltage sharing among the *n*th device and $n+1$th device. Orderly, the voltage sharing of all the devices is balanced. Besides, the last power device is connected to the last device snubber and the first device snubber to achieve the symmetrical main circuit parameters for all the devices. The operation principle of multiple devices in series is similar to the two devices in series. Thus, it is ignored here.

Moreover, although the above-mentioned analysis is using the gate driving signal mismatch as an example, for other influential factors, the voltage imbalance elimination effect is still valid since the close loop compensation method is adopted in the proposed method.

It can be concluded that the proposed strategy functions only when there is a drain source voltage deviation among the devices. When there is no drain source voltage imbalance, the proposed circuit has little influence on the normal driving of the devices. Besides, the feedback back loop is based on passive components. Thus, it is possible to achieve fast response speed to ensure proper tracking of the unbalanced voltage under extremely unbalanced voltage conditions.

III. Modeling and Parameters Design of Proposed Circuit

Based on the working principle of the proposed voltage balancing method, in this section, the mathematical model is given to assist the parameter design in applications.

Considering two devices in series, the equivalent circuit is demonstrated in Fig. 2. In the following analysis, the resistor in the snubber is ignored due to it is typically very small. Since SiC MOSFETs are fully controllable power devices, during the voltage rising period of the SiC MOSFETs, the channel current i_{ch} of the two MOSFET devices satisfies [31]

$$i_{ch} = g_s(v_{gs} - V_{th})^2 \tag{3}$$

where g_s is the transconductance of the SiC power MOSFETs and V_{th} is the threshold voltage. Both parameters represent the intrinsic characteristics of the device and can be extracted from the datasheet. Since the external current i_L is the same for the series-connected devices, the voltage deviation is caused by the different charging current of the parallel capacitors.

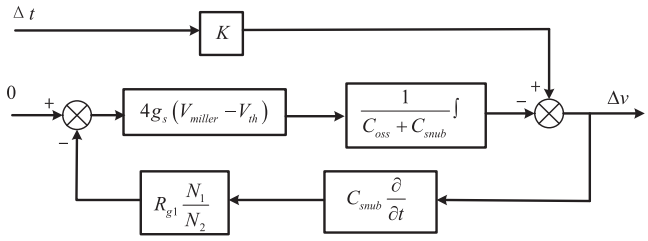


Fig. 6. Close loop control diagram of the proposed circuit.

The differential drain voltage Δv satisfies

$$\frac{d\Delta v}{dt} = \frac{i_{ch1} - i_{ch2}}{C_{oss} + C_{snub}} \tag{4}$$

where C_{oss} is the output capacitor of the SiC MOSFET and C_{snub} is the snubber capacitor. It should be pointed out that C_{oss} is a nonlinear junction capacitance. In this article, C_{oss} is selected as the average junction capacitance to simplify the analysis.

As demonstrated in Fig. 3, in the proposed circuit, extra feedback signal Δv_{gs_comp} is added to the gate voltage, thus

$$\frac{d\Delta v}{dt} = \frac{g_s(V_{miller}-V_{th}+v_{gs\_comp})^2 - g_s(V_{miller}-V_{th}-v_{gs\_comp})^2}{C_{oss}+C_{snub}} = \frac{4g_s v_{gs\_comp}\,(V_{miller}-V_{th})}{C_{oss}+C_{snub}}. \tag{5}$$

Obviously, the voltage deviation is directly controlled by the compensated gate voltage. If there is no proposed active voltage balance circuit, the unbalanced voltage caused by the time delay is a time-dependent function, namely

$$\Delta v\,(t) = F_{turnoff}\,(t, \Delta t)\,. \tag{6}$$

The function $F_{turnoff}(t)$ indicates the variation of the unbalanced voltage with the time to the beginning of the turnoff process. Generally, the analytical model of $F_{turnoff}(t)$ is difficult to acquire due to the nonlinear parameters of the device. From another perspective, the voltage imbalance at the end of the turnoff process can be selected as the criterion to evaluate the performance of the voltage balancing method. In this article, the nonlinear transition modeling of the voltage rising is ignored. In this sense, the unbalanced voltage typically refers to the voltage deviation when the drain source voltage rises to the dc bus voltage. Previous analysis and experiments have verified that the final imbalance voltage ΔV is proportional to the gate driver time delay, namely, (6) can be simplified as

$$\Delta V = K\Delta t \tag{7}$$

where K is the proportional coefficient. Parameter K can be acquired by experiments or analytically modeled from the parameters in the circuit [20].

Thus, the feedback control loop of the voltage imbalance in the time domain is demonstrated in Fig. 6. As depicted, the feedback signal is sampled by the snubber capacitor and through negative feedback, the compensated signal is added to the gate source voltage and modifies the channel current to change the charging current of the parallel capacitors.

Assuming the voltage rising time is t_{rv}, based on the transfer function, the time-dependent output deviation voltage is

$$\Delta v = K\Delta t - \frac{N_1 R_{g1}}{N_2}\frac{4g_s C_{snub}}{(C_{oss}+C_{snub})}\int_0^t (V_{miller}-V_{th})d\Delta v. \tag{8}$$

Considering that when the drain source voltage reaches the dc bus voltage, the unbalanced voltage has the maximum value. When $t = t_{rv}$, the final imbalance voltage ΔV is

$$\Delta V = \frac{K\Delta t}{1 + \frac{N_1 R_{g1}}{N_2}\frac{4g_s C_{snub}(V_{miller}-V_{th})}{(C_{oss}+C_{snub})}}. \tag{9}$$

Let

$$\mathrm{VIRR} = 1 + \frac{N_1 R_{g1}}{N_2}\frac{4g_s C_{snub}\,(V_{miller}-V_{th})}{(C_{oss}+C_{snub})} \tag{10}$$

where VIRR is called the voltage imbalance rejection ratio. It can be seen from (7) that when there is no proposed coupled inductor, the imbalance voltage is $K\Delta t$. Therefore, parameter VIRR indicates the ratio between the unbalanced voltage before and after the proposed method. Or put it in another way, for the desired VIS, VIRR offers another attenuation coefficient abandoning the large snubber capacitor requirement.

Here, the physical meaning of VIRR is straightforward and can be adopted to assess the voltage balancing performance. For example, if VIRR = 100, the unbalanced voltage after the proposed method is 1/100 of the unbalanced voltage without the coupled inductor. In the selection of the VIRR, due to the various influential factors exist in the real circuit, the selection should be determined considering these factors. And a certain margin is suggested based on the real application scenario.

Ideally, VIRR should be as large as possible. From the expression of the VIRR, the turns ratio of the coupled inductor, the snubber capacitor, the gate driver resistor, and the device parameters have a direct influence on the proposed method. By proper selection of these parameters, the unbalanced voltage can be effectively suppressed. Among these parameters, R_{g1}, C_{snub}, and turns ratio can be flexibly defined by the users and will be discussed in the following section.

IV. Parameters and Practical Design Considerations

In this section, the practical design is discussed to achieve the optimized performance of the coupled inductor based voltage balancing circuit. To achieve the tradeoff between the voltage balancing performance and switching loss reduction, the general constraints in selecting the parameters should satisfy: first, the snubber capacitor should be chosen as small as possible to reduce the switching loss; second, the parasitic parameters in the loop should be as small as possible to increase the response speed of the dynamic voltage buffer.

A. Voltage Balancing Coordination Between Snubber Capacitor and the VIRR Parameter

It can be seen in VIRR expression that both the snubber capacitor and the coupled inductor can be adopted to reduce the voltage imbalance. Thus, there exists coordination between the snubber capacitor value and the coupled inductor value. This section gives a step by step parameter selection to achieve low switching loss as well as reliable operation, judging from the engineering perspective.

1) First, the snubber capacitor is selected to roughly tune the unbalanced voltage. Basically, the blocking voltage of the power devices, including the SiC MOSFETs and the body diode, must be limited below the certain value to ensure the power devices operates within the safe operation area (SOA). To avoid the overvoltage protection triggering in the gate driver of the power devices in the normal operation, the snubber capacitor is selected to ensure that the voltage of the power devices is limited within the SOA without any active voltage balancing methods, which is in case some extreme conditions where the active voltage balancing circuit fails.
2) Second, the coupled inductor is designed to finely tune the unbalanced voltage. It can be seen that only within SOA is not enough. The equally important issue is to ensure the precisely balanced voltage sharing among the power devices to ensure the even power loss distribution, which is critical to ensure longtime stable operation.

To achieve the above-mentioned process, the snubber capacitor is selected to limit the maximum voltage imbalance. The relationship between the snubber capacitor and the voltage imbalance should be obtained first. This can be acquired from the results of the published literature [32]. In this article, the index of the voltage imbalance, called voltage imbalance sensitivity (VIS), is adopted to evaluate the performance of the voltage imbalance. The VIS is defined as

$$\mathrm{VIS} = \frac{\Delta V}{\Delta t}. \tag{11}$$

VIS has a clear physic meaning—the unbalanced voltage caused by the unit gate driver time delay. A simple approximation of the VIS is [32]

$$\mathrm{VIS} = \frac{i_L}{2C_{snub}} \tag{12}$$

where i_L is the load current, which can be viewed as constant in inductive load conditions. An example of the relationship between the VIS and the i_L curve is pictured in Fig. 7. Based on the equation, if the desired VIS = 20 V/ns, which means 20 V voltage deviation is caused by 1 ns delay in the gate driving signals, the C_{snub} is selected under the maximum load current conditions. In practice, the desired VIS is evaluated by the design and the random distribution variation of the parameters. For example, if the allowed maximum differential voltage among the devices is 200 V, and the maximum time delay among all the power devices is 10 ns, the desired VIS is 20 V/ns.

It should be pointed out that the model in (12) is deduced under the linear model of the devices. In reality, the device model

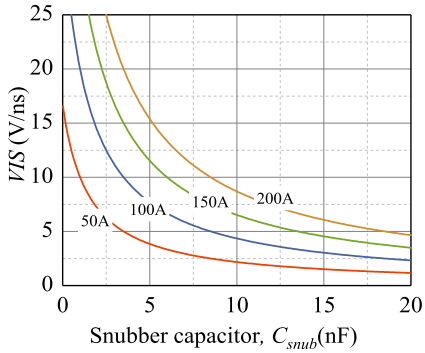


Fig. 7. Relationship between VIS and the snubber capacitance. $C_{oss} = 1.5$ nF.

is highly nonlinear and influenced by the error of the device's datasheet. The curve in Fig. 7 can also be directly measured from a standard test, such as the double pulse test.

Then considering the proposed method is added to the circuit, adopting (9), the modified VIS can be expressed as

$$\mathrm{VIS} = \frac{\mathrm{VIS}_{pre}}{\mathrm{VIRR}} \tag{13}$$

where VIS_{pre} is the VIS without the coupled inductor. It can be seen that VIRR dramatically reduces the voltage imbalance. Based on this parameter, the desired VIRR can be selected in advance. For example, if the desired VIS with the proposed method is to reduce the unbalanced voltage to 0.01 times of the original VIS_{pre}, then VIRR = 100 is selected. Based on (10), the circuit parameter satisfies

$$\frac{N_1 R_{g1}}{N_2} = \frac{(C_{oss} + C_{snub})(\mathrm{VIRR} - 1)}{4 g_s C_{snub} (V_{miller} - V_{th})}. \tag{14}$$

Then it comes to determine N_1, N_2, and R_{g1}. Considering that R_{g1} is the gate driver resistor, which is selected based on the optimal switching of the power devices, such as reducing the switching loss, limiting the *di/dt* etc., in this article, the gate driving resistance is considered as a known parameter that it is designed by other constraints, not for voltage balancing purpose. Then R_{g1} is calculated by gate resistance minus the internal gate resistance of the power module.

Moreover, as given in Fig. 1, relatively high-voltage insulation is required for the coupled inductor. To simplify the insulation coordination design as well as reducing the parasitic capacitance between the primary side and secondary side of the coupled inductor, one or two turns of the secondary side is selected. Since the secondary side turn number is relatively small, the structure is simplified and the overlap between the primary side and secondary side is reduced and consequently, the parasitic capacitance of the coupled inductor is limited. As a result, the primary side turns ratio N_1 is calculated as

$$N_1 = \frac{N_2}{R_{g1}} \frac{(C_{oss} + C_{snub})(\mathrm{VIRR} - 1)}{4 g_s C_{snub} (V_{miller} - V_{th})}. \tag{15}$$

Besides, the coordination between R_{g1} and L_g is important to ensure reliable gate driving of the device. First, the potential oscillation in the gate driving loop should be properly damped. As demonstrated in Fig. 4, the gate loop circuit can be viewed as

a second-order system in the frequency domain. The transfer function between the gate source voltage v_{gs} and the input driving voltage v_{in} is

$$\frac{v_{gs}}{v_{in}} = \frac{1 + \frac{sL_g}{R_{g1}}}{\left(1 + \frac{R_{g2}}{R_{g1}}\right) C_{gs}L_g \cdot s^2 + \left(R_{g2}C_{gs} + \frac{L_g}{R_{g1}}\right) \cdot s + 1}. \tag{16}$$

The characteristic equation of the gate loop circuit is

$$\Delta = \left(1 + \frac{R_{g2}}{R_{g1}}\right) C_{gs}L_g \cdot s^2 + \left(R_{g2}C_{gs} + \frac{L_g}{R_{g1}}\right) \cdot s + 1. \tag{17}$$

Since the inductor is added to the circuit, the important consideration is that enough damping must be added into the loop. The damping ratio ξ of the circuit is

$$\xi = \frac{R_{g2}C_{gs} + \frac{L_g}{R_{g1}}}{2\sqrt{L_g C_{gs}\left(1 + \frac{R_{g2}}{R_{g1}}\right)}}. \tag{18}$$

Based on engineering experience, the critical damping ratio $\xi = 1$ is adopted to avoid possible oscillation in the circuit. Based on the aforementioned equation, the inductance can be calculated by

$$L_g \geq {R_{g1}}^2 C_{gs}\left(\sqrt{1 + \left(\frac{R_{g2}}{R_{g1}}\right)^2} - 1\right). \tag{19}$$

In reality, L_g can be determined by the proper magnetic core selection. It should be pointed out that the above-mentioned analysis does not consider the Miller clamp effect when the drain source voltage is fast rising. Since the gate source voltage is clamped as nearly constant in this stage, the potential oscillation can be ignored in the Miller clamp stage.

Moreover, another important consideration is the increased switching speed due to the parallel inductor. In some cases, the switching speed should be limited, considering the drain source voltage overshoot and EMI issues. This can be solved by adding small extra gate driver resistance in R_{g2} to compensate the switching speed slightly. Such selection can be tuned in a double pulse test or with the help of the analytical model of the SiC MOSFETs.

B. Layout Optimization

The above-mentioned analysis is under the ideal condition without considering the stray parameters. However, there are several nonideal parameters that may influence the performance of the snubber. The most critical one is the parasitic leakage inductance in the snubber circuit. Ideally, the leakage inductance of the snubber circuit should be designed as small as possible to reduce the impedance of the loop. However, in reality, during the charging and discharging of the snubber capacitor, there exists leakage inductance in the snubber loop.

Taking widely applied EconoDUAL type half-bridge package, for example, Fig. 8(a) and (b) demonstrates two possible layout configurations of the RC snubber. The first one is to put snubbers of the two devices on both sides of the module and the

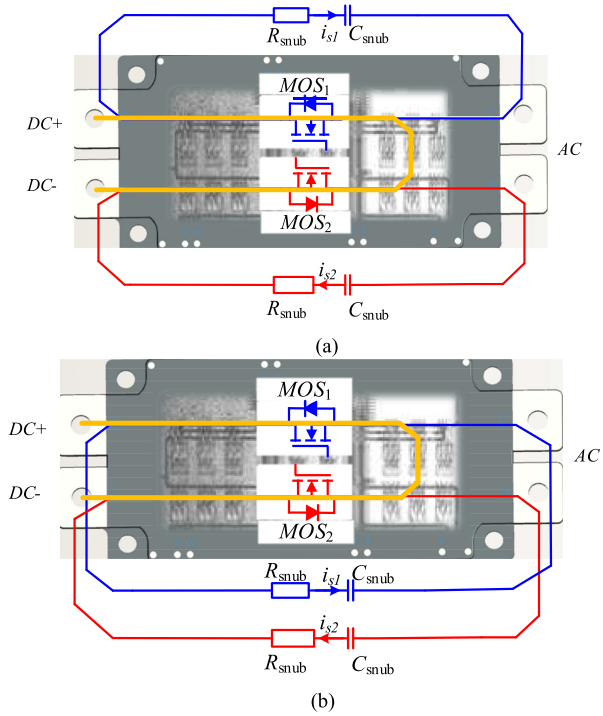


Fig. 8. Optional layout illustration. (a) Snubber circuit on both sides of the power module. (b) Snubber circuit on one side of the module.

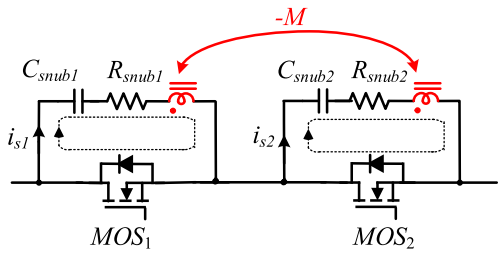


Fig. 9. Equivalent circuit of layout (b) in Fig. 8.

second one is to place the snubbers on one side of the package. It is obvious that the second option has a laminated busbar effect that the magnetic fields generated in the snubber loop of the two snubbers of the power devices are in the opposite direction. Thus, they cancel each other to reduce the total leakage inductance in the loop. This effect can be mathematically explained in Fig. 9. There exists a negative mutual inductance that reduces the total leakage inductance [12]. Herein, in practice, the layout (b) in Fig. 8 is suggested. A similar layout concept can also be adapted to other types of packages for the series connection of the power devices.

Further, Fig. 10 presents a highly integrated layout of the proposed voltage balancing circuit together with the snubbers. In the proposed layout, the coupled inductor is inserted between the power loops of the two snubbers. The winding of the coupled inductor is connected to the snubbers' wiring. With the proper selection of the current direction, the magnetic field inside the magnetic core is in the opposite direction. As stated before, the secondary side of the coupled inductor is one turn and parallel connected to the gate resistor.

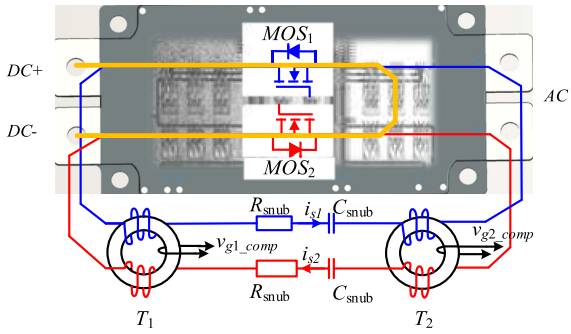


Fig. 10. Placement of the coupled inductor in the series connection of power devices in the same power module.

In this section, the parameter design and optimized layout of the coupled inductor are discussed to guide the practical design of the proposed voltage balancing method. The number of turns is calculated, and the layout of the coupled inductor is given with engineering consideration.

V. Experiments and Simulation Verification

To verify the effectiveness of the proposed method, a prototype is built and tested under various operating conditions. The experimental setup, comparison under different operating points and different snubber capacitors are given in this section.

A. Prototype and Experimental Platform

As a standard package type, two EconoDUAL package SiC power modules (1200 V/200 A) from Rohm are selected as the device under test [33]. As indicated in Fig. 11(a), the two devices in one half-bridge module are connected in series, which forms a single 2400 V/200 A power device.

The picture of the designed snubber is demonstrated in Fig. 11(b). Fig. 11(c) is the final assembly of the power module, snubber circuit, and gate driver. To reduce the volume of the snubber, the TO-247 package resistor is selected in the RC snubber. The snubber capacitor is the film capacitor, which has superior high-frequency response performance. The output capacitor of the power module is 1.5 nF.

In selecting the parameters of the snubber capacitor, the condition that the 10 ns gate driver time delay caused unbalanced voltage should be less than 200 V at 200 A load current is adopted. Thus, according to (11), VIS = 20 V/ns. Using the method in (12), the snubber capacitor is 5 nF. In reality C_{snub} = 4.7 nF is selected. Besides, the snubber resistor is selected as 5 Ω to offer enough damping to the circuit. For the selected device, $V_{th} = 3$ V, $g_s = 1.8$ A/V^2 is extracted from the datasheet. In designing the coupled inductor, VIRR is selected as 120, and R_{g1} = 1.1 Ω is adopted. Besides, in the experiments, R_{g2} = 1.55 Ω, C_{gs} = 18 nF, according to (19), the required magnetic inductor L_g should be larger than 16 nH.

Adopting (15), if $N_2 = 2$, the number of the primary turn N_1 is 4. Considering the rated blocking voltage of the power devices is 1200 V, the insulation voltage among the primary turns is 1200 V, which can be realized by silicon wires or transformer bobbin.

TABLE I
Parameters of the Coupled Inductor

Parameters	Value
Turns ratio (N_1:N_1:N_2)	4:4:2
Magnetic core	Kool Mu MAX
Primary side magnetic inductance L_p	415.3nH
Secondary side inductance L_g	93.8nH
Leakage inductance in the RC snubber loop L_σ	31.0nH

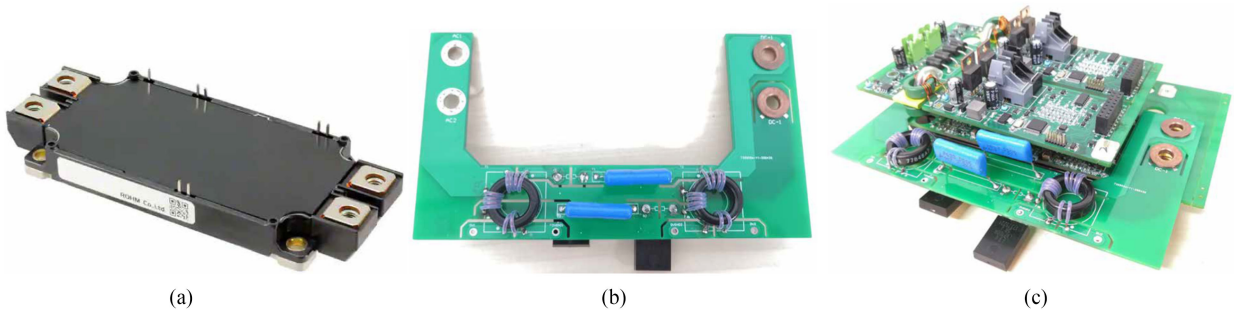
In the final design, the parameters of the coupled inductor are given in Table I.

In the experiments, in each half-bridge module, two devices have independent gate drivers. The digital controller sends the drain source voltage to an FPGA by communication through fiber optics. And the driving PWM of the gate driver can be controlled independently. In the experiments, a manually added 7 ns gate driver time delay is added to simulate the gate driver time delay in real applications. The proposed circuit is verified in a double pulse test platform, as demonstrated in Fig. 12. The load inductor is 500 μH. The current measurement bandwidth is 200 MHz and the voltage measurement bandwidth is 70 MHz.

B. Experimental Waveform

Based on the built circuit and the test platform, first, the operation waveform is acquired through a multiple pulse test. To demonstrate the performance, a comparison between the proposed method and only RC snubber is conducted. In the comparison of results, for the RC snubber cases, the coupled inductor still exists in the RC snubber. However, the feedback winding parallel to the gate resistor R_{g1} is disconnected. The measured waveform is shown in Fig. 13. Fig. 13(a) is the waveform with RC snubber and Fig. 13(b) is the waveform with the proposed method. The waveform is acquired at 1300 V dc bus voltage and 200 A load current. When there is only RC snubber and no active approach is adopted, the unbalanced voltage is 99 V. The peak voltage for MOS_1 is around 800 V. When the proposed method is added, the unbalanced voltage in the turnoff state is almost the same for the two devices, $\Delta V = 2$ V in this case. And the peak voltage is 830 V. Additionally, Fig. 14 demonstrates the zoomed turn OFF transient waveform with (a) turn OFF with RC snubber; (b) turn OFF with proposed method; (c) turn ON with RC snubber; (d) turn ON with the proposed method. In Fig. 14(b), additional oscillation occurs due to the mutual coupling effect and the voltage is almost the same in the steady-state. Comparing with purely RC snubber, the existence of the coupled inductor is good for the voltage sharing of the series-connected power devices.

Further, it is of vital importance to verify the switching loss of the two devices. Table II gives the comparison result of the switching loss of the power devices at 1300 V/200 A. In the table, the switching loss indicates the total loss generated in a switching period, which includes turnon loss, turnoff loss, and the power



(a) (b) (c)

Fig. 11. Design results of the SiC power module for series connection of SiC MOSFETs. (a) Photograph of SiC power module. (b) Prototype of the proposed snubber circuit. (c) Final assembly of the power module, snubber circuit, and gate driver.

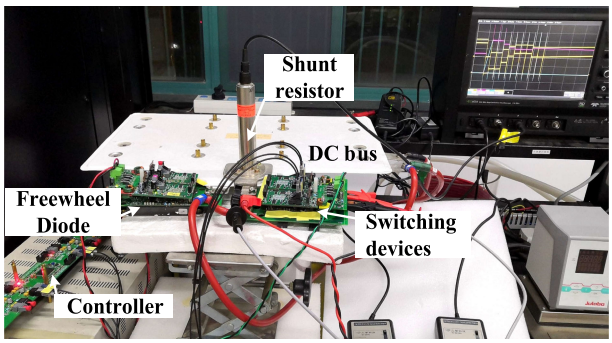


Fig. 12. Photograph of the test platform.

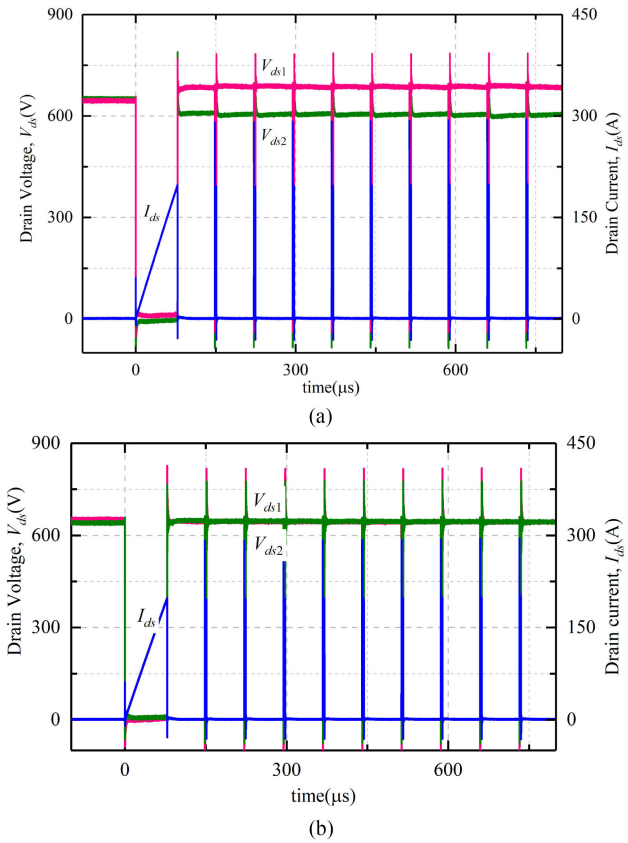


Fig. 13. Multiple pulse test of the two SiC MOSFETs in series. (a) RC snubber. (b) With coupled inductor.

TABLE II
SWITCHING LOSS COMPARISON

	RC snubber (mJ)	Proposed method (mJ)
MOS_1	14.0	10.6
MOS_2	8.8	9.7
Total	22.8	20.3

loss on the snubber resistor. It can be seen that when there is only RC snubber, the switching loss of MOS_1 is 8.8 mJ and the switching loss of MOS_2 is 14 mJ. The difference is quite large, which means under the same thermal dissipation conditions, the junction temperature of MOS_2 will be much higher than MOS_1. The uneven temperature distributions are harmful to the long-time stable running of the converters. When the proposed method is adopted, the switching loss of MOS_1 is 9.7 mJ and the switching loss of MOS_2 is 10.6 mJ. The switching loss difference reduces from 5.2 to 0.9 mJ. The total switching loss is slightly reduced from 22.8 to 20.3 mJ. Above all, the proposed method functions well under the test points and demonstrates significant improvements over the RC snubber conditions.

As demonstrated in Fig. 15, the comparison between the gate source voltage of series-connected devices before and after the proposed method is given. When there is no obvious voltage change across the drain source voltage, the gate source voltage is almost the same before and after the method. When the voltage is fast rising, the gate source voltage is different due to the feedback from the coupled inductor. The device with higher drain voltage has been added a negative voltage, resulting in reduced voltage rising slop, and vice versa. Besides, it is also obvious that the inserted L_g has little influence on the normal driving of the SiC MOSFETs with the proper circuit design.

C. Operation Under Different Load

Another noteworthy performance is the voltage balancing effect under various operating points. A series of tests are conducted in this section and the voltage imbalance before and after the test is given in Fig. 16. Comparing (a) and (b), it can be seen that the unbalanced voltage is significantly reduced under various operating conditions. It should be noticed that the voltage balancing effect increases with load current. This can be

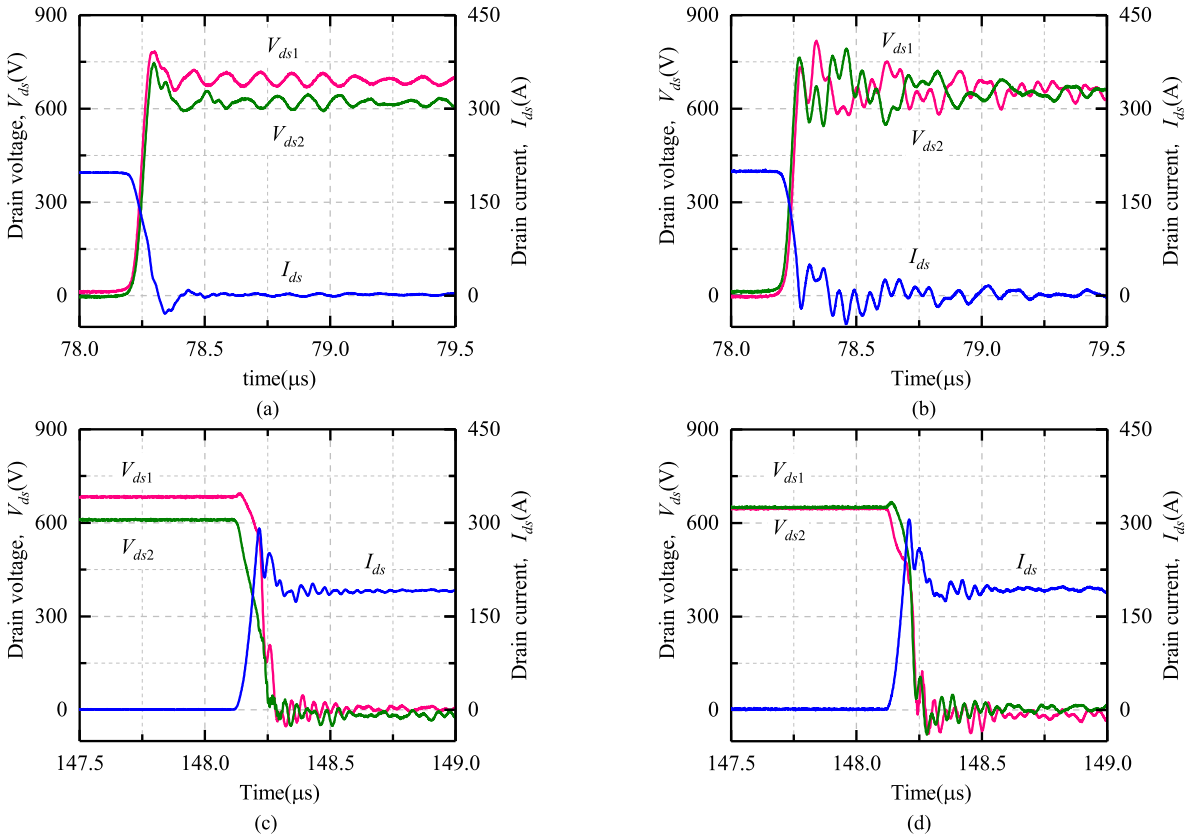


Fig. 14. Zoomed waveform comparison. (a) RC snubber turnOFF. (b) Proposed circuit turnOFF. (c) RC snubber turnON. (d) Proposed circuit turnON.

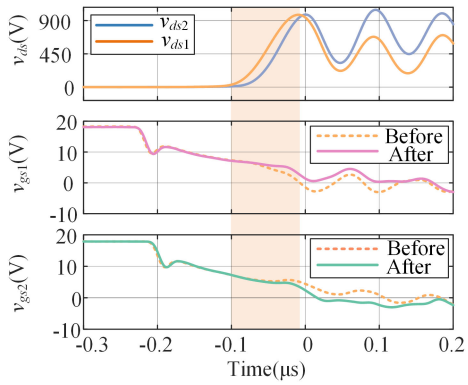


Fig. 15. Measured gate source voltage of devices before and after proposed method at 1300 V/200 A.

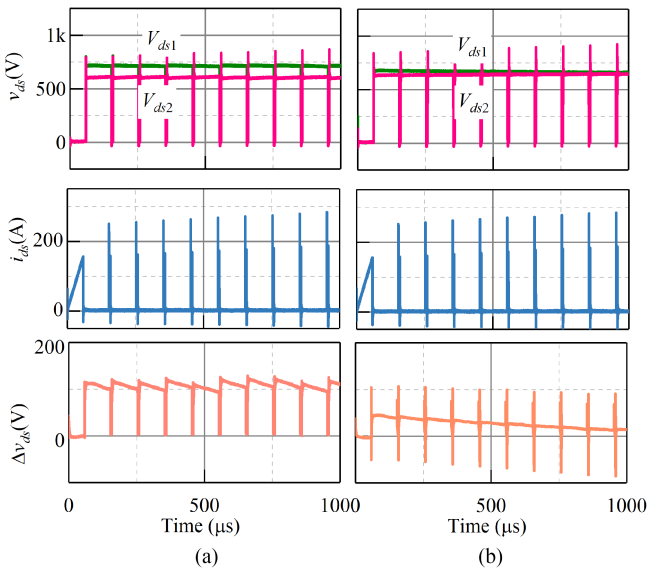


Fig. 16. Performance comparison under different switching currents, from 150 to 190 A. (a) RC snubber. (b) With coupled inductor. Both (a) and (b) share the same axis scale.

explained by (10), when the load current decreases, the miller plateau voltage V_{miller} decreases, as a result, VIRR decreases. Nevertheless, superior voltage balancing can still be ensured. Before the active method, the voltage deviation is around 100 V. After the compensation, as demonstrated in Fig. 16(b), the unbalanced voltage reduces from 30 to 5 V when the load current increases from 150 to 190 A.

C. *Influence of the Snubber Capacitor*

As state before, the selection of the snubber capacitor considers the safe operation of the power devices. Thus, it is typically determined before the selection of the parameters of the coupled inductor. In this part, the performance of under different snubber capacitors is given in Fig. 17. In the experiments, the turnon and turnoff waveform at $C_{snub} = 1$ nF and $C_{snub} = 14.7$ nF is given in order. Both snubbers demonstrate a significantly improved

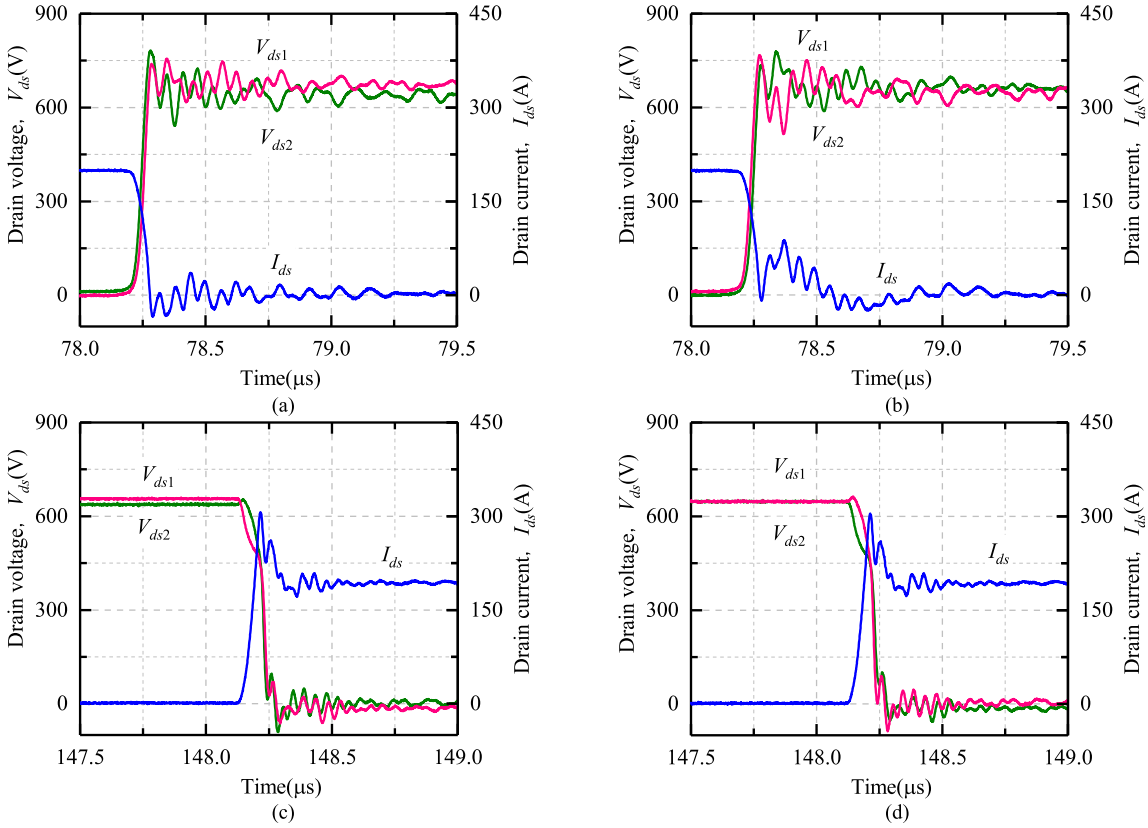


Fig. 17. Switching waveform under different snubber capacitors. (a) Turn OFF with 1 nF snubber capacitor. (b) Turn OFF with 14.7 nF snubber capacitor. (c) Turn ON with 1 nF snubber capacitor. (d) Turn ON with 14.7 nF snubber capacitor.

voltage balancing effect. The experimental results verify that the proposed method can operate under different snubber capacitor conditions.

It is of interest to compare the parallel capacitance requirement with and without the proposed method for achieving the same voltage balancing effect. In purely RC snubber, looking up the curve in Fig. 7, 7 ns gate driver time delay will introduce around 42 V voltage imbalance at 15 nF snubber capacitor condition. In contrast, with the proposed method, a 1-nF capacitor is enough to reduce the unbalanced voltage far below 42 V, as demonstrated in Fig. 17(c). Therefore, the snubber capacitance is significantly reduced by the proposed method, which is beneficial for high-speed switching of the SiC devices.

In conclusion, with the proposed method, the required snubber capacitor to achieve the same voltage sharing effect is greatly reduced compared with purely RC snubber condition. Thus, the switching loss of the snubber and the power devices can be effectively reduced with the proposed method.

D. Simulation Results for Multiple Devices in Series

Due to the limitations of the experimental platform, the verification of the multiple devices in series is conducted in Spice simulation. The simulation parameters are the same as the experimental platform and the device model is from Rohm company, which includes the circuit parasitic parameters in the package. Four devices from two power modules (v_{ds1} and v_{ds2} in one module, v_{ds3} and v_{ds4} in another module) are connected in series to form a single 4800 V/200 A power devices externally. In the simulation, a 5-ns gate driving signal delay is implied orderly for the four devices. The waveform is acquired at 3600 V/200 A condition, as shown in Fig. 18. The simulation results demonstrate that the voltage among the devices can be properly balanced with the proposed method. The unbalanced voltage is reduced from 500 to 50 V with the help of the multiple devices in series circuit.

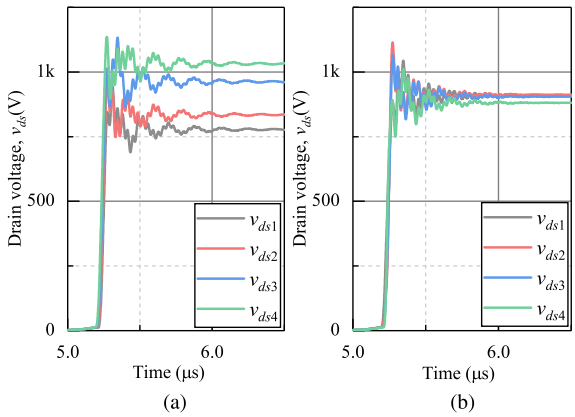


Fig. 18. Simulation verification of four devices in series (a) without and (b) with the proposed method. The total switching voltage is 3600 V/200 A, 5 ns gate driving time delay is orderly inserted for four devices in series.

Further, although the proposed method can be adopted in multiple devices in series. The main challenge is the layout of the coupled inductor among the cascaded devices. The optimized layout of the devices in Section IV cannot be satisfied with the method. The side influence is the increased leakage inductance in the snubber loop, which reduces the potential benefits of the method. In general, the proposed method is better suitable for two devices in series, especially for high power modules to form a single high voltage device. Meanwhile, it can also be applied to multiple devices in series but requires further research in the optimized layout of the circuit.

In conclusion, the voltage balancing effect at different operating points and snubber capacitors are fully tested. The experimental results demonstrate the significantly improved performance of the proposed coupled inductor-based voltage balancing method. The proposed method demonstrates its flexibility and robustness under various conditions. It should be pointed out that the size is increased and the assembly is more complex compared with purely RC snubber. The potential improvement is to integrate the snubber circuit into the gate driver board or into the package to increase the power density.

VI. Conclusion

To achieve fast response speed and voltage imbalance sampling at the same time, a multiport coupled inductor is adopted to dynamically balance the voltage sharing of the series-connected SiC power MOSFETs. The output of the coupled inductor acts as the unbalanced voltage-controlled voltage source and is added to the gate electrode by paralleling with the gate driving resistor. The operation principle, parameter design, and practical layout is given in this article. On the basis of the RC snubber, the proposed method offers another attenuation coefficient to reduce voltage imbalance. As a result, the snubber capacitor can be reduced with the proposed method and maintains the high-speed switching of SiC MOSFETs in the series connection. The experimental results demonstrate a significant voltage balancing effect. From the test, at 1300 V/200 A switching, the unbalanced voltage reduces from 99 V to 2 V. Meanwhile, the switching loss deviation reduces from 5.2 to 0.9 mJ. The proposed method is low cost and can be applied to the series connection of the SiC MOSFETs under various voltage classes and packages, which is hoping to expand the operation voltage of SiC power MOSFETs greatly. Future works on a highly integrated module package will be developed based on the circuit proposed in this article.

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Chengmin Li (Member, IEEE) received the B.S. degree in electrical engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2013, and the Ph.D. degree from Zhejiang University, Hangzhou, China in 2019.

He is currently a Postdoc with Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. From March 2016 to March 2017, he was a Research Intern with the GE Global Research Center, Shanghai, China. His research interests include medium voltage converters and applications of SiC power MOSFETs.

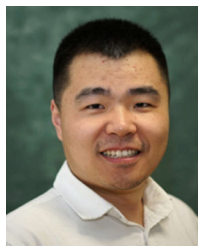
Saizhen Chen (Student Member, IEEE) received the B.S. degree, in 2018, in electrical engineering from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, where she is currently working toward the M.Sc. degree.

Her research interests include the driver design and application of series connected SiC devices.

Haoze Luo (Member, IEEE) received the B.S. and M.S. degrees from the Department of Electrical Engineering, Hefei University of Technology, Hefei, China, in 2008 and 2011, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 2015.

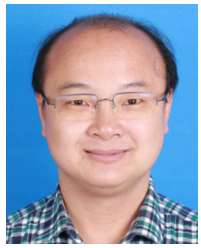
From January to April 2015, he was a Visiting Researcher with Newcastle University, Newcastle upon Tyne, U.K. From October 2015 to May 2018, he was a Postdoc with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. From May 2018 to September 2019, he was a Senior R&D Engineer with Dynex Power Inc., Lincoln, U.K. Since October 2019, he has been with Zhejiang University, as a Research Fellow. His research interests include packaging technology and reliability assessment for high-power modules.

Dr. Luo is currently an Associate Editor for the IET POWER ELECTRONICS and has been a Guest Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.



Chushan Li (Member, IEEE) received the B.E.E. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2008 and 2014, respectively.

He is currently an Assistant Professor with Zhejiang University, Hangzhou, China, and University of Illinois at Urbana-Champaign Institute, Zhejiang, China. From April to September in 2008, he was an Internship Student with the Power Application Design Center in National Semiconductor (Hong Kong) Company Ltd. From December 2010 to October 2011, he was a Visiting Scholar with the Freedom Center in North Carolina State University. From December 2013 to June 2014, he was a Research Assistant with Hong Kong Polytechnic University, Hong Kong. From July 2014 to July 2017, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include high power density power converter design and ac-dc power conversion.



Wuhua Li (Member, IEEE) received the B.Sc. and Ph.D. degrees in power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2004 to 2005, he was a Research Intern, and from 2007 to 2008, a Research Assistant in GE Global Research Center, Shanghai, China. From 2008 to 2010, he was with the College of Electrical Engineering, Zhejiang University, Hangzhou, China, as a Postdoctor, and in 2010 was promoted as an Associate Professor. Since 2013, he has been a Full Professor with Zhejiang University. From 2010 to 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include power devices, converter topologies, and advanced controls for high power energy conversion systems. He has authored or coauthored more than 200 peer-reviewed technical papers and holds more than 30 issued/pending patents.

Dr. Li was the recipient of one National Natural Science Award and four Scientific and Technological Achievement Awards from Zhejiang Provincial Government and the State Educational Ministry of China. Due to his excellent teaching and research contributions, he was also the recipient of the 2012 Delta Young Scholar from Delta Environmental & Educational Foundation, the 2012 Outstanding Young Scholar from National Science Foundation of China (NSFC), the 2013 Chief Youth Scientist of National 973 Program, and the 2014 Young Top-Notch Scholar of National Ten Thousand Talent Program. He serves as the Associated Editor of *Journal of Emerging and Selected Topics in Power Electronics*, IET POWER ELECTRONICS, *CSEE Journal of Power and Energy Systems*, Proceedings of the Chinese Society for Electrical Engineering, Guest Editor of IET RENEWABLE POWER GENERATION for Special Issue "DC and HVDC System Technologies," and Member of the Editorial Board for *Journal of Modern Power System and Clean Energy*. He was appointed as the Most-Cited Chinese Researchers by Elsevier since 2014.

Xiangning He (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer with the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer with Zhejiang University. In 1991, he received a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University, as an Associate Professor. Since 1996, he has been a Full Professor with the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute, the Head of the Department of Applied Electronics, the Vice Dean of the College of Electrical Engineering, and is currently the Director of the National Specialty Laboratory for Power Electronics, Zhejiang University. His research interests include power electronics and their industrial applications.

Dr. He was appointed as IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is also a fellow of the Institution of Engineering and Technology (formerly IEE), U.K.