A Four-Phase Current-Fed Push–Pull DAB Converter for Wide-Voltage-Range Applications

Tat-Thang Le, Sunju Kim, and Sewan Choi, *Fellow, IEEE*

***Abstract*—In this article, a four-phase current-fed push–pull dual active bridge converter is proposed for applications requiring high power and a wide-voltage range. In addition to the conventional advantages of a small filter inductor, a small clamp capacitor, and low current stress in the primary switches due to the effect of four-phase interleaving, the proposed converter has a low total rms current of switches when operating at a wide-voltage range compared with the existing two- and three-phase converters. Also, the proposed converter was shown to be capable of the complete ZVS turn-ON of all switches under a wide duty cycle range of 0.25–0.75 in both power-flow directions when small auxiliary inductors were added. A balanced four-phase transformer structure is proposed not only to cancel the dc-flux offset caused by the dc component of the primary winding current but also to reduce the core volume, footprint, and height of the transformer compared with the separated-core transformer. The experimental results from a 15-kW prototype are provided to validate the proposed concepts. The converter achieved a peak efficiency of 98% and maintained high efficiency when operated at a wide-voltage range.**

***Index Terms*—Bidirectional dc–dc converter, current-fed, dual-active-bridge, four-phase, high power, push–pull, wide-voltage range.**

I. Introduction

RECENTLY, high-power bidirectional dc–dc converters capable of operating at a wide-voltage range have aroused much interest in many applications, such as energy storage systems (ESS), uninterruptible power supplies, and electric vehicles. Among others, the current-fed dual active bridge (CF-DAB) with the active clamp control converters has recently been considered, given their advantages over voltage-fed converters, such as a wider voltage range and lower current ripple, especially in battery applications [1]–[16], [27]–[30]. The active clamp circuit is used not only to increase the zero-voltage switching (ZVS) range but also to clamp the surge voltage at the low-voltage side (LVS) and reduce the circulating power. The clamp voltage can be controlled by adjusting the duty cycle (D_L) of the LVS switches according to the LVS voltage. The performance when operated at a wide-voltage range is analyzed based on the working range of D_L [1].

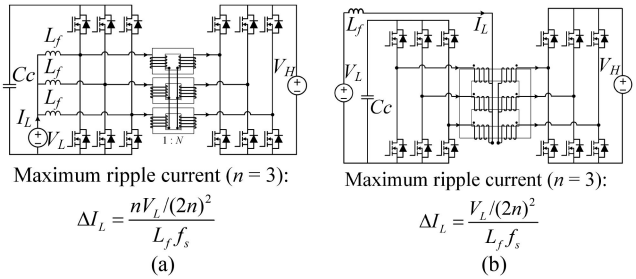

Fig. 1. Three-phase CF-DAB converters. (a) Current-fed half-bridge [7]. (b) Current-fed push–pull [1], [8].

Common CF-DAB converters for wide-voltage applications include two topologies: the half-bridge [2]–[7] and the push–pull [1], [8] types. Challenges associated with the existed converters include a reduced circulating current under a wide D_L range and the complete ZVS condition under a wide D_L range and all power ranges in both power-flow directions. The two-phase CF half-bridge converter, shown to be the simplest type, has been the topic of numerous studies [2]–[5]. However, the optimal operation point is found only at a D_L value of 0.5. When $D_L > 0.5$ and $D_L < 0.5$, greater levels of circulating current arise resulting in low efficiency. Moreover, the ripple of the converter is high when operating under a wide-voltage range. Indeed, one study [2] shows the circulating current of a single-phase half-bridge converter when D_L ranges from 0.5 to 0.7, indicating significantly reduced efficiency at an extreme duty cycle. Another study [6] found that the winding rms current of $D_L = 0.25$ is nearly twice as large as that of $D_L = 0.5$. The three-phase CF half-bridge and push–pull types in Fig. 1 have been studied in relation to a wider D_L range of 0.33–0.66 [7], [1]; however, in lower and higher D_L ranges, the circulating current interval starts to increase, resulting in low efficiency [1].

Another challenge is the ZVS turn-ON operation of all switches of a converter, recognized to be an important characteristic of these types of converters. Although wide-bandgap devices, such as SiC MOSFETs and GaNs, have superior switching performance, the ZVS condition is still highly desired given that the ZVS turn-ON loss is still dominant over the turn-OFF loss [17]. Electromagnetic interference is also reduced compared with hard switching due to the high *dV/dt* and *dI/dt*, and the

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power loss of the gate driver is reduced. Additionally, ZVS turn-ON can eliminate the crosstalk problem between the complementary switches, thereby reducing the probability of the occurrence of the leg shoot-through phenomenon [17]. All of the aforementioned bidirectional current-fed topologies cannot readily achieve complete ZVS turn-ON of all switches under both power-flow directions and when operating with a wide-voltage range.

The high-voltage-side (HVS) switches of the current-fed converter are identical to those of most DAB converters, and soft switching can be achieved under a heavy load by increasing the leakage inductance. However, it is difficult to ensure ZVS under a light load. Additionally, an increase in the leakage inductance reduces the power transfer capability of the converter when operating under a wide-voltage range [1]. At high voltages, high-power applications with long deadtime are required, and the converter can also lose its ZVS turn-ON capabilities under a medium load because the parasitic capacitor of switch C_{oss} is recharged again before the switch is turned ON. This phenomenon is detailed in Section III of this article. The work in [2] shows that the ZVS of secondary-side switches can be achieved in the reverse mode; however, that method can cause the circulating current to increase and can lead to more conduction losses as well.

The ZVS condition of the LVS switches becomes more challenging due to the effect of the dc filter current on the LVS. A three-phase half-bridge converter, as shown in Fig. 1(a), reduces the filter inductance for increasing the ZVS range of LVS switches, with this also increasing the ripple current and increasing the conduction loss of the converter. Hence, there are tradeoffs between the ZVS condition and the reduction of the current ripple. These become more serious at higher voltage applications that require relatively high-power levels. The push–pull topology in Fig. 1(b) has the advantage of a smaller size of the filter inductor, given its use of only one filter inductor compared with the three filter inductors of the half-bridge topology in Fig. 1(a). However, it is more difficult to achieve the ZVS condition of LVS switches, and it is also difficult to design the transformer due to the dc-flux offset in the transformer.

In this article, through a comprehensive analysis of the rms current and the ZVS condition considering the deadtime effect of the existing current-fed converters under operation at a wide-voltage range, a four-phase current-fed push–pull converter with small auxiliary inductors is proposed for high-power, wide-voltage-range applications. The features of the proposed converter are as follows.

1) The duty cycle range can largely vary from 0.25 to 0.75 with a low total rms current.
2) Complete ZVS turn-ON of all switches is achieved under a wide duty cycle range of $0.25<D_L<0.75$ in both power-flow directions by employing auxiliary inductors combined with the proposed V_{Cc} adjustment method.
3) A small filter inductor, a small clamp capacitor, and a low current stress exist in the primary switches due to the effect of four-phase interleaving.

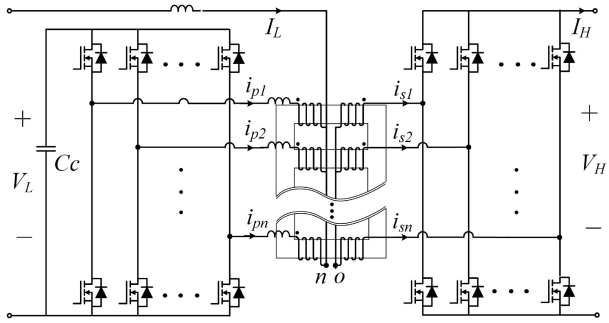


Fig. 2. Proposed general n-phase current-fed push–pull DAB converter.

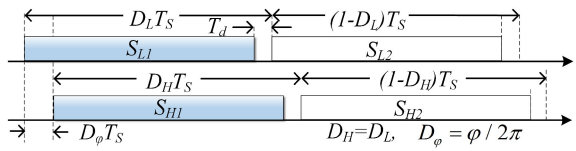


Fig. 3. PWM PPS switching method for the n-phase current-fed push–pull DAB converter: the duty cycle D_L is used to control capacitor voltage V_{Cc}, and φ is the phase shift between the LVS and the HVS to control the transferred power [1].

4) The converter can achieve a peak efficiency of 98% and high efficiency when operating under a wide-voltage range.

This article is an extension of the conference paper presented in [31], and the optimal design of the auxiliary inductor and V_{Cc} control to realize ZVS are also provided. The concept of the combined-core four-phase converter is also proposed with dc-flux cancelation. It is shown that the proposed transformer achieves a lower total volume and smaller footprint compared with the separated-core design. The proposed concept is clearly explained and can also be applied for general four-phase DAB converters. A prototype of a 15-kW bidirectional four-phase push–pull converter was built and tested to validate the proposed concept.

II. Operating Principles of the Proposed Converter

A. Generalization of the Multiphase CF Push–Pull DAB

Fig. 2 shows the generalized circuit of the multiphase CF push–pull DAB converter for high-power, wide-voltage-range applications. The n phases of the converter are connected in parallel, with the phase shift among the phases set to $360°/n$.

Fig. 3 shows the switching patterns of the well-known pulsewidth modulation (PWM) plus phase-shift (PPS) switching method of the converter. The duty cycle D_L is used to control the clamping capacitor voltage V_{Cc} to minimize the circulating power caused by voltage mismatch between V_{Cc} and V_H/N [1], $V_{Cc} = V_L/D_L = V_H/N$, where N is the transformer turn ratio. The range of D_L theoretically varies from 0 to 1, depending on the voltage range of V_L. However, due to the limit on power transfer capability, the range of D_L is also limited, and the detailed analysis of the optimal operation range of D_L will be shown in

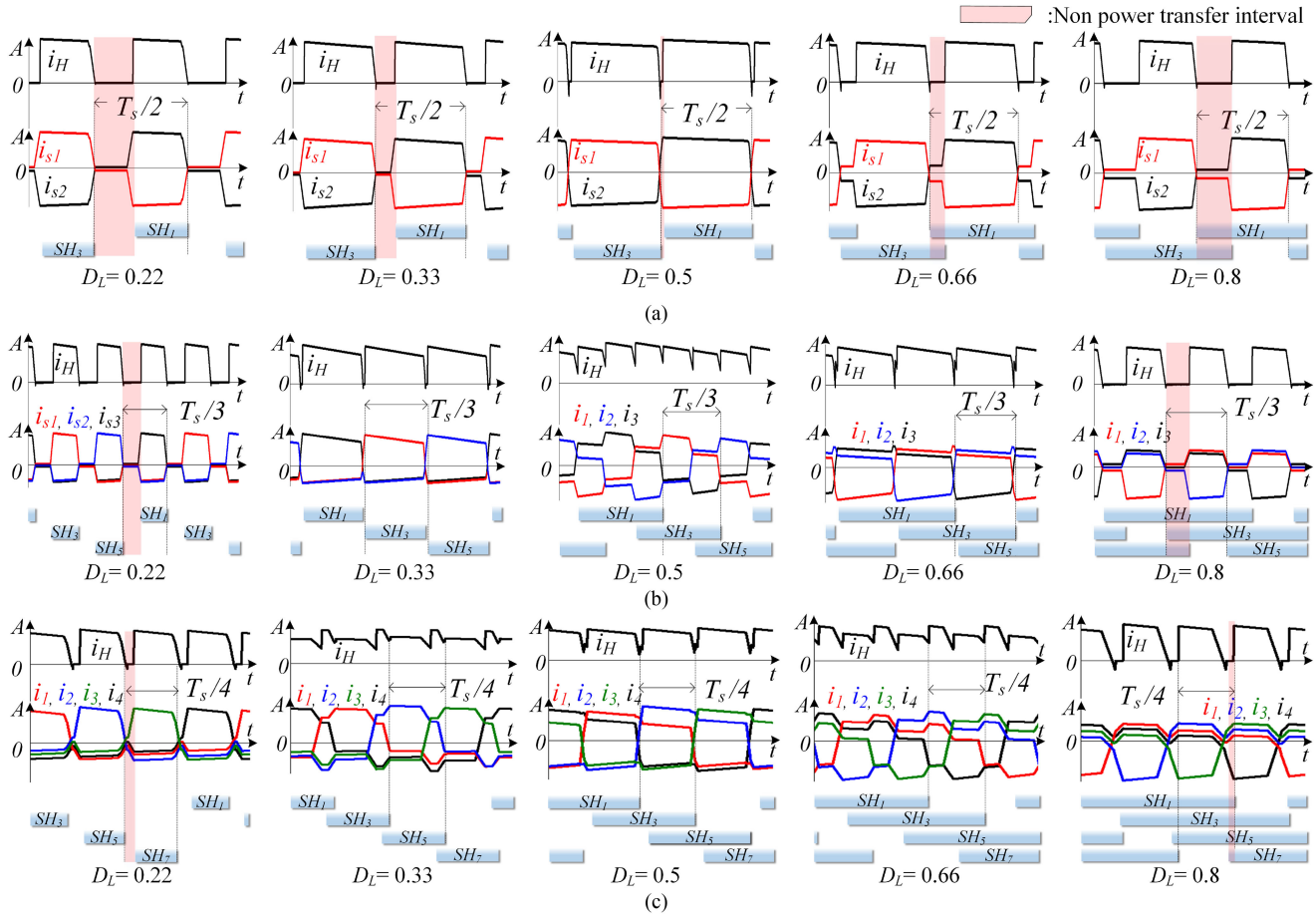


Fig. 4. Key waveforms of the secondary transformer and HVS currents with PPS switching method. (a) Two-phase design. (b) Three-phase design. (c) Four-phase design. The nonpower transfer interval is indicated by as the red shadowed area. The nonpower transfer interval is eliminated when D_L is 0.5 (two phases), when in the range of 0.33–0.66 (three phases), and when in the range of 0.25–0.75 (four phases). As the number of phases is increased, the nonpower transfer interval is reduced, resulting in lower total rms current under wide duty cycle/wide-voltage range.

this section. φ is the phase shift between the LVS and the HVS to control the power. The sign of φ determines the power-flow direction of the converter.

B. Advantages of Increasing the Number of Phases

In addition to the conventional advantages of the reduced current stress on the switches and the lower current ripple, an increase in the number of phases is realized for operation at a wide-voltage range with a lower total rms current and wider ZVS range.

1) Operation Principles Under a Wide Duty Range: Fig. 4(a)–(c) shows the key waveforms of the secondary transformer current and load current of two-phase, three-phase, and four-phase converters, respectively. Assume that V_{Cc} always equals V_H/N by controlling D_L. The nonpower transfer interval is represented as the red shadowed interval where the upper switches or lower switches are turned ON together, and the output current is equal to zero ($I_H = 0$). The calculation of this interval is expressed as the function of duty cycle D_L regardless of the phase shift or transferred power. The nonpower transfer interval is eliminated when D_L is 0.5 (two phases) in the range of 0.33–0.66 (three phases) and in the range of 0.25–0.75 (four phases), as shown in Fig. 5(a). It should be noted that when the number of phases increases, the nonpower transfer interval is reduced, resulting in higher power transfer capability and lower total rms current in a wide duty range.

Fig. 5 shows the power transfer capability of the multiphase converters under a wide-voltage range with the same parameters. When the duty cycle increases from 0.5 to 0.75, the power transfer capability of the two-phase converter reduces 50%, meanwhile that of the three-phase and four-phase converters reduces 43% and 25%, respectively. This analysis confirms the benefit of the four-phase converter on increased power transfer capability due to the reduced nonpower transfer interval in a wide-voltage range. Fig. 6(a) and (b) shows that the total rms current of the switches of these topologies rapidly increases when the circulating current interval starts to increase. Thus, the four-phase converter is a better solution, as it operates under a wide-voltage range. (The duty range can range from 0.25 to 0.75 without a nonpower transfer interval, resulting in lower rms current.)

2) Lower Turn-ON Current Under a Wide Duty Range: Fig. 7 shows the turn-ON current of the three-phase and four-phase converters under a wide D_L range. It should be noted that the turn-ON current of the three-phase converter rapidly increases

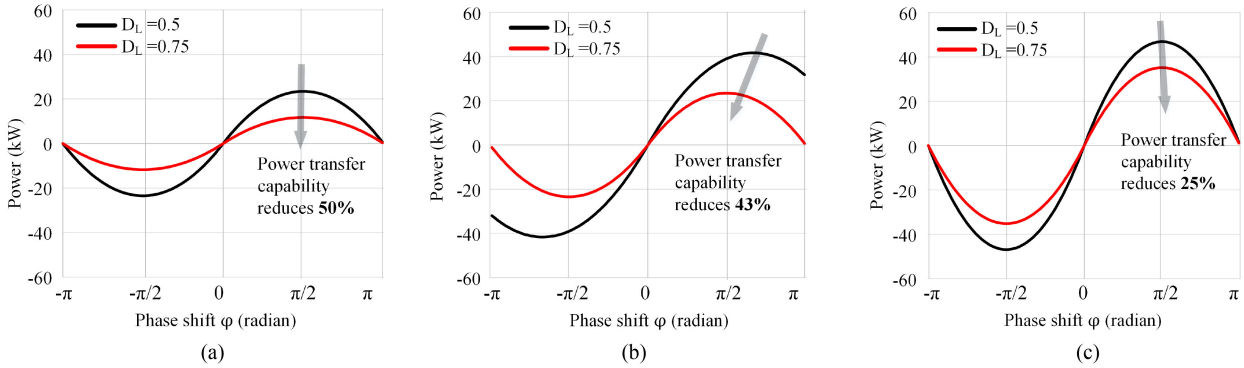


Fig. 5. Power transfer capability of multiphase converter under different duty cycles. (a) Two phases. (b) Three phases. (c) Four phases. The calculation results derive from power equation in Table IV in the Appendix, $f_s = 50$ kHz, leakage inductor $L_k = 30$ μH, transformer turn ratio $N = 1{:}1$, $V_H = 750$ V, $V_L = 357$ V ($D_L = 0.5$), and $V_L = 560$ V ($D_L = 0.75$).

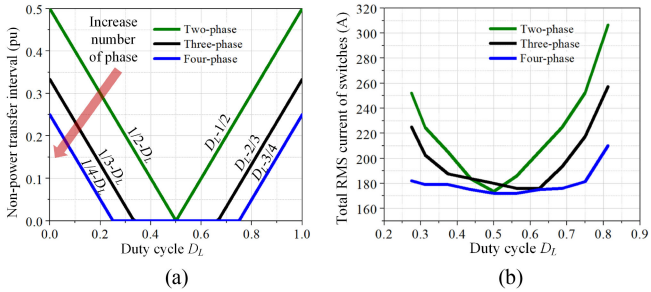


Fig. 6. Effect of increasing number of phases in the multiphase converter on (a) circulating current interval and (b) total rms current of all switches, showing the reduction of the rms current when the number of phases increases under a wide duty cycle range. (The results in (b) derive from the simulation results of converters under the same power level of $P_o = 22$ kW, and D_L is from 0.22–0.81.)

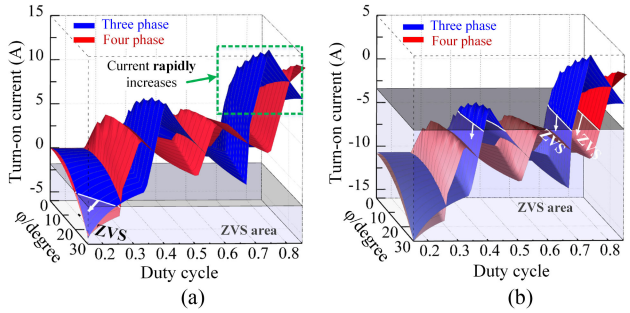


Fig. 7. Effect of increasing number of phases on reducing turn-ON current of the LVS switches under a wide duty range in the multiphase converter. (a) Without $L_{\rm au}$, (b) With additional $L_{\rm au}$ ($D_L = 0.15$–0.85, $f_{\rm sw} = 80$ kHz, and $P = 20$ kW under a forward power).

when $D_L > 0.66$, whereas that of the four-phase converter is $D_L > 0.75$. This leads to the important conclusion that the four-phase converter can easily achieve ZVS turn-ON under a wider duty cycle range compared with the three-phase converter. The ZVS condition is determined considering the deadtime effect. The turn-ON current of the switch should be large enough to completely discharged the parasitic capacitor $C_{\rm oss}$ of switches and remain negative before the switch turns ON. The analysis is detailed in Section III.

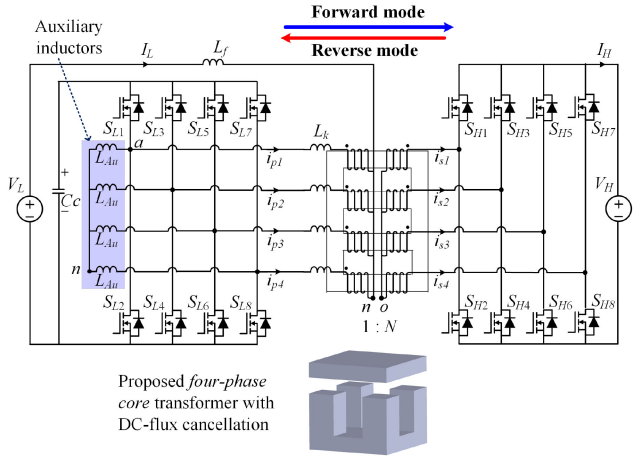


Fig. 8. Proposed four-phase current-fed push–pull DAB with auxiliary inductors.

C. Proposed Four-Phase Push–Pull Converter

Considering the aforementioned advantages of increasing the number of phases of the push–pull converter, Fig. 8 shows the proposed bidirectional four-phase push–pull converter for operation under a wide-voltage range with the possibility of fully achieving ZVS for all switches under both power-flow directions. The phase shift among phases is 90°. The converter operates in the forward mode when a low-voltage source V_L, i.e., a battery, delivers energy to the high-voltage source V_H, while in the reverse mode, the battery is charged by V_H.

The auxiliary inductors $L_{\rm au}$ are employed on the primary side to ensure the ZVS condition of the primary-side switches S_{L1}–S_{L8}, as shown in Fig. 7(b). When $L_{\rm au}$ is reduced, the ZVS turn-ON current of the primary switches increases negatively. It should also be noted that the ZVS condition of the primary switches mainly depends on the ac current ripple through $L_{\rm au}$ and does not depend on the filter current ripple I_L. Therefore, the proposed converter overcomes the drawback of the current-fed half-bridge converter, as described in earlier work [7], which involves a tradeoff between the ZVS condition and reducing the ripple current. The complete ZVS turn-ON methods for this

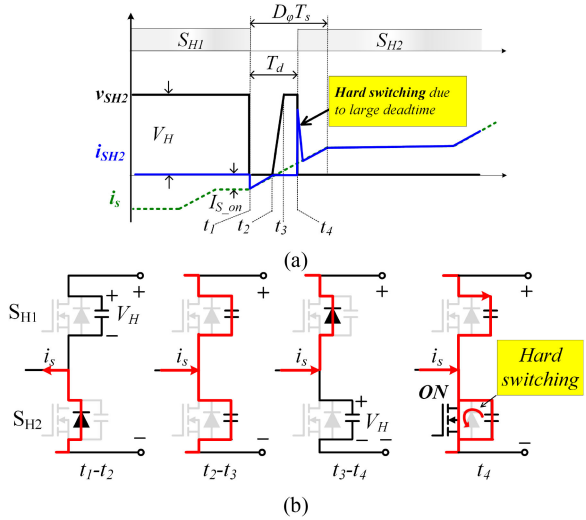


Fig. 9. Switching characteristic of the switches with the deadtime effect. (a) Waveform. (b) Mode-by-mode operation. At $[t_1]$, the lower $C_{\rm oss}$ is completely discharged with the initial turn-ON current of $I_{S\_{\rm on}}$, $[t_1$–$t_2]$: the leakage current i_s starts to increase from a negative value of $i_s = I_{s\_{\rm on}}$ until $i_s = 0$. $[t_2$–$t_3]$: the lower $C_{\rm oss}$ is charged with positive i_s current, and the voltage is increased to V_H. The upper $C_{\rm oss}$ is discharged and its *voltage* is reduced to zero. $[t_3$–$t_4]$: The lower $C_{\rm oss}$ is fully charged. $[t_4]$: at t_4, S_{H2} is turned ON, the lower $C_{\rm oss}$ becomes a short circuit with a high dV/dt, and the switch operates under the hard-switching condition, resulting in capacitive turn-ON loss and noise. At this time, the upper switch can experience the crosstalk problem. This analysis is also true for both the primary and secondary switches.

converter are detailed in Section III. The proposed converter must use one core transformer with a star connection to cancel the dc-flux offset caused by the LVS dc current I_L. The proposed four-phase core transformer is described in detail in Section IV.

III. Proposed Complete ZVS Turn-ON Methods of the Converter

In general, the ZVS turn-ON of the switch is achieved when the current through the leakage inductor should be large enough to discharge the parasitic capacitors of the upper and lower switches during the deadtime interval, as expressed in (1), where $I_{S,\rm on}$ is the initial turn-ON current of the switches. However, when deadtime becomes larger, the capacitor could be recharged again. Fig. 9(a) outlines the effect of the deadtime on the ZVS condition. It is important to note that despite having a negative initial turn-ON current and zero voltage of the switch at time t_1, the switch can lose the ZVS condition due to the recharge of the parasitic capacitor $C_{\rm oss}$ during the deadtime. As shown in Fig. 9(a), in order to achieve ZVS considering the effect of deadtime, the converter should meet the conditions in (2). The complete ZVS turn-ON condition should satisfy both (1) and (2), where $C_{\rm oss}$ of the switch is completely discharged, while i_s still maintains at a negative value before the switches turn ON

$$I_{S,\rm on} \geq 2C_{\rm oss}\frac{V_H}{T_d} \tag{1}$$

$$\begin{cases} \Delta T \geq T_d & \text{if}(D_\varphi T_s \geq T_d) \\ \Delta T \geq D_\varphi T_s & \text{if}(D_\varphi T_s < T_d). \end{cases} \tag{2}$$

The time interval ΔT for the switch current, as it increases from its initial value of $I_{S,\rm on}$ to zero, is expressed as

$$\Delta T = t_2 - t_1 = -\frac{L_k}{V_{Cc}/4 + (V_H/N)/2} I_{S,\rm on}. \tag{3}$$

From (2) and (3), the ZVS condition under the effect of the deadtime becomes

$$I_{S,\rm on} \leq I_{\rm ZVS\_surf} \tag{4}$$

where the ZVS surface $I_{\rm ZVS\_surf}$ is determined as follows:

$$I_{\rm ZVS\_surf} = \begin{cases} -\frac{V_{Cc}/4+(V_H/N)/2}{L_k} T_d & \text{if}(D_\varphi T_s \geq T_d) \\ -\frac{V_{Cc}/4+(V_H/N)/2}{L_k} D_\varphi T_s & \text{if}(D_\varphi T_s < T_d). \end{cases} \tag{5}$$

From (1) and (4), the final ZVS condition is obtained as

$$I_{S,\rm on} \leq I_{\rm ZVS\_surf} \leq -2C_{\rm oss}\frac{V_H}{T_d}. \tag{6}$$

In order to satisfy the condition in (6), there are three well-known approaches: minimizing the deadtime T_d (T_d control), increasing the switching frequency (frequency variation), and increasing the leakage induction.

Minimize T_d: According to the load change, T_d can be reduced to meet the condition in (6). However, if T_d is small, $C_{\rm oss}$ of all switches (on both sides) cannot be fully discharged during the turn-OFF commutation under a light-load condition. Moreover, the control of T_d according to the load change becomes a challenge in the stability control. In practice, a fixed deadtime is often used. The value of T_d is minimized from the parameter of the switches, including $C_{\rm oss}$ and voltage rating of the switches. Discussions pertaining to the selection of an appropriate deadtime can be found in [19] and [20].

Frequency control: Increase of the frequency under a light load can be a viable solution for extending the soft-switching region to the light-load condition. This strategy can be found in many studies [19], [21], [22]. Similar to reducing T_d, changing the frequency directly changes the output power. Functions related to the phase shift, frequency, and power are usually highly nonlinear, which complicates the stable control.

Another approach is to increase the leakage inductance to increase ΔT. This method faces the problem of the limitation of the power transfer capability at extremely high duty cycles [1], [16]. It should be noted that in high-power and wide-voltage-range applications, the design should not allow the L_k value to be too high. The maximum L_k value can be determined by the desired power and voltage range.

Regardless of the above approaches, the converter can lose its ZVS capability under a light-load condition [21]. Table I presents a summary of the ZVS turn-ON condition of all switches. Here, in general, ZVS of the HVS and LVS switches is difficult to achieve in the reverse and forward mode, respectively. Therefore, the ZVS condition of the HVS switches, S_{H1}–S_{H8}, is analyzed in the reverse mode, while the ZVS condition of the LVS switches, S_{L1}–S_{L8}, is analyzed in the forward mode.

The following section describes the overall solution to realize the ZVS condition of all switches in both power-flow directions

TABLE I
SUMMARY OF THE ZVS CONDITION OF ALL SWITCHES WITH AND WITHOUT THE PROPOSED METHOD

		Forward mode		Reverse mode	
		LVS switches	HVS switches	LVS switches	HVS switches
without L_{au}	without V_{Cc} adjusted	X	O	O	Δ
	with V_{Cc} adjusted	X	O	X	O
with L_{au}	without V_{Cc} adjusted	O	O	O	Δ
	with V_{Cc} adjusted	O	O	O	O

O: Guarantee the ZVS condition.
X: Hard switching.
Δ: Losing ZVS due to the large deadtime effect or too small ZVS energy.

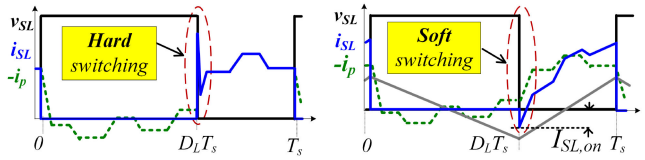


Fig. 10. Effect of adding auxiliary inductor on the ZVS characteristics of the LVS switches. (a) Without $L_{\rm au}$. (b) With $L_{\rm au}$ (*proposed*).

with the additional auxiliary inductance $L_{\rm au}$ and with proper control of V_{Cc}.

A. Forward Mode

Fig. 10(a) shows the hard-switching characteristic of the primary switches in the case without $L_{\rm au}$. Fig. 10(b) shows that the primary switches utilize the current through auxiliary inductor $L_{\rm au}$ for completely achieving ZVS. The relationship among the switch current i_{SL}, the primary transformer current $i_{Lk,p}$, and the auxiliary inductor current $i_{L\rm au}$ during the turn-ON interval is expressed as follows:

$$i_{SL}(t) = -i_{Lk,p}(t) + i_{L\rm au}(t). \tag{7}$$

The initial turn-ON current $I_{SL,\rm on}$ of the LVS switches is determined at $t = D_LT_s$ and is expressed as follows:

$$I_{SL,\rm on} = i_{SL}(D_LT_s) = i_{L\rm au}(D_LT_s) - i_p(D_LT_s). \tag{8}$$

From (6) and (8), the ZVS condition of the primary switches under the effect of the deadtime becomes

$$I_{SL,\rm on} = i_{L\rm au}(D_LT_s) - i_p(D_LT_s) \le I_{\rm ZVS,surf} \le -2C_{\rm oss}\frac{V_H}{T_d}. \tag{9}$$

The calculation of $i_p(D_LT_s)$ can be done by analyzing the voltage across through the leakage inductance. The value of $i_{L\rm au}(D_LT_s)$ depending on the ripple through $L_{\rm au}$ is expressed as follows:

$$i_{L\rm au}(D_LT_s) = -\frac{\Delta I_{L\rm au}}{2}. \tag{10}$$

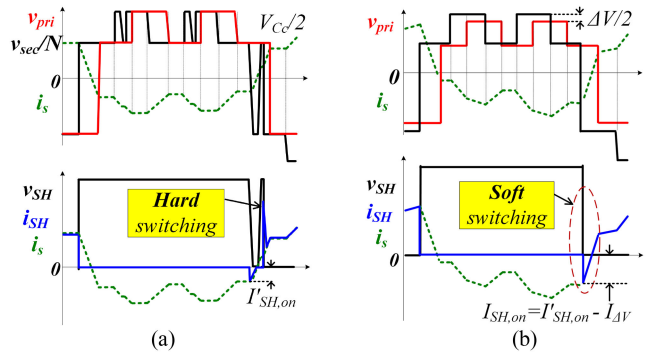


Fig. 11. Effect of adjusting the *Cc* voltage on the ZVS characteristics of the HVS switches. (a) $\Delta V = 0$ (conventional) hard switching due to the deadtime effect. (b) $\Delta V > 0$ (*proposed*), V_{Cc} is reduced and the slope of the secondary current increases, allowing ZVS turn-ON to be achieved.

The value of $L_{\rm au}$ can be optimally designed such that it satisfies (9) throughout the load and wide duty ranges. This is detailed in Section IV. The complete ZVS turn-ON condition of LVS switches is achieved in a wide duty range and all power ranges, as shown in Fig. 7(b).

B. Reverse Mode

Fig. 11(a) shows the hard-switching characteristic of the HVS switches under the conventional control method. Fig. 11(b) shows the proposed method of reducing V_{Cc} with the amount of ΔV in (11). As V_{Cc} is reduced, the slope of the secondary current increases, resulting in the realization of ZVS. Hence, the converter can achieve ZVS throughout the load range. The clamp voltage V_{Cc} is controlled by the duty cycle D_L.

The contribution of the auxiliary inductor $L_{\rm au}$ always guarantees the ZVS condition of the LVS switches. Therefore, the addition of $L_{\rm au}$ on the primary side combined with the V_{Cc} control method is a good solution for achieving ZVS of both the LVS and HVS switches in the proposed converter.

$$V_{Cc} = \frac{V_H}{N} - \Delta V. \tag{11}$$

A higher ΔV value results in higher rms current and higher turn-OFF current outcomes. Therefore, ΔV should be optimally determined for both achieving ZVS and minimizing the rms current.

By reducing V_{Cc} with the amount of ΔV, the initial turn-ON current can be reduced with the amount of $I_{\Delta V}$, which is determined by

$$I_{\Delta V} = \begin{cases} \frac{1}{8}\frac{\Delta V}{L_k}(D+\frac{1}{2})T_s & \text{if}(0.25 < D < 0.5) \\ \frac{1}{8}\frac{\Delta V}{L_k}(\frac{3}{2}-D)T_s & \text{if}(0.5 < D < 0.75). \end{cases} \tag{12}$$

The ZVS condition from (6) becomes

$$I_{SH,\rm on} = I'_{SH,\rm on} - I_{\Delta V} \le I_{\rm ZVS\_surf} \le -2C_{\rm oss}\frac{V_H}{T_d} \tag{13}$$

$$\Delta V \ge \begin{cases} -\frac{8L_k}{(D+\frac{1}{2})T_s}(I_{\rm ZVS\_surf} - I'_{SH,\rm on}) & \text{if}(0.25 < D < 0.5) \\ -\frac{8L_k}{(\frac{3}{2}-D)T_s}(I_{\rm ZVS\_surf} - I'_{SH,\rm on}) & \text{if}(0.5 < D < 0.75) \end{cases}$$

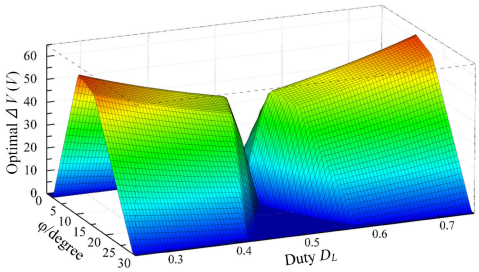


Fig. 12. Optimal ΔV for achieving the ZVS condition of HVS switches under the wide duty cycle range and load condition in the reverse mode.

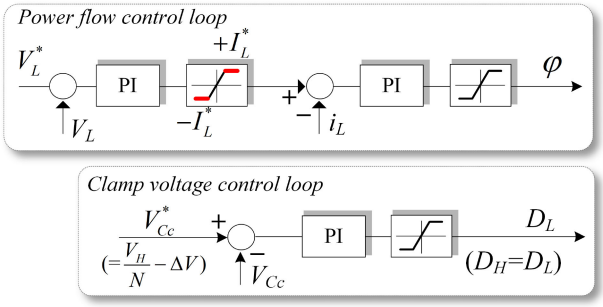


Fig. 13. Control block diagram of the converter.

$$\Delta V = 0 \text{if}((I_{\text{ZVS\_surf}} - I'_{SH,\text{on}}) \geq 0) \tag{14}$$

where $I'_{SH,\text{on}}$ is the initial turn-ON current of the HVS switches in the reverse mode without V_{Cc} control ($\Delta V = 0$). The calculation formula of $I'_{SH,\text{on}}$ was devised after analyzing the voltage across the leakage inductance. From (12) and (13), the final optimal value of ΔV is obtained by (14).

Fig. 12 shows the optimal ΔV for the complete ZVS turn-ON condition of the HVS switches in a wide duty range and all power ranges. For a simple control technique, in the reverse mode, ΔV is always controlled to a constant value of 60 V. The complete control block diagram is shown in Fig. 13.

IV. Proposed a Compact Four-Phase Core Transformer and Design of the Converter

A. Proposed a Compact Four-Phase Transformer

In this section, the proposed four-phase transformer with dc-flux cancelation is realized in several steps. It starts with four separate transformers connected in a *Y* configuration, as shown in Step 1 in Fig. 14. Fig. 15 shows the equivalent circuit with the primary winding current and magnetizing flux waveform of one of the separate cores. The primary winding current i_p includes both dc and ac components, and its dc current component is expressed as

$$I_{\text{DC}} = I_L/4. \tag{15}$$

The flux generated by the primary winding current also includes ac- and dc-flux components, as shown in Fig. 15(a)

$$\phi = \phi_{\text{ac}} + \phi_{\text{dc}}. \tag{16}$$

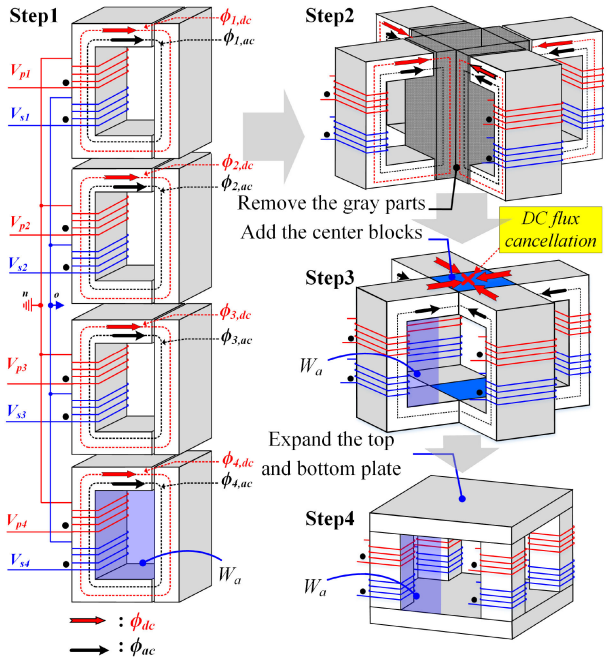


Fig. 14. Steps for developing the four-phase core transformer from four separate transformers.

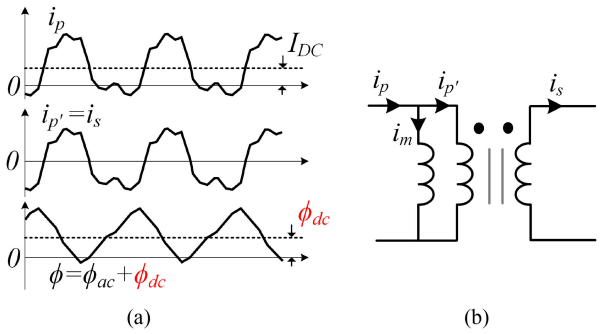


Fig. 15. Primary winding current and magnetizing flux waveform of one of the separated cores. (a) Current and flux waveform. (b) Equivalent circuit.

Only the ac-flux component contributes to the power transfer from the primary to the secondary sides. The dc flux increases the peak flux, B_{peak}, resulting in increased core size, core loss, and possible saturation. The ac fluxes are determined by the phase voltages. Fig. 16 shows the waveforms of four-phase (winding) voltages, with a 90° phase shift among the phases. Because the sum of the four instantaneous phase voltages is zero, the sum of the instantaneous ac-flux components is also zero. Fig. 17(a) shows that the dc flux exists in each flux path in Step 1 in Fig. 14. Note that a large airgap should be used to prevent any saturation that may arise due to the dc flux. Step 2 shows a simple rearrangement of the four separate transformers used to form a four-phase transformer. In Step 3, the gray part of Step 2 is removed, and the blue parts are added at the top and bottom, respectively, after which the dc fluxes from each phase are canceled. The four legs, as shown in gray, can be removed because the sum of the four ac fluxes is zero. It is noted that the

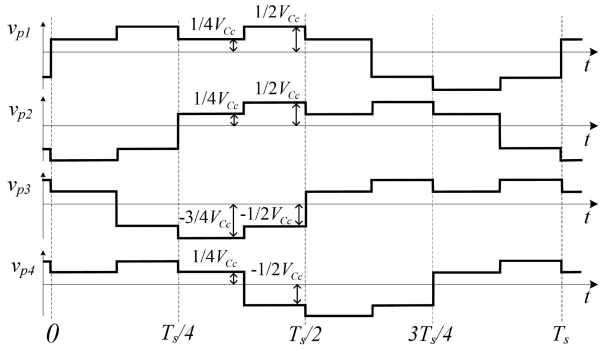


Fig. 16. Phase voltage waveforms.

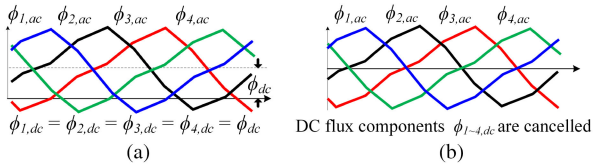


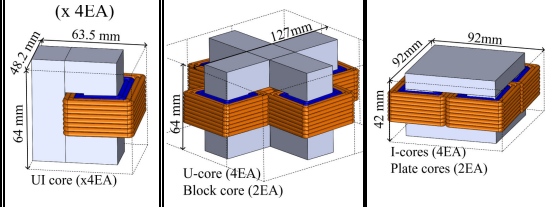
Fig. 17. Flux waveform of the transformer. (a) DC flux exists in separated core. (b) DC-flux cancelation in the proposed combined-core structure.

airgap is also eliminated due to the dc-flux cancelation in Step 3. Therefore, the core volume of the structure in Step 3 is smaller than that in Step 2. However, the winding area of the structure in Step 3, as shown here in blue, is limited. Therefore, the structure in Step 4 is proposed; it expands the top and bottom plates and relocates the phase legs with square-shaped I-cores to the corner. It should be noted that the thickness of the top and bottom plates of structure in Step 4 can be reduced by half, resulting in a 34% decrease in the core height compared with Step 3. Moreover, due to the increased winding space, the footprint of the structure in Step 4 is reduced by half. This ends up with a dramatic reduction of the total core volume of 65%.

A detailed comparison of the separated-core (Step 1) structure and two types of combined cores (Step 3 and 4) under identical conditions (electrical rating, cross-sectional area A_c, and winding area W_a) is given in Table II. The structure in Step 3 shows a 34% reduction in the core volume compared with the structure in Step 1 due to the removal of the I-cores stemming from the dc-flux cancelation. However, the total volume is increased by 24% due to the limited winding area. As an improvement over the structure in Step 3, the proposed structure in Step 4 shows a smaller footprint by 31% and smaller core volume by 44%, resulting in a total volume reduction of more than 54% compared with the separate transformers of Step 1.

Fig. 18 shows the simulation comparison of the peak flux density and winding current in different types of transformers using 3-D finite element method (FEM) simulations. In the separated core, in order to keep the peak flux under 0.2 T, a large airgap of 6 mm must be added to reduce the peak flux due to the existing dc-flux component. However, a larger airgap lowers the magnetizing inductance, resulting in a high ripple current of 30 A, thus leading to high conduction loss. A larger airgap also causes increased flux ringing, resulting in a higher

TABLE II
COMPARISON OF DIMENSIONS OF FOUR-PHASE TRANSFORMERS ($F_s = 80$ kHz, $B_{MAX} = 0.285$ T, $N_p = 15$; $N_s = 14$, $I_p = 14$ A, $D_{MAX} = 0.75$, $A_c = 484$ mm^2, $W_a = 336$ mm^2, $J = 5$ A/mm^2, AND CROSS-SECTIONAL AREA OF THE WIRE: 6.37 mm^2.)

	Separated core in step 1 (x 4EA)	Structure in step 3	Proposed structure in step 4
			
Height	64mm	64mm	42mm
Footprint	12242 mm^2	16129mm^2	8464 mm^2
Core volume	0.292L	0.192L	0.164L
Total Volume	0.78 L	1.03 L	0.36 L

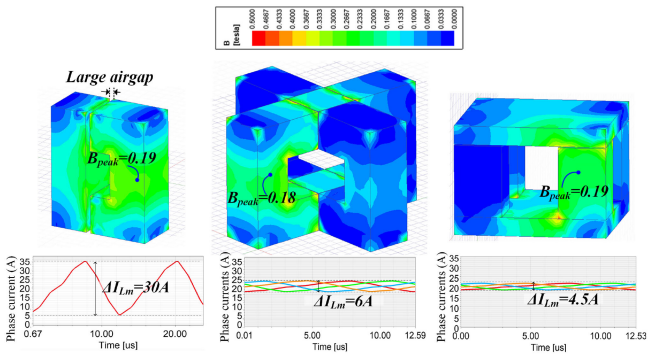


Fig. 18. Simulation of the maximum flux density and winding current in different types of transformers. (a) Separated core. (b) Structure in Step 3. (c) Structure in Step 4. Simulations are carried out using 3-D FEM simulation software with ac voltage (as shown in Fig. 16) and dc current excitation.

eddy-current winding loss. Fig. 18(b) and (c) shows that even with a high dc current of 20 A flow, $B_{\rm peak}$ remains at less than 0.2 T; the magnetizing current is also small at around 5 A. Hence, an important conclusion is that the final proposed combined-core transformer can cancel the dc flux caused by the dc component of the primary winding current while also reducing the core volume, footprint, and height of the transformer compared with the separated-core transformer.

B. Filter Inductor Design

The filter inductance of the proposed converter is calculated based on the maximum requirement of LVS current ripple ΔI_L of 3.7 A. From the current ripple formula of a push–pull converter with $n = 4$, the value of L_f is calculated to be 63 μF. Considering a reasonable margin, $L_f = 90$ μF was used.

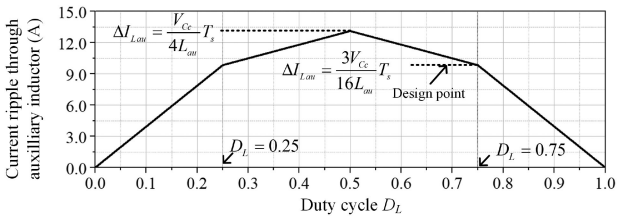


Fig. 19. Current ripple through the auxiliary inductor to realize ZVS current of the LVS switches.

C. Clamp Capacitor Design

The maximum voltage ripple of the clamp capacitor Cc under a wide duty cycle range can be obtained as follows:

$$\Delta V_{Cc} = \frac{1}{4}\frac{1}{C_c}\left(\frac{V_{Cc}}{L_k} D_\varphi T_s + \frac{P_o}{V_{Cc}} + \frac{1}{4}\frac{V_{Cc}}{L_{\mathrm{au}}} T_s\right) D_\varphi T_s \quad (17)$$

where the output power P_o is principally determined as a function of the phase-shift duty D_φ

$$P_o = \frac{V_H V_{Cc}}{L_k} D_\varphi T_s (1 - 2D_\varphi). \quad (18)$$

The capacitance of the proposed converter is calculated based on the requirement of the voltage ripple ΔV_{Cc} of 1 V; hence, $Cc = 15\ \mu$F. Considering a reasonable margin, $Cc = 30\ \mu$F was used.

D. Auxiliary Inductor Design

The ripple current through L_{au} determines the ZVS condition of the primary switches in the reverse mode. Fig. 19 shows the ripple current through L_{au} under a wide duty cycle. Here, the ripple changes slightly in the duty range of 0.25–0.75 and is dramatically reduced when the duty range exceeds 0.75 and is less than 0.25, complicating the ZVS condition in these ranges. The minimum current ripple of the converter in the duty cycle range of 0.25 and 0.75 is determined from the following equation:

$$\Delta I_{L\,\mathrm{au}} = \frac{3V_{Cc}}{16L_{\mathrm{au}}} T_s. \quad (19)$$

From (10), the required ripple to achieve ZVS is expressed as

$$\Delta I_{L\,\mathrm{au\_min}} \geq \left|2(I_{\mathrm{ZVS,surf}} + i_p(D_L T_s))\right|. \quad (20)$$

By substituting (19) into (20), the value of L_{au} for the ZVS condition can be expressed as

$$L_{\mathrm{au}} \leq \frac{3}{16} \frac{V_{Cc}}{\left|2(I_{\mathrm{ZVS,surf}} + i_p(D_L T_s))\right|} T_s. \quad (21)$$

The value of $I_{\mathrm{ZVS,surf}}$ is calculated by (5). Finally, the maximum of L_{au} is calculated to be 140 μF. Considering a reasonable margin, $L_{\mathrm{au}} = 110\ \mu$F was used.

The final designed parameters of the converter are given in Table III. The leakage inductance and turn-ratio values of the transformer are optimally designed depending on the power transfer capability and reduction of the rms current, as presented in [1] and [16].

TABLE III
EXPERIMENTAL SPECIFICATIONS OF THE PROPOSED FOUR-PHASE PUSH–PULL CONVERTER

Items	Value and Rating		Selected devices
HVS voltage	750V		-
LVS voltage	200V-580V (D_L=0.25~0.75)		-
Maximum Power	15kW		-
Maximum current	37.5A		-
LVS Current ripple	10% of I_{max}		-
Switching frequency	80kHz		-
Switches (S_{L1}-S_{L8}, S_{H1}-S_{H8})	V_{pk} I_{rms}	800 V 15 A	FF23MR12W1M (SiC MOSFET, T_d= 300 *ns*)
Clamp capacitor C_C	Value V_{pk}	30μF 800 V	B32678G8156K00 0*B (2ea)
Transformer turn ratio	N=N_s/N_p	15/14	I cores (4ea) Plate cores (2ea) (PM7)
Leakage inductor L_k	Value	17μH	
Magnetizing inductor L_m	Value	250μH	
Filter inductor	Value	90μH	CH610125 (1ea)
Auxiliary inductor	Value	110μF	CM467025 (4ea)

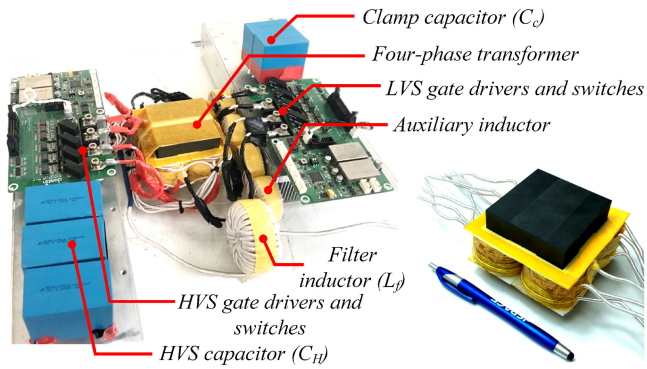


Fig. 20. Photograph of a 15-kW four-phase push–pull converter prototype.

V. EXPERIMENTAL RESULTS

Fig. 20 shows a photograph of an implemented 15-kW prototype of the bidirectional four-phase push–pull converter. Table III presents the main specifications, the design parameters, and selected prototype devices.

Figs. 21 and 22 show the experimental waveforms of the phases current under a wide-voltage range ($0.25 < D_L < 0.75$) in the forward and reverse modes, respectively. Here, the converter operates under the wide duty cycle range of $0.25 < D_L < 0.75$ without nonpower transfer interval, resulting in high efficiency compared with the three-phase converter in earlier work [26]. The experimental results are in good agreement with the analysis and simulation results, as shown in Fig. 2.

According to the experimental results in Fig. 23(a), showing hard switching in the primary switches at 3.9 kW without L_{au}, the capacitor could not fully discharge due to the small initial turn-ON current of -2.5 A. Fig. 23(b) shows that the primary switches utilize the current ripple through auxiliary inductor L_{au},

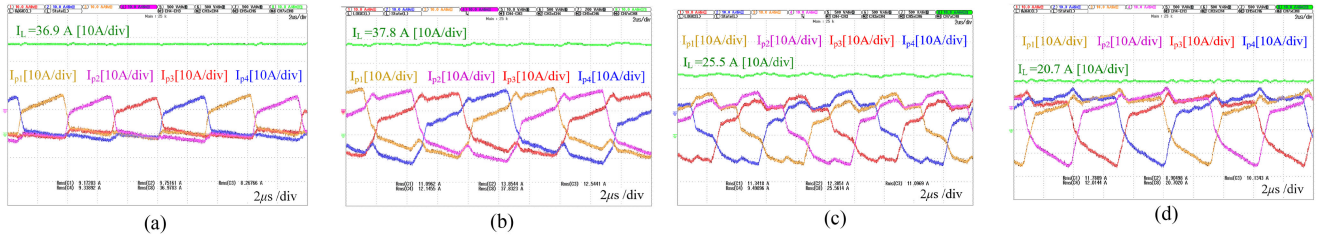


Fig. 21. Experimental waveform of the filter inductor and primary current in the *forward mode*. (a) $V_L = 200$ V, $D_L = 0.25$, and $P = 7.4$ kW. (b) $V_L = 400$ V, $D_L = 0.49$, and $P = 15$ kW. (c) $V_L = 520$ V, $D_L = 0.65$, and $P = 13.3$ kW. (d) $V_L = 580$ V, $D_L = 0.74$, and $P = 12$ kW.

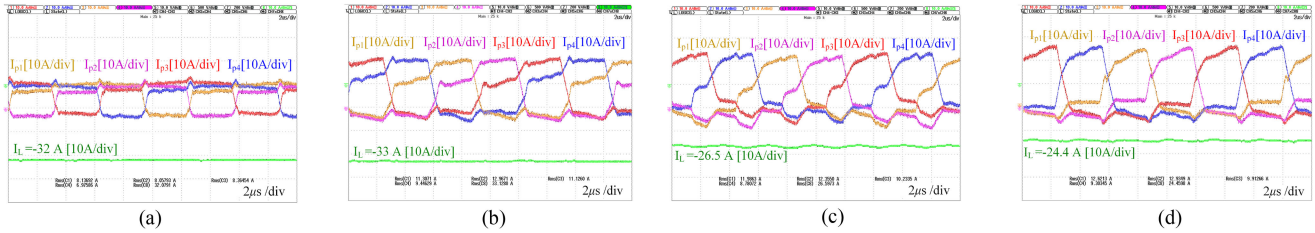


Fig. 22. Experimental waveform of the filter inductor and primary current in the *reverse mode*. (a) $V_L = 200$ V, $D_L = 0.27$, and $P = 6.4$ kW. (b) $V_L = 400$ V, $D_L = 0.53$, and $P = 13.2$ kW. (c) $V_L = 500$ V, $D_L = 0.66$, and $P = 13.25$ kW. (d) $V_L = 550$ V, $D_L = 0.733$, and $P = 13.42$ kW.

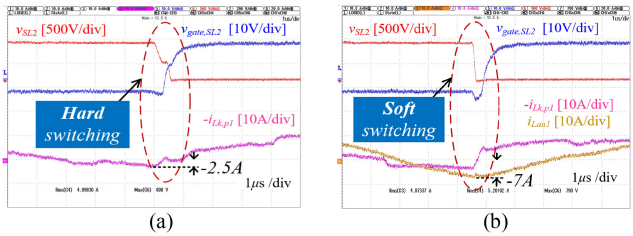


Fig. 23. Experimental waveform showing the achievement of ZVS of the primary switches in the forward mode by means of auxiliary inductance ($D_L = 0.62$, $V_L = 500$ V, and $P_o = 3.9$ kW). (a) Without auxiliary inductors. (b) With auxiliary inductors.

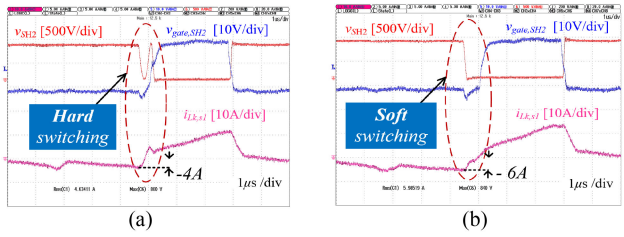


Fig. 24. Experimental waveform showing the achievement of ZVS of the secondary switches in the reverse mode by means of the proposed V_{Cc} control method ($D_L = 0.73$, $V_L = 550$ V, and $P_o = 5.2$ kW). (a) With $\Delta V = 0$ (conventional). (b) With $\Delta V = 60$ V (*proposed*).

with the initial turn-ON current of the switches reduced to less than -7 A, resulting in a successful ZVS turn-ON outcome.

The experimental results in Fig. 24(a) show the hard-switching characteristic of the secondary switches at a middle power level of 5.2 kW with the conventional control method [26]. Here, despite that, the capacitor is discharged with the initial turn-ON current of -4 A, the capacitor is charged again during the deadtime interval before the switch turn-ON, as in the previous analysis. The experimental results in Fig. 24(b) show that the initial turn-ON current is reduced to -6 A when reducing V_{Cc} with ΔV set to 50 V.

Figs. 25 –27 show the complete ZVS turn-ON of the secondary switches in the reverse mode with a different duty cycle at a high-power range in the midlevel power range and at zero power, respectively. Similarly, the experimental results in Figs. 28 –30 show the achievement of complete ZVS turn-ON of the primary switches in the forward mode in all power ranges and a wide-voltage range. The experimental results confirm that with auxiliary inductances combined with V_{Cc} control, the CF converter can achieve the complete ZVS turn-ON of all switches under the entire load range, with a wide-voltage range in both power directions.

It should be noted that the hard switching could make the four-phase voltages unbalance due to the voltage ringing of the switches, resulting in the four-phase transformer current unbalance. Comparing the experimental results of the converter in Fig. 31 clearly show the advantage of adding auxiliary inductors in four-phase current balancing.

Fig. 32 shows the temperature measurement of the transformer under zero and full power levels. The core temperature distribution is uniform due to the balanced structure. The maximum core temperature is around 48 °C.

Fig. 33 shows the efficiency curves of the converter under different LVS voltages, as measured using a Yokogawa WT3000 device. The maximum efficiency is 98.1% at 7 kW when $V_L = 350$ V and is reduced to 97.8% under a full load of 15 kW. Under a wide-voltage range, the efficiency is slightly reduced

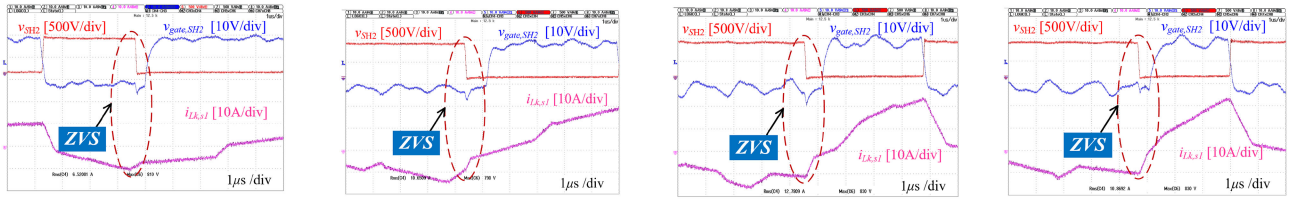


Fig. 25. Experimental waveform showing the achievement of ZVS of the *secondary switches in the reverse mode* with different duty cycles *in the high-power range*. (a) $D = 0.27$, $V_L = 200$ V, and $P = 7.5$ kW. (b) $D = 0.46$, $V_L = 350$ V, and $P = 14$ kW. (c) $D = 0.66$, $V_L = 500$ V, and $P = 15$ kW. (d) $D = 0.73$, $V_L = 550$ V, and $P = 15$ kW.

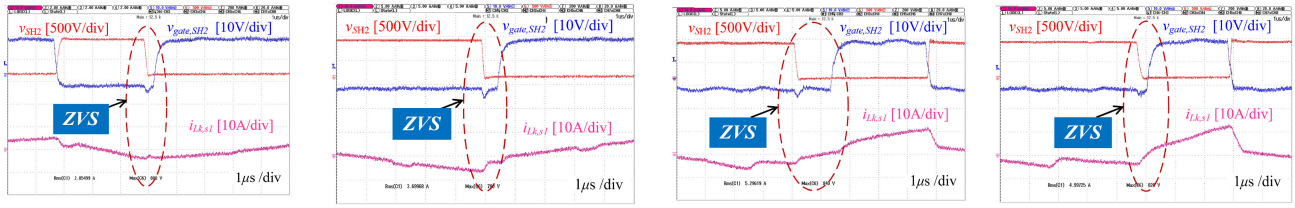


Fig. 26. Experimental waveform showing the achievement of ZVS of the *secondary switches in the reverse mode* with different duty cycles *in the medium-power range*. (a) $D = 0.27$, $V_L = 200$ V, and $P = 1.5$ kW. (b) $D = 0.45$, $V_L = 350$ V, and $P = 5.4$ kW. (c) $D = 0.66$, $V_L = 500$ V, and $P = 5.4$ kW. (d) $D = 0.73$, $V_L = 550$ V, and $P = 5.2$ kW.

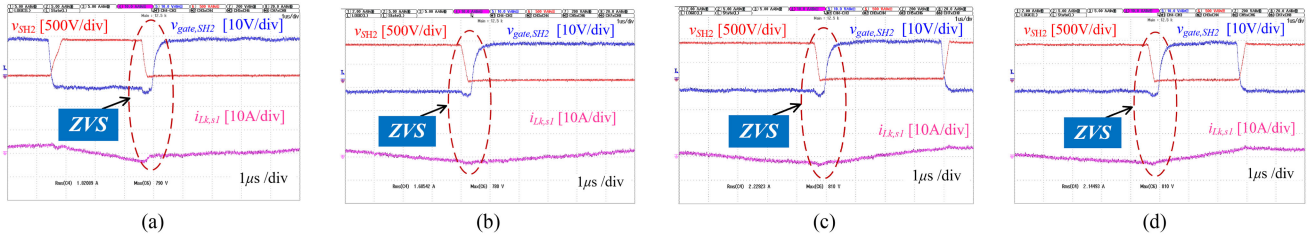


Fig. 27. Experimental waveform showing the achievement of ZVS of the *secondary switches in the reverse mode* with different duty cycles at *zero power*. (a) $D = 0.27$, $V_L = 200$ V, and $P = 0$ W. (b) $D = 0.46$, $V_L = 350$ V, and $P = 0$ W. (c) $D = 0.66$, $V_L = 500$ V, and $P = 0$ W. (d) $D = 0.73$, $V_L = 550$ V, and $P = 0$ W.

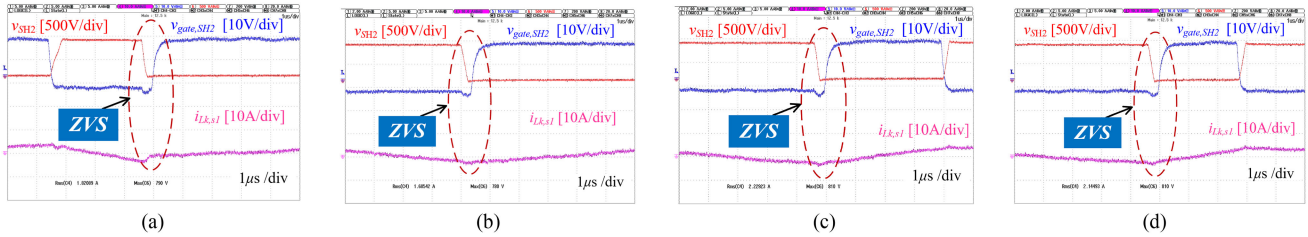


Fig. 28. Experimental waveform showing the achievement of ZVS *of the primary switches in the forward mode* with different duty cycles *in the high-power range*. (a) $D = 0.25$, $V_L = 200$ V, and $P = 7.4$ kW. (b) $D = 0.44$, $V_L = 350$ V, and $P = 14$ kW. (c) $D = 0.62$, $V_L = 500$ V, and $P = 14.8$ kW. (d) $D = 0.725$, $V_L = 580$ V, and $P = 15$ kW.

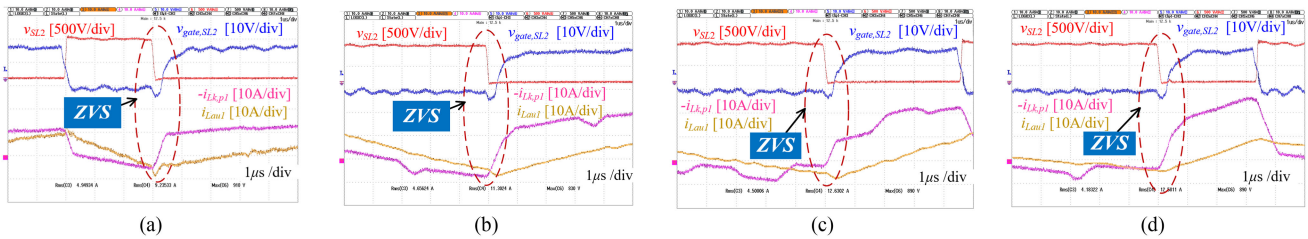


Fig. 29. Experimental waveform showing the achievement of ZVS of the *primary switches in the forward mode* with different duty cycles *in the medium-power range*. (a) $D = 0.25$, $V_L = 200$ V, and $P = 1.5$ kW. (b) $D = 0.44$, $V_L = 350$ V, and $P = 3.9$ kW. (c) $D = 0.62$, $V_L = 500$ V, and $P = 5.3$ kW. (d) $D = 0.725$, $V_L = 580$ V, and $P = 5.8$ kW.

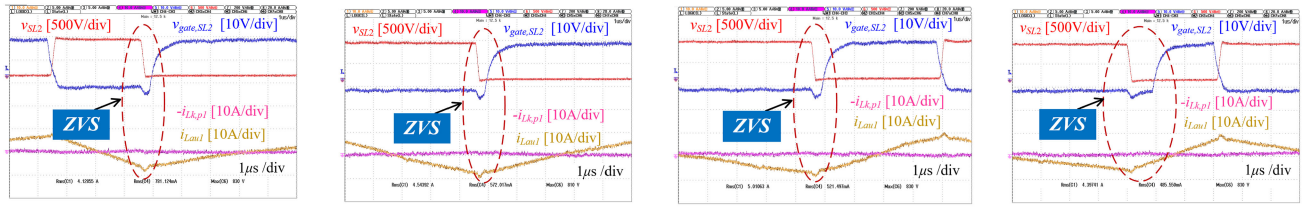


Fig. 30. Experimental waveform showing the achievement of ZVS of the *primary switches in the forward mode* with different duty cycles *at zero power.* (a) $D = 0.27$, $V_L = 200$ V, and $P = 0$ W. (b) $D = 0.46$, $V_L = 350$ V, and $P = 0$ W. (c) $D = 0.66$, $V_L = 500$ V, and $P = 0$ W. (d) $D = 0.73$, $V_L = 550$ V, and $P = 0$ W.

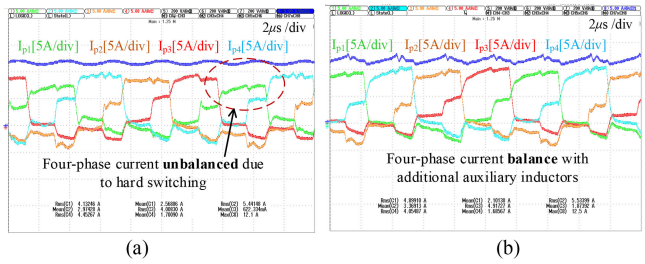


Fig. 31. Experimental result comparison of the converter showing the advantage of adding auxiliary inductors in four-phase current balancing. (a) Without auxiliary inductors. (b) With auxiliary inductors.

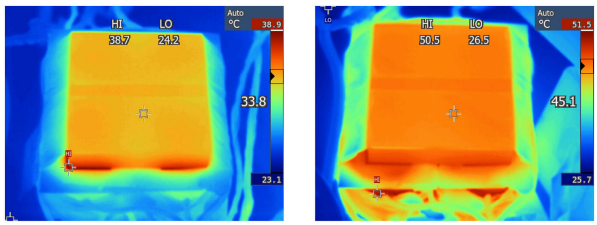


Fig. 32. Experimental results of the temperature distribution in the transformer showing the balanced structure and low loss under low and full loads.

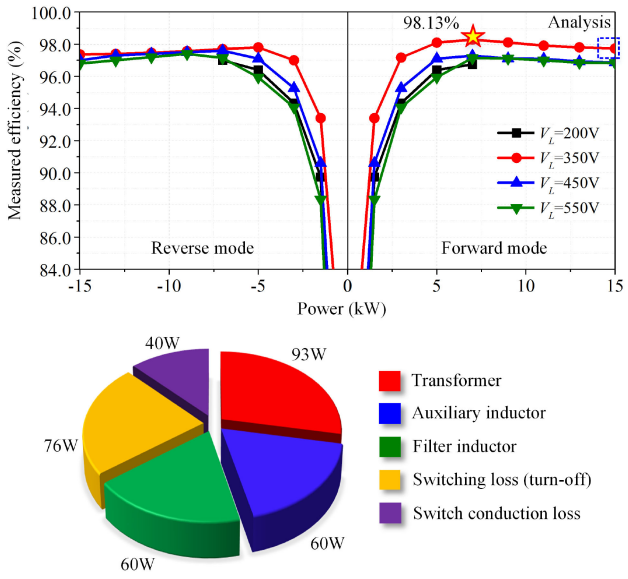


Fig. 33. Measured efficiencies of the converter as a function of the output power with different V_L ($I_{L,\max} = 37.5$ A when $V_L < 400$ V).

by less than 1% from 97.8% to 96.9%. This approach outperforms a three-phase converter in the literature [26], where the efficiency is reduced by nearly 3% times under a wide-voltage range due to the appearance of circulating current in both the high duty cycle ($D_L > 0.66$) and low duty cycle ($D_L < 0.33$) range.

VI. Conclusion

In this article, through a comprehensive analysis of the existing CF-DAB converters on nonpower transfer interval, ZVS conditions, and considering the challenge of the design of the transformer, a *four-phase current-fed push–pull DAB* converter with auxiliary inductors is proposed. In addition to the conventional advantages of a small filter inductor, a small clamp capacitor, and low current stress in the primary switches due to the effect of four-phase interleaving, the proposed converter can achieve complete ZVS turn-ON of all switches under a wide duty cycle range of $0.25 < D_L < 0.75$ in both power-flow directions by adding auxiliary inductors combined with the proposed V_{Cc} adjustment method. The duty cycle range can largely vary from 0.25 to 0.75 without nonpower transfer interval, resulting in a lower total rms current of switches. The proposed combined-core transformer can cancel the dc flux caused by the dc component of the primary winding current while also reducing the core volume, footprint, and height of the transformer compared with the separated-core transformer. The experimental results from the 15-kW prototype are provided to validate the proposed concept. The converter achieved a peak efficiency of 98% and high efficiency when operated at a wide-voltage range. The proposed transformer structure can also be applied to other four-phase voltage-fed and current-fed converters. The proposed method of the addition of auxiliary inductors combined with V_{Cc} adjustment is also valid for two-phase and three-phase structures with the optimal operating duty cycle ranges near 0.5 and 0.33–0.66, respectively.

Appendix

The power equations of the multiphase converters with different D_L of 0.5 and 0.75 under the PPS switching method are established in Table IV to show the advantage of the four-phase converter, which are carried out based on the analysis of the secondary winding current and the power transfer interval ignoring the effect of deadtime.

TABLE IV
POWER TRANSFER EQUATIONS OF THE MULTIPHASE CONVERTERS WITH DIFFERENT D_L UNDER PPS SWITCHING METHOD

Items	Two-phase	Three-phase	Four-phase
D_L= 0.5	$P=\frac{V_H^2}{L_k N^2}(1-D_L-\frac{\varphi}{2\pi})(\frac{\varphi}{2\pi}T_s)$	$P=2\frac{V_H^2}{L_k N^2}(\frac{1}{3}-\frac{1}{2}\frac{\varphi}{2\pi})(\frac{\varphi}{2\pi}T_s)$	$P=4\frac{V_H^2}{L_k N^2}(\frac{1}{4}-\frac{1}{2}\frac{\varphi}{2\pi})(\frac{\varphi}{2\pi}T_s)$
D_L= 0.75	$P=\frac{V_H^2}{L_k N^2}\left((1-D_L-\frac{1}{2}\frac{\varphi}{2\pi}\right)(\frac{\varphi}{2\pi}T_s)$	$P=2\frac{V_H^2}{L_k N^2}((1-D_L)-\frac{1}{2}\frac{\varphi}{2\pi})(\frac{\varphi}{2\pi}T_s)$	$P=3\frac{V_H^2}{L_k N^2}\left(\frac{1}{4}-\frac{1}{2}\frac{\varphi}{2\pi}\right)(\frac{\varphi}{2\pi}T_s)$

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