A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization

Chao Ding, *Student Member, IEEE*, Heziqi Liu, Khai D. T. Ngo, *Fellow, IEEE*, Rolando Burgos, *Senior Member, IEEE*, and Guo-Quan Lu, *Fellow, IEEE*

***Abstract*—Planar, double-side cooled power modules are emerging in electric-drive inverters because of their low profile, better heat extraction, and lower package parasitic inductances. However, there is still a concern about their reliability due to the rigid interconnection between the device chips and two substrates of the power module. In this article, a porous interposer made of low-temperature sintered silver is introduced to reduce the thermomechanical stresses in the module. A double-side cooled half-bridge module consisting of two 1200 V, 149 A SiC MOSFETs was designed, fabricated, and characterized. By using the sintered-Ag instead of solid copper interposers, our simulation results showed that, at a total power loss of 200 W, the thermomechanical stress at the most vulnerable interfaces (interposer-attach layer) was reduced by 42% and in the SiC MOSFET by 50% with a tradeoff of only 3.6% increase in junction temperature. The sintered-Ag interposers were readily fabricated into the desired dimensions without postmachining and did not require any surface finishing for die bonding and substrate interconnection by silver sintering. The porous interposers were also deformable under a low force or pressure, which helped to accommodate chip thickness and/or substrate-to-substrate gap variations in the planar module structure, thus simplifying module fabrication. The experimental results on the electrical performance of the fabricated SiC modules validated the success of using the porous silver interposers for fabricating planar, double-side cooled power modules.**

***Index Terms*—Double-side cooled power module, reduction of thermomechanical stress, sintered-Ag die-attach, sintered-Ag interposer.**

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Chao Ding is with the Department of Materials Science and Engineering, Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: dingchao@vt.edu).

Heziqi Liu is with the Department of Materials Science and Engineering, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: llhhzzqq@gmail.com).

Khai D. T. Ngo and Rolando Burgos are with the Bradley Department of Electrical and Computer Engineering, Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: kdtn@vt.edu; rolando@vt.edu).

Guo-Quan Lu is with the Department of Materials Science and Engineering, Virginia Tech, Blacksburg, VA 24061 USA, and also with the Bradley Department of Electrical and Computer Engineering, Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: gqlu@vt.edu).

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I. Introduction

ADVANCES of wide bandgap devices, e.g., SiC and GaN, are enabling the development of higher efficiency and higher power-density power electronics converters by increasing the switching frequency and device junction temperature [1]–[3]. These efforts have posed significant challenges on power module packaging, as the packaging structures, materials, and processing conditions significantly influence the thermal, electrical, mechanical performance, and reliability of the modules [4], [5]. Currently, the wire-bond interconnect technology is widely used for the device's top-side terminals because of the technology's maturity, low cost, and flexibility [6], [7]. However, the wire-bonded packages have relatively high parasitic inductances and can only cool the devices from one side, the die-attach side. Due to mismatched coefficients of thermal expansion (CTE) between the wire bonds and semiconductor device, the bonded areas are prone to fatigue failure caused by thermomechanical stresses [8]. Paralleled wire bonds [9], ribbon bond [10], direct lead bonding [11], and copper clip structures [12] have been practiced to improve current capacity, reduce parasitic inductances, and improve reliability. Modules made by these interconnect techniques, which use long and thin conductors to connect to the device's top terminals, are still limited to cooling from the die-attach side of the device chips. To improve package thermal performance, double-side cooled modules have been introduced, such as the metal-postinterconnected parallel-plate structure [13], flip-chip-on-flex [14], dimple array [15], embedded power [16], [17], silicon interposer [18], solder bump [19], metal bump [20]–[23], flip chip [24], power overlay [25], [26], and press pack [27]–[29]. All of these package structures have a common feature, i.e., the device chips are sandwiched between two electrically and thermally conductive substrates, one for die attach and the other for top-terminal interconnection. The top connection is usually formed with short metal interposers covering a significant portion of the device area. The result is a package with much improved thermal performance or double-side cooling and having a smaller footprint and lower package

parasitic inductances due to the additional metal plane for routing. However, the double-side cooled package is structurally more rigid than its single-side cooled wire-bonded package, raising concerns for its thermomechanical reliability.

To make a double-side cooled package, interposers, such as metal brick, ball, or tube, have been used for device top interconnection [13], [20], [23], [30]–[32], and copper (Cu) is the most widely used interposer material [13], [31], [32]. Cao *et al*. [33]–[38] have shown that the use of solid Cu interposers introduces more thermomechanical stresses in the device chips and at the bonded interfaces than those in a wire-bonded module. To reduce the thermomechanical stresses, interposers made of molybdenum (Mo) [34]–[36] or Cu/Mo/Cu [37] were evaluated because the CTE of Mo (4.8 ppm/K) is closer to semiconductor materials (2.6 ppm/K for Si and 3.7 ppm/K for SiC) than Cu (17 ppm/K). But Mo has a lower thermal conductivity than Cu and requires a surface metallization (e.g., Ti/Ni/Ag) to be compatible with soldering or silver sintering. Other interposer structures, such as a trenched Cu plate [33], X-shaped, octagon shaped [38], and Ag tubing [39], were explored to reduce thermomechanical stress, but they all suffer from higher thermal resistance than a solid Cu brick due to a smaller heat conduction area. One of the main concerns with high thermomechanical stresses in double-side cooled modules is the reduction of fatigue life of the bonding material at the chip attach, interposer–chip, or interposer–substrate interface. Solders are the most commonly used bonding materials in power module assembly, and they are also easily fatigued under thermomechanical stresses due to low melting temperatures, low elastic moduli, and the formation of brittle intermetallic. Thus, the use of solders for bonding power modules limits their reliable operation temperatures below 200 °C [37]. Furthermore, for assembling double-side cooled modules, it typically requires multiple bonding steps, thus needing a set of solders with different melting temperatures, which further limits the operation temperature [36].

Recently, low-temperature silver sintering [40] has emerged as an alternative bonding technology to soldering. The sintering process takes place at less than 250 °C with or without pressure [41]; and, once the sintered-Ag joint is formed, it melts at 960 °C and has over three times higher thermal and electrical conductivities, and at least two times better reliability than soldered joints [42], [43]. These advantages make the silver sintering an excellent lead-free and reliable solution for packaging double-side cooled and high-temperature power modules. However, to apply the sintering process for bonding double-side cooled modules, one is challenged by variations in device chip thickness, substrate flatness, and interposer height. Since solders melt and solidify, they can easily "absorb" these variations to maintain continuity at all the bonded interfaces. However, in the low-temperature silver sintering process, silver does not melt; instead, the sintered bond is formed through solid-state atomic diffusion and large volume shrinkage from densification, thus cannot accommodate large geometric variations in the bondline. It was also reported in [44] that the bonding strength of the sintered-Ag joint decreases with bondline thickness. DiMarino *et al*. [34] and Wang *et al.* [35] built their double-side cooled modules using Ag sintering for die attach and Mo-interposer-to-die attach but had to use a thick layer of solder ($\sim$200 μm) for the interposer-to-substrate bonding to compensate different gap spacing existed between the interposers and the top substrate. A bondline thickness of 200-μm-thick sintered Ag would be too weak to compensate the geometric variations.

One solution to enable silver sintering for all the bonded interfaces in a double-side cooled module is to use interposers that can be plastically deformed under a low applied load during the assembly process to level all the geometric variations. And to reduce the thermomechanical stresses, it would be desirable that the interposer is made of a material or structures having low CTE or low elastic modulus or both. Deformable Ag tubing [30] and metal foams [45], [46] have been explored as interposers to achieve adjustable height, but the tradeoff is large thermal resistance through the top terminals because of the small heat conduction area.

In this article, we fabricated interposers by low-temperature sintering of a pressureless silver paste and used them along with the silver-sintering process to interconnect a double-side cooled SiC MOSFET module. The interposers were made by filling and sintering the paste inside a trench on a Teflon block. The trench width defined the interposer height. Because the sintered-silver interposer was porous, it could be deformed easily during the assembly process to accommodate the various geometric variations. And the porous interposer had a low elastic modulus to cut down the thermomechanical stresses. Furthermore, there was no need to surface finish the interposer for bonding by silver sintering. To demonstrate the advantages of the sintered-Ag interposer, we designed and fabricated a double-side cooled half-bridge power module using 1.2 kV, 149 A SiC MOSFET chips. In the following, we describe in detail the layout design of the module with thermal and thermomechanical simulations to show the advantages of the porous sintered-Ag interposer for interconnecting the module. Then, we present the processes for fabricating the interposers and the module, followed by the measurement results on the electrical performance of the module. Future work includes evaluation of these modules in electric-drive inverters and tests on their reliability.

II. Module Design and Simulations

A. Module Layout

Fig. 1 shows the layout design of an SiC half-bridge power module for demonstrating the porous interposers in making double-side cooled modules. Each module consisted of two SiC chips sandwiched between two aluminum nitride (AlN) direct-bond-copper (DBC) substrates. The power-loop interconnection within each module was achieved through six sintered-Ag interposers, two for each device connecting the source terminal to the top substrate and two connecting the two substrates. The overall module dimensions were 2.4 cm $\times$ 1.8 cm $\times$ 0.36 cm. All of the power terminals were on one side, and the connectors (G_1, SS_1, G_2, and SS_2) for the gate drivers were on the other side, as marked in Fig. 1(a). The power terminal configuration can be tailored to different busbar structures. The rest of the connectors were designed for current sensor and desaturation protection in future research. The parasitic inductances of the power loop and drive loop were 4.4 nH and 3.0 nH extracted from ANSYS Q3D, respectively. The low power-loop parasitic inductance can be attributed to having two parallel metal planes for routing.

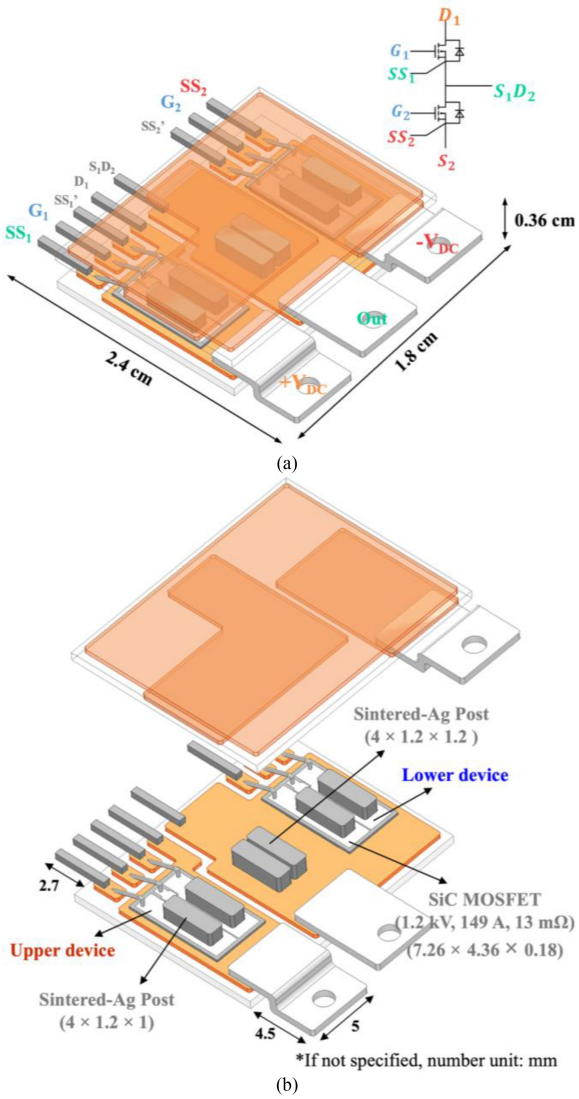

Fig. 1. (a) Layout design and (b) stacked view of the 1.2 kV, 149 A SiC MOSFET double-side cooled half-bridge module.

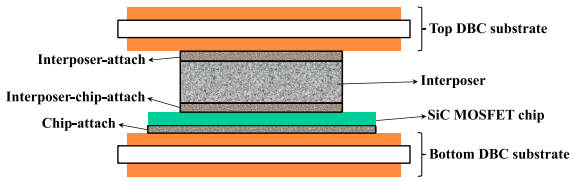

Fig. 2. Cross-sectional view of the double-side cooled module showing the layers of different interconnect materials across a device.

Fig. 2 is a view of the double-side cooled module cut across one device to show the layers of interconnects. There were three different bonded interfaces: chip attach, interposer–chip attach, and interposer–substrate attach.

B. Thermal Simulation

ANSYS Workbench was used to simulate the temperature distributions in the module, as shown in Fig. 1. For comparison,

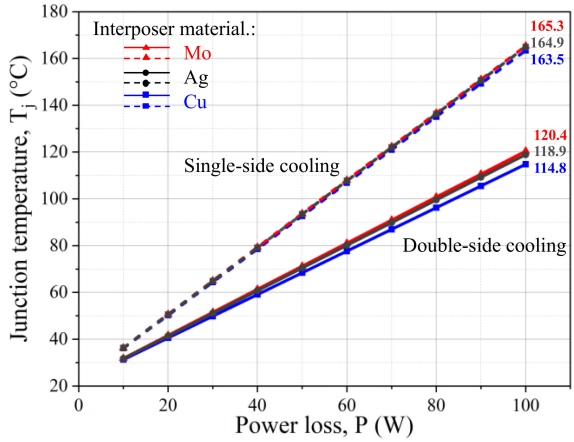

Fig. 3. Maximum junction temperature versus power loss of single-side cooled and double-side cooled modules with Cu, Mo, and sintered-Ag interposers.

the temperature distributions of the modules with Cu and Mo interposers were also simulated. The thermal conductivities of Cu, Mo, and sintered Ag are 385, 142, and 175 W/m·°C, respectively [30]. The high thermal conductivity of sintered Ag can be attributed to the percolation of Ag matrix with microstructurally distributed pores [47], [48]. In the simulations, the power dissipation from each SiC MOSFET device was varied from 10 to 100 W at an increment of 10 W, and the initial temperature was set at 22 °C. Since both devices in the half-bridge module were die attached on the bottom substrate, for single-side cooling, we assumed a convection coefficient of 8000 W/m^2·°C at the bottom substrate and 20 W/m^2·°C at the top substrate. For double-side cooling, a convection coefficient of 8000 W/m^2·°C was assumed at both the top and bottom substrates.

Fig. 3 shows the simulated results on device junction temperature (T_j) versus chip power loss showing the general trend of increasing T_j with power loss. Although the three types of interposer material have thermal conductivity values differing by nearly 300%, the differences in their T_j are small, less than 5% under either single-side or double-side cooling. This is because the major portion of the heat generated in the device was taken away through the die-attach layer, not through the interposers. Nevertheless, the effect of double-side cooling is significant, approximately 30% in reduction of the junction temperature over that with only one-side cooling. For example, at a total power loss of 200 W (100 W from each chip), T_j of the module with the sintered-Ag interposer and double-side cooling decreases by 28% (or 46 °C) over that with single-side cooling. Fig. 4 shows the temperature distributions of the modules using sintered-Ag, Cu, and Mo interposers with single-side and double-side cooling, respectively. The modules with double-side cooling have not only lower T_j but also more uniform temperature distributions.

To see how much improvement a double-side cooled module can improve the power handling capability of the device, thermal simulations were run for plots of the chip power loss versus the heatsink convection coefficient with the maximum allowed junction temperature to be 150, 200, or 250 °C. Fig. 5 shows that double-side cooling significantly improves the chip power handling capability. For example, assuming a convection coefficient of 10 000 W/m^2·°C and the maximum junction temperature of

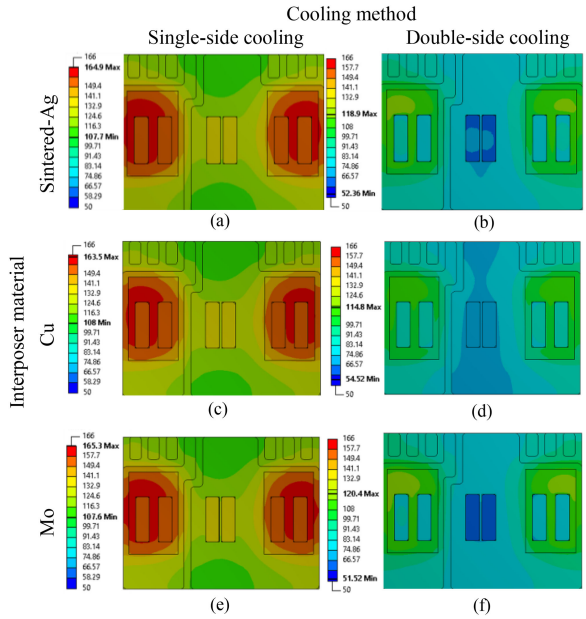

Fig. 4. Temperature distributions at a total power loss of 200 W for the modules with three different interposer materials and two different cooling schemes. (a) Sintered Ag and single-side cooling. (b) Sintered Ag and double-side cooling. (c) Cu and single-side cooling. (d) Cu and double-side cooling. (e) Mo and single-side cooling. (f) Mo and double-side cooling.

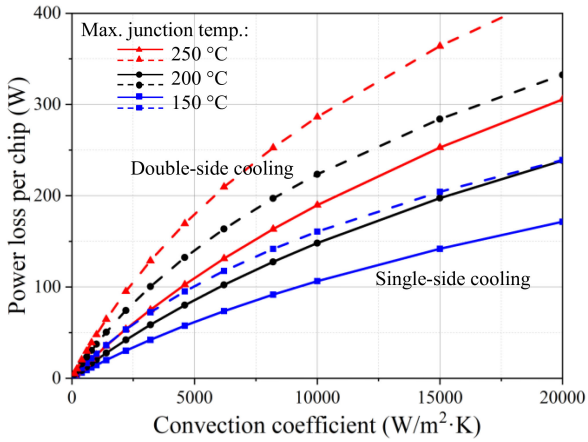

Fig. 5. Thermal simulation results of power loss per chip versus required convection coefficient for a single-side cooled or a double-side cooling to limit the maximum junction temperature under 150, 200, or 250 °C.

150 °C, the maximum power loss per chip that our module can support is 107 W if cooled from one side and is 161 W if cooled from both sides. Double-side cooling gives the device 50% more power handling capability than single-side cooling.

C. Thermomechanical Simulation

ANSYS Workbench was used to simulate the thermomechanical stresses in the double-side cooled module with Cu, Mo, or sintered-Ag interposers. In the simulations, the Anand viscoelasticity model was used to describe the viscoelastic behavior of all sintered-Ag elements with parameters taken from the article presented in [49]. Other material parameters for the simulations

TABLE I
MATERIAL PROPERTIES OF CU, MO, AND SINTERED AG [30]

Material	Elastic modulus (GPa)	CTE (ppm/°C)	Thermal conductivity (W/(m·°C))	Density (kg/m^3)
Cu	128	16.5	385	8960
Mo	320	4.9	142	10200
Sintered-Ag	6	18.9	175	8500

TABLE II
MAXIMUM VON MISES STRESS IN EACH COMPONENT OF POWER MODULE

Von Mises stress (MPa)	Interposer	Chip	Interposer -substrate attach	Interposer-chip attach	Chip attach
Sintered-Ag	9.2	41.0	14.9	14.1	12.9
Cu	47.4	81.6	25.5	20.4	11.7
Mo	29.7	60.1	17.6	11.3	11.2

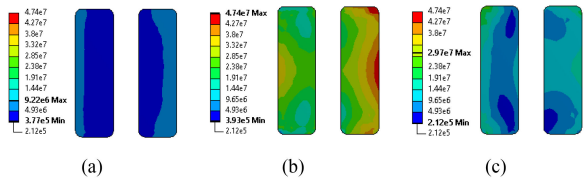

Fig. 6. Von Mises stress distribution in (a) sintered-Ag interposer, (b) Cu interposer, and (c) Mo interposer.

are listed in Table I. To simplify the simulations, we ignored the wire bonds and encapsulant. The stress-free temperature was set at 245°C, close to the Ag-sintering temperature for die attach and interposer attach. The simulation runs included first finding the thermomechanical stresses due to cooling from the sintering temperature down to room temperature and then the stresses from heating by the total module power loss of 200 W, i.e., 100 W per chip.

In reliability studies of power modules, the simulations of von Mises stresses in various layers of the module, specifically at the venerable joint locations, are widely used to correlate with the reliability measurement data. Jeon *et al.* [38] simulated the von Mises stresses of attached layers using several spacers or interposer geometries and measured the number of temperature cycles to failure. They showed that the number of cycles to failure is inversely correlated to the maximum von Mises stress. For each of the three types of module in this work, Table II summarizes the maximum von Mises stresses in the interposer, SiC chip, interposer-to-substrate attach, interposer-to-chip attach, and chip attach. Figs. 6–10 show the respective von Mises stress distributions in the key components. As given in Table II and Fig. 6, the sintered-Ag interposer had the lowest stress among all the interposer materials, namely 81% and 69% lower than the Cu and Mo interposers, respectively. This is because the sintered Ag has two orders of magnitude lower elastic modulus and no CTE mismatch between the sintered-Ag interposer and the sintered-Ag attachment. The stresses in the SiC MOSFETs were also significantly reduced when using the sintered-Ag

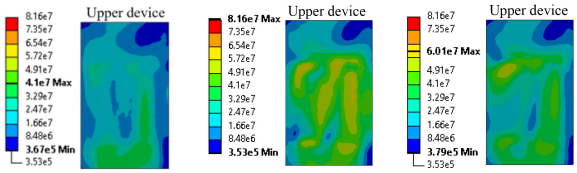

Fig. 7. Von Mises stress distribution in the SiC MOSFET chip in the module with (a) sintered-Ag interposer, (b) Cu interposer, and (c) Mo interposer.

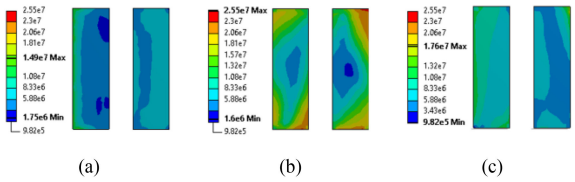

Fig. 8. Von Mises stress distribution at the interposer-to-substrate interface layer of the module with (a) sintered-Ag interposer, (b) Cu interposer, and (c) Mo interposer.

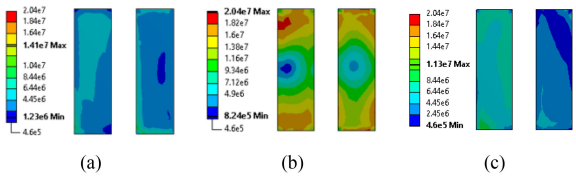

Fig. 9. Von Mises stress distribution at the interposer-to-chip interface layer in the module with (a) sintered-Ag interposer, (b) Cu interposer, and (c) Mo interposer.

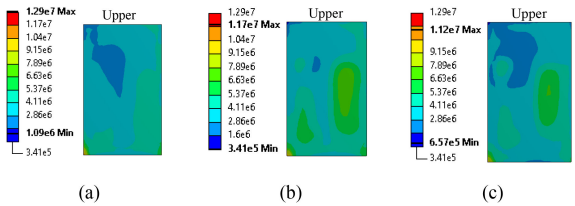

Fig. 10. Von Mises stress distribution at the chip-attach layer in the module with (a) sintered-Ag interposer, (b) Cu interposer, and (c) Mo interposer.

interposer, i.e., by 50% and 32% compared with that with Cu and Mo interposers, respectively, as given in Table II and Fig. 7.

Figs. 8–10 show for each module the von Mises stress distributions in the three bonded interfaces, i.e., interposer–substrate attach, interposer–chip attach, and chip attach. The bonded interface in a module is usually the first to fail [38], [50]. The stresses at the bonded interfaces with the sintered-Ag interposer were much lower than those with the Cu interposer, while they were similar to those with the Mo interposer. Of the three bonded interfaces in each module, the interposer-to-substrate interface had the highest stress; thus, it is the most likely site to fail first.

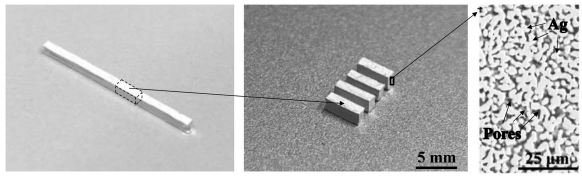

Fig. 11. (a) Sintered-Ag bar. (b) Few pieces of the cut interposers. (c) SEM image showing the porous microstructure of sintered-Ag interposer.

Considering together the thermal simulation results, as presented in Section II-B, we see that by using the sintered Ag instead of Cu for making interposers to interconnect the double-side cooled module, one can realize substantial reductions in thermomechanical stresses at the most vulnerable interfaces, i.e., by 42% in interposer–substrate attach layer with the tradeoff of raising the junction temperature by only 3.6%.

III. Interposer and Module Fabrication

A. Interposer Fabrication

A nanosilver paste from NBE Tech, LLC, was acquired for making the porous interposer, chip bonding, and interposer–chip and interposer–substrate bonding. To make the interposers, a trench was machined on a Teflon block with its width being the height and its depth being one of the other two dimensions of the interposer. The silver paste was squeezed into the trench using a squeegee, followed by pressureless sintering at 245 °C for 15 min. The sintered Ag was easily demolded out of the trench and cut into individual interposers. Fig. 11(a) and (b) shows a bar of the sintered silver after demolding and the samples of the interposer cut from the bar. Due to shrinkage after sintering, the top surface of the silver bar was recessed. Because the width of the trench defined the height of the interposer, the height uniform of the interposers was ensured. The two other dimensions of the interposer, one being the recessed depth and the other being the cut length from the bar, are not critical.

Fig. 11(c) shows a scanning electron microscope (SEM) image of the porous sintered-Ag interposer. The pores were distributed in a percolating Ag matrix, resulting in the high thermal conductivity of sintered Ag [47], [48].

B. Materials Used in the Module

Table III is a list of the materials used for making the half-bridge module. CREEs SiC MOSFET chips rated at 1.2 kV, 149 A, and 13 mΩ were bought from SemiDice. The drain pad of the device was metalized with a nickel (Ni)/gold (Au) surface finish, thus compatible with Ag sintering, but the source and gate pads were aluminum (Al), which is wire bondable but not Ag sinterable. To make the source pad Ag sinterable, a metallization of 100-nm Ti and 100-nm Ag was deposited by magnetron sputtering through a stainless-steel contact mask. Since the gate pad was too small for the metallization process, the gate and Kevin-source pads were wire bonded by a 0.25-mm-diameter Al wire. The AlN DBC substrates were obtained from Rogers, Inc., and came with Ag surface finish for bonding by Ag sintering. The terminal leads were locally machined from copper plates

TABLE III
MATERIAL LIST FOR MODULE CONSTRUCTION

Part	Materials	Specifications
SiC MOSFET	CREE CPM3-1200-0013A	1.2 kV, 149 A, and 13 mΩ
Substrate	Rogers AlN-DBC with Ag finish	Cu/AlN/Cu thickness: 0.3 mm/0.6 mm/0.3 mm
Chip attach	NBE Tech Nanosilver paste	Melting temp.: 961 °C Printed thickness: 50 μm
Interposer-chip attach & interposer-substrate attach	NBE Tech Nanosilver paste	Melting temp.: 961 °C Printed thickness: 100 μm
Interposer	Sintered-Ag made by NBE Tech Nanosilver paste	Dimension: 4×1×1 mm^3 and 4×1×1.2 mm^3
Gate-bonding wire	TANAKA Aluminum wire	Diameter: 0.25 mm
Encapsulant	LORD ME-531 underfill	Cured at 165 °C for 15 min
Terminals	Local machined copper plate	Thickness: 0.5 mm
Terminal attachment	SolderPlus Solder (Sn10/Pb88/Ag2)	Melting temp.: 278 °C

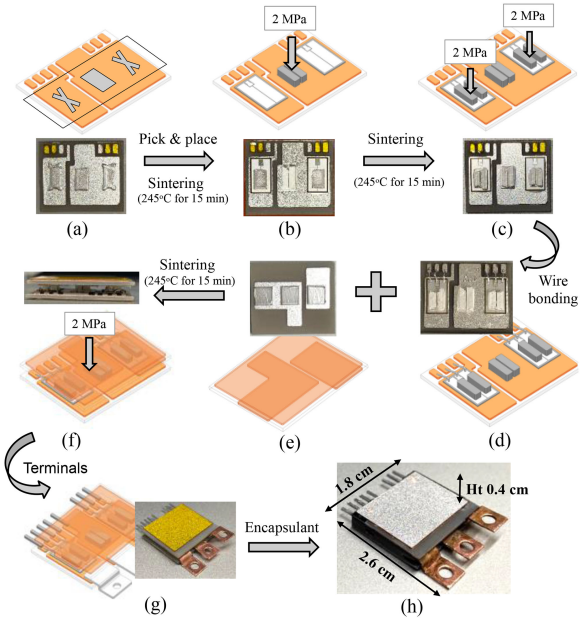

Fig. 12. Fabrication steps of the double-side half-bridge module.

and attached to the module by soldering with a high-Pb solder alloy. An underfill material was used to encapsulate the devices and bond the structure together.

C. Module Assembly

Fig. 12 shows the process for fabricating the SiC half-bridge module. First, the silver paste was stencil printed on a patterned DBC substrate, and two SiC MOSFET chips and two interposers were mounted on the substrate. Then, the assembly was heated at a ramp rate of 5 °C/min from room temperature to 245 °C for 15 min to sinter the chip attach and interposer-to-substrate attach. During the sintering, 2-MPa pressure was put on the sintered-Ag interposers to hold their positions. The next step was to mount and sinter two interposers on the source pad of each

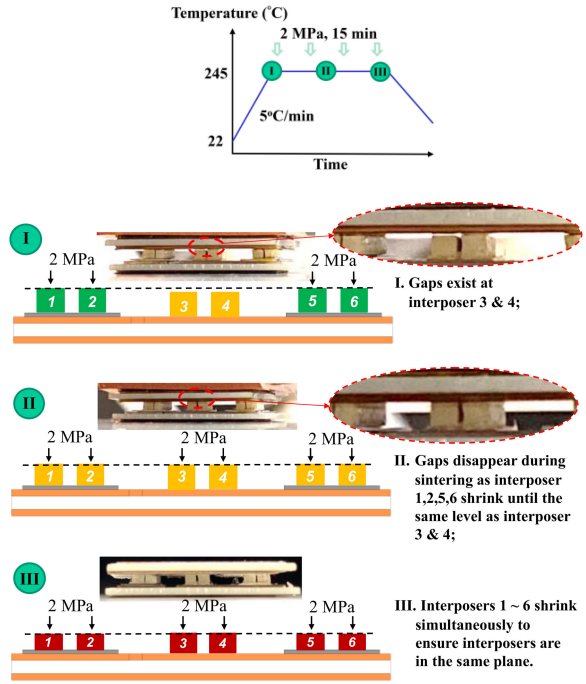

Fig. 13. Illustration of the ease of deformation of the sintered-Ag interposer to level the heights of the interposers for interconnection between the two substrates.

SiC chip, as shown in Fig. 12(c). The gate pad and Kelvin-source connections to the substrate were made through bond wires, as shown in Fig. 12(d). Afterward, the nanosilver paste was stencil printed on another DBC substrate, and the two substrates were bonded together by sintering under a 2-MPa pressure using the same heating profile as before. The buffer sheets of rubber and Teflon were added between the top platen of the hot press and the top DBC substrate to ensure uniform pressure applied to the module. The next was to solder the copper terminal leads for power and pins for the gate and Kelvin-source connection. Finally, an underfill material was extruded into the empty space between the two substrates and cured in place. The encapsulation material keeps oxygen and or moisture away from the silver joints and interposers, thus mitigating the silver migration risk [51]. Fig. 12(h) shows the finished half-bridge module measured at 2.7 cm× 1.9 cm× 0.4 cm. The thickness variation of the module was less than 0.01 cm, which can easily be compensated by a thermal interface material to be inserted between the module and heatsink. The footprint of this finished part was slightly larger than the design in Fig. 1(a) because the DBC substrates and terminal leads were made slightly larger.

Of the fabrication steps described above, the most critical one is shown in Fig. 12(f), i.e., bonding the top substrate to the six interposers from the bottom substrate, namely the four already bonded on the device chips and two bonded directly on the bottom substrate. Here, the pressure-assisted sintering was necessary to close any gaps in the interconnection caused by variations in chip thickness, interposer height, and substrate distortion. To illustrate its working, Fig. 13 shows the gaps between the top substrate and the interposers prior to sintering and elimination of the gaps by applying a nominal pressure of

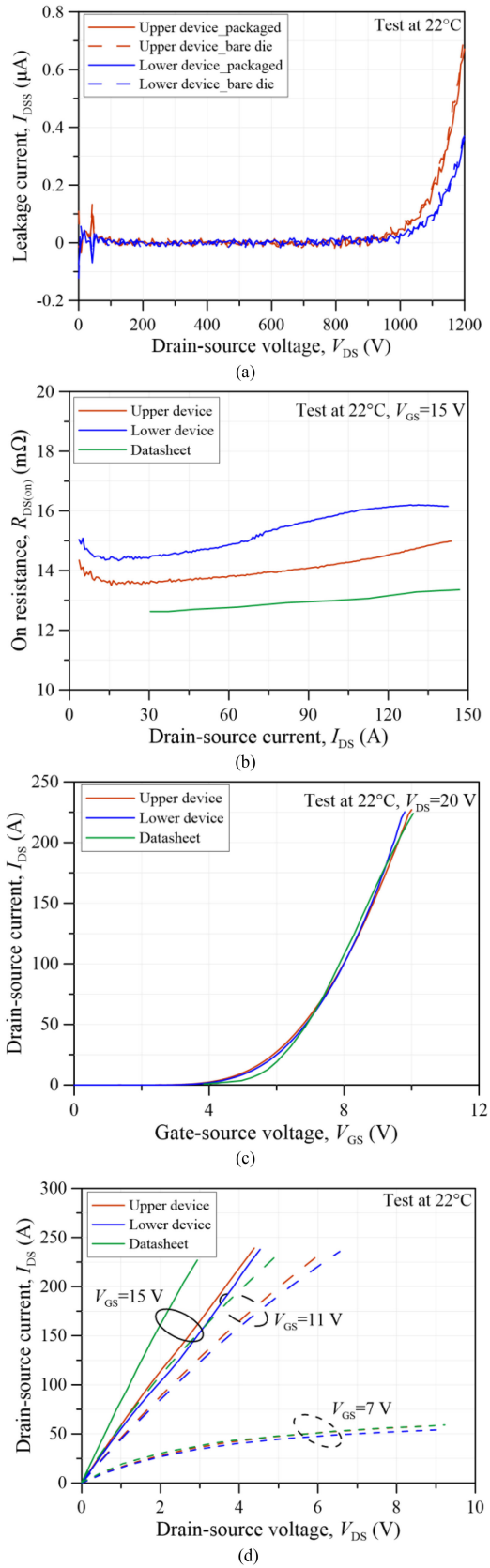

Fig. 14. Measured static characteristics of the devices in the half-bridge module. (a) Zero-gate-voltage drain current. (b) Drain–source ON-state resistance. (c) Transfer characteristics. (d) Output characteristics.

2 MPa during the Ag-sintering process. When the heights of the interposers were different, at first, all of the applied loads were on the taller one(s), which then quickly shrank due to their porous structure until all the interposers were leveled and evenly shared the load. The fact that the sintered-Ag interposer could be easily deformed under a low load significantly increased our assembly yield. Thus, it has the potential to enable the low-cost fabrication of double-side cooled modules with all the critical bonded interfaces done by Ag sintering to realize higher thermal performance, higher junction temperature, and improved reliability.

IV. Module Electrical Characterization

The static characteristics of the fabricated SiC MOSFET module were tested in an Agilent B1505A curve tracer. Fig. 14(a) shows the zero-gate-voltage drain currents, and Fig. 14(b) shows the ON-state resistance of the upper and lower SiC MOSFETs. The leakage currents of the SiC MOSFETs before and after packaging were almost the same. The package interconnects and the terminal leads only added about 2 mΩ ON-resistance to the device. Fig. 14(c) and (d) shows the transfer characteristics and the *I–V* output characteristics, respectively. The slight discrepancy between the output characteristics of the die listed in its datasheet and those measured after packaging came from the added resistance of the package. Overall, the static *I–V* characteristics of the packaged die were similar to those of the bare die. Similarities of the static characteristics between the packaged and bare device suggest that our packaging process, including the sintering steps under 2-MPa pressure, did not alter the device. More characterizations (switching test, reliability evaluation, etc.) on the double-side cooled power modules with sintered-Ag interposers will be presented in the future.

V. Conclusion

A planar double-side cooled SiC MOSFET half-bridge module using sintered-Ag interposers and all sintered-Ag joints was designed, fabricated, and characterized. The thermomechanical simulations showed that the use of the sintered-Ag interposer reduced the thermomechanical stresses at vulnerable interfaces by nearly 50% over using solid Cu interposer. The porous sintered-Ag interposer was easily deformable under a low load, which improved the yield of module interconnection in the presence of imperfections caused by variations in die thickness, interposer height, and substrate distortion. The experimental results on the electrical performance of the fabricated SiC modules validated the fabrication of a module design that employs the sintered-Ag interposers and all sintered-Ag joints for making high-power-density converters with reliable operations at high junction temperatures.

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Chao Ding (Student Member, IEEE) received the B.S. degree in materials science and engineering from Tianjin University, Tianjin, China, in 2016. He is currently working toward the Ph.D. degree in materials science and engineering with Virginia Tech, Blacksburg, VA, USA.

He had an internship with Apple, Inc., on electromagnetic analysis of wireless charging systems. His research interests include modeling and development of magnetic pastes, additive manufacturing of power magnetics, and high-temperature power electronics packaging for electric drives.

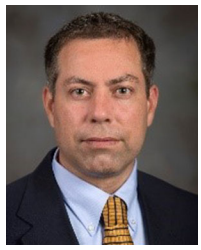
Mr. Ding is a member of the IEEE Power Electronics Society.

Heziqi Liu received the B.S. degree in material processing and control engineering in 2020 from Tianjin University, Tianjin, China, where he is currently working toward the Ph.D. degree in material processing engineering.

He was an Exchange Student with Virginia Tech, Blacksburg, VA, USA, in 2020.

Khai D. T. Ngo (Fellow, IEEE) received the B.S. degree from California State Polytechnic University, Pomona, CA, USA, in 1979, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 1980 and 1984, respectively, all in electrical and electronics engineering.

He is currently a Professor of electrical and computer engineering with Virginia Tech, Blacksburg, VA, USA. From 1984 to 1988, he was a member of Technical Staff with the General Electric Corporate Research and Development Center, Schenectady, NY, USA. From 1988 to 2006, he was with the University of Florida, Gainesville, FL, USA. With Virginia Tech, he pursues technologies for integration and packaging of power passive and active components to realize building blocks for power electronic systems. These technologies lead to power conversion systems with higher efficiency and higher power density. His current research interests include topologies, control, emission, and integration issues for radio frequency power converters, magnetic materials and components, energy reclamation, and power-integrated circuits.



Rolando Burgos (Senior Member, IEEE) received the B.S. degree in electronics engineering, the Electronics Engineering Professional degree, and the M.S. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 1995, 1997, 1999, and 2002, respectively.

In 2002, he joined as a Postdoctoral Fellow with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, becoming a Research Scientist in 2003, and Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research, Raleigh, NC, USA, where he was a Scientist from 2009 to 2010, and a Principal Scientist from 2010 to 2012. In 2010, he was appointed as an Adjunct Associate Professor with the Department of Electrical and Computer Engineering, North Carolina State University with the Future Renewable Electric Energy Delivery and Management Systems Center. In 2012, he returned to Virginia Tech as an Associate Professor with The Bradley Department of Electrical and Computer Engineering, where he was promoted to a Professor in 2019. His research interests include high-power-density wide-bandgap semiconductor-based power conversion—low-voltage and medium-voltage applications, packaging and integration, electromagnetic interference, and electromagnetic compatibility, multiphase multilevel power converters, modeling and control, grid power electronics systems, and the stability of ac and dc power systems.

Dr. Burgos is a member of the IEEE Power Electronics Society, where he currently serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the *IEEE Journal of Emerging and Selected Topics in Power Electronics*. He is also the past Chair of the Technical Committee on Power and Control Core Technologies. He is also a member of the IEEE Industry Applications Society, the IEEE Industrial Electronics Society, and the IEEE Power and Energy Society.

Guo-Quan Lu (Fellow, IEEE) received the double-major B.S. degree in physics and the M.S.E. degree from Carnegie-Mellon University, Pittsburgh, PA, USA, in 1984 and the Ph.D. degree in applied physics/materials science from Harvard University, Cambridge, MA, USA, in 1990.

He is a Professor jointly appointed between the Department of Materials Science and Engineering and the Bradley Department of Electrical and Computer Engineering with Virginia Tech, Blacksburg, VA, USA. He has worked with Alcoa Technical Center before joining Virginia Tech. He has authored or coauthored more than 160 peer-reviewed journal articles.

Dr. Lu was a recipient of the Virginia Tech Teaching Award and a National Science Foundation CAREER Award. His development of a nanoscale silver paste was recognized with an R&D 100 Award in 2007.