A Cost-Reliability Trade-Off Fault-Tolerant Series-Resonant Converter Combining Redundancy and Reconstruction

Jiangming Huang, Guipeng Chen, *Member, IEEE*, and Haochen Shi

***Abstract*—Adding redundant converters or switches are two common strategies to achieve fault-tolerant operation of converters. The former one is straightforward but costly, while the latter one is cost-effective but with sacrifice on the reliability as it only works for switches' failure. Aiming to achieve a good trade-off between cost and reliability, a novel fault-tolerant full-bridge series-resonant converter (FB-SRC) which only needs a redundant half-bridge SRC (HB-SRC) to gain fault tolerance for all fault-prone components is proposed in this article. The proposed converter can keep working normally when short-circuit fault or open-circuit fault happens on switches, diodes, or the output filter capacitor. After fault occurs, the redundant HB-SRC converter will combine the remaining healthy part of original FB-SRC to reconstruct an input-parallel and output-series dual HB-SRC, which can maintain the rated output power with reduced cost. In the article, component's reliability of SRC is first analyzed. Then, operation and performance analysis of the proposed fault-tolerant converter is introduced in detail. As the voltage/current stresses of components are almost the same during the prefault and postfault operation, the converter design is simple. Finally, experimental results of a 500 W prototype are also given to verify the effectiveness.**

***Index Terms*—Cost-reliability trade-off, fault-tolerant, series-resonant converter (SRC), topology reconstruction.**

I. Introduction

DUE to its soft-switching characteristic, resonant dc–dc converter has been widely used in a number of mission-critical applications such as more electric aircraft (MEA) [1], [2] and data center [3]–[5], in which continuous operation is of paramount importance. For example, the resonant converter in electrical power system of MEA should keep supplying power to all critical mission loads after converter failure, otherwise the MEA would be out of control and suffer security risk. In order to meet the high reliability requirement, there are two main fault-tolerant strategies for dc–dc converters, which can be classified as module-level [6]–[12] and switch-level [13]–[17].

In the module-level methods [6]–[12], fault-tolerant ability of any active/passive component can be acquired by employing modular redundancy, which is highly reliable. When fault occurs, the faulty submodule would be isolated and the redundant submodule would automatically join to maintain the continuous operation. However, to realize k fault-tolerant abilities in the system with n original submodules, the overall system cost is increased by k/n times, which increases with the decrement of n. Especially, when $n = 1$ and $k = 1$, a full backup of original converter is needed to achieve once fault-tolerant capability, resulting in undesired additional cost. Therefore, although the module-level method achieves high reliability, high cost is also incurred when the number of original submodules is small.

Aiming to optimize the cost and volume, switch-level method is proposed in [13]–[17], which only focuses on the fault-tolerant operation of switches instead of all components, as switches are considered to be relatively vulnerable according to a large number of industrial surveys [18]. In [13], [14], a redundant switch is added in parallel with the original switch. This idea to realize fault-tolerant operation is straightforward. When the original switch fails, the redundant one starts to work to maintain the same operation. In [15], a redundant switch is added to a buck converter, which can help to reconfigure into a buck–boost converter to remain the output voltage after switch failure. Nevertheless, a TRIAC is also required to connect in series with the redundant switch, which is always turned-OFF before the original switch fault to avoid the unnecessary damage on redundant switch. In addition, by adding redundant switches and TRIACs to original switches is not an optimal solution for converters with a relatively large number of switches, e.g., full-bridge (FB) converters, since the overall cost and volume will deteriorate with the increase of switches.

On the other hand, because the FB converter has inherent topology reconstruction characteristic that it can be reconfigured into a half-bridge (HB) converter after a switch failure, no redundant switch is demanded to achieve fault-tolerant operation in [16], [17]. For example, when short-circuit fault (SCF) occurs on one switch in the FB series-resonant converter (FB-SRC), it will transform into an HB-SRC by just turning OFF the other switch

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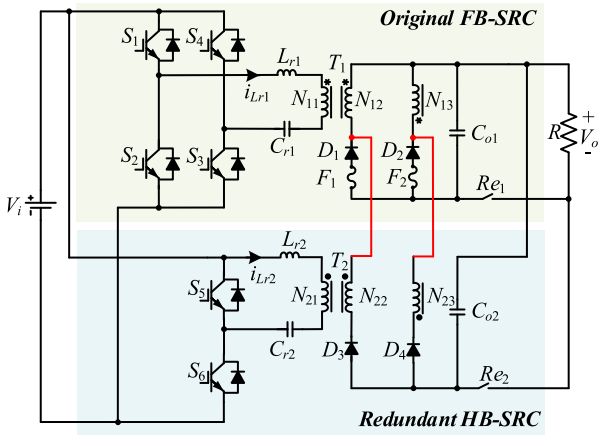


Fig. 1. Proposed fault-tolerant SRC.

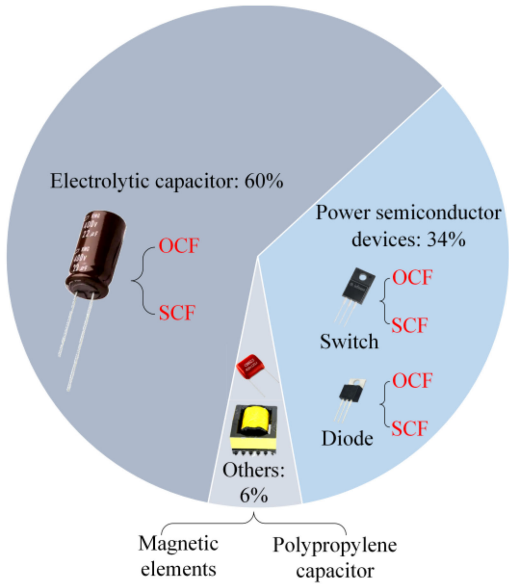


Fig. 2. Failure probability and mode of different components [19].

in the same leg and utilizing the remaining healthy switches [16]. However, in the practice, because the output voltage in post-fault HB converter is reduced to half of the original FB converter, additional voltage-double cell is needed. Besides, the available output power is also half reduced after topology reconstruction, which may not achieve a true fault-tolerant capability. More importantly, in all aforementioned switch-level methods, diodes and output filter capacitor which are also fragile components are not considered, and hence enhanced reliability is expected.

From above, high reliability is obtained in the module-level fault-tolerant method but with high cost, while it is contrary in the switch-level alternative that low cost is realized with low reliability. In order to make a trade-off between reliability and cost, a fault-tolerant SRC combining redundancy and reconstruction, is proposed in Fig. 1. First, a redundant HB-SRC instead of FB-SRC is added; hence, the overall cost is effectively optimized from the reduction of two switches and their corresponding drivers. Second, the proposed converter can remain normal operation not only when fault occurs on switches, but also on diodes and output filter capacitor. As these three components have very high fault probability in comparison with other components such as transformer, the reliability of proposed converter approximates that of the conventional module-level strategy with a redundant FB-SRC. Last, with the aid of the redundant HB-SRC having modified connection of secondary windings of transformer, the proposed converter will reconstruct into an input-parallel-output-series (IPOS) HB-SRC after failure. Consequently, the output voltage as well as the rated power can remain almost the same as the original FB-SRC.

The remainder of this article is organized as follows. The reliability analysis of components in FB-SRC is first introduced in Section II. Then, prefault and postfault operation of the proposed fault-tolerant SRC are presented in Section III. In Section IV, performance analysis including voltage gains and voltage/current stresses are demonstrated, and a 500 W prototype is accordingly designed in Section V. Finally, experimental results are provided in Section VI, and the conclusion is drawn in Section VII.

II. Component's Reliability Analysis of FB-SRC

As shown in Fig. 1, the typical FB-SRC consists of four switches $S_1 \sim S_4$, two diodes $D_1 \sim D_2$, one output filter capacitor C_{o1}, one resonant capacitor C_{r1}, one resonant inductor L_{r1}, and one transformer T_1 with n_1:1:1 turns ratio. The reliability of different components varies due to the different physics characteristics, which is explained in detail as follows:

1) *Switches $S_1 \sim S_4$ and Diodes $D_1 \sim D_2$:* According to the MIL-BK 217F standard [19], power semiconductor devices are prone to failure caused by vibration, high electrical and thermal stresses, which are responsible for 34% of the breakdowns of converters as shown in Fig. 2. Switches $S_1 \sim S_4$ in FB-SRC usually use IGBT due to the zero-current-switching (ZCS) operation. There are two possible failure types for IGBT: open-circuit fault (OCF) and SCF. The main reasons of OCF include bond-wire lift off or rupture and the failure of gate drive. On the other hand, the SCF of switches $S_1 \sim S_4$ will happen under energy shock, second breakdown, and static or dynamic latch up [20]. Similarly, diodes $D_1 \sim D_2$ also have OCF related with the damage of bond wire and SCF. The SCF of diode might be the result of static high-voltage breakdown, rising of leakage current, snappy recovery, and reverse recovery dynamic avalanche [21]. In the FB-SRC converter, the consequence of diode SCF is much worse than OCF, because high short current will induce to damage the whole converter. Hence, it is better to add fuses $F_1 \sim F_2$ in series with diodes $D_1 \sim D_2$ to exclude them from converter after SCF, as illustrated in Fig. 1.
2) *Output Filter Capacitor C_{o1}:* Electrolytic capacitor has been widely used as filter and energy storage due to the favorable features of large capacitance and low cost. However, the electrolytic capacitor is considered as one

of the most fragile components [19], which accounts for 60% of the converter breakdowns, as shown in Fig. 2. Electrolytic capacitor faults can be divided into SCF and OCF. The dominant failure mode of electrolytic capacitor is OCF. It is mainly caused by the oxide film existing between the lead and the aluminum foil, which is generated by penetration of electrolyte into the ambient cracks. In addition, self-healing dielectric breakdown induced by high electrical and thermal stress can also lead to the OCF. On the other hand, SCF of electrolytic capacitor might happen under dielectric breakdown of oxide layer [22].

3) *Other Components:* Polypropylene capacitor is usually used for resonant capacitor C_{r1}, and inductor L_{r1} and transformer T_1 are magnetic elements. In general, they are not easy to be faulty.

From above, switches $S_1 \sim S_4$, diodes $D_1 \sim D_2$, and output filter capacitor C_{o1} have much higher fault probability than the other components in the FB-SRC. In the proposed converter in Fig. 1, fault tolerance of all these components including SCF/OCF of switches, diodes, and output filter capacitor is realized; hence, its reliability is close to the module-level strategy with a full-backup redundant FB-SRC. Besides, only an auxiliary HB-SRC instead of FB-SRC is needed to reconstruct the converter after failure, the overall cost is optimized. Therefore, the proposed converter can achieve a good trade-off between cost and reliability, by combining redundancy and reconstruction.

III. Operation of Proposed Fault-Tolerant SRC

In the proposed converter, a redundant HB-SRC consisting of two switches $S_5 \sim S_6$, two diodes $D_3 \sim D_4$, one output filter capacitor C_{o2}, one resonant inductor L_{r2}, one resonant capacitor C_{r2}, and one transformer T_2 with turn ratio n_2:1:1 is employed to achieve fault-tolerant capability of switches, diodes, and output filter capacitor in original FB-SRC, as shown in Fig. 1. The secondary windings N_{22} and N_{23} of the transformer T_2 are, respectively, connected to the cathode of diode D_1 and D_2, so that topology reconstruction can be implemented after failure to guarantee normal operation.

According to the fault condition, operation of the proposed converter can be classified into three modes (modes 1, 2, and 3). In mode 1, relay R_{e1} is ON. The original FB-SRC works normally and supplies power from input to the output load. Relay R_{e2} is turned OFF, and the redundant HB-SRC is stand-by. Once SCF/OCF of any switch $S_1 \sim S_4$, diode $D_1 \sim D_2$, and output filter capacitor C_{o1} happens in the original FB-SRC, the operation transits from mode 1 to mode 2. There are three possible submodes 2A, 2B, and 2C in mode 2, which, respectively, correspond to the fault of switch, diode, and output filter capacitor, as illustrated in Fig. 3. In mode 2, relay R_{e2} is ON. The redundant HB-SRC starts working, which will reconstruct an IPOS converter with the aid of the remaining healthy components in the original FB-SRC to maintain the output voltage/power. Besides, in mode 2B or mode 2C with failure on diode or output filter capacitor, if a switch in original FB-SRC is also faulty, the proposed converter can still work normally, which is denoted as mode 3.

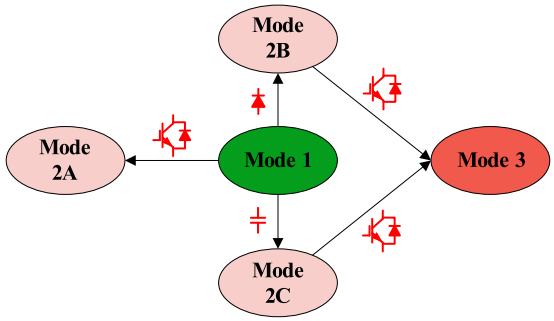


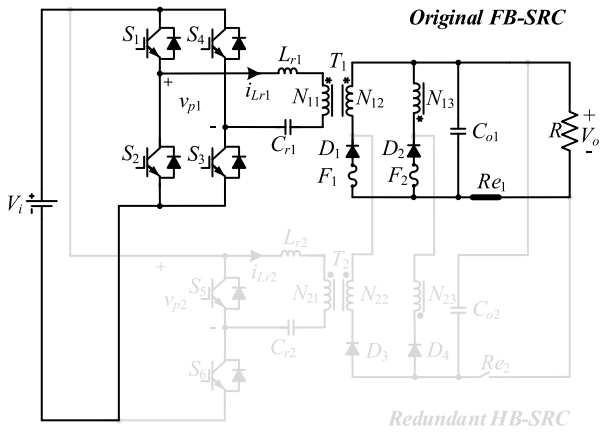
Fig. 3. Flow diagram of mode transition.

A. Mode 1: Prefault Operation

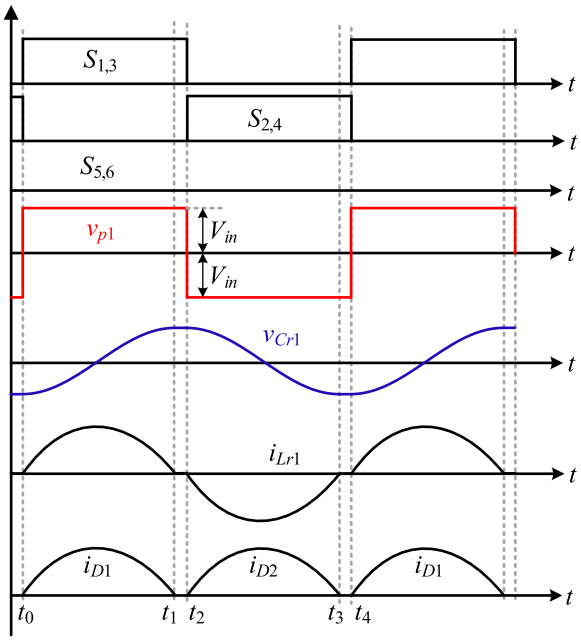
In mode 1, relay R_{e1} is ON and R_{e2} is OFF; hence, only the original FB-SRC takes part in work. Fig. 4(a) shows the equivalent circuit, and Fig. 4(b) shows the key waveforms of the original FB-SRC operating below the resonant frequency ($f_s < f_r$), where f_s is switching frequency and $f_r = 1/(2\pi\sqrt{L_r C_r})$ is resonant frequency. The operation principle of this mode is consistent with that of traditional FB-SRC. In this mode, switches $S_{1,\,3}$ and $S_{2,\,4}$ operate at 50% duty cycle, respectively, and switches $S_5 \sim S_6$ are always turned OFF, as shown in Fig. 4(b). Inductor L_{r1} and capacitor C_{r1} resonant during this each half of period. The absolute value of current i_{Lr1} increases first and then decreases to zero, and it remains zero until the next half switching period comes. The collector-to-emitter current of switches S_1 and S_3 (S_2 and S_4) are equal to the resonant current i_{Lr1} ($-i_{Lr1}$) when they are turned ON, which is zero at turn-ON moment t_0 (t_2) and turn-OFF moment t_1 (t_3). Therefore, ZCS operation is achieved for all IGBTs. Besides, from Fig. 4(b), secondary diode D_1 and D_2 are also ZCS turned OFF. Therefore, SRC working in half-cycle discontinuous-conduction-mode (HC-DCM) can realize ZCS operation for all power semiconductor devices. The power is transformed from the input V_i to the output V_o through diode D_1 and D_2 in each half period, and the average voltage V_{p1} and V_{cr1} are equal to zero in a switching period.

B. Mode 2: First Postfault Operation

1) Mode 2A: In this mode, SCF/OCF happens on one of switches $S_1 \sim S_4$. Taking switch S_3 as an example, the equivalent postfault circuit is shown in Fig. 5(a)$\sim$(b). In Fig. 5(a), switch S_3 is assumed to be ideal SCF, whose resistance is considered to be very small. For the faulty switches having large resistance in practice, additional relays can be added in parallel with switches to bypass the faulty switch. The additional relay is turned OFF when its parallel switch is healthy, and it is turned ON when the switch is SCF. In order to maintain the rated output voltage/power, switch S_4 in the same bridge with S_3 is turned OFF, and then the remaining healthy HB $S_{1,\,2}$ combines the redundant HB $S_{5,\,6}$ to reconstruct as an IPOS dual HB-SRC with the aid of secondary diode D_3 and D_4. Switches $S_{1,\,6}$ and $S_{2,\,5}$ are complementarily operated with 50% duty cycle, as shown in Fig. 5(a). On



(a)



(b)

Fig. 4. Equivalent circuit and key operating waveforms of the proposed converter in mode 1. (a) Equivalent circuit. (b) Waveforms.

the other hand, switch S_3 is assumed to be ideal OCF in Fig. 5(b), whose resistance is considered to be infinite. The postfault operation is the same as that of SCF, except for the drive signal of switch S_4 which should be always turned ON, as shown in Fig. 5(b). It is noteworthy that the secondary diode $D_{1,2}$ and output filter capacitor C_{o1} in original FB-SRC are all bypassed after the reconstruction of two HB-SRC.

2) Mode 2B: In this mode, SCF/OCF happens on diode D_1 or D_2. If a diode has OCF, the faulty diode would be isolated automatically. On the other hand, if a diode SCF occurs, the fuse in series would be melted, and then it also can be bypassed. According to mode 2A, the original diodes $D_{1,2}$ will not take part in operation after topology reconstruction, and hence the proposed converter can keep working by similarly reconstructing into an IPOS dual HB-SRC. Because all switches $S_1 \sim S_4$ are healthy in this mode, there are four possible modulation strategies that two switches in a leg is complementarily operated, while the remaining two switches in another leg is either ON or OFF. Fig. 5(c) depicts an example with S_3 always ON, S_4 always OFF, and $S_1 \sim S_2$ complementarily operated.

3) Mode 2C: In this mode, output filter capacitor C_{o1} is in SCF/OCF. When OCF occurs on C_{o1}, the faulty capacitor would be also isolated automatically. If its SCF occurs, the secondary windings of transformer T_1 will be shorted and the fuse $F_{1,2}$ would be consequently melted. Thus, the faulty output filter capacitor can also be bypassed. The operation of mode 2C is similar to that in mode 2B, and an example equivalent circuit in mode 2C is shown in Fig. 5(d).

C. Mode 3: Second Postfault Operation

Because four switches $S_1 \sim S_4$ in the original FB-SRC are all healthy during mode 2B or mode 2C, the proposed converter can continue uninterrupted operation even if a second fault happens on one of $S_1 \sim S_4$. Fig. 5(e)~(f) also shows two examples in mode 3 with SCF/OCF on S_3 after mode 2B and mode 2C. It is easy to know that the operation in this mode is the same as that of mode 2A due to the same equivalent circuits.

D. Operation Principle of Postfault Converter

From above, the proposed converter works as a typical FB-SRC in mode 1 when there is no fault. It will be reconstructed into an IPOS dual HB-SRC with the redundant HB-SRC to ensure continue operation, under first SCF/OCF of any switch $S_1 \sim S_4$, diode $D_1 \sim D_2$, or output filter capacitor C_{o1} in mode 2, and even under second SCF/OCF on switch $S_1 \sim S_4$ in mode 3 if they do not fail in mode 2. According to the postfault equivalent circuits in Fig. 5, in all modes 2 and 3, the reconstructed converter after fault is a same IPOS dual HB-SRC. The remaining healthy HB part and redundant HB part provide 50% of output power, respectively. Taking mode 2A as an example, the key operation waveforms of the IPOS dual HB-SRC working in HC-DCM are depicted in Fig. 6. A switching period includes four different states and their equivalent circuits are shown in Fig. 7.

State 1 [t_0, t_1]: Before t_0, $i_{Lr1,2}$ is zero. Hence, ZCS turn-ON of switches $S_{1,6}$ is achieved when they are turned ON at t_0. Then, inductors L_{r1} and L_{r2} resonate with capacitor C_{r1} and C_{r2}, respectively. Because the diode D_1 and D_2 are all reverse biased and relay R_{e1} is turned OFF, two secondary windings are connected in series. Thus, the resonant inductor current i_{Lr1} is equal to i_{Lr2}. Resonant capacitor voltage $v_{Cr1,2}$ increases in this state. From Fig. 7(a), the diode current $i_{D3} = n_1 i_{Lr1} = n_2 i_{Lr2}$ can be obtained. The current $i_{Lr1,2}$ and i_{D3} reaches zero at t_1. Thus, diode D_3 is ZCS turned OFF. The power transfers from input V_i to the output V_o and the resonant capacitors $C_{r1,2}$.

State 2 [t_1, t_2]: Diodes D_3 and D_4 are reverse biased during this state. Therefore, $i_{Lr1,2}$ remains zero until the next half switching period starts at t_2, when switches $S_{1,6}$ are turned OFF. Thus, switches $S_{1,6}$ are ZCS turned OFF. The resonant capacitor

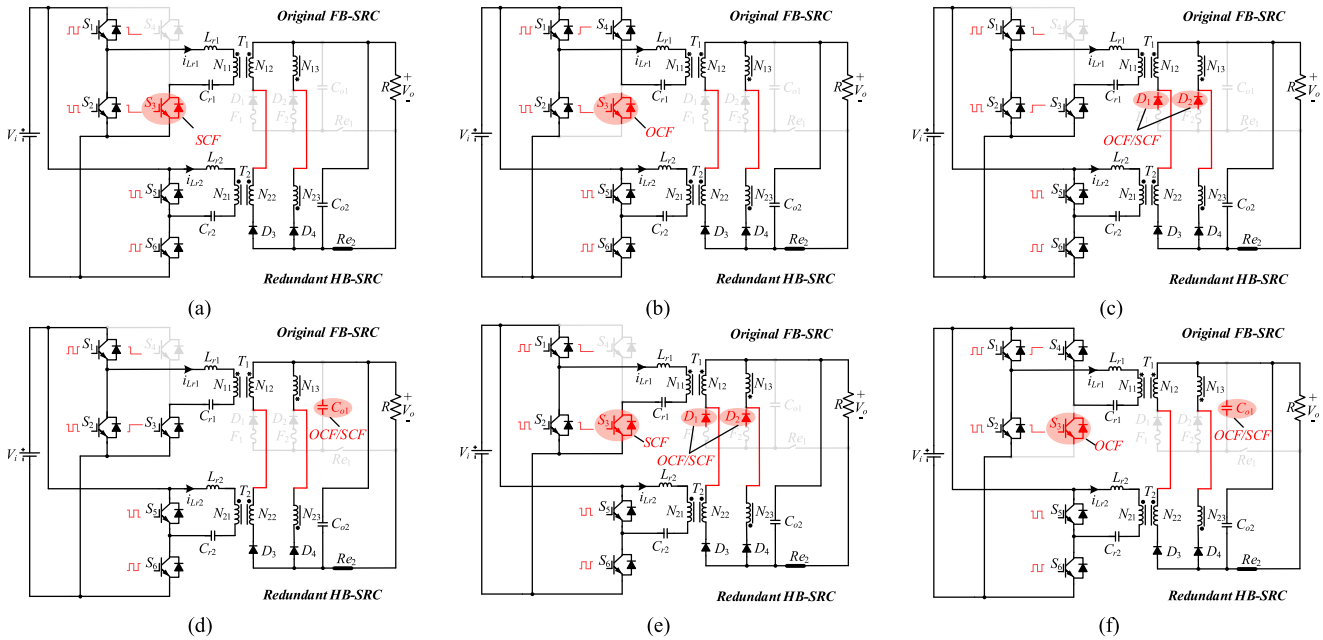


Fig. 5. Equivalent circuits of the proposed fault-tolerant SRC in Mode 2∼3. (a) SCF on S_3. (b) OCF on S_3. (c) OCF/SCF on $D_{1\text{-}2}$. (d) OCF/SCF on C_{o1}. (e) OCF/SCF on $D_{1\text{-}2}$ and SCF on S_3. (f) OCF/SCF on C_{o1} and OCF on S_3.

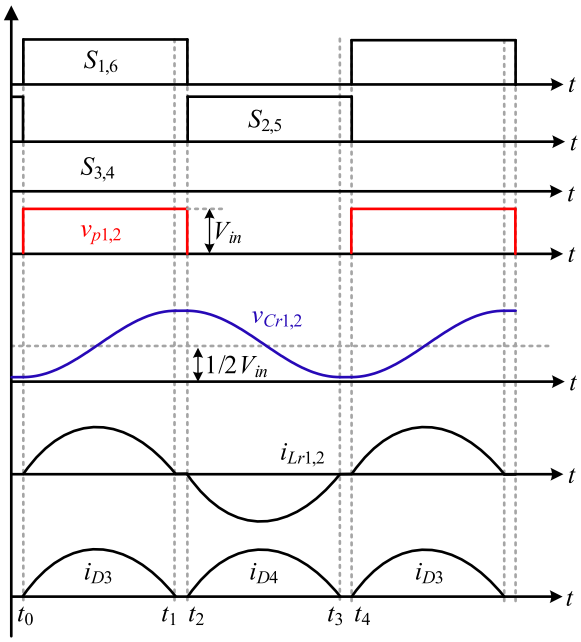


Fig. 6. Key operating waveforms of the proposed converter in mode 2A.

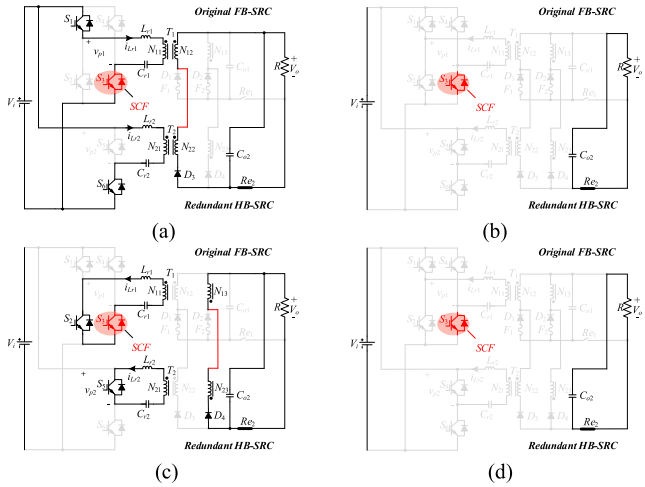


Fig. 7. Equivalent circuits of mode 2A at different states. (a) State 1: $[t_0, t_1]$. (b) State 2: $[t_1, t_2]$. (c) State 3: $[t_2, t_3]$. (d) State 4: $[t_3, t_4]$.

voltage $v_{Cr1,2}$ remains maximum and constant during this state. The output power is supplied by output filter capacitor C_{o2} in this state, as shown in Fig. 7(b).

State 3 [t_2, t_3]: At t_2, $i_{Lr1,2}$ is zero, and switches $S_{2,5}$ are turned ON. Hence, ZCS turn-ON of $S_{2,5}$ is achieved. Then, inductors L_{r1} and L_{r2} resonate with capacitor C_{r1} and C_{r2}, respectively. In this state, the resonant inductor current i_{Lr1} is equal to i_{Lr2}, and they are all negative. Resonant capacitor voltage $v_{Cr1,2}$ decreases in this state. From Fig. 7(c), the diode current $i_{D4} = -n_1 i_{Lr1} = -n_2 i_{Lr2}$ can be obtained. The current $i_{Lr1,2}$ and i_{D4} reaches zero at t_3. Thus, diode D_4 is ZCS turned OFF. The power transfers from the resonant capacitors $C_{r1,2}$ to the output V_o.

State 4 [t_3, t_4]: At this state, $i_{Lr1,2}$ remains zero until the next half switching period starts at t_4, when switches $S_{2,5}$ are turned OFF. Hence, switches $S_{2,5}$ are ZCS turned OFF. The resonant capacitor voltage $v_{Cr1,2}$ remains minimum and constant in this state. The output power is supplied by output filter capacitor C_{o2} in this state, as shown in Fig. 7(d).

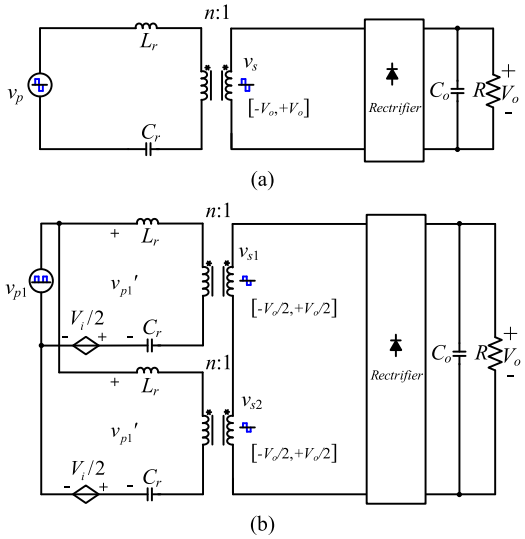


Fig. 8. Simplified circuit of the proposed SRC in different modes. (a) Mode 1. (b) Modes 2∼3.

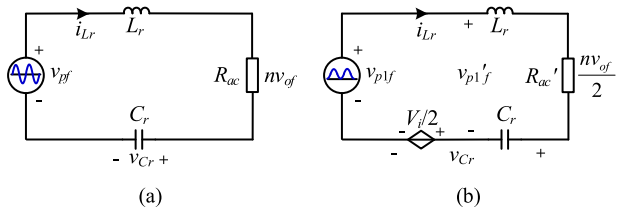


Fig. 9. Equivalent circuit of the proposed SRC in different modes. (a) Mode 1. (b) Modes 2∼3.

IV. Performance Analysis

In this section, the performance of the proposed fault-tolerant SRC including the voltage gain between output voltage and input voltage and the voltage/current stress of different components in different modes are analyzed and compared. To simplify the analysis, values of L_{r1}∼L_{r2}, C_{r1}∼C_{r2} and n_1∼n_2 are assumed to be identical, which are denoted as L_r, C_r, and n, respectively. The switching frequency f_s is close to resonant frequency f_r, so intervals $[t_1, t_2]$ and $[t_3, t_4]$ are ignored.

A. Voltage Gain

The simplified circuit of the proposed fault-tolerant SRC in different modes is shown in Fig. 8. In mode 1, the proposed fault-tolerant SRC is a typical FB-SRC. The input voltage $v_p(t)$ of resonant tank is a square wave with a peak-to-peak value of $\pm V_i$, and the secondary voltage $v_s(t)$ of transformer T_1 is also a square wave with a peak-to-peak value of $\pm V_o$, as illustrated in Fig. 8(a). Their Fourier series are expressed in (1) and (2), respectively.

Based on the first harmonic analysis (FHA) [23], the impedance of resonant tank composed of L_r and C_r is approximately zero when f_s is approximately equal to f_r

$$v_p(t) = \frac{4V_i}{\pi} \sum_{k=1,3,5,\ldots} \frac{1}{k} \sin(2k\pi f_r t) \tag{1}$$

$$v_s(t) = \frac{4V_o}{\pi} \sum_{k=1,3,5,\ldots} \frac{1}{k} \sin(2k\pi f_r t). \tag{2}$$

Hence, the fundamental component $v_{pf}(t)$ and $v_{sf}(t)$ of $v_p(t)$ and v_s(t) in (3) and (4) should satisfy $v_{pf}(t)/v_{sf}(t) = n$. Then, the voltage gain M between output voltage V_o and input voltage V_{in} is calculated in (5), which is equal to 1/n:

$$v_{pf}(t) = \frac{4V_i}{\pi} \sin(2\pi f_r t) \tag{3}$$

$$v_{sf}(t) = \frac{4V_o}{\pi} \sin(2\pi f_r t) \tag{4}$$

$$M = \frac{V_o}{V_i} = \frac{1}{n}. \tag{5}$$

In modes 2∼3, the converter can be equivalent to a dual HB-SRC. In each HB converter, the input voltage $v_{p1}(t)$ of the resonant tank is a square wave with minimum value 0 V and maximum value V_i, and the average voltages $v_{Cr1,2}$ of capacitors have V_i/2 dc bias, as illustrated in Fig. 8(a). Therefore, the equivalent input voltage $v_{p1'}$ of resonant tank is equal to a square wave with a peak-to-peak value of $\pm V_i$/2. On the other hand, as the secondary windings of two transformers T_1∼T_2 are connected in series, the secondary voltages v_{s1} and v_{s2} is a square wave with a peak-to-peak value of $\pm V_o$/2. Similarly, the fundamental components $v_{p1'f}$ and v_{s1f} of $v_{p1'}$ and v_{s1} are expressed in (6) and (7), and their ratio should be equal to n according to FHA. Therefore, the voltage gain between output voltage V_o and input voltage V_i in modes 2∼3 is also equal to 1/n, which is the same as mode 1:

$$v_{p1'f}(t) = \frac{2V_i}{\pi} \sin(2\pi f_r t) \tag{6}$$

$$v_{s1f}(t) = v_{s2f}(t) = \frac{2V_o}{\pi} \sin(2\pi f_r t). \tag{7}$$

B. Voltage/Current Stress

According to Fig. 8, the equivalent resonant circuit in three modes are further shown in Fig. 9, where $R_{\rm ac} = 8n^2R/\pi^2$ and $R'_{\rm ac} = 4n^2R/\pi^2$ are the equivalent output resistance in modes 1 and 2∼3. With these equivalent circuits, the resonant inductor current i_{Lr} during mode 1∼3 is calculated in (8), which are equal. From (8), the resonant capacitor voltages v_{Cr} in different modes can also be obtained, as shown in (9). It is verified that the resonant capacitor $C_{r1,2}$ will superimpose a V_i/2 dc bias voltage in modes 2∼3 in comparison with mode 1

$$i_{Lr}(t) = \frac{v_{pf}}{R_{\rm ac}} = \frac{v_{p1'f}}{R_{\rm ac'}} = \frac{4V_i}{\pi R_{\rm ac}} \sin(2\pi f_r t) \tag{8}$$

$$v_{Cr}(t) = \begin{cases} -\frac{8V_i f_r L_r}{R_{\rm ac}} \cos(2\pi f_r t) & \text{mode } 1 \\ \frac{V_i}{2} - \frac{8V_i f_r L_r}{R_{\rm ac}} \cos(2\pi f_r t) & \text{mode } 2,3. \end{cases} \tag{9}$$

According to (8), the root-mean-square (rms) value $I_{Lr,\rm rms}$ of resonant inductor during mode 1∼3 is calculated in (10). Because the collector-to-emitter current of switches $S_{1\text{–}6}$ are equal to the resonant current in each half period, the rms value

$I_{s,\mathrm{rms}}$ of collector-to-emitter current in three modes is depicted in (11). From Figs. 4(a) and 5, the average current of each secondary diode $I_{D,\mathrm{ave}}$ is equal to half of the output load current I_o. Therefore, the average current of each diode is calculated in (12):

$$I_{Lr,\mathrm{rms}} = \frac{2\sqrt{2}V_i}{\pi R_{\mathrm{ac}}} \tag{10}$$

$$I_{s,\mathrm{rms}} = \frac{2V_i}{\pi R_{\mathrm{ac}}} \tag{11}$$

$$I_{D,\mathrm{ave}} = \frac{V_o}{2R}. \tag{12}$$

In addition, no matter working in modes 1, 2 or 3, the turn-OFF voltage of switches is clamped by the input voltage V_i, and voltage stresses of all diodes $D_1 \sim D_4$ are equal to $2V_o$.

As a summary, the voltage/current stresses of all components remain unchanged before and after the fault except the voltage of resonant capacitor. In practical applications, a capacitor array with multiple capacitors in series and parallel is adopted as the resonant capacitor with large voltage margin, and hence it will not cause additional problem. Therefore, the design of the proposed converter is simple, since it is similar to that of the typical SRC which is already mature.

C. Further Extension

From above analysis, the proposed fault-tolerant FB-SRC can keep working normally after SCF/OCF on switches, diodes, and output capacitor with only a backup of HB-SRC, and the voltage/current stresses of most components remain unchanged after fault. Therefore, the proposed fault-tolerant SRC can achieve high reliability at a low cost. Moreover, the proposed fault-tolerant scheme is not limited to the SRC, but also can be employed in other relevant converters, e.g., FB-LLC converter. FB-LLC converter is another famous resonant converter with soft-switching characteristics. The magnetizing inductor is additionally adopted in the resonant tank of FB-LLC converter than FB-SRC, and it can realize ZVS operation of primary switches. From the view of structure, except for the resonant tank, the connections of switches, diodes, and capacitors are basically the same in FB-LLC converter and FB-SRC. Thus, the proposed fault-tolerant scheme can also be applied in the FB-LLC converter, as illustrated in Fig. 10.

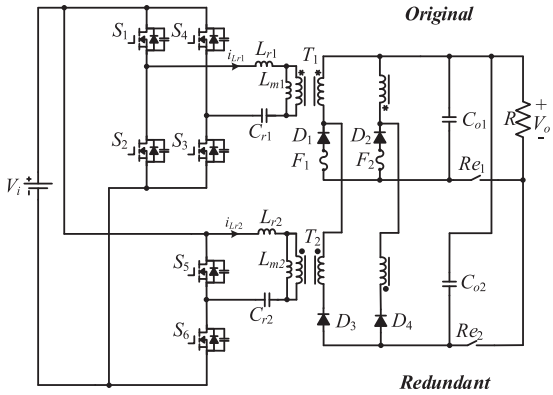


Fig. 10. Extension to fault-tolerant LLC converter.

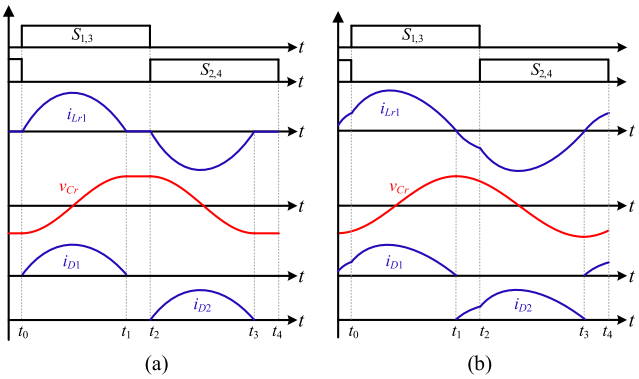


Fig. 11. Key waveforms of SRC working in HC-DCM and CCM. (a) HC-DCM. (b) CCM.

V. Design Considerations

In order to achieve ZCS operation of all switches in the proposed fault-tolerant converter during both prefault and postfault conditions, the parameters of resonant tank should be well designed. In addition, the corresponding drive signals of switches $S_{1\text{–}6}$ in different modes are also summarized in this section. Last, the fault detection methods of all fragile components are introduced in detail.

A. Resonant Tank Design

The proposed fault-tolerant SRC is expected to work in HC-DCM as shown in Fig. 11(a), to achieve ZCS operation for all switches to reduce switching losses. However, if the resonant tank is not well designed, it will work in continuous-conduction-mode (CCM), as illustrated in Fig. 11(b). From Fig. 11, the inductor current i_{Lr1} increases first and then decreases to zero during $[t_0, t_1]$ in both HC-DCM and CCM. It remains zero during $[t_1, t_2]$ in HC-DCM, but it will continue decreasing to be negative in CCM. As a result, high spike turn-OFF voltage of switches will be caused by the reverse recovery of the parallel diode and thus undesired hard-switching operation of switches will happen at t_2 in CCM.

According to the operation principle of typical FB-SRC, whether it works in HC-DCM or CCM depends on the capacitor voltage $v_{Cr1}(t_1)$ at t_1. As shown in Fig. 12(a), if $v_{Cr1}(t_1)$ is greater than the input voltage V_i plus the primary voltage nV_o of the transformer T_1, diode D_2 will conduct at t_1 and the inductor current i_{Lr1} will keep decreasing. Then, the typical FB-SRC will operate in CCM and i_{Lr1} flows through the diodes of $S_{1,3}$ during $[t_1, t_2]$. Consequently, switches are hard-switching at t_2. Therefore, in order to achieve ZCS operation for switches in typical FB-SRC, $v_{Cr1}(t_1)$ needs to be smaller than $V_i + nV_o$, so that diodes $D_{1,2}$ are both reverse biased and i_{Lr1} remains zero during $[t_1, t_2]$, as illustrated in Fig. 12(b). On the other hand, the proposed converter is reconstructed into an IPOS dual HB-SRC after fault, and $v_{Cr1}(t_1)$ should be smaller than $V_i + nV_o/2$ to similarly achieve ZCS operation for switches.

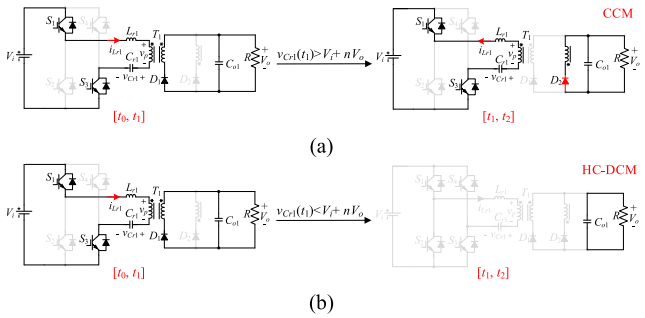


Fig. 12. Equivalent circuits of FB-SRC operating in CCM and HC-DCM during $[t_0, t_2]$. (a) CCM. (b) HC-DCM.

Finally, combining with (9), the design criterions of L_r/C_r in modes 1∼3 are calculated in (13). From (13), in order to achieve ZCS operation for the proposed converter in both prefault and postfault conditions, L_r/C_r should be less than $\pi^2 R_{\rm ac}^2/16$

$$\begin{cases} \frac{L_r}{C_r} < \frac{\pi^2 {R_{\rm ac}}^2}{16} & \text{mode } 1 \\ \frac{L_r}{C_r} < \frac{\pi^2 {R_{\rm ac}}^2}{4} & \text{modes } 2, 3. \end{cases} \tag{13}$$

B. Drive Signals Generation

On the basis of the operation process in Section III, the operation can be divided into three modes (modes 1, 2, and 3). In mode 1, all components are healthy. There are three submodes 2A, 2B, and 2C in mode 2, which, respectively, correspond to the fault of switch, diode, and output filter capacitor. Mode 2A can also be further divided according to the fault of four switches S_{1-4}, namely, mode 2Aa, 2Ab, 2Ac, and 2Ad. Similarly, mode 3 can be classified into four submodes 3a, 3b, 3c, and 3d according to the fault of four switches S_{1-4}. Drive signals of switches S_{1-6} during different modes are depicted in Table I, where 1 is high-level drive signal and 0 is low-level drive signal. And D_{RA} and D_{RB} are complementary drive signals. In mode 1, switches $S_{1,3}$ and switches $S_{2,4}$ in original converter work with complementary drive signals D_{RA} and D_{RB} to supply the power from input to the output, and switches $S_{5,6}$ are all turned OFF. In mode 2Ac with SCF on S_3, switch S_4 is shut down, and drive signal DR_A and DR_B are distributed to switches $S_{1,6}$ and switches $S_{2,5}$, respectively. Likewise, the driving signal of mode 2Aa, mode 2Ab, and mode 2Ad are shown in Table I. In modes 2B and 2C, there are four feasible types of drive signals for choosing. The drive signals of modes 3a–3d are consistent with modes 2Aa–2Ad, respectively, as also shown in Table I.

C. Fault Detection

The conventional fault detection method with voltage/current measurement can be simply employed in the proposed converter.

Switches SCF/OCF: As shown in Fig. 13, the input current $i_{\rm in}$ and the mid-point voltage $V_{1,2}$ of each arm are measured to monitor the SCF/OCF of each switch. For example, if S_3 is SCF when switches $S_{2,4}$ are ON, the input current $i_{\rm in}$ will increase rapidly and the voltage V_2 will decrease from V_i to $R_{\rm SCF}/(R_{\rm SCF}$ $+ R_{\rm ON})\times V_{\rm in}$ ($R_{\rm ON}$ is the ON-resistance and $R_{\rm SCF}$ is the SCF resistance of switch). In addition, if S_3 is OCF when switches $S_{1,3}$ are ON, the parasitic capacitor of S_3 will be charged and thus V_2 will increase. Consequently, by monitoring $i_{\rm in}$ and V_2, the SCF and OCF of switch S_3 can be quickly detected within one switching period. Similarly, the fault detection of other switches can also be effectively implemented, as summarized in Table II.

Diode SCF/OCF: As shown in Fig. 13, the OCF of diode $D_{1,2}$ can be monitored by the voltage V_3 between two cathodes of diodes D_1 and D_2, which is equal to $2(V_{D1}-V_o)$. Taking diode D_1 as example, in prefault mode, the minimum value of V_{D1} is zero when it conducts, and hence the minimum value of V_3 is $-2V_o$. If D_1 is OCF, the minimum value of V_{D1} will be less than zero, thus V_3 will be accordingly smaller than $-2V_o$. Likewise, if another

TABLE I
DRIVE SIGNALS OF SWITCHES S_{1-6} IN THREE MODES

Mode	Fault type	S_1	S_2	S_3	S_4	S_5	S_6
1	NO	DR_A	DR_B	DR_A	DR_B	0	0
2Aa	SCF	0	0	DR_A	DR_B	DR_B	DR_A
	OCF	0	1	DR_A	DR_B	DR_B	DR_A
2Ab	SCF	0	0	DR_A	DR_B	DR_B	DR_A
	OCF	1	0	DR_A	DR_B	DR_B	DR_A
2Ac	SCF	DR_A	DR_B	0	0	DR_B	DR_A
	OCF	DR_A	DR_B	0	1	DR_B	DR_A
2Ad	SCF	DR_A	DR_B	0	0	DR_B	DR_A
	OCF	DR_A	DR_B	1	0	DR_B	DR_A
2B,2C	SCF/OCF	1	0	DR_A	DR_B	DR_B	DR_A
		0	1	DR_A	DR_B	DR_B	DR_A
		DR_A	DR_B	1	0	DR_B	DR_A
		DR_A	DR_B	0	1	DR_B	DR_A
3a	SCF	0	0	DR_A	DR_B	DR_B	DR_A
	OCF	0	1	DR_A	DR_B	DR_B	DR_A
3b	SCF	0	0	DR_A	DR_B	DR_B	DR_A
	OCF	1	0	DR_A	DR_B	DR_B	DR_A
3c	SCF	DR_A	DR_B	0	0	DR_B	DR_A
	OCF	DR_A	DR_B	0	1	DR_B	DR_A
3d	SCF	DR_A	DR_B	0	0	DR_B	DR_A
	OCF	DR_A	DR_B	1	0	DR_B	DR_A

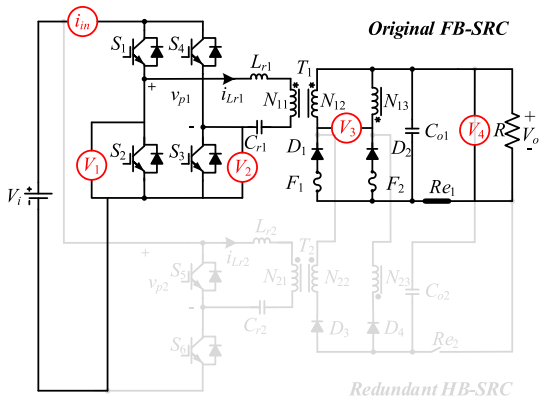


Fig. 13. Fault detection with voltage/current measurement.

TABLE II
SCF/OCF DETECTION OF SWITCHES $S_{1\sim4}$, DIODES $D_{1,2}$, AND CAPACITOR Co_1 WITH THE MEASUREMENT OF CURRENT I_{IN} AND VOLTAGE $V_1\sim V_3$

	i_{in} rapidly increase to undesired high level		-------				
$S_{2,4}$ are on	SCF of S_1: V_1 increases	SCF of S_3: V_2 decreases	OCF of S_2: V_1 increases	OCF of S_4: V_2 decreases	OCF of D_2: V_3 increase	SCF of C_{o1}: V_4=0	OCF of C_{o1}: The ripple of V_4 increase
$S_{1,3}$ are on	SCF of S_2: V_1 decreases	SCF of S_4: V_2 increases	OCF of S_1: V_1 decreases	OCF of S_3: V_2 increases	OCF of D_1: V_3 decrease		

TABLE III
SYSTEM PARAMETERS

Input voltage	V_{in}=270V	Output voltage	V_{out}=28V
Rated power	P_{out}=500W	Switching frequency	f_s=17kHz
Resonant inductances	L_{r1}=L_{r2}=288μH	Resonant capacitances	C_{r1}=C_{r2}= 220nF
Turns ratio	n:1:1=45:5:5	Output capacitance	C_o=4000μF
Switches $S_{1\text{-}6}$	IKA15N65ET6XKSA2	Diodes $D_{1\text{-}4}$	MBR30100CT

diode D_2 is OCF, the maximum value of V_3 will increase to be larger than the normal value $2V_o$. Therefore, the OCF of diodes $D_{1,2}$ can be effectively detected with voltage measurement V_3, which are summarized in Table II. On the other hand, if SCF occurs on a diode, the fuse in series would be melted, and then the SCF would be converted into OCF.

Output Capacitor SCF/OCF: As shown in Fig. 13, the output capacitor voltage V_4 is employed to monitor the SCF/OCF of output capacitor C_{o1}. If it is SCF, the voltage V_4 would be decrease from V_o to 0. If it is OCF, the ripple voltage of V_4 would increase, as summarized in Table II.

VI. EXPERIMENT RESULTS

In order to verify the effectiveness of the proposed fault-tolerant SRC, a 500-W prototype with input voltage 270 V and output voltage 28 V is designed and built. In addition, the loss in the proposed converter is analyzed.

A. Experimental Setup

The switching frequency is set to 17 kHz because the switches are IGBTs. In order to achieve ZCS operation for the proposed converter, the resonant frequency should be greater than switching frequency, and the parameters of resonant inductor and resonant capacitor should be satisfied $L_r/C_r < \pi^2 {R_{\rm ac}}^2/16$. After calculation, choose 20 kHz as the resonant frequency, and the resonant inductor and resonant capacitor parameters are 288 μH and 220 nF, respectively. Considering the loss of the whole converter, the turns ratio 45:5:5 is employed. IGBT IKA15N65ET6XKSA2 and diode MBR30100CT are chosen. All system parameters are summarized in Table III. In addition, the input source of prototype employs a dc power supply EA-PS9750-06 from Elektro-Automatik, and a dc electronic load IT8816 from ITECH is used as the load.

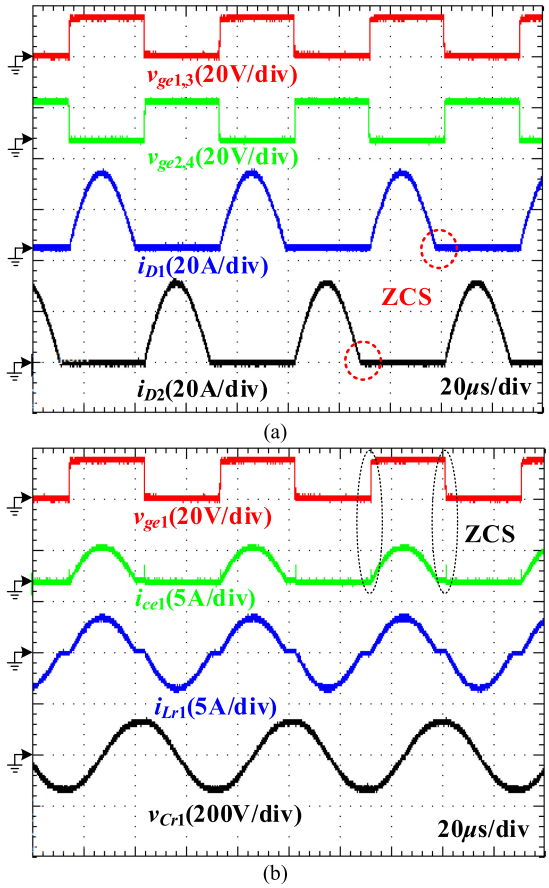


Fig. 14. Steady-state waveforms in mode 1. (a) $v_{ge1,3}$, $v_{ge2,4}$, i_{D1}, i_{D2}. (b) v_{ge1}, $i_{\rm ce1}$, i_{Lr1}, v_{Cr1}.

The steady-state experiments of mode 1 and mode 2Ac are carried out. Moreover, mode transition process experiments including mode 1 to mode 2Ac (S_3 SCF), mode 2b (D_1 OCF), and mode 3c (S_3 SCF and D_1 OCF) were also done. In the experiment, the SCF of switch is emulated by locking the corresponding drive signal at high level, and the OCF of diode is emulated by turning OFF the auxiliary switch connected in series with the diode. All control signals are generated by TMS320F2808.

B. Steady State

The steady-state waveforms of mode 1 with normal operation and mode 2Ac with SCF on S_3 are depicted in Figs. 14 and 15, respectively, which shows that the proposed converter works well in both two modes.

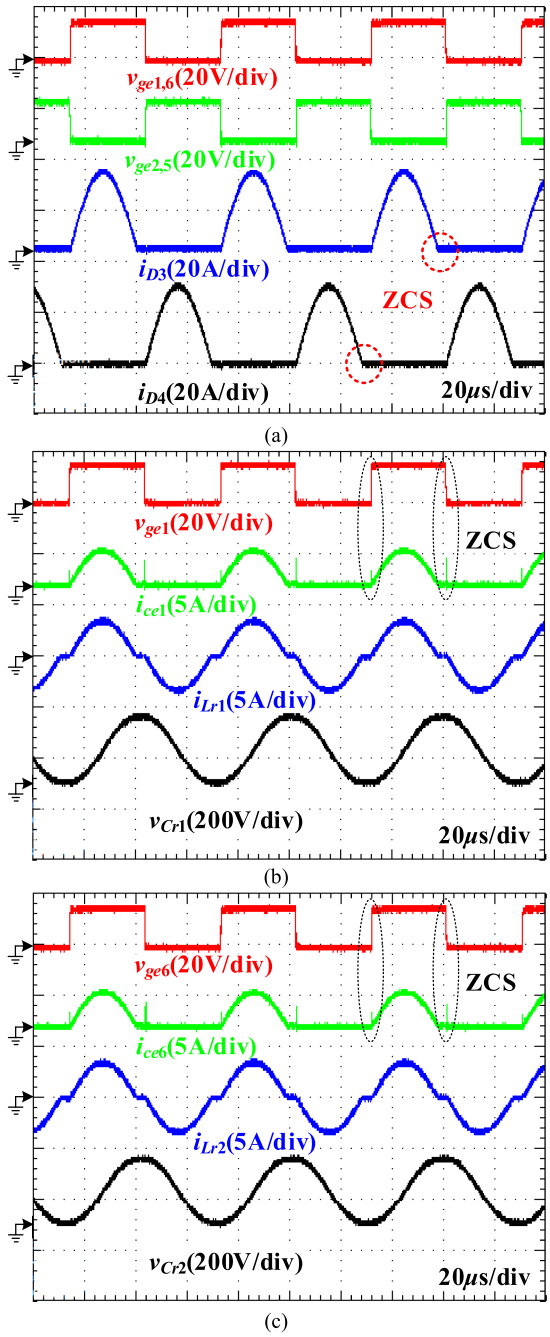


Fig. 15. Steady-state waveforms in mode 2Ac with SCF on S_3. (a) $v_{ge1,6}$, $v_{ge2,5}$, i_{D3}, i_{D4}. (b) v_{ge1}, i_{ce1}, i_{Lr1}, v_{Cr1}. (c) v_{ge6}, i_{ce6}, i_{Lr2}, v_{Cr2}.

As shown in Fig. 14, drive signals $v_{ge1,3}$ of switches $S_{1,3}$ and $v_{ge2,4}$ of switches $S_{2,4}$ are complementary with 50% duty cycle. The resonant inductor current i_{Lr1} and the resonant capacitor voltage v_{Cr1} are approximately sinusoidal with $\pi/2$ phase-shift angle, with the neglect of the short interval of $i_{Lr1} = 0$. At secondary side, diodes D_1 and D_2 are forward biased in each half switching period. Hence, in mode 1, the inductor L_{r1} and capacitor C_{r1} resonate to transfer power from the input to the output through secondary diodes D_1 and D_2. At both turn-ON and turn-OFF of S_1, the collector-to-emitter current i_{ce1} is zero. Therefore, ZCS operation is achieved for switches. Besides, secondary diodes D_1 and D_2 are also ZCS.

As the postfault circuit is the same after SCF/OCF occurs on switches, diode, and the output filter capacitor, the postfault operation of SCF on switch S_3 is depicted as an example. Fig. 15 shows the steady-state waveforms of mode 2Ac with SCF on S_3. In mode 2Ac, the remaining healthy HB $S_{1,2}$ and the redundant HB $S_{5,6}$ work together to reconstruct an IPOS dual HB-SRC. At parallel-connected primary side, the resonant inductor current i_{Lr1} remains almost unchanged, and the resonant inductor current i_{Lr2} is similar to i_{Lr1}. On the other hand, diodes $D_{3,4}$ other than $D_{1,2}$ conduct alternatively in each half switching period, so that the secondary windings of two transformers are connected in series. From Figs. 14 and 15, key waveforms of mode 2Ac are almost the same as mode 1. Hence, ZCS operation is also achieved for switches and diodes in mode 2Ac. The main difference lies in the resonant capacitor voltage $v_{Cr1,2}$ which has $V_i/2$ dc bias. It is also in well coincidence with the theoretical analysis.

As the number of active switches and diodes are the same, and the voltage/current stresses of all components remain almost unchanged in prefault and postfault conditions, the semiconductor conduction loss and other loss are very near in prefault and postfault conditions, which are 32.06 and 34.12 W, respectively. Their difference mainly lies in the winding conduction loss because one transformer works in prefault mode, and two transformers work simultaneously in postfault mode, which are 7.94 and 15.88 W, respectively. In summary, the sum of losses in postfault mode is slightly greater than that in prefault mode, but they are close.

C. Transition Process

Figs. 16–18 show the transition process from prefault mode to three postfault modes. Before all faults occurrence, the original converter (v_{ge1}) works while the redundant converter (v_{ge6}) is shut down in prefault mode.

As shown in Fig. 16, after SCF occurs on switch S_3, the drive signal of S_1 remains the same, and the drive signal of S_6 is set to be the same as S_1 in mode 2Ac. The redundant HB-SRC and remaining healthy HB-SRC works together to reconstruct an IPOS dual HB-SRC. From Fig. 16, it is further verified that the current i_{Lr1} of inductor L_{r1} remains almost the same after failure, and the voltage v_{Cr1} of capacitor C_{r1} has $V_i/2$ dc bias because the input voltage of resonant tank v_p changes from a square wave with $[-V_i, V_i]$ to $[0, V_i]$.

Fig. 17 shows the transition process from mode 1 to mode 2B with OCF on D_1. After OCF occurs on diode D_1, the drive signal of S_1 remains the same, and the drive signal of S_6 is set to be the same as S_1 in mode 2B. After failure, diode current i_{D1} drops to 0, and diode voltage changes from a square wave with $[0, 2V_o]$ to $[V_o/2, 3V_o/2]$ because the voltage of secondary winding is half reduced after the fault.

Fig. 18 shows the transition process from mode 1 to mode 3c with OCF on D_1 and SCF on S_3. After D_1 OCF and S_3 SCF, the converter turns to work in mode 3c. The drive signal of S_1 remains unchanged, the drive signal of S_6 is set to be the same

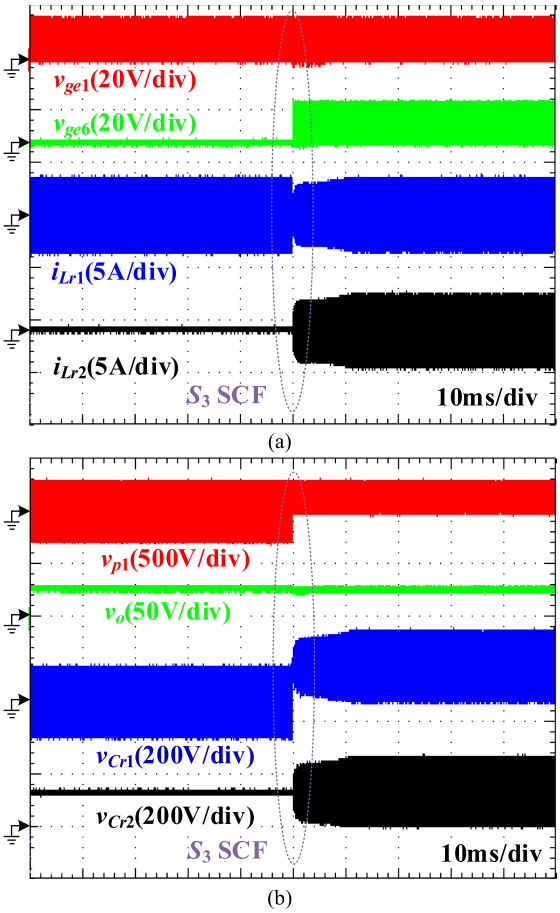


Fig. 16. Transition process from mode 1 to mode 2Ac with SCF on S_3. (a) v_{ge1}, v_{ge6}, i_{Lr1}, i_{Lr2}. (b) v_{p1}, v_o, v_{Cr1}, v_{Cr2}.

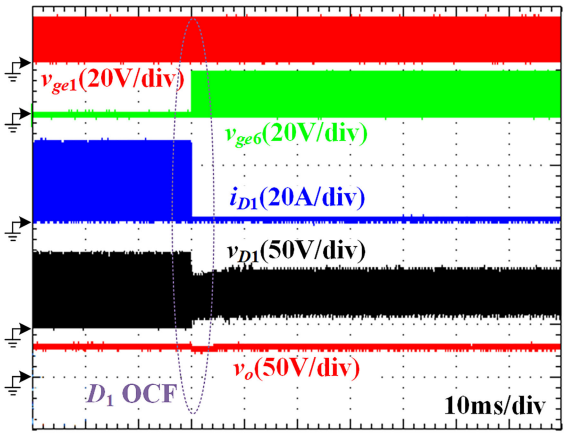


Fig. 17. Transition process from mode 1 to mode 2B with OCF on D_1.

as S_1, and the drive signal of switch S_3 is set at high level. After failure, the current i_{D1} of diode D_1 drops to 0.

During the transition process, switching frequency is temporarily increased to suppress the possible spike voltage/current of capacitor/inductor, and there is no spike of i_{Lr1} and v_{Cr1}, as shown in Fig. 16. The recovery time in transition process is about 12 ms and the output voltage drop is about 3 V. Therefore,

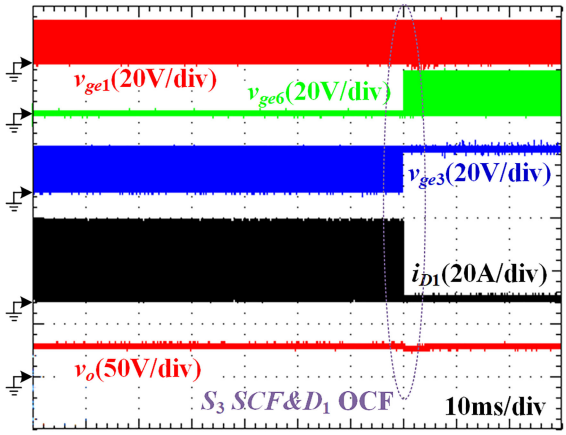


Fig. 18. Transition process from mode 1 to mode 3c with OCF on D_1 and SCF on S_3.

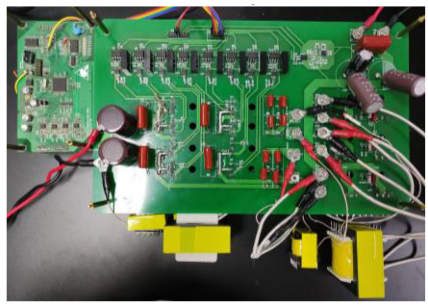


Fig. 19. Photograph of the prototype circuit.

the proposed fault-tolerant SRC can also smoothly transit from prefault mode to postfault mode. Finally, photograph of the prototype circuit is depicted in Fig. 19.

VII. Conclusion

A novel fault-tolerant SRC was proposed in this article, which can keep working normally after the SCF/OCF of all fault-prone components. The operational mode, performance characteristics, and design considerations were systematically analyzed, and a 500-W prototype was built to validate the effectiveness of the converter. According to theoretical analysis and experimental results, the proposed fault-tolerant SRC has the following advantages.

1) It can maintain normal operation when SCF/OCF happens on switches, diodes, or the output capacitor, which has higher stability than the switch-level redundancy.
2) Only a redundant HB-SRC is needed, which reduces the cost and volume compared to module-level redundancy.
3) The voltage/current stresses of almost all components remain unchanged before and after the fault, which helps to simplify the circuit design.
4) The proposed fault-tolerant scheme is not limited to the SRC, and it is also effective for other dc–dc converters, such as FB-LLC converter.

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