Letters

Series-Resonator Buck Converter—Viability Demonstration

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***Abstract*—The series-capacitor buck converter doubles the duty ratio, and equalizes the current between two phases. A series-resonator buck converter is realized by adding a resonant tank in series with the series capacitor C_s. All switches turn ON at zero voltage, and the low-side switches turn OFF at zero current. The resonant tank generates additional loss and increases the voltage stress of the low-side switches. A 2-MHz prototype with a peak efficiency of 98.5%, 48 V at the input and 7 V, 20 A at the output was built to demonstrate the viability of the topology.**

***Index Terms*—Multiphase converter, resonant converter, series-capacitor buck (SCB) converter, soft switching.**

I. Introduction

INTERLEAVED multiphase buck converters have been adopted for point-of-load regulation below 3.3 V and above 10 A from input voltage exceeding 12 V [1]–[13]. The series-capacitor buck (SCB) converter was synthesized by adding a series capacitor in a two-phase buck converter to reduce voltage stresses under the steady state [1], [2]. Side benefits include doubling the duty cycle, reduction of the switching loss, and equalization of the phase currents. Hard switching has hindered efforts to reduce volume via increased switching frequency although a monolithically integrated SCB converter has boosted current density exceeding 60 A/cm^3 in [3]. The switching loss caused the efficiency dropped by 5% as the frequency increased from 1 to 3 MHz in [4]. Coupled inductors, tapped inductors, and resonant tanks were suggested in [5]–[11] to enable soft switching, but switch voltage stresses exceeded 1.6 times the input unless snubbers or extra switches were added.

A series-resonator buck (SRB) converter with soft turn-ON is synthesized by adding a resonant tank in series with the series-capacitor C_s in Fig. 1(a). The gate signals are shown in Fig. 1(b). All switches turn ON at zero voltage (ZVOn), and the low-side switches turn OFF at zero current (ZCOff) in Fig. 1(c) with specifications in Table I and switches' output capacitance

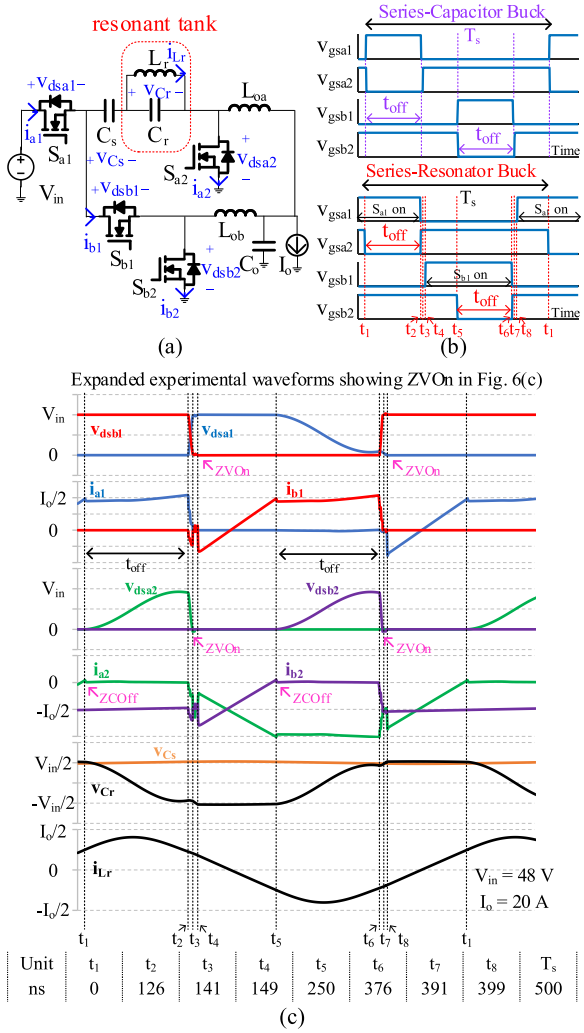

Fig. 1. (a) SRB converter. (b) Comparison of the gate signals for the SCB and SRB converters' high-side and low-side switches. (c) Switches' voltages and currents in the SRB converter.

$C_{oss} = 300$ pF. No snubber is needed to limit the voltage stresses to the input voltage.

The SRB was first described in [12]. Tu *et al.* [12] assume ideal switches, fixed load, and fixed switching frequency. In this letter, the switches' output capacitances are included so that soft-switching operation over a wide load range could be addressed, and a method to control switching frequency range

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TABLE I
SPECIFICATIONS FOR THE PROOF-OF-CONCEPT SRB PROTOTYPE

Specified Parameters	Definitions	Value
V_{in}	Input voltage	48 V
V_o	Output voltage	7 V
I_{oMax}	Maximum output current	20 A
I_{oMin}	Minimum output current	5 A
F_{sMin}	Minimum f_s at 100% I_{oMax}	2 MHz
F_{sMax}	Maximum f_s at 25% I_{oMax}	3 MHz

TABLE II
SEQUENTIAL DESIGN PROCEDURES OF THE SRB CONVERTER IN Fig. 1(a), WITH NUMERICAL EXAMPLES BASED ON TABLE I

Designed Parameter	Methods	Value
L_{oA} and L_{oB}	To keep peak-to-peak current ripple at 20% I_{oMax} [13]	1.2 μH
R_n	Suggested by Fig. 3(b) to minimize E_{tank} (5)	0.1
C_n	According to Fig. 4 for the specified F_{sMax}/F_{sMin}	50
f_r	$f_r = F_{r@V_o}(C_n, R_n)$ from step 1	3.75MHz
L_r	$L_r = V_o/I_{oMax}(2\pi f_r R_n)$ by (2), (3)	150 nH
C_r	$C_r = 1/L_r/(2\pi f_r)^2$ by (2)	12 nF
C_s	$C_s = C_n * C_r$ by (4)	600 nF

by C_s design is reported. Circuit operations, voltage regulation, and component stresses are revisited ahead.

II. OPERATION

The L_r–C_r tank in Fig. 1(a) generates the resonant voltage $v_{\rm Cr}$ that opens up the opportunity for the drain-to-source voltage $v_{\rm dsa1}$ and $v_{\rm dsb1}$ reach zero for ZVOn of $S_{\rm a1}$ at t_8 and $S_{\rm b1}$ at t_4 in Fig. 1(c). A voltage sensor monitors the drain–source voltage $v_{\rm dsa1}$ and $v_{\rm dsb1}$ for zero-crossing points at which the switches are turned ON for minimizing device loss and EMI. The L_r–C_r tank also adds the resonant current $i_{\rm Cs}$ to $i_{\rm a2}$ ($i_{\rm b2}$), which can now reach zero for ZCOff of $S_{\rm a2}$ ($S_{\rm b2}$) at t_1 (t_5). The low-side switches function as synchronous rectifiers.

The gate signals for the SCB and SRB converters are compared in Fig. 1(b) to identify a unified variable for output regulation. The waveforms of the gate to source voltage $V_{\rm gsa2}$ and $V_{\rm gsb2}$ of the low-side switches are identical, whereas those of the high-side switches are not. Their OFF-time ($t_{\rm off}$) is, thus, recommended as the unified regulating variable. Simulation suggests that $t_{\rm off}$ is linearly proportional to the SRB's voltage gain. Compared to an ideal switch model, the new simulation with $C_{\rm oss} = 300$ pF shows the output voltage increases by 10% with the same $t_{\rm off}$. It suggests the parasitic capacitance slows down the turn-ON transition of the low-side switches and, thus, $t_{\rm off}$ needs to be tuned smaller after adding $C_{\rm oss}$. Taking the converter in Tables I and II as an example, voltage gain is 0.146, 0.110, and 0.075 with $t_{\rm off}$ equals 126 ns, 113 ns, and 100 ns, respectively. The relationship between the voltage gain, regulating variable, and state variables in the presence of resonance and soft switching will be delivered in a full-length paper.

In both converters, there is a 180° phase shift between the gate signals for phases A and B. In each phase, there is no ON-signal overlap between the high-side and low-side switches in the SCB converter, but it is not the case for the SRB converter because the high-side switches are turned ON earlier for a smaller conduction loss.

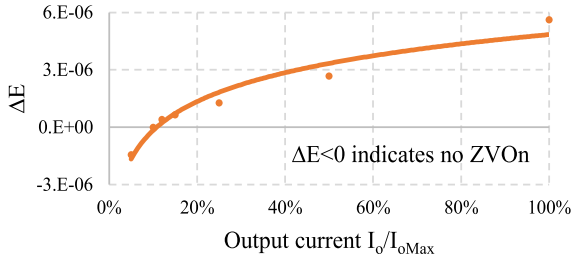

Fig. 2. Soft-switching region of $S_{\rm a1}$ and $S_{\rm b1}$ in Fig. 1(a) with parameters in Tables I and II and $C_{\rm oss} = 300$ pF (same device in the prototype).

The ZVOn region of the high-side switches in the SRB accounts for about 90% of the load range. The size of the hard-switching region depends on the circulating energy reserved in the resonant inductor before $S_{\rm b1}$ ($S_{\rm a1}$) is turned ON at $t_3(t_7)$. Take $S_{\rm b1}$ as an example. The energy available for soft switching in L_r at t_3 is $\frac{1}{2}L_r i_{Lr}(t_3)^2$. The energy required by $S_{\rm b1}$ for ZVOn is $\frac{1}{2}(C_r + 2C_{\rm oss})((\frac{V_{\rm in}}{2})^2 - v_{\rm Cr}(t_3)^2)$. The energy supplied by L_r should be larger than needed

$$\Delta E = \frac{1}{2} L_r i_{Lr}(t_3)^2 - \frac{1}{2}(C_r + 2C_{\rm oss})\left(\left(\frac{V_{\rm in}}{2}\right)^2 - v_{Cr}(t_3)^2\right) > 0. \quad (1)$$

A smaller load makes $i_{\rm Lr}(t_3)$, $v_{\rm Cr}(t_3)$ and, thus, ΔE smaller in Fig. 2. Under heavy load condition, ΔE is well above zero meaning achieving ZVOn is easy. The energy difference ΔE turns negative below 10% load condition meaning ZVOn is lost.

III. NUMERICAL DESIGN PROCEDURES

The converter in Fig. 1(a) was simulated parametrically to understand its operation, e.g., the relationships among the timing variables and component values on the voltage gain, soft switching, and components' stresses over a prescribed load range. The design procedures distilled from numerical observations are outlined in the first two columns of Table II. The last column in Table II lists the resultant values for the prototype meeting the exemplary specifications in Table I. The resonant frequency f_r, the normalized load resistance R_n, and the capacitor ratio C_n are defined as

$$f_r = 1/\left(2\pi\sqrt{L_r C_r}\right) \quad (2)$$

$$R_n = V_o / \left(I_{oMax}\sqrt{L_r/C_r}\right) \quad (3)$$

$$C_n = C_s / C_r. \quad (4)$$

Step 1: Select R_n using Fig. 3 to minimize tank energy. The normalized tank energy $E_{\rm tank}$ of the resonant tank is calculated:

$$E_{\rm tank} = \left(L_r {I_{LrPk}}^2 + C_r {V_{CrPk}}^2\right) f_r / \left(2V_o I_{oMax}\right) \quad (5)$$

where I_{LrPk} is the peak current through L_r, V_{CrPk} is the peak voltage across C_r, and $I_{o\,Max}$ is the maximum average output

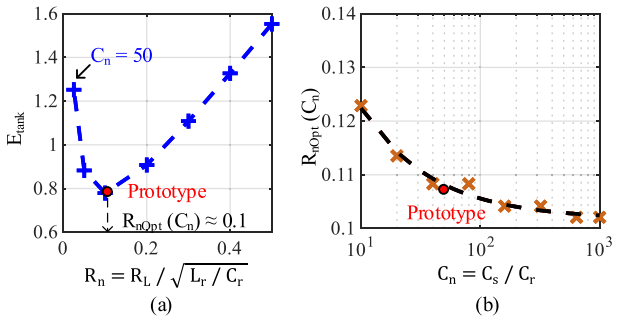

Fig. 3. Design figure for R_n. (a) Normalized tank energy $E_{\rm tank}$ versus normalized load R_n (3) when C_n (4) is 50. (b) $R_{n\rm Opt}$ that minimizes $E_{\rm tank}$ versus C_n. $R_{n\rm Opt} \approx 0.1$ is suggested to start the design.

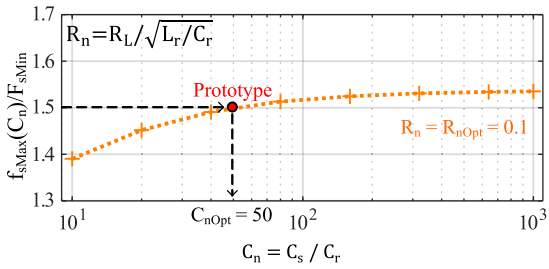

Fig. 4. Design figure for C_n; ratio of $f_{s\rm Max}$ and $F_{s\rm Min} = 2$ MHz versus C_n (4). $C_{n\rm Opt} = 50$ is suggested from $f_{s\rm Max}/F_{s\rm Min} = 1.5$ marked by the dot.

current. The reason for using the peak value rather than the instantaneous value is that the sizes of L_r and C_r depend on the peak current and peak voltage, respectively. In one switching cycle, the instantaneous energy in the SRB's tank is not constant and a bigger peak value of the instantaneous energy does not necessarily result in a bigger tank size. The steps to generate the design curves in the circuit simulator are as follows:

1) set the current source I at I_{oMax} as load and f_s at $F_{s\rm Min}$;
2) initialize C_n at 10, R_n at 0.025 ($= 0.17V_o/V_{\rm in}$), and f_r at $F_{s\rm Min}$;
3) sweep f_r toward $2F_{s\rm Min}$ with an increment of $F_{s\rm Min}/k_1$ where $k_1 = 100$ to obtain Fig. 3(a) and simulate to identify $f_r = F_{r@\rm Vo}(C_n, R_n)$ at which V_o is achieved;
4) calculate $E_{\rm tank}$ using (5);
5) sweep R_n toward 0.5 ($= 3.5V_o/V_{\rm in}$) with an increment of $(0.17V_o/V_{\rm in})/k_2$ where $k_2 = 1$ to obtain Fig. 3(a); return to step 3);
6) identify $R_{n\rm Opt}(C_n)$ at which $E_{\rm tank}$ is minimized; $R_{n\rm Opt}(50)$ is exemplified Fig. 3(a);
7) sweep C_n toward 1000 via $C_{n+1} = k_3C_n$ where $k_3 = 2$ to obtain Fig. 3(b);
8) plot $R_{n\rm Opt}(C_n)$ versus C_n as exemplified in Fig. 3(b), which suggests $R_{n\rm Opt} = 0.1$ for all C_n in this prototype.

The parameters k_1, k_2, and k_3 should be adjusted if more accuracy is desired at the expense of the simulation time.

Step 2: Select C_n using Fig. 4 to set switching frequency range. The steps to generate the design curves in the circuit simulator are as follows:

1) set the current source I at $I_{o\rm Min}$ as load, R_n at $R_{n\rm Opt}$ from step 1, and f_r at $F_{r@\rm Vo}(C_n, R_n)$ from step 1;
2) initialize C_n at 10 and f_s at $F_{s\rm Min}$;
3) sweep f_s toward $2F_{s\rm Min}$ with an increment $= k_1F_{s\rm Min}$ and identify $f_{s\rm Max}(C_n)/F_{s\rm Min} = f_s/F_{s\rm Min}$ at which $V_{\rm o}$ is achieved;
4) sweep C_n toward 1000 via $C_{n+1} = k_3C_n$ where $k_3 = 2$ to obtain Fig. 4; return to step 3);
5) plot C_n versus $f_{s\rm Max}(C_n)/F_{s\rm Min}$ as exemplified in Fig. 4. $C_{n\rm Opt} = 50$ is suggested from $f_{s\rm Max}(50)/F_{s\rm Min} = 1.5$ marked by the red dot in Fig. 4.

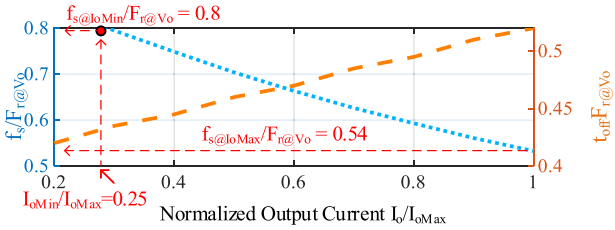

Fig. 5. Control curves for keeping voltage gain $V_o/V_{\rm in} = 7/48$ over the load range in Table I. Normalized OFF-time $t_{\rm off}F_{r@\rm Vo}$ is linearly proportional to $I_o/I_{o\rm Max}$ as shown by the dash line.

Step 3: Generate control curves. The steps are as follows:

1) set R_n at $R_{n\rm Opt}$ from step 1, f_r at $F_{r@\rm Vo}(C_n, R_n)$ from step 1, C_n at $C_{n\rm Opt}$ from step 2;
2) initialize the current source I at $I_{o\rm Max}$ as load and f_s at $F_{s\rm Min}$;
3) sweep f_s toward $2F_{s\rm Min}$ with an increment of $F_{s\rm Min}/k_1$ where $k_1 = 100$ to obtain Fig. 5; calculate $f_s(I_{\rm o})/F_{r@\rm Vo}$ and $t_{\rm off}(I_{\rm o})F_{r@\rm Vo}$;
4) sweep load current source I toward $I_{o\rm Min}$ with a decrement of $I_{o\rm Max}/k_4$ where $k_4 = 10$ to obtain Fig. 5; return to step 3);
5) plot $f_s/F_{r@\rm Vo}$ and $t_{\rm off}F_{r@\rm Vo}$ versus load current as exemplified in Fig. 5. Under full-load (25% load) condition, the switching frequency is $0.54f_r$ ($0.8f_r$).

The other component values are calculated according to (2)–(4). The equations are also summarized in Table II.

The prototype fabricated based on Tables I and II is shown in Fig. 6(a). All switches were enhancement-mode power transistor EPC2045 with $R_{\rm ds(on)} = 7$ mΩ and $C_{\rm oss} = 300$ pF. A PLT core and an E core with ML-91s material from Hitachi were used to fabricate the resonant inductor L_r. The resonant capacitor C_r was eight discrete multilayer ceramic capacitors (CGA3E2NP02A152J080AA) in parallel. The series capacitor C_s was six discrete capacitors (C3216C0G2A104J160AC) in parallel. The measured drain–source voltages of all switches are shown in Fig. 6(b) and (c). The measurement results were exported from the oscilloscope MSO5104B. All switches turn ON at zero-voltage. The area of the power loop and the gate driving loops were minimized to reduce the parasitic loop inductance. The currents in the switches were not measured since the insertion of current probes or shunts was undesirable in a tight layout. The slopes of $v_{\rm dsa2}$ and $v_{\rm dsb2}$ are virtually zero at the OFF timing, suggesting $S_{\rm a2}$ and $S_{\rm b2}$ carried negligible currents at turn-OFF moments.

The peak efficiency of the SRB prototype is 98.5%, and the full-load efficiency is 97.3%, as shown in Fig. 7(a). The

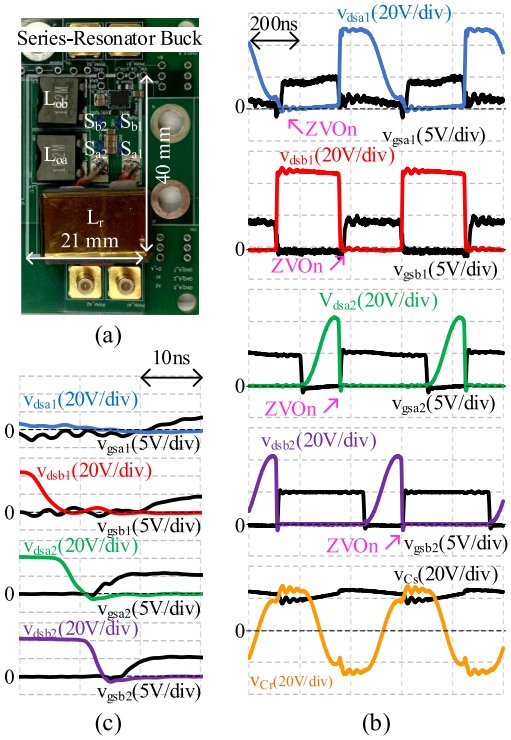

Fig. 6. (a) Prototype of SRB converter using the components in Table II. (b) Experimental voltage waveforms of all the switches in Fig. 1(a) measured by the oscilloscope. (c) Expanded experimental waveforms showing ZVOn.

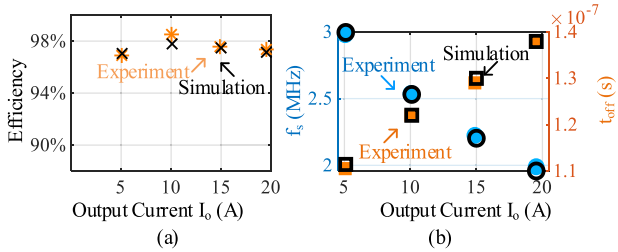

Fig. 7. (a) Efficiency and (b) switching frequency of the SRB prototype in Fig. 6 while keeping $V_{\rm in} = 48$ V and $V_o = 7$ V (hollow circle: f_s in simulation, solid circle: f_s in experiment, and hollow square: $t_{\rm off}$ in simulation, solid square: $t_{\rm off}$ in experiment).

switching frequency was adjusted under the load condition, as shown in Fig. 7(b). The measurement results are compared with simulation. The converter was simulated with the nonideal switch model provided by EPC. Each capacitor was with an equivalent series resistor (ESR) at the switching frequency from the datasheets. Each output inductor's loss was from TDKs inductor selection tool online and was with an ESR according to the simulated loss. The resonant inductor's loss was 0.9 W included in SRB's other loss in Fig. 8(a). This inductor was simulated with finite-element analysis (FEA) in Ansys Maxwell [12] and was with an ESR according to the FEA result. The discrepancy between simulation and measurement is less than 0.5%.

The major improvements with the series resonator are shown in Fig. 8. Two cases are compared using simulation at the same full-load operating point in Table I. GaN FET EPC2045 (100 V, $R_{\rm dson} = 7$ mΩ, $C_{\rm oss} = 295$ pF) is selected for all the switches in the SRB converter. The low-side switches' voltage stress is $V_{\rm in}/2$ in the SCB converter. EPC2045 for the high-side switches and EPC2049 (40 V, $R_{\rm dson} = 5$ mΩ, $C_{\rm oss} = 350$ pF) for the low-side switches are selected. The nonideal switch models are provided by EPC.

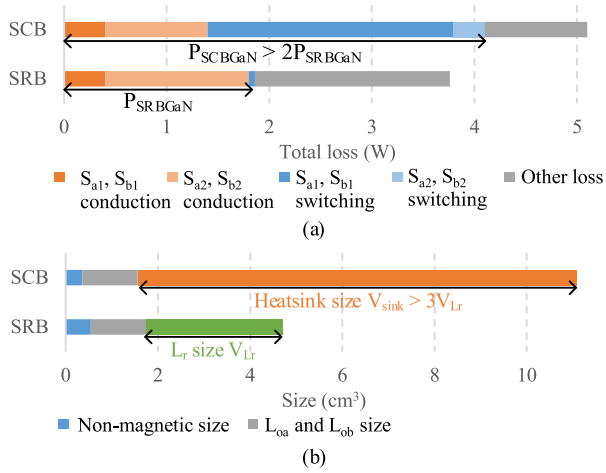

Fig. 8. (a) Total loss and (b) converter size comparison between the SRB converter in Fig. 6 and the SCB converter under the same full-load condition in Table I. A heatsink (374024B60023 made by Aavid Thermalloy) is added for the SCB converter to keep the same switch's average junction temperature. The SRB converter reduces switch loss by a factor of 2. Its resonant inductor size is less than one-third of the heatsink size in the SCB converter.

The average switch junction temperatures of both cases are the same. A heatsink is added to the SCB converter due to hard-switching loss. The total loss is compared in Fig. 8(a). The SCB converter has a switch loss twice the switch loss in the SRB converter. The series resonator saves about 30% overall converter loss. The size comparison is shown in Fig. 8(b). Both cases have the same output inductors. The heatsink size of the SCB converter is three times larger than the resonant inductor size of the SRB converter.

IV. Conclusion

The presence of the resonant tank in the SRB converter reduces all switches' voltages to zero at turn-ON, and all low-side switches' currents to zero before turn-OFF. A preliminary design procedure was established from circuit simulation to minimize the tank energy, constrain the frequency range, and regulate the output voltage. A 2-MHz prototype with a peak efficiency of 98.5%, 48 V at the input and 7 V, 20 A at the output was built to demonstrate the viability of the topology.

The measured voltage waveforms, efficiency, switching frequency, and regulating variable ($t_{\rm off}$ of the low-side switches) were within 0.5% of the expectations. While the results confirm the viability of the SRB topology, mathematical analysis, optimization, and design tradeoffs are among the issues to be resolved.

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