Interleaved LCLC Resonant Converter With Precise Current Balancing Over a Wide Input Voltage Range

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***Abstract*—An interleaved LCLC resonant converter with accurate current balancing performance over a wide input voltage range is proposed. Resonant tank components have slight tolerances that can unbalance load sharing between paralleled phases. Because of the steep voltage gain curve of the LCLC resonant tank, most conventional current sharing approaches might not be effective. In the proposed converter, the impedances of the resonant tanks are matched by a switch-controlled capacitor (SCC) that is in series with the resonant capacitor resulting in precise load current balancing between phases. The impact of various unbalanced situations on the interleaved LCLC resonant converter is investigated, a minimum operating angle for the SCC circuit is identified, the basic accuracy of SCC current balancing via digital control is investigated, and a control strategy is proposed to perform the current sharing. Computer simulation results and experimental results from a GaN-based prototype validate the performance of the proposed interleaved LCLC converter with precise current sharing over a wide input voltage range from 250 to 400 V. Using enhancement mode GaN and benefiting from the interleaving feature, a high conversion efficiency is achieved on a two-phase 1 kW LCLC converter with peak efficiency of 96.7%.**

***Index Terms*—Interleaved resonant converter, LCLC resonant converter, load current sharing, multiphase, switch-controlled capacitor (SCC).**

I. Introduction

In THE past decade, electrical energy demand has been extremely boosted in various applications due to rapid advancement in their technologies. Hence, the electric power conversion ability should keep up with the rising need in all kinds of electric power conversion applications, (i.e., dc-dc, dc-ac, ac-dc, and ac-ac). The electrical energy requirement of data centers and electric vehicles (EVs) has significantly increased because of the fast development of cloud computing and energy storage technologies, respectively. With the technological development of power electronics circuits, more reliable electric energy will be delivered to consumer loads [1]–[6]. LLC resonant converters are widely used in many industrial applications due to their interesting characteristics such as zero-voltage switching (ZVS) for primary-side switches and zero-current switching for secondary side diodes/switches. In datacenter power processing and EV auxiliary low voltage onboard battery charger applications, it is needed for the dc-dc stage to operate in a wide input voltage range, (e.g., ∼250 to ∼400 V) to enhance the availability of power at the low voltage dc bus, (e.g., 12–14 V) for a longer time.

Various techniques have been used to modify the LLC converter to be more appropriate for wide input voltage applications [7]–[11]. Most of these techniques require additional power/sensing components and/or control methods. On the other hand, some resonant converters are intrinsically suitable for a wide input voltage application without additional components or control. LCLC resonant converter is a new resonant converter with a sharp voltage gain, which makes it suitable for wide input voltage applications. It has been reported that the LCLC converter with four resonant elements has enhanced performance in a wide input voltage operating range compared with an equivalent LLC resonant converter [12].

Another challenge in datacenter and EV applications is the high load current level, (i.e., hundreds of ampere) at low voltage dc bus, which often limits the power level of a single module resonant converter used in these applications to 1 kW. Hence, it is required to use multiphase resonant converters to allow high power realization by distributing the current stress. Furthermore, by implementing interleaving, a reasonably sized capacitor can be used at the output due to the reduced current stress. Phase interleaving in resonant converters that are normally frequency-controlled for output voltage compensation can be challenging as the voltage gain of each phase is reliant on the impedance of the resonant tank that can vary on each phase due to different component tolerances. In multiphase converters, a slight voltage gain imbalance leads to a significant imbalance in load current sharing among paralleled phases. Asymmetrical loading of paralleled phases is a critical matter in interleaved resonant converters as it reduces efficiency and reliability because of adding too much thermal pressure on one phase.

Various current sharing methods either active or passive methods have been proposed for multiphase LLC resonant converters [13]–[23]. Various passive impedance matching (PIM) methods and automatic current charing approaches have been studied for the LLC resonant converter in [13]–[15]. The PIM is an attractive approach as often no extra active or passive elements and/or control methods are required. However, the current balancing performance will deteriorate with large tolerances in resonant elements. Moreover, phase shedding is a

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crucial feature in multiphase converters for light-load efficiency improvement, and it is not possible to be realized with most of the passive current balancing approaches.

In [16], an interleaved three-phase LLC converter is proposed with a single integrated magnetic and a balancing transformer for automatic current sharing. This method is only applicable to three-phase resonant converters and similar to other methods that employ an integrated magnetic; this approach is not so successful in the current balancing of wide voltage range resonant converters. In [17], a coupling cell is implemented between every two phases of a multiphase LLC resonant converter for automatic current sharing. This method is relatively effective in current balancing for any number of phases; however, it requires an additional transformer in each cell, and interleaving is not easily possible with this method.

In [18], an interleaved three-phase LLC converter with Y connected transformers and 120° phase shift is introduced, which can achieve a relative automatic current sharing. Then, an accurate current sharing is performed through the modulation phase shift control between the phases. This method is only applicable to three-phase resonant converters. In [19], a double-phase half-bridge LLC converter is proposed for EV application. The voltage gain difference between the phases is adjusted by using different switching frequencies for each phase, which prevents interleaving. An interleaved LLC converter is introduced in [20] that takes advantage of phase shift control for controlling the voltage gain for current sharing purposes. The method can only be applied in a full-bridge topology, and it is not good for large tolerances as it introduces too much current stress due to large phase shifts for current balancing. In [21], a two-phase interleaved LLC converter is proposed from texas instruments (TI), which utilizes duty-cycle adjustment of a higher current carrying phase to do the current balancing. The duty-cycle in this method cannot be reduced much without compromising efficiency. Although in all these active current sharing methods only new control methods are needed, each has its limitations and they are not so effective for wide input voltage range operation.

In [22] and [23], current sharing is implemented through using a switch-controlled capacitor (SCC) or a switch-controlled inductor (SCI) in series with the resonant tank capacitor or inductor, respectively, to slightly alter the resonant tank impedance in order to compensate the voltage gain. This approach provides a precise current sharing between paralleled phases that can be applied to any number of phases with either half- or full-bridge topology. The only limitations related to this method is the additional component cost for each SCC/SCI circuit and the complexity of the current sharing control, which both are reliant on the number of paralleled phases. It should be mentioned that the additional circuitry does not add any switching losses to the original converter and there is only extra conduction losses via the added switching devices, which is not significant considering the rating of the switch.

Unlike from DCX resonant converters with fixed input and output voltages, it is not efficiency-wise appropriate to implement printed circuit board (PCB) windings to achieve small tolerance inductors in wide input voltage range resonant converters [24]. Moreover, the combination of tolerances in a four-element resonant tank can lead to more complex imbalance conditions than with the LLC tank. Hence, the SCC technique is a better solution than traditional passive and active methods, which can handle different imbalance conditions for the proposed interleaved LCLC converter.

The main contribution of this article can be summarized as follows.

1) The voltage imbalance condition in a multiphase LCLC resonant converter is studied and an unforeseen voltage gain relationship is observed over the wide input voltage variation.
2) The SCC circuit accuracy and performance is evaluated in a steep voltage gain resonant converter, (i.e., LCLC converter) for the first time in the literature.
3) A minimum operating angle is identified for the SCC circuit in this article to have a stable operation over a wide operating range.
4) A new control algorithm is developed considering the identified current balancing requirements for the proposed interleaved LCLC resonant converter.
5) The accuracy of the SCC current sharing is verified in a steep gain interleaved resonant converter over a wide input voltage range using the proposed control algorithm. An early version of this article has been published in [25] with less analysis, simulation, and experimental results.

The rest of this article is organized as follows. Section II introduces the proposed interleaved LCLC converter. In Section III, the abnormal unbalanced behavior of a multiphase LCLC converter is studied and an appropriate SCC operating range is identified. Moreover, the accuracy of current sharing via the SCC circuit implemented in digital control is investigated. In Section IV, a control strategy is proposed to accurately perform the current balancing in the proposed interleaved LCLC converter. Computer simulation and experimental results are provided in Section V to verify the analysis and current sharing performance in a wide input voltage range. Finally, the article is concluded in Section VI.

II. Proposed Interleaved LCLC Resonant Converter

A. LCLC Resonant Tank Versus LLC Resonant Tank

In [12], an improved LLC converter with an additional capacitor was proposed with narrow switching frequency for a wide input voltage application, which is named LCLC resonant converter. The LCLC resonant converter consists of two resonant inductors, (i.e., L_s and L_p) and two resonant capacitors, (i.e., C_s and C_p), which theoretically is equivalent to an LLC converter with a variable magnetizing inductor. Resonant converters are mostly controlled via switching frequency variation to meet different operating conditions resulting in a variable equivalent magnetizing inductor in the LCLC resonant tank. This is because the magnetizing impedance of the LCLC tank is variable at different switching frequencies, which is because of the resonant parallel capacitor connected in series with the resonant parallel inductor. The impedance of the equivalent magnetizing inductor

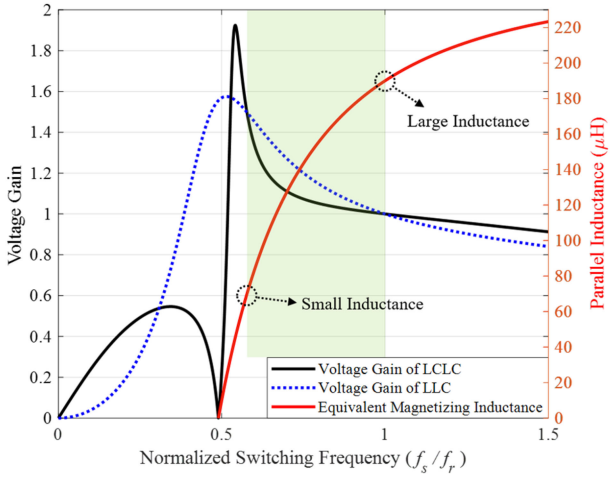

Fig. 1. Voltage gain curves of LCLC and LLC resonant tanks at different switching frequencies along with the variable magnetizing inductance of the LCLC tank.

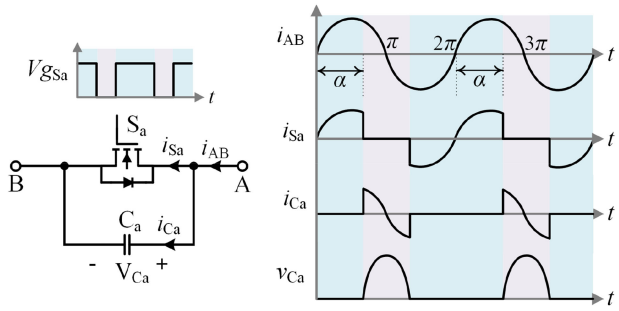

Fig. 2. Half-wave SCC power circuit and its basic waveform assuming sinusoidal current.

($L_{\mathrm{m\_eq}}$) can be found as in

$$L_{\mathrm{m\_eq}} = L_p - \frac{1}{(2\pi f_s)^2 C_p}. \tag{1}$$

The voltage gain of the LCLC resonant tank (M_{LCLC}) can be derived based on the voltage gain of the conventional LLC resonant tank by substituting (1) in place of the magnetizing inductance as follows:

$$M_{\mathrm{LCLC}} = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_{\mathrm{m\_eq}}} - \frac{L_r}{L_{\mathrm{m\_eq}} f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{2}$$

where the series-resonant frequency (f_r), normalized-frequency (f_n), the equivalent-resistance transferred to the transformer primary side (R_e), and the quality factor (Q) are as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{3}$$

$$f_n = \frac{f_s}{f_r} \tag{4}$$

$$R_e = \frac{8 \times n^2}{\pi^2} \times R_L \tag{5}$$

$$Q = \frac{\sqrt{L_s/C_s}}{R_e}. \tag{6}$$

Fig. 1 illustrates the voltage gain curves of LCLC and LLC resonant tanks. The voltage gain of the LLC tank is drawn using a fixed 70 μH magnetizing inductor to achieve the same voltage gain as in the LCLC tank gain curve. However, the equivalent magnetizing inductance of the LCLC tank is variable with switching frequency. With high input voltages, the required voltage gain is small, and therefore, the switching frequency should be high and around the series-resonant frequency (f_n~1), which results in a large magnetizing inductance. Therefore, the transformer's primary side current is lower than in an equivalent LLC converter. On the other side, with low input voltages, the required gain is high, and hence, the switching frequency should be low and around the parallel resonant frequency, (e.g., f_n~0.6), which results in a small magnetizing inductance.

It can be seen from Fig. 1 that the voltage gain curve of the LCLC tank is much sharper than the voltage gain of the LLC tank. Due to using two inductors in the LCLC resonant tank, the impact of resonant component tolerances can introduce unforeseen voltage gain behaviors in a paralleled LCLC resonant converter, which makes the current balancing challenging. Therefore, to compensate for the LCLC voltage gain anomalies accurately and actively over the entire operating range, an SCC circuit can be integrated into the resonant tank of the paralleled LCLC converters to solve the current balancing problem.

B. Principles of Half-Wave SCC

Fig. 2 illustrates a half-wave SCC circuit consisting of an auxiliary capacitor (C_a) that is connected in parallel with a switch (S_a). MOSFET S_a shares a common source with the lower side switch of the half-bridge switches, and hence, a low side driver can be used for driving the SCC MOSFET. The basic operational waveform of the half-wave SCC circuit assuming a sinusoidal current is illustrated in Fig. 2. Current I_{AB} represents the resonant current that is passing through the SCC circuit. The current zero-crossing instants are at 0, π, 2π, …, etc. It is considered that S_a is turned OFF at angle $2n\pi+\alpha$. After S_a is turned OFF, the resonant current flows through the SCC capacitor and charges C_a until the next current zero-crossing instant at $(2n + 1)\pi$. Then, the capacitor C_a discharges as the current direction reverse. After the SCC capacitor is discharged, the negative current is going to flow in a reverse direction from B to A through the body diode of S_a. To reduce reverse conduction loss through the body diode, S_a is turned ON at this instant and continue conducting for the remaining of the cycle. S_a is turned OFF again at an angle $(2n+2)\pi+\alpha$.

The resulting capacitance of half-wave SCC (C_{SCC}) is determined by the SCC MOSFET turn ON α angle that can be found from [26]

$$C_{\mathrm{SCC}} = \frac{2C_a}{2 - (2\alpha - \sin 2\alpha)/\pi}. \tag{7}$$

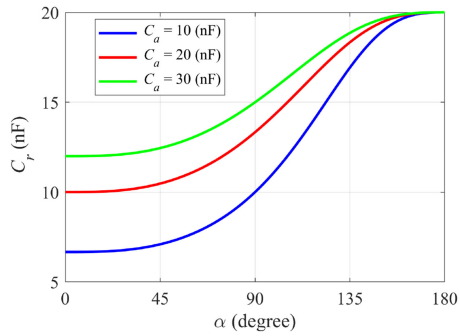

Fig. 3. 2-D plot of the theoretical total resonant capacitance ($\boldsymbol{C_r}$) due to the variation of α angle considering $\boldsymbol{C_s}$ = 20 nF.

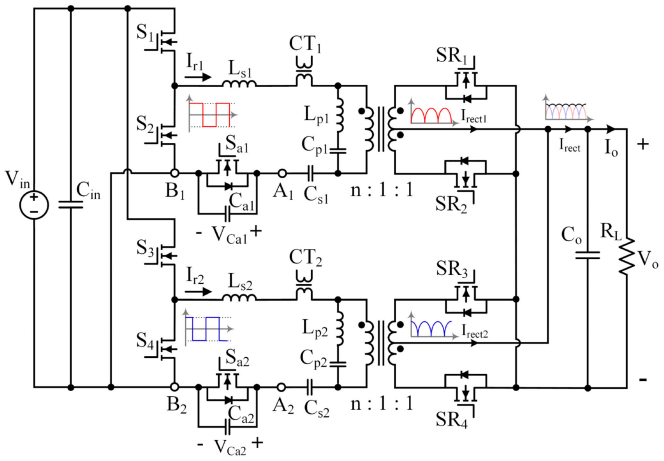

Fig. 4. Proposed interleaved LCLC resonant converter.

The equivalent total resonant capacitance ($C_r = C_{\text{SCC}} \,||C_s$) can then be expressed as a function of α

$$C_r = \frac{2C_aC_s\pi}{2C_a\pi + 2C_s\pi - 2C_s\alpha + C_s sin2\alpha} \tag{8}$$

where C_s is the series resonant capacitor of the LCLC tank.

The SCC duty-cycle full range is from 0% to 100% that is corresponding to delay angle (α) changing from 0 to π. Operating from 0 to π changes the resulting resonant capacitance (C_r) from its minimum to maximum value. When $\alpha = 0$, the resonant current goes through the SCC capacitor only, which connects C_s and C_a in series resulting in a minimum C_r. When $\alpha = \pi$, the resonant current goes through the SCC switch only, which bypasses the SCC capacitor, and hence, the maximum resonant capacitance will be equal to the original series resonant capacitance, (i.e., $C_r = C_s$). To rephrase it, C_r can be changed between C_s and a smaller value to do the impedance matching for voltage gain compensation. Fig. 3 illustrates the aforementioned characteristics of three different SCC capacitor values over the full range of α variation.

C. Proposed Interleaved LCLC Resonant Converter

Fig. 4 illustrates the schematic of the proposed interleaved LCLC converter with the SCC circuit implemented in both phases. To be able to tune the impedance of both phases reliably, the SCC circuits are used in both phases. Switches S_{a1} and S_{a2} are half-wave SCC MOSFETs that are operating with respect to resonant current to switch-in and -out the SCC capacitors, (i.e., C_{a1} and C_{a2}) to change the resonant tank impedances allowing a compensated voltage gain for both phases. Two current-transformers, (i.e., CT_1 and CT_2) are utilized for the detection of current zero-crossing instants that is necessary for the synchronization of SCC gate pulses as well as for the resonant current measurement and proper operating angle generation, (i.e., a_1 and a_2). All the captured information will go to a microcontroller unit (MCU) and proper SCC driving pulses will be generated for the switches. More analysis regarding the impact of the SCC circuit and implemented control strategy is provided in the following sections.

III. Analysis of Tolerances in LCLC Resonant Converter and Active Current Sharing Accuracy Analysis of SCC Technology

A. Analysis of Imbalances in Multiphase LCLC Resonant Converters

The effect of resonant component tolerances in an LCLC tank comprising of four resonant components can be worse than of in the LLC tank. It is obvious that making identical inductors is not possible in practice, and hence, having some tolerances is unavoidable. As discussed before, any tolerances can cause imbalances in the impedance of the resonant tanks. Since the resonant converters are frequency-controlled, the voltage gain of the paralleled resonant converters can be different at a specific switching frequency. Hence, it is crucial to study the impact of tolerances in resonant elements on the voltage gain behavior of the proposed interleaved LCLC resonant converter.

Using the design approach provided in [11] for the input values of $V_{\text{in\_min}} = 250$ V, $V_{\text{in\_max}} = 400$ V, $V_o = 12$ V, $P_o = 500$ W, $f_{\text{s\_min}} = 170$ kHz, and $f_{\text{s\_max}} = 280$ kHz, the following values can be selected for the power circuit of the LCLC converter for each phase: $L_s = 16$ μH, $C_r = 20$ nF, $L_p = 240$ μH, $C_p = 5$ nF, and n = 18. The abovementioned values are utilized in the rest of the article unless otherwise is stated. To consider a large enough tolerance for the components, $\pm 10\%$ adjustment is assumed for the LCLC tank elements. Furthermore, phase 1 is assumed to be the reference phase for the analysis provided in the following.

First, only the impact of one resonant element variation on the voltage gain of phase 2 is considered. Fig. 5 illustrates the impact of variation in the value of each individual resonant component in the voltage gain of the LCLC converter. Since phase 1 is the reference phase, the values of components in phase 2 are normalized based on their counterparts in phase 1. Moreover, as the difference between the voltage gain of an unbalanced two-phase LCLC converter is important here, the switching frequency cannot be normalized. From Fig. 5(a) and (b), it can be inferred that the direction of voltage gain change is the opposite of the variation of L_s and C_s values at all frequencies, (i.e., the blue surface (phase 2) is under the orange surface (phase 1) for increased values of capacitance/inductance). From Fig. 5(c) and (d), it can be inferred that the direction of voltage gain

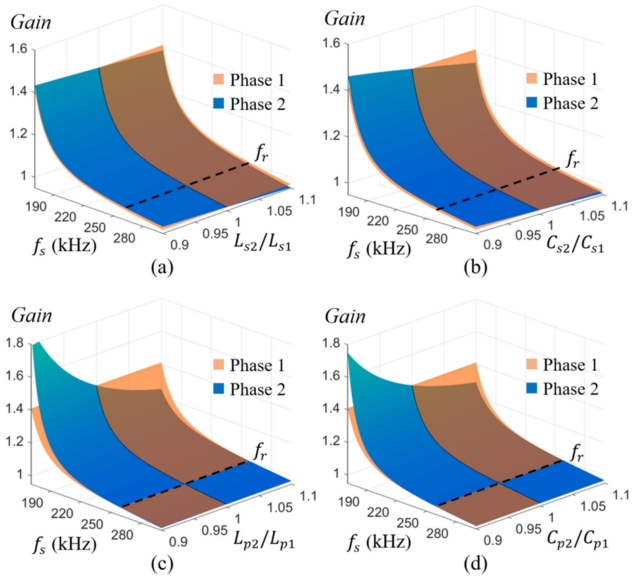

Fig. 5. 3-D illustration of the impact of one component tolerance at a time on the voltage gain of the proposed two-phase LCLC converter. (a) ±10% tolerance in $\boldsymbol{L_{s2}}$. (b) ±10% tolerance in $\boldsymbol{C_{s2}}$. (c) ±10% tolerance in $\boldsymbol{L_{p2}}$. (d) ±10% tolerance in $\boldsymbol{C_{p2}}$.

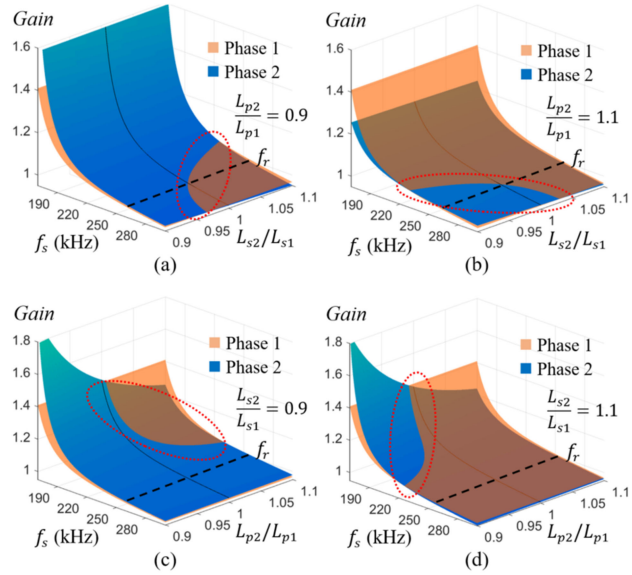

Fig. 6. 3-D illustration of the impact of two component tolerances at the same time on the voltage gain of the proposed two-phase LCLC converter. (a) ±10% tolerance in $\boldsymbol{L_{s2}}$ while $\boldsymbol{L_{p2} < L_{p1}}$. (b) ±10% tolerance in $\boldsymbol{L_{s2}}$ while $\boldsymbol{L_{p2} > L_{p1}}$. (c) ±10% tolerance in $\boldsymbol{L_{p2}}$ while $\boldsymbol{L_{s2} < L_{s1}}$. (d) ±10% tolerance in $\boldsymbol{L_{p2}}$ while $\boldsymbol{L_{s2} > L_{s1}}$.

change is the opposite of the variation of L_p and C_p values until the resonant frequency and above the resonant frequency the voltage gain change is in the same direction of the variation of the respective resonant component values.

Second, the impact of two resonant element variations is considered at the same time as a uniform variation only in one resonant element cannot show any imbalance anomalies. Here, the effect of inductor tolerances is only illustrated as in practice usually many small capacitors are connected in parallel usually with a less than 5% tolerance for each, so the effect of capacitance tolerances is less than of the inductor tolerances. Fig. 6 shows the variation in the value of the resonant inductor and magnetizing inductor by assuming a 10% decrease or increase in the inductance of L_{s2} and L_{p2}, respectively. It can be observed that the intersection of two voltage gain surfaces occurs in a curve shape with variable voltage gain at different switching frequencies, which are highlighted with red dotted lines in Fig. 6(b). This phenomenon demonstrates that the voltage gain of each phase in a multiphase LCLC converter can be both below and above the other phase's voltage gain within the operating switching frequency. The latter makes the SCC current sharing control complex over a wide operating range. Consider the case shown in Fig. 6(c), if the value of L_{p2} is considerably larger than the value of L_{p1}, at low switching frequencies, the voltage gain of phase 1 is higher than phase 2, (i.e., the orange surface [phase 1] is above the blue surface [phase 2]), and at high switching frequencies, the voltage gain of phase 2 is higher than phase 1, (i.e., the blue surface [phase 2] is above the orange surface [phase 1]). The mentioned situations are likely to happen in wide input/output voltage applications; hence, it is crucial to use SCC on both phases to precisely do the current sharing at every operating point. Here the impact of resonant capacitors variation is not shown due to brevity. It should be mentioned that any small capacitor tolerance deviates the intersection curve a little bit from its current position in Fig. 6.

Two scenarios are considered here to observe the effect of gain imbalances and SCC circuit performance in such scenarios. The first scenario is shown in Fig. 7(a), where the voltage gain of phase 2 is always higher than phase 1. Based on Fig. 5, this scenario can only happen when one or more components have tolerances that are all in the same direction. In this case, only one direction current balancing is needed, and hence only one SCC circuit on phase 1 is enough to compensate for the gain difference at both low switching frequency, (i.e., 170 kHz) and high switching frequency, (i.e., 250 kHz). The second scenario is shown in Fig. 7(b) where there is an intersection between the voltage gain curves of phase 1 and phase 2, which is located somewhere below the resonant frequency (f_r) around 210 kHz. According to Fig. 6, the mentioned scenario can only happen when at least two resonant elements have tolerances in the opposite direction meaning one resonant component is larger and one resonant element is smaller than their counterparts on the other phase. This case is more likely to happen in real practice as the proposed interleaved LCLC resonant converter has four resonant elements on each phase with uncontrollable tolerances. As can be seen in Fig. 7(b), the SCC circuit on phase 2 is compensating for the gain difference at a low frequency while the other phase SCC is shut down, (i.e., $\alpha_1 = 180°$ and $\alpha_2 = 123°$), and the SCC circuit on phase 1 is compensating at high frequency while the other phase SCC is shut down, (i.e., $\alpha_1 = 147°$ and $\alpha_2 = 180°$). It should be noted that if the maximum value of α is set to 170–180° the other phase's α value does not change noticeably as any α value close to 180° barely varies the resonant capacitor. This phenomenon can be observed in Fig. 3.

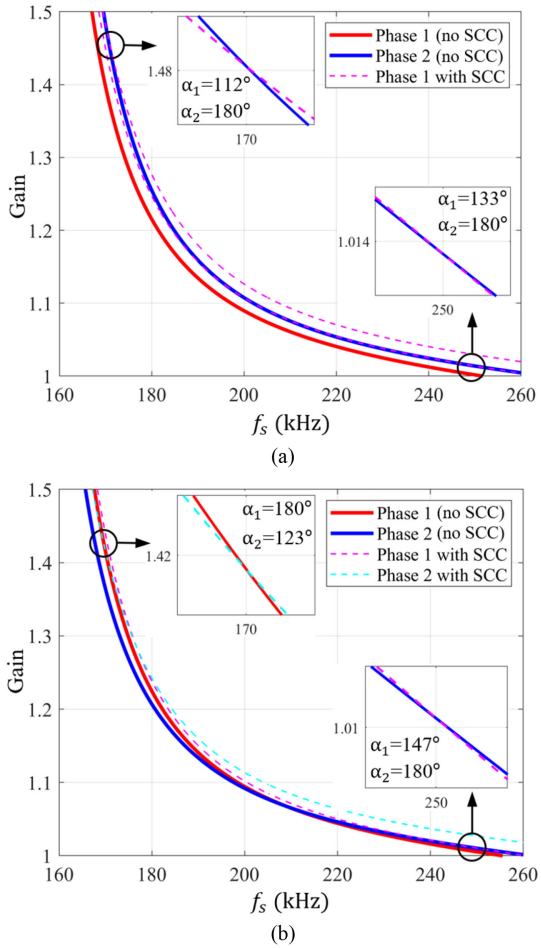

Fig. 7. Performance of the SCC circuit ($C_a = 20$ nF) on two different voltage gain scenarios. (a) Scenario 1 with no intersection. (b) Scenario 2 with an intersection at below resonant frequency.

To avoid slowing down the current balancing, it is recommended to use a lower upper limit for the α angle in practice, (e.g., 170°).

B. Analysis of SCC Current Sharing and Accuracy With Digital Control

As discussed in the previous subsection, when the impedance of the resonant tank varies, the voltage gain curve alters, and hence the load share and the resonant rms current of each phase change. Therefore, to observe the current balancing performance, the effect of variation in α angle can be investigated in the rms value of the resonant current. For simplicity in theoretical calculations, a near-resonant operation ($f_s = f_r$) is assumed with a purely sinusoidal current. Therefore, the resonant inductor current (i_r) can be expressed as follows:

$$i_r\ (t) = \sqrt{2}\, I_{r\_\mathrm{rms}} \sin\left(2\pi f_s t - \phi\right) \tag{9}$$

where I_{r_rms} is the resonant rms current.

The current through the magnetizing inductor can be expressed as follows:

$$i_m\,(t) = \begin{cases} -I_{\mathrm{m\_pk}} + \frac{nV_o}{L_{\mathrm{m\_eq}}} t \\ I_{\mathrm{m\_pk}} - \frac{nV_o}{L_{\mathrm{m\_eq}}} \left(t - \frac{T_s}{2}\right) \end{cases} \tag{10}$$

where T_s is the switching period and $I_{\mathrm{m\_pk}}$ is the maximum value of the magnetizing current that is found in

$$I_{\mathrm{m\_pk}} = \frac{nV_o T_s}{4L_{\mathrm{m\_eq}}}. \tag{11}$$

The equivalent magnetizing inductance ($L_{\mathrm{m\_eq}}$) must be calculated at the switching frequency in the above equations. The rms current through the series resonant inductor can be found in (12), which is calculated by subtracting the circulating current through the magnetizing inductor from the resonant inductor current

$$I_{r\_\mathrm{rms}} = \frac{V_o \sqrt{4\pi^2 + n^4 {R_L}^2 \left(\frac{1}{L_{\mathrm{m\_eq}} f_s}\right)^2}}{4\sqrt{2} n R_L} \tag{12}$$

By the operation of the SCC circuit in each phase, the total resonant capacitance value of that phase changes leading to an altered voltage gain and hence altered resonant current. Considering (2), the resonant current of the LCLC converter dependent on the resonant components can be derived as (13) shown at the bottom of the next page. After inserting the equivalent series-resonant capacitance (C_r) from (8) into (13), the rms resonant current is dependent on f_s and α.

To have current balancing for the worst-case scenario, the following equation should be met:

$$I_{r_{\mathrm{rms\_high}}}\left(f_{\mathrm{s\_min}}, C_{r0}\right) = I_{r_{\mathrm{rms\_low}}}\left(f_{\mathrm{s\_min}}, C_{\mathrm{r\_min}}\right) \tag{14}$$

where C_{r0} is the initial resonant capacitance when the SCC is not operating on the phase with a higher load share ($I_{r_{\mathrm{rms\_high}}}$), and $C_{\mathrm{r\_min}}$ is the minimum resonant capacitance on the phase with a lower load share ($I_{r_{\mathrm{rms\_low}}}$), which is required to be tuned by the SCC operation to make the current share balanced. When the minimum required resonant capacitance is found, the SCC capacitor can be selected based on the desired SCC operating angle range and the SCC MOSFET voltage stress. A large C_a increases the SCC operating range that will reduce the current balancing speed, while a small C_a increases the voltage stress on the SCC MOSFET. This process needs fine-tuning for practical implementation as the theoretical design using the first harmonic approximation (FHA) leads to overdesign. The maximum of the SCC capacitor voltage stress can be found from the initial resonant capacitor maximum voltage stress ($V_{\mathrm{Cr0\_max}}$) as follows:

$$V_{\mathrm{Ca\_max}} = \frac{C_s}{C_s + C_a}\left(V_{\mathrm{Cr0\_max}} - \frac{V_{\mathrm{in}}}{2}\right). \tag{15}$$

Any small α angles using small SCC capacitors can alter the total resonant capacitance significantly leading to a large variation in the half-cycle resonant frequency, which will lead to asymmetrical operation causing an increased power loss. Therefore, in practical implementation using any value smaller than 90° is not recommended. A 3-D plot for the change in resonant rms current due to the change in SCC operating angle (α) and switching frequency is illustrated in Fig. 8. As can be observed, the slope of the resonant current change is the largest at low switching frequencies related to low input voltages. Furthermore, by reducing the α angle from 180°, the resonant

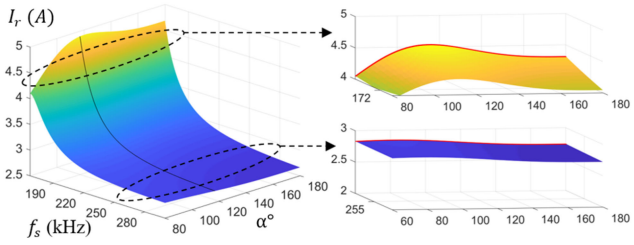

Fig. 8. 3-D plot for the variation of the resonant current versus the variation in switching frequency (f_s) and α angle (with $C_a = 20$ nF).

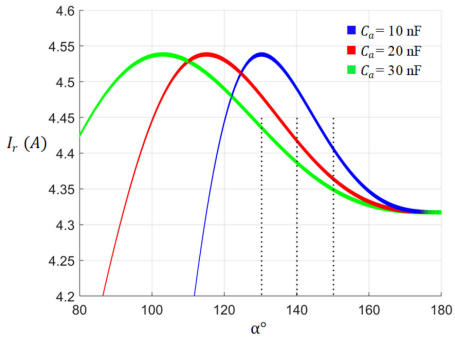

Fig. 9. 2-D plot of the variation of the resonant current versus the variation in α angle at fixed 170 kHz switching frequency with different C_a values.

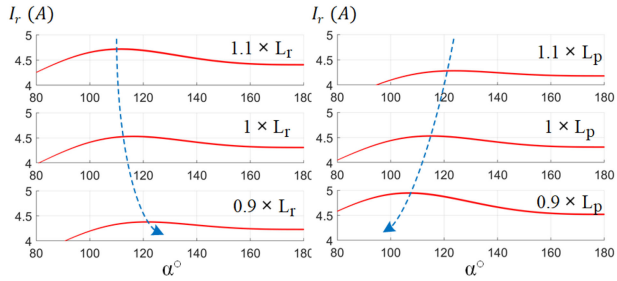

Fig. 10. Variation of the resonant current versus the variation in α angle. (a) Different L_s values. (b) Different L_p values.

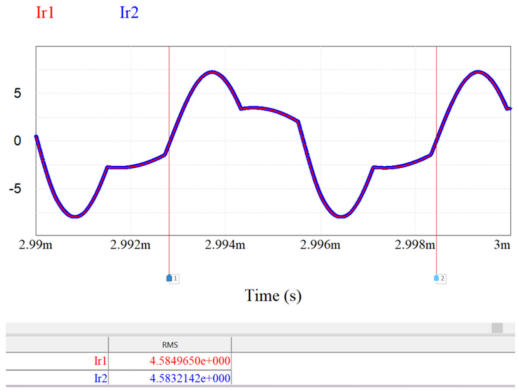

Fig. 11. Simulation result of the rms vales of the resonant currents.

current first increases to a maximum value and then decreases sharply. To have a safe SCC operation, a monotonic change of current is always sought from the SCC circuit. Therefore, it is favorable to set the minimum limit of the operating range of SCC ($\alpha_{\min}$) to the angle related to the maximum resonant current. In practice, an α value smaller than but close to 180° might be selected for the maximum α limit, (e.g., $\alpha_{\max} = 170°$) since the variation of resonant capacitance, and hence, balancing is slow at high α angles close to 180°. It is worth mentioning that finding $\alpha_{\min}$ from (13) leads to overdesign as this equation is based on the FHA and the actual lower limit will be smaller than what is observed in Fig. 8.

In Fig. 9, different SCC capacitances are utilized, and it is obvious that the maximum value of resonant current is constant, while the α angle related to the maximum value that we set to $\alpha_{\min}$ is altering. When C_a is decreased, $\alpha_{\min}$ is increased and the slope of current change gets steeper. The latter decreases the effective operating range and reduced the current sharing accuracy of the SCC circuit. As the tolerances in inductors are more significant than in capacitors, only the effect of tolerances in the series-resonant inductor and parallel-resonant inductor on the resonant current at a low switching frequency is shown in Fig. 10. The operating range of SCC is increasing by the increase in L_s and the operating range of SCC is decreasing by the increase in L_p. In both cases when the operating range increases, (i.e., $\alpha_{\min}$ decreases), more SCC compensation range is available. This is very important in the design of the resonant tank components of the proposed interleaved converter as in some cases the available compensation might not be enough to perform accurate current sharing (see $0.9 \times L_s$ and $1.1 \times L_p$ conditions in Fig. 12).

To find out the precision of current balancing, the effect of the smallest change for α angle in digital control can be calculated through the resonant rms current variation. With 1 ns change in a duty-cycle that is available with most pulse width modulation (PWM) modules of low-cost microprocessors, α angle varies by 0.066°. This small change should be investigated in the resonant current change where the variation slope is maximum. The maximum slope change is roughly marked with dashed lines in Fig. 11 with different SCC capacitors, which is 150, 140, and 130° for $C_a = 10$ nF, $C_a = 20$ nF, and $C_a = 30$ nF, respectively. For each case, the α angle of both phases is set to an equal value and the smallest change is applied only to phase 2. For example, for the case with $C_a = 20$ nF, it is considered $\alpha_1 = \alpha_2 = 140°$ for the SCC circuit. Then, the deviation in the resonant current (Δ_{I_r}) can be found from (13) considering that the α angle of

$$I_{r\_\mathrm{rms}} = \frac{V_{\mathrm{in}}\sqrt{4\pi^2 + n^4 {R_L}^2 \times \left(\frac{1}{L_{\mathrm{m\_eq}} f_s}\right)^2}}{8\sqrt{2}n^2 R_L \sqrt{\left(1 + \frac{L_s}{L_{\mathrm{m\_eq}}} - \frac{L_s}{L_{\mathrm{m\_eq}}} \times \frac{1}{4\pi^2 L_s C_r f_s^2}\right)^2 + \frac{L_s}{C_r} \times \left(\frac{\pi^2}{8n^2 R_L}\right)^2 \left(2\pi\sqrt{L_s C_r} f_s - \frac{1}{2\pi\sqrt{L_s C_r} f_s}\right)^2}} \tag{13}$$

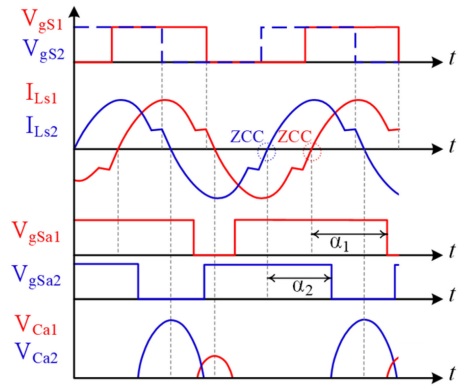

Fig. 12. Key waveforms of the interleaved LCLC converter with SCC.

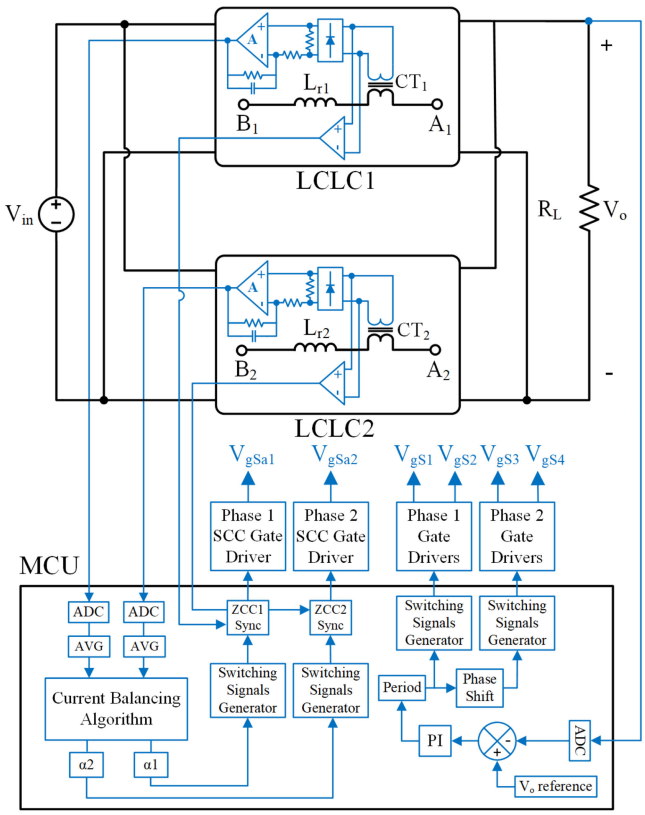

Fig. 13. Proposed digital control implementation for the interleaved LCLC resonant converter.

phase 2 will be $\alpha_2 = 140.066°$ with the smallest possible change in α. The resonant current change due to the smallest change in α is calculated with different SCC capacitors as follows:

$$\Delta_{I_r}^{10nF} = I_{r1\_\mathrm{rms}} - I_{r2_{\mathrm{rms}}} \rightarrow \Delta_{I_r} = 0.001 \text{ A}$$
$$\Delta_{I_r}^{20nF} = I_{r1\_\mathrm{rms}} - I_{r2_{\mathrm{rms}}} \rightarrow \Delta_{I_r} = 0.0007 \text{ A}$$
$$\Delta_{I_r}^{30nF} = I_{r1\_\mathrm{rms}} - I_{r2_{\mathrm{rms}}} \rightarrow \Delta_{I_r} = 0.0006 \text{ A}. \quad (16)$$

Therefore, the maximum theoretical precision in current sharing tuning using a 16 bit MCU for the proposed LCLC resonant converter can be calculated as 0.018%, 0.012%, and 0.01% with

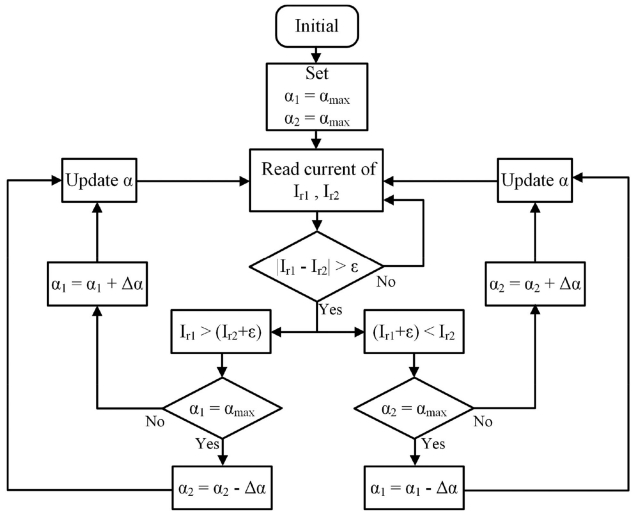

Fig. 14. Current balancing control algorithm flowchart.

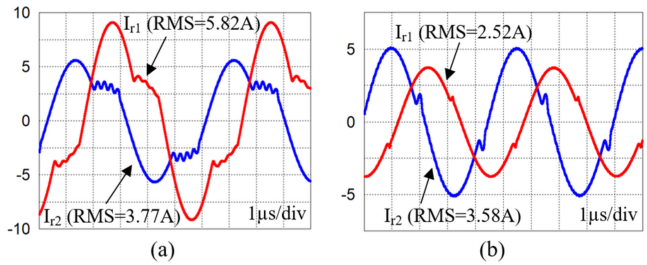

Fig. 15. Simulation results without current balancing at the full-load condition. (a) With 250 V input voltage. (b) With 400 V input voltage.

$C_a = 10$ nF, $C_a = 20$ nF, and $C_a = 30$ nF, respectively. The proposed converter is simulated in PSIM software using the same parameters in theoretical calculation. The resonant current waveforms of both phases are shown in Fig. 13 using $C_a = 20$ nF for the SCC circuit. The rms current difference observed in the simulation is $\Delta_{I_{Lr}} = 0.0017$ A, and hence, the precision of current balancing will be calculated as 0.037%. It should be mentioned that because of using FHA in the calculations, the difference with simulation results is considerable that is because of the large inaccuracy of FHA at frequencies far below f_r.

IV. Proposed Control Strategy for Interleaved LCLC Resonant Converter

Key operational waveforms of the proposed interleaved LCLC resonant converter with SCC current sharing is shown in Fig. 12. It is considered that the load share in phase 2 is smaller than phase 1 in the demonstrated condition, and hence, a smaller SCC angle is needed on phase 2 to compensate for the current difference, (i.e., α_2 smaller than α_1). As illustrated in Fig. 12, the zero-current crossing (ZCC) instants of the resonant current needs to be monitored for both phases to synchronize the turn ON time of the SCC switches.

Fig. 13 illustrates the implemented digital control scheme for the proposed interleaved LCLC resonant converter. The LCLC tank resonant current is sensed via a small current-transformer

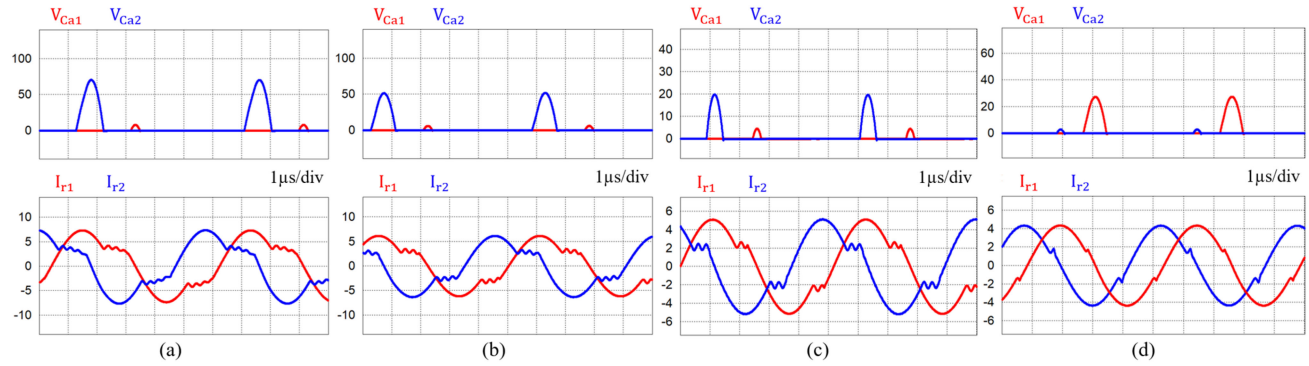

Fig. 16. Simulation results with current balancing at the full-load condition. (a) With $V_{\rm in} = 250$ V. (b) With $V_{\rm in} = 500$ V. (c) With $V_{\rm in} = 350$ V. (d) With $V_{\rm in} = 400$ V.

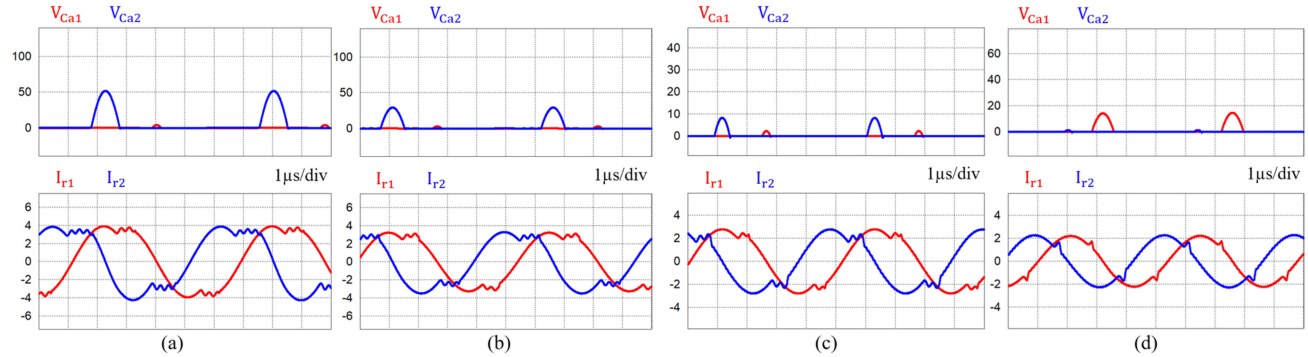

Fig. 17. Simulation results with current balancing at the half-load condition. (a) With $V_{in} = 250$ V. (b) With $V_{\rm in} = 500$ V. (c) With $V_{\rm in} = 350$ V. (d) With $V_{\rm in} = 400$ V.

(CT) on each phase to realize the load balancing between the paralleled phases. Then the resonant currents are rectified, amplified, and filtered to take the scaled average value out. To avoid constant changing of the α angle in the control algorithm, the average value of the sensed current is found over a specific time, (i.e., 100–200 μs) and it is used for comparison purposes. Then, the appropriate command for current sharing is decided in the MCU, and the α angle of each SCC either increases or decreases according to the control algorithm. In practical implementation, the same CT that is utilized for the current level measurement can be used to synchronize the turn ON of the SCC MOSFET with the current ZCC of each phase. In the proposed LCLC resonant converter, the output voltage level is regulated by a frequency-controlled proportional-integral (PI) loop that is working separately from the current balancing function. The current balancing loop is intentionally made slower than the output voltage loop to have a stable operation during transients. A complete flowchart of the current balancing control algorithm is shown in Fig. 14.

To diminish the impact of the SCC circuit on the normal operation of the LCLC converter, it is desirable to boost the α angle of the higher current carrying phase to its maximum limit and then reduce the α angle of the other phase. Different steps of the current balancing control are as follows.

1) Initially, the α angles of both phases are set at the maximum. If there is an imbalance in the system, the load sharing will be unbalanced.
2) Then, the current share of both phases is measured via the CTs implemented on each phase. Then, the absolute value of the difference between the sensed average currents is checked to be larger than a specified threshold (ε). If the output state of the comparison holds positive for a defined time, the appropriate command to increase/decrease the α angle is generated. The process of balancing will not begin if the sensed currents are close enough, and the process of reading and comparing continues.
3) When the balancing starts, the average of the sensed current of both phases is compared to see which phase has a larger current. Then if this state continues for a couple of switching cycles, the appropriate command for the α angle is generated. Consider the case that the current of phase 1 is larger than the current of phase 2, the SCC angle of phase 1 (the larger current phase) should be checked to be at maximum, if not, the α angle of phase 1 should be increased until getting to the maximum value.
4) After the α angle of the higher current carrying phase gets to the maximum value, the α angle of the other phase should be reduced until the difference between the resonant current of both phases gets smaller than ε. At this point, the α angle will not change further until the absolute current difference is larger than ε.

TABLE I
PARAMETERS FOR BOTH SIMULATION AND EXPERIMENT

Description	Value/Parameter
Power Rating	1 kW
Input Voltage range (V_{in})	250 V – 400 V
Output Voltage (V_o)	12 V
Maximum Output Current (I_o)	80 A
Switching Frequency range (f_s)	170 kHz – 250 kHz
Transformer's Turns Ratio (n)	18 : 1 : 1
Leakage inductance (L_k)	4.2 μH (Ph1) – 4.1 μH (Ph2)
Series-Resonant Inductor (L_s)	13.4 μH (Ph1) - 12.5 μH (Ph2)
Parallel-Resonant Inductor (L_p)	239 μH (Ph1) – 245.6 μH (Ph2)
Series-Resonant Capacitor (C_s)	20 × 1 nF = 20 nF ± 5%
Parallel-Resonant Capacitor (C_p)	5 × 1 nF = 5 nF ± 5%
SCC Capacitor (C_a)	5 × 3.3 nF = 16.5 nF ± 5%
Input Capacitor (C_{in})	120 μF ± 5%
Output Capacitor (C_o)	20 × 47 μF = 940 μF ± 5%
HB GaNs (S_1-S_4)	GPI65015TO - $R_{DS(on)}$=92 mΩ
SR MOSFETs (SR_1-SR_4)	IRLB3813 - $R_{DS(on)}$=1.95 mΩ
SCC MOSFETs (Sa_1, Sa_2)	CSD19536KCS - $R_{DS(on)}$=2.7 mΩ

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Computer Simulation Results

Computer simulation of the proposed interleaved LCLC resonant converter is carried out in a PSIM environment with digital control and using a detailed circuit model similar to the 1 kW laboratory prototype. A list of the parameters and semiconductors used for both simulation and experiment is provided in Table I. Computer simulation results without current balancing are shown in Fig. 15 for both low input voltage and high input voltage conditions to see the effect of slight tolerances in resonant tank components on the current sharing of the interleaved LCLC resonant converter. In the 250 V input voltage condition the larger part of the load is carried by phase 1 and in the 400 V input voltage condition, the larger part of the load is carried by phase 2. The imbalance condition is considerably large for both cases and the resonant current difference is larger in the 250 V input voltage condition. Based on the discussion provided in Section III related to Fig. 7(b), it can be inferred that the voltage gain of the two phases has an intersection somewhere below the resonant frequency.

The simulation results with current balancing control at the full-load condition with different input voltages are shown in Fig. 16. Fig. 16(a) illustrates the resonant currents and SCC capacitor voltages with a 250 V input voltage. As expected from Fig. 15(a), to have a balanced current sharing, more compensation is required in phase 2 that is achieved by the current sharing control method. The α angle decreases based on required impedance compensation on the phase with lower current, hence the SCC capacitor value decreases that leads to an increase in the voltage across it. The maximum α is set to 170° to keep the effective SCC operating range narrow, since close to 180° the impedance compensation is so small. From Fig. 9, it can be observed that even with small SCC capacitor values the resonant current variation is negligible between 170 and 180°. Fig. 16(b) shows the full-load operation with a 300 V input voltage. From Fig. 7(b), the expected required compensation

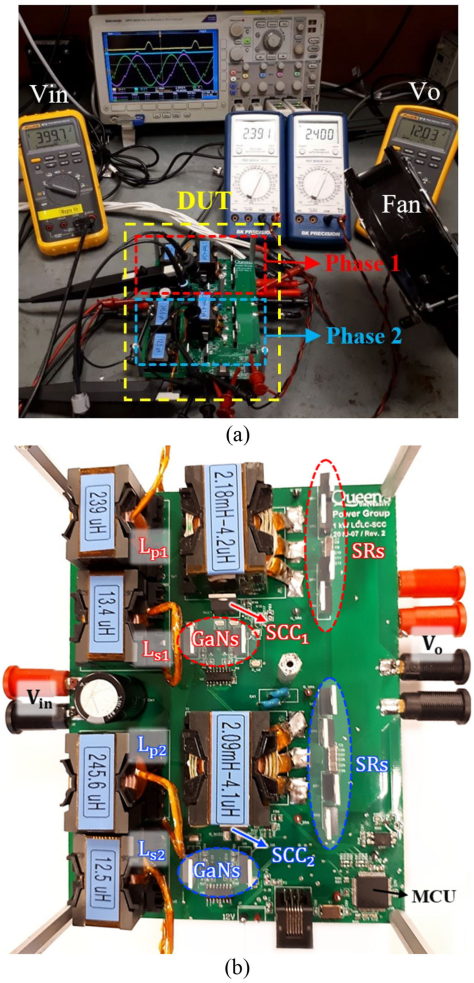

Fig. 18. Photograph of the laboratory prototype. (a) Test setup under the full-load condition. (b) Device under test.

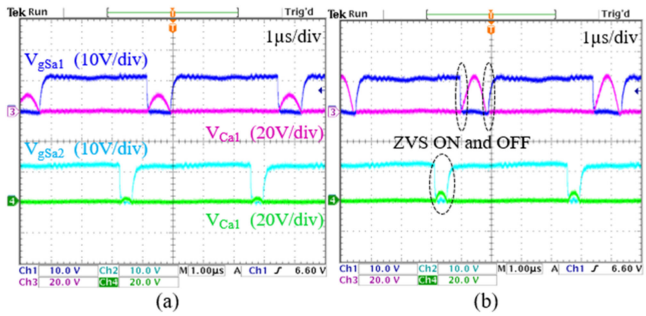

Fig. 19. SCC switching performance. (a) $V_{\text{in}} = 400$ V, $I_o = 40$ A, and $\alpha_1 = 148°$. (b) $V_{\text{in}} = 400$ V, $I_o = 80$ A, and $\alpha_1 = 151°$.

in phase 2 is less than in the case with 250 V as the voltage gain difference gets smaller when the switching frequency increases. The mentioned phenomenon can be observed from the reduced voltage stress across C_{a2}. Fig. 16(c) shows the full-load condition with a 350 V input voltage. Since the voltage stress across the SCC capacitor is small on both phases it can be inferred that the operating point is just below the crossing frequency (f_{cross}) related to the intersection of voltage gains and

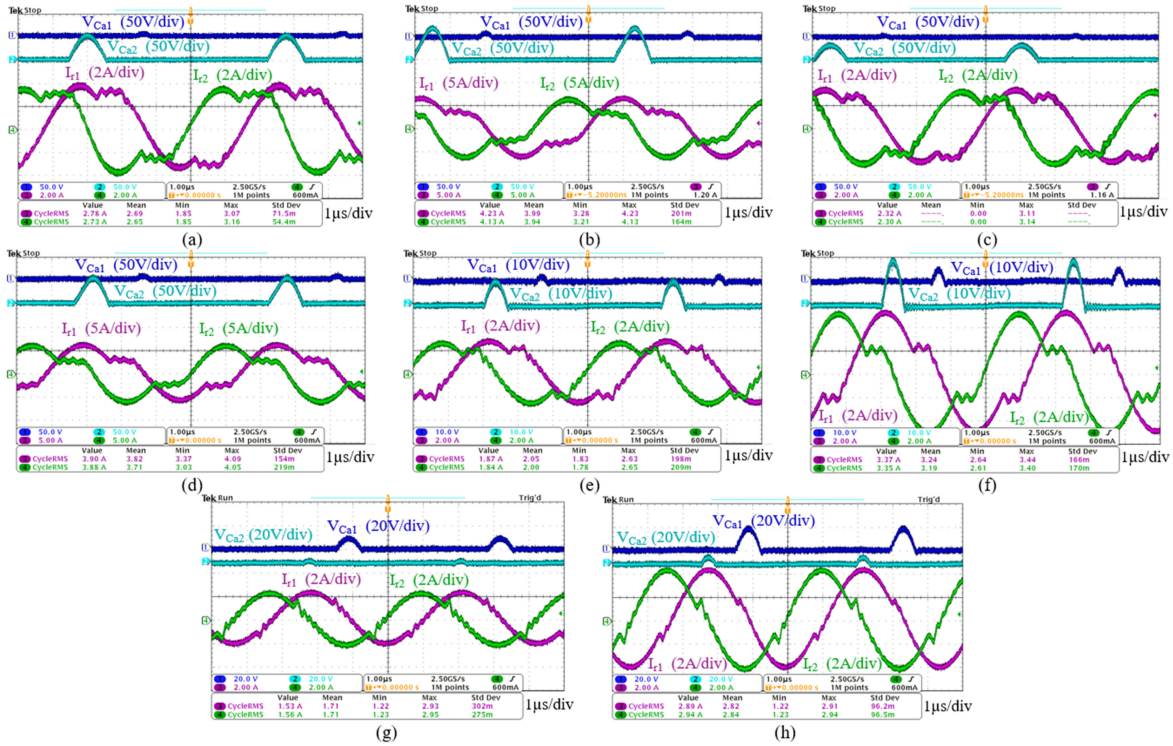

Fig. 20. Experimental results with current balancing. (a) Half-load with $V_{\rm in} = 250$ V. (b) Full-load with $V_{\rm in} = 250$ V. (c) Half-load with $V_{\rm in} = 300$ V. (d) Full-load with $V_{\rm in} = 300$ V. (e) Half-load with $V_{\rm in} = 350$ V. (f) Full-load with $V_{\rm in} = 350$ V. (g) Half-load with $V_{\rm in} = 400$ V. (h) Full-load with $V_{\rm in} = 400$ V.

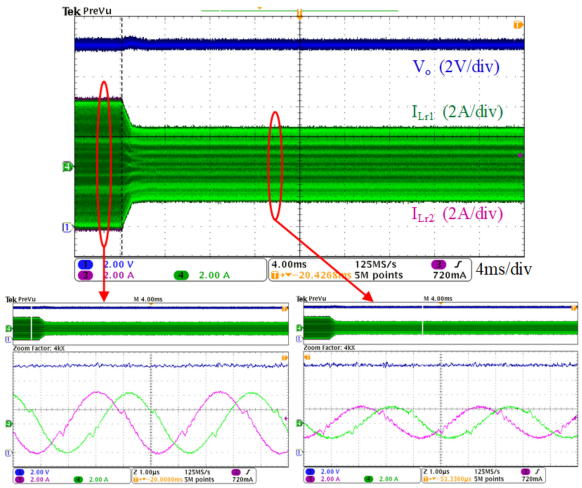

Fig. 21. Load step change from full-load to half-load with $V_{\rm in} = 400$ V.

the difference is small at the switching frequency. Fig. 16(d) shows the full-load condition with a 400 V input voltage. As expected from Fig. 15(b), more compensation is required in phase 1 to have a balanced current sharing, which is achieved by the current balancing control. The operating frequency with a 400 V input voltage is between the crossing frequency and the resonant frequency of both phases. Fig. 17(a) to (d) show the resonant currents and SCC capacitor voltages at the half-load condition with 250 to 400 V input voltages, respectively. The observed trend in current balancing at half-load condition is likewise the full-load condition but with less gain compensation requirement, which corresponds to less voltage gain imbalance at half-load operation.

B. Experimental Results

A laboratory prototype is built and tested to verify the analysis and simulation results. A low-cost MCU from Microchip, dsPIC33FJ32GS608, is used for digital control implementation. Fig. 18 demonstrates the test setup under full-load operation and a close view of the laboratory prototype. In the prototype, E-mode GaN switches with the TO-220 package are used for the primary side bridges, and for consistency, the same package of the switch is used for synchronous rectifiers (SRs) and SCC MOSFETs. Furthermore, the resonant inductors for each phase are intentionally made with different values to observe the abnormal voltage gain condition between the two phases with an intersection below the resonant frequency. It should be noted that high turn ratio CTs are used in practice to reduce the effect of possible mismatch. Moreover, to further reduce the current sensing loops mismatches, 0.1% resistors and C0G/NP0 capacitors are used for the amplification of the sensed signal.

The SCC capacitor voltage of both phases along with the gate pulses for the SCC MOSFETs are shown in Fig. 19 for both half-load and full-load conditions. It can be observed that the SCC MOSFETs are turned ON and OFF with ZVS condition and hence there are no switching losses. Moreover, as the voltage stress of SCC MOSFET can be designed to be below 100 V, small drain-source on-resistance MOSFET (e.g., $R_{\rm DS(on)} = 2$–5 mΩ)

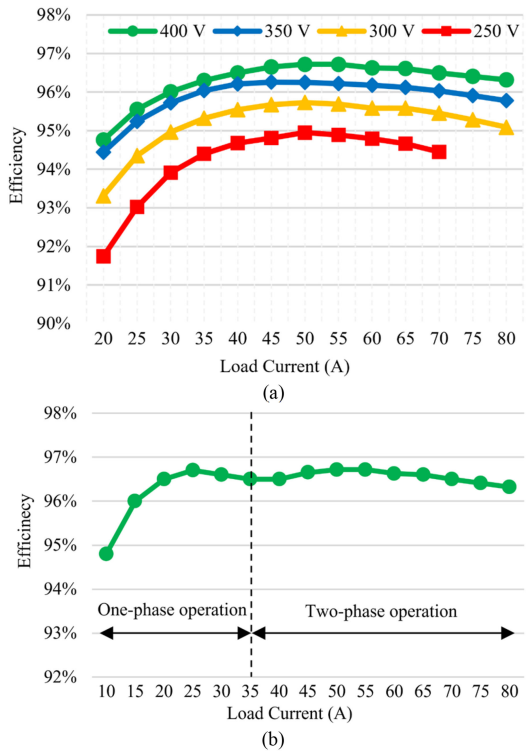

Fig. 22. Experimentally measured efficiency of the proposed interleaved LCLC converter (a) for different input voltages and (b) for 400 V input voltage condition.

can be implemented, so the conduction loss is negligible. Therefore, the effect of the SCC circuit on efficiency is not significant. Fig. 20(a) and (b) illustrates the steady-state experimental results of the resonant current and SCC capacitor voltage with 250 V input voltage at half-load and full-load conditions, respectively. As discussed earlier in the article, the required SCC compensation is the maximum near peak voltage gain, hence at the full-load condition the SCC capacitor voltage stress on phase 2 is around 75 V. Fig. 20(c) and (d) illustrates the steady-state experimental results with 300 V input voltage at half- and full-load conditions, respectively. The voltage stress on the SCC capacitor is lower than the previous case as the voltage gain is less at the frequency associated with 300 V input voltage. Fig. 20(e) and (f) illustrates the steady-state experimental results with 350 V input voltage at half-load and full-load conditions, respectively. As can be observed the voltage stress on the SCC capacitor on both phases is below 20 V, which means the voltage gain of both phases is close to each other at the switching frequency associated with 350 V input voltage conditions. Fig. 20(g) and (h) illustrates the steady-state experimental results with 400 V input voltage at half-load and full-load conditions, respectively. In this case, the SCC capacitor voltage for phase 2 is around 20 V and for phase 1 is lower than 10 V. As discussed in the simulation section, here, the operating frequency is between f_{cross} and f_r and the voltage gain of phase 1 is lower than the voltage gain of phase 2 at the switching frequency.

It can be observed from the experimental results shown in Fig. 20 that the proposed interleaved LCLC resonant converter can actively balance the current between both phases for different input voltages and load conditions. Furthermore, the SCC operating angle for the phase that carries a higher load current is kept at the highest value to diminish the asymmetric impact of the SCC circuit operation. Overall, all the operating points from 250 to 400 V input voltages are in accordance with the theoretical analysis and computer simulation results. The dynamic response of the proposed interleaved LCLC converter due to a load step change is shown in Fig. 21. In this test, the converter is operating with 400 V input voltage and regulating the output voltage to a fixed 12 V at 80 A load current where a sudden step load change is performed to 40 A load current. As can be seen, the current balancing is working accurately before and after the step load change. It should be mentioned that the current balancing control is intentionally made much slower than the output voltage loop to achieve an accurate and stable operation for every operating point.

The efficiency measurement of the experimental prototype is carried out for a wide load range with 250 to 400 V input voltages and the result is shown in Fig. 22(a). The proposed interleaved LCLC converter can reach high efficiency with all input voltage and the maximum efficiency recorded is above 96.7%. Fig. 22(b) illustrates the efficiency curve with one phase disabled at light load with a 400 V input voltage. As can be observed a flat efficiency curve with more than 96% can be achieved by phase shedding for a large load range from 15 to 80 A.

VI. Conclusion

An interleaved LCLC converter with accurate current balancing is proposed in this article for wide input voltage applications. The impact of tolerances in resonant elements is considered for the paralleled LCLC resonant converters with normal unidirectional gain variation throughout the operating frequency and with abnormal bidirectional gain variation containing an intersection below the resonant frequency. Moreover, a minimum angle is identified for a reliable and effective operation of the SCC circuit in the proposed LCLC resonant converter. Based on the behavior of the proposed converter, a control strategy is developed and digitally implemented for the interleaved LCLC resonant converter to perform an accurate current sharing at every operating point. A high efficiency 1-kW GaN-based prototype is built to verify the performance of the proposed interleaved LCLC converter. The practical current sharing performance in a wide input voltage range is in correspondence with the analysis and simulation results, which proves accurate current balancing behavior of SCC in resonant converters with steep voltage gain curves over a wide input/output voltage range.

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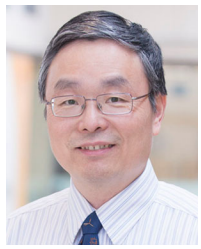

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