Design Techniques of Sub-ns Level Shifters With Ultrahigh *dV/dt* Immunity for Various Wide-Bandgap Applications

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***Abstract*—In high-frequency gate drivers, especially for wide-bandgap applications, hundreds of voltages per nanosecond noise would be generated. Therefore, the sub-ns delay level shifter with high *dV/dt* immunity is necessary for signal conversion among different voltage domain areas. This article presents design techniques for the sub-ns delay level shifter with ultrahigh *dV/dt* immunity. The propagation delay of the proposed floating level shifter is dramatically reduced by utilizing the edge detection technique. In order to further improve the performance, auxiliary pull-up circuit, promoting delay matching, and self-calibration techniques are adopted, which make the proposed level shifters more suitable for high-frequency wide-bandgap applications. The level shifter is fabricated in a 0.5 μm bipolar CMOS DMOS (BCD) process, whose results demonstrate the final level shifter achieves zero static power consumption, a 0.024 mm^2 active area, and *dV/dt* immunity up to 250 V/ns. The measurement results show that the sub-ns delay level shifter can be realized, and the minimum delay is only 664 ps at VSSH 25 V. Its figure of merit is just 0.044 ns/(μm $\times$ V), which is optimal among previous level shifters. The level shifters are also simulated at the 0.18 μm BCD process, and the propagation delay can be decreased by more than 60%.**

***Index Terms*—Auxiliary pull-up circuit, delay matching, *dv/dt* immunity, edge detection technique, high voltage gate driver, level shifter, propagation delay, self-calibration function, wide bandgap applications.**

I. Introduction

With the development of automotive electronics and 5G techniques, there is a considerable demand for high-voltage (HV) power converters with great advantage in high-frequency, high-efficiency, and miniaturization [1]–[3]. It is difficult for silicon (Si)-based power devices to meet these requirements. Hence, wide-bandgap semiconductors represented by gallium nitride (GaN) and silicon carbide (SiC) have been studied gradually, and some achievements have been made in high-frequency and high-power applications [4], [5]. Compared with Si-based power devices, GaN and SiC-based power devices have a lower parasitic effect and higher breakdown field, which indicates that the wide-bandgap semiconductors are more suitable for high-frequency and high-power applications [1]–[9].

In HV power converters, power MOSFET is essential, and it needs a fast HV gate driver. To improve the performance of HV power converters for wide-bandgap power devices, the high-speed full integrated HV gate drivers may be the appropriate solution, which is beneficial to miniaturization [10]–[13]. Fundamental full integrated HV gate drivers include asynchronous gate drivers and synchronous gate drivers. Synchronous gate drivers have a significant advantage in improving efficiency [10]. Nevertheless, in the existing wide-bandgap power device products, SiC-based power devices are mainly used above 1 kV, and the supply voltage usually does not exceed 600 V for GaN-based power devices. Currently, the maximum voltage allowed for commercial integrated processes is less than 1 kV. So, GaN and SiC MOSFETs are often applied to different architectures, as shown in Fig. 1.

As shown in Fig. 1(a), for SiC MOSFET, the high-speed gate driver should use a higher positive voltage, about 15 V, while a negative voltage is needed to suppress noise, about –5 V [14]. To obtain the best driving performance, the thin-oxide lateral DMOS (LDMOS) need be used in the power stage of HV and negative voltage regions, where its Vds can allow high-voltage, but its Vgs should not be more than 5 V. In Fig. 1(a), MP and MN use the thin-oxide LDMOS and 5 V MOSFETs are adopted for the "Buf." Therefore, the HV floating level shifter is required to transfer LV signals to the HV and negative voltage regions [11]–[14]. Furthermore, the HV floating level shifter is one of the core technologies of the high-speed gate driver for SiC MOSFET. SiC MOSFET with small parasitic capacitors has a very fast switching speed and therefore produces a huge *dV/dt* noise. In order to optimize the switching characteristics of SiC MOSFET, a multilevel drive design method is used, in which the information of SiC MOSFET is sampled and fed back to the gate driver to achieve high speed and low noise switching [4]. This requires relevant circuits to respond quickly and control the switching state of SiC MOSFET. Therefore, the level shifter, which is the core block of SiC MOSFET's gate driver, needs a

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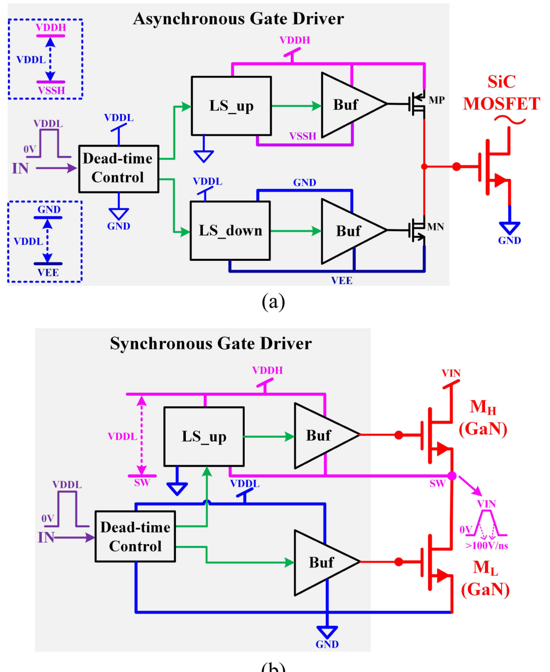

Fig. 1. Basic HV gate drivers for wide-bandgap MOSFET. (a) Asynchronous gate driver for SiC MOSFET. (b) Synchronous gate driver for GaN MOSFET.

very small delay, preferably below ns. For GaN, its switching speed and operating frequency are getting higher and higher as described in [2] and [13]. Then, a sub-ns level shifter is also needed. At the same time, the reference voltage of the HV region for GaN gate drivers is V_{SW}, which could switch between GND and VIN. Therefore, the HV reference voltage of the level shifter in Fig. 1(b) varies from GND to VIN, while its HV power supply maintains a constant value with V_{SW}, about VDDL. According to [13], for GaN MOSFET, the *dV/dt* of node SW could reach more than 200 V/ns. Hence, in the synchronous gate driver for GaN MOSFETs, the HV floating level shifter not only requires a sub-ns delay but also has a higher *dV/dt* immunity [13]. In a word, for wide-bandgap applications, the HV floating level shifter has two most essential requirements, one is a sub-ns delay, and the other is ultrahigh dV/dt immunity.

In previous research works, many HV floating level shifters have been introduced. The generic structure of HV floating level shifter is presented in [8], where DMOS cascode transistors are used to protect the LV MOSFET in HV and LV regions. Although this structure can transform the signal from an LV region to an HV region, its response speed is very slow. Other similar architectures have improved the response speed to about a few nanoseconds [9], [15], [16]. In these level shifters, there is a fast path and a slow path, and its delay can be influenced by the parasitic capacitance of the HV MOSFETs in the slow path. So, the delay of level shifters [9], [15], [16] is usually above nanoseconds. In [17], the level shifter uses resistors to clamp HV signals, which requires a compromise between delay and power consumption. Moreover, the delay of the level shifter is also above nanosecond [17]. Then, based on [8], [9], [15], and [16], the topology presented in [18] accelerates transient response of the slow path by utilizing a pull-up circuit and logic circuit. The delay can be shrunk to 2.2 ns. The circuits presented in [19] also adopts the same architecture and realizes a 3 ns delay. For the above level shifters, it is very difficult to achieve a sub-ns delay. Besides, the *dV/dt* immunity is also not mentioned. High *dV/dt* immunity of reported level shifters are 20 V/ns in [20], 50 V/ns in [2], 75 V/ns in [21], where *dV/dt* immunity is not enough for wide-bandgap applications. Then, the level shifter in [22] has 120 V/ns slew immunity. Certainly, the *dV/dt* immunity has been improved greatly, but their response speed is slow. In order to realize a sub-ns delay level shifter, the short pulse generator and high bandwidth current mirror are introduced to achieve zero static power consumption and fast response speed [12]. Its delay can be reduced to 370 ps at a 0.18 μm process. Nevertheless, its *dV/dt* immunity is only 30 V/ns. To improve *dV/dt* immunity, Liu *et al*. in [13] use complicated circuits based on [12], which achieves a sub-ns delay and ultrahigh *dV/dt* immunity. However, additional power supply circuits, HV power supply, and complex circuits are also needed in [13], which could increase the chip area and complexity of the design.

There are various problems with the previous level shifters in order to achieve the sub-ns delay and high *dV/dt* immunity. This article proposes the new design techniques to realize sub-ns delay level shifters with ultrahigh *dV/dt* immunity. The edge detection technique is used for decreasing the propagation delay. Besides, for wide-bandgap applications, such as high frequency, narrow pulsewidth, and feedback signal of power MOSFETs, the level shifter needs to handle the above problems well. Therefore, several design techniques, for example, delay match, shorten switching time and dynamic consumption power, and self-calibration function, are applied to the level shifter to improve its performance. These proposed level shifters are better fit for different wide-bandgap applications, such as high-speed driving circuits with operating frequencies of tens of MHz, and closed-loop multilevel gate driver, etc. The proposed level shifter realizes an ultrahigh *dV/dt* immunity without the complex auxiliary circuit. Measurement results show that the level shifter achieves the lowest figure of merit (FOM) among reported HV level shifters, only 0.044 ns/(μm $\times$ V) and a 664 ps average propagation delay for VSSH of 25 V under the 0.5 μm bipolar CMOS DMOS (BCD) process.

The rest of the article is organized as follows: Section II describes the proposed HV floating level shifter. Section III shows the improvements in the proposed level shifter in order to meet various wide-bandgap applications. Then, the *dV/dt* immunity of the proposed level shifters has been analyzed in Section IV. Section V discusses measurement results and comparison to previous works. Finally, the conclusion is demonstrated in Section VI.

II. Proposed Level Shifter

In the cross-coupling level shifter [18], during every transition of its input signal, one path of the level shifter is pulled down quickly, and the other path is pulled up at the lowest speed, which is called the fast path and the slow path, respectively. However, the delay in the conventional HV floating level shifter

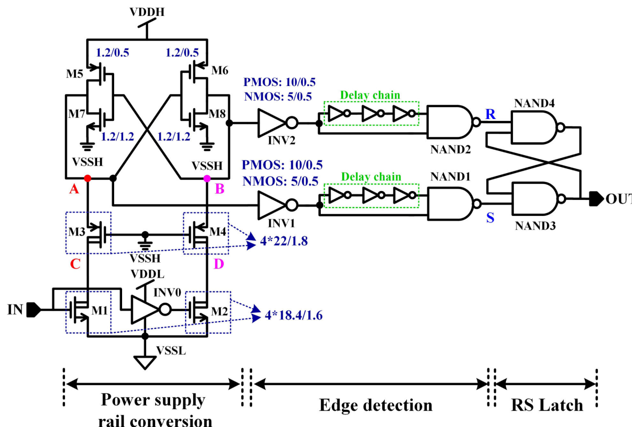

Fig. 2. Schematic of the proposed level shifter.

is determined by the slow path. In [18], the transient response of a slow path could be accelerated by auxiliary pulling-up circuits to reduce the propagation delay. For the proposed level shifter, the propagation delay is just related to the fast path, which can reduce the delay of the level shifter significantly. Therefore, compared with [18], the proposed level shifter can realize a smaller delay.

The proposed HV floating level shifter is shown in Fig. 2, which is composed of three parts: power supply rail conversion, edge detection, and RS latch. Power supply rail conversion is used to transform signals from the LV region to the HV region, and then the edge detection senses the signal of a fast path rapidly. The RS latch locks the output signal until the next input signal transition. In Fig. 2, VSSH is connected to the gate of M3 and M4, which can isolate signals between the HV region and the LV region. M1–M4 use 30 V LDMOS, and the others are isolated 5 V MOSFET. VDDL-VSSL and VDDH-VSSH are power supply rails of LV and HV regions, respectively, where HV and LV regions have the same power supply rail voltage. In this article, the power supply rail voltage is set at 5 V, and VDDH can be up to 30 V.

A. Dynamic Operation of the Proposed Level Shifter

The mechanism of the proposed level shifter is described as shown in Fig. 3, in which the low-to-high switching and the high-to-low switching operation can be demonstrated.

In Fig. 3(a), the low-to-high switching operation of the proposed level shifter is shown. Before IN goes high, V_A and V_C are VDDH, V_B is VSSH, and V_D is VSSL. During signal transmission, the following sequence takes place.

1) When IN goes high, the power supply rail conversion is active. M1 switches ON, V_C begins to drop rapidly, and V_A follows V_C. The delay in this process is called t_{r1}. Because M1 and M3 have enough pull-down capacity, the response speed of nodes A and C is fast. So, t_{r1} is minimized.
2) The edge detection circuit samples the falling edge of node A. When V_A becomes low, the output of INV1 becomes high, and the low short pulse, V_s is generated by NAND1 and delay chain. The t_{r2} is a delay of the edge detection circuit. The delay of INV1 and NAND1 determines it.

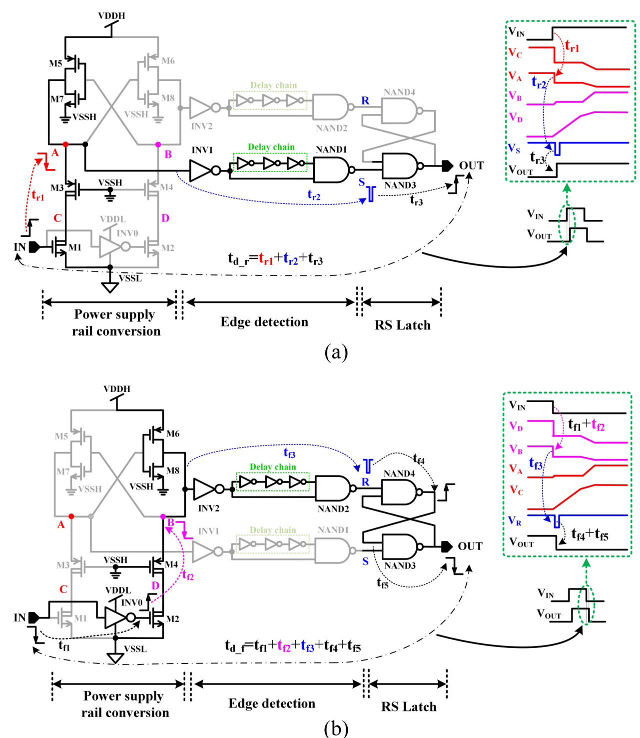

Fig. 3. Switching operation of the proposed level-shifter. (a) Low-to-high switching operation. (b) High-to-low switching operation.

3) Due to the low short pulse V_S, NAND3 responds. The low-to-high transition of OUT completes, and OUT remains VDDH until the low short pulse occurring at node R. The delay between V_S and OUT is described by t_{r3}. The delay of NAND3 is also t_{r3}.

During the low-to-high switching operation, M1 and M3 are ON, and M2 and M4 are OFF. So, nodes B and D could rise by M6, which is the slow path. V_A becomes low quickly, M6 is turned ON, nodes B and D could be pulled up slowly. When V_D is smaller than V_B, M6 is ON, and M4 also generates a small current. At this stage, V_D is charged by the small current of M6, and V_B could maintain a low voltage. After V_D is close to V_B, the positive feedback loop composed of M5–M8 begins to take effect. In the end, V_B and V_D go up to VDDH, and V_A and V_C continue to go down to VSSH and VSSL, respectively. In this case, there is no falling edge at node B, so the R of latch remains high and the output of latch keeps high.

As shown in Fig. 3(a), the rising delay of the level shifter, t_{d_r}, is made up of t_{r1}, t_{r2}, and t_{r3}, in which t_{r1} is very tiny, $t_{r2,}$ and t_{r3} are only the delay of three logic gates. Therefore, the level shifter can achieve an ultrafast response speed, and the process node determines t_{d_r}. According to the above analysis, the level shifter's rising delay is only dependent on the response speed of the fast path (nodes A and C) by utilizing the edge detection technique.

For a high-to-low switching operation, a similar operation happens, as shown in Fig. 3(b). The falling delay of the level shifter, t_{d_f}, is made up of t_{f1}, t_{f2}, t_{f3}, t_{f4}, and t_{f5}. Due to the symmetry of the proposed level shifter, t_{r1} is equal to t_{f2}, t_{r2} is equal to t_{f3}, and t_{r3} is equal to t_{f4}. Compared with t_{d_r}, t_{d_f} is

added with t_{f1} and t_{f5}, which are the delay of INV0 and NAND4, respectively. So, in the proposed level shifter, t_{d_f} is larger than t_{d_r}, which makes delay matching decrease.

B. Device Sizes and Simulation Results of the Proposed Level Shifter

In order to achieve the level shifter with high speed, the main design algorithm is as follows.

1) All devices use minimum length allowed to reduce parasitic capacitance.
2) M1 and M2 should adopt a larger size to pull down nodes C and D quickly.
3) The low-to-high switching operation is taken as an example to illustrate the design method of M3–M8.

When IN goes high, node A could be pulled down quickly and lower than the trigger voltage of INV1 as described in Section II-A. To make V_A lower than the trigger voltage of INV1, the current capacity of M3 needs to be higher than that of M5. However, a large size of M3 can also reduce the response speed of node A due to a larger parasitic capacitance of LDMOS. Therefore, the design method of M3 and M5 is as follows: M5 chooses the minimized size allowed, and the size of M3 ensures that the drop of node A is sufficient to be lower than the trigger voltage of INV1. Of course, sizes of M4 and M6 are the same as above.

Before IN goes high, V_B is pulled down to VSSH by M2. When IN becomes high, V_B maintains low. Therefore, after A drops and stabilizes below the trigger voltage of INV1, M5, M6, and M8 are ON and M7 is OFF. V_B and V_D could be pulled up to VDDH by M6 as described in Section II-A. Therefore, the current capacity of M8 should be less than that of M6. Since M6 adopts the minimum width and length, M8 uses the minimum width and appropriate length to reduce the current capability. Similarly, M7 has the same size as M8.

In summary, the size relationship of M3–M8 is as follows: $(W/L)_{M3–M4}$ is the largest, $(W/L)_{M5–M6}$ is medium, and $(W/L)_{M7–M8}$ is the minimum.

4) The ratio (W/L)p/(W/L)n of logic gates is equal to 2 so that the trigger voltage is half of the supply voltage. Then, the logic gates can inhibit noise disturbance. At the same time, the sizes of INV1 and INV2 should be appropriately enlarged to enhance the response speed of NAND1 and NAND2.

From the above design algorithm, device sizes of the proposed level shifter are shown in Fig. 2. In this article, the 0.5 μm BCD process is used. In this process, the minimum channel length of 5 V MOSFET is 0.5 μm, but the minimum channel width of 5 V MOSFET is not less than 1.2 μm, which could increase the propagation delay of the proposed level shifter. Under the condition that the proposed level shifter achieves a low delay, the design considerations for *dV/dt* immunity are also needed, which can be described in detail in Section IV.

Fig. 4 shows simulation results of the propagation delay of the proposed level shifter and the ultrafast mode level shifter in [18]. Fig. 4(a) and (b) shows the rising and falling waveforms, respectively. The ultrafast mode level shifter in [18] is verified at

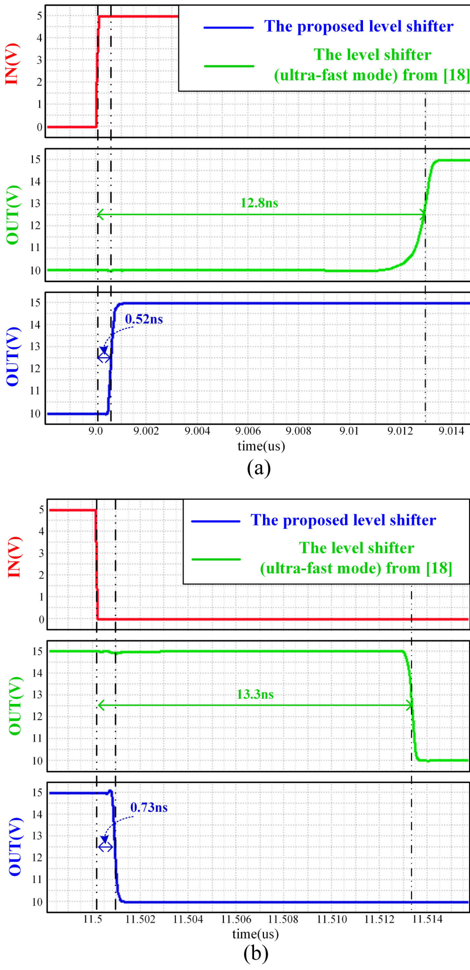

Fig. 4. Simulation results of the level shifter's propagation delay from [18] and this article, respectively. (a) Rising delay. (b) Falling delay.

the process in this article, where $(W/L)_{P/NMOS}$ of all MOSFETs is the same as [18]. Simulation results show that rising and falling delays of the proposed level shifter are 520 and 730 ps, respectively. The propagation delay is reduced by 20 times. However, compared with the simulation results in [18], after adopting the process in this article, the delay of the ultrafast mode level shifter increases by more than four times. This is because the ultrafast mode level shifter uses the 0.35 μm HV CMOS process, in which the minimum width and length of LV MOSFET are 0.35 μm. In the process of this article, the minimum length of LV MOSFET is enlarged by more than 1.4 times, while its width is increased by more than 3.4 times. Besides, the length of LDMOS is also increased by more than 2.2 times. Therefore, using the process in this article, the size of MOSFETs for the ultrafast mode level shifter in [18] can be greatly increased, the parasitic capacitance is also increased, and then the response speed could be dramatically reduced.

C. Influence of Process Node on the Proposed Level Shifter

As mentioned earlier, the delay of the proposed level shifter only depends on the delay of logic gates, which is determined by the process node. The 0.5 μm BCD process used has a large

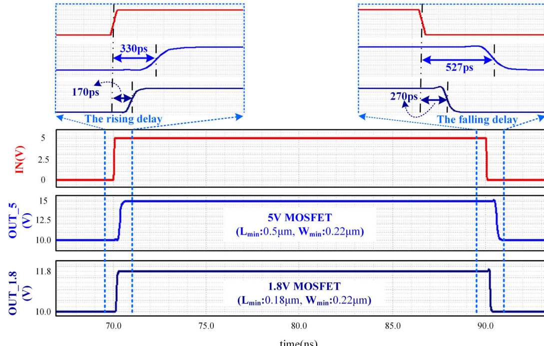

Fig. 5. Simulation results of the proposed level shifter at the 0.18 μm BCD process.

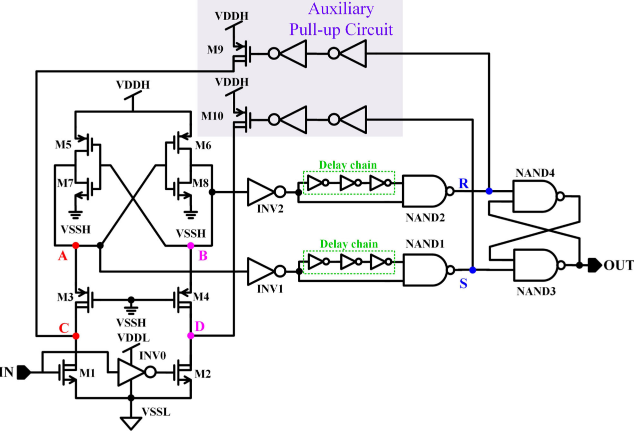

Fig. 6. Proposed level shifter improvement I-LS_I.

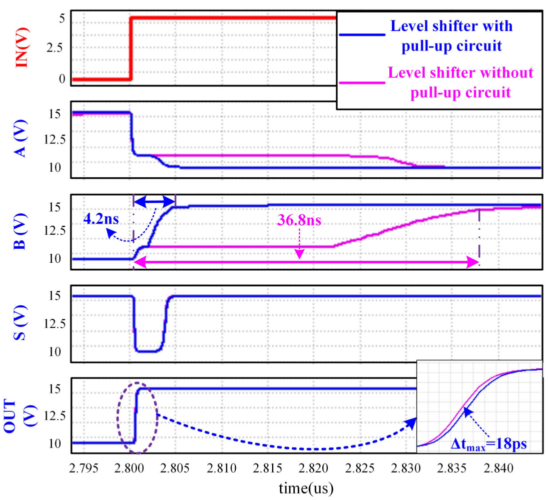

Fig. 7. Simulation results of LS and LS_I.

width, which would increase the propagation delay. Then, the 0.18 μm BCD process is used at the same simulation conditions to demonstrate the effect of the process node. Minimum width and length of 5 V MOSFET are 0.22 and 0.5 μm in the 0.18 μm BCD process. The minimum length of 5 V MOSFET is the same as that in the 0.5 μm BCD process. For 1.8 V MOSFET, the minimum width and length allowed are 0.22 and 0.18 μm. Then, the proposed level shifter is verified in the HV region with 1.8 and 5 V MOSFETs, respectively.

Fig. 5 shows the simulation results of the level shifter at the 0.18 μm BCD process. Using 5 V MOSFETs, the rising and falling delay is less than 600 ps and has been reduced by 36.5% and 27.8%, respectively, which is because a minimum width of 5 V MOSFET is only 0.22 μm under the 0.18 μm BCD process. Using the 1.8 V MOSFET transistors, the rising and falling delay can be reduced by more than 60%, which are only 170 and 270 ps, respectively.

The same level shifter architecture is verified under different sizes of processes, and the propagation delay is significantly improved under the smaller process node. The above analysis and simulation results are sufficient to demonstrate that the proposed level shifter architecture has excellent advantages.

III. Design Improvements of the Proposed Level Shifter

In Section II, although the proposed level shifter can achieve a sub-ns delay, it still has some disadvantages. For example, the rising/falling delay has a noticeable difference in the larger process nodes. At the same time, the response speed of slow paths needs a long time, which could increase the dynamic power consumption and also reduce the maximum working frequency of the level shifter. In this section, a series of design improvements have been presented so that better performance level shifter can be applied for wide-bandgap applications in different scenarios. The following level shifters are simulated under the 0.5 μm BCD process, which are also applicable to other processes.

A. Improvement I—Reducing Setup Time and Dynamic Power Dissipation

For wide-bandgap applications, as shown in [20], switching frequencies may be up to more than 10 MHz, and the turn-ON time of power transistor is less than 10 ns. Switches of the gate driver, including the level shifter, must be completed within a few nanoseconds. The proposed level shifter has a sub-ns delay, but the response speed of slow paths is very long, which can limit the maximum operating frequency. Auxiliary pull-up circuits can be used to charge the slow path during every transition, and the response speed of the slow path can be accelerated significantly. So, the level shifter can be applied to high frequencies, and the above problem can be solved well. This improvement of the proposed level shifter is called LS_I, and the schematic is shown in Fig. 6. In the LS_I, M1 and M2 have a strong pull-down capacity, so the auxiliary pull-up circuit is added at nodes C and D to decrease the parasitic capacitance influence. Using the method mentioned, the LS_I not only can increase the response speed of the slow path but also can reduce the average power consumption. Besides, the pull-up circuit can also improve the *dV/dt* immunity, which is analyzed in detail in Section IV.

Due to the symmetry of the level shifter, the low-to-high transient is only simulated in Fig. 7. The simulation result shows that the charging time of a slow path can be reduced at 4.2 ns in the LS_I, while more than 30 ns charging time is generated in the proposed level shifter without the auxiliary pull-up circuit. Besides, although the peak current of LS_I increases, its average

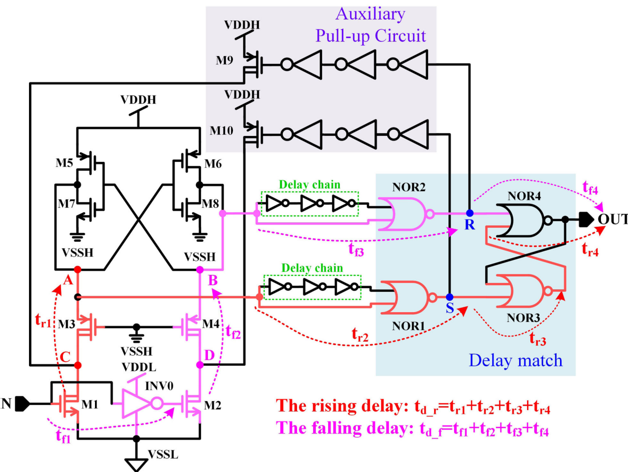

Fig. 8. Proposed level shifter improvement II-LS_II.

current consumption still is reduced, from 56.1 to 19.9 μA. In fact, for high-power converters, especially for wide-bandgap applications, power consumption has a limited impact. The proposed level shifter can realize zero static power consumption, so its influence is smaller or even ignored. Compared with the level shifter without auxiliary pull-up circuits, the propagation delay of the LS_I have a slight increase. Hence, the proposed level shifter with pull-up circuits is more suitable for narrow pulse width in high-frequency gate drivers.

B. *Improvement II—Improving Delay Matching*

In high-speed gate drivers, inferior delay matching of the level shifter can lead to duty cycle distortion of the control signal, especially for high-frequency and smaller duty cycle applications. So, the level shifter needs not only a sub-ns delay but also a good delay matching. As mentioned in Section III-A, the switches frequency in the high-speed gate driver is more than 10 MHz. For wide-bandgap gate drivers, the several-hundred picoseconds delay matching of the level shifter also causes a significant distortion. For example, the switches frequency is 10 MHz, and the duty cycle is 10%. Then, 0.5 ns delay matching can cause a 5% distortion. Furthermore, with the duty cycle decreasing, a better delay matching level shifter is demanded. The delay of logic gates determines the delay of the proposed level shifter. Therefore, the second improvement has been presented to improve delay matching, and its schematic is shown in Fig. 8. LS_II names the level shifter with a second improvement.

The rising delay (t_{d_r}) is composed of a delay of node A (t_{r1}) and three delays of NOR (t_{r2}, t_{r3}, and t_{r4}). The falling delay (t_{d_f}) is made up of a delay of node B (t_{f1}), one delay of INV0 (t_{f2}), and two delays of NOR (t_{f3} and t_{f4}). Nodes A and B have the same delay, and the delay of NOR1–NOR3 has a little distinction. Thus, the difference between delay of INV0 and NOR3 decides delay matching of the LS_II.

Fig. 9 shows the simulation result of LS_II. For the LS_II, the rising delay is 626 ps, and the falling delay is 615 ps, which demonstrates only 11 ps delay matching is obtained. The delay matching can be significantly improved. Because of

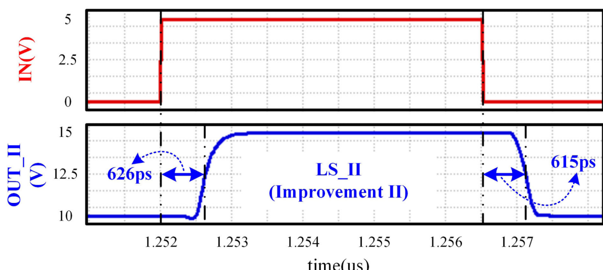

Fig. 9. Simulation results of the delay for LS_II.

the limited driving capacity of pre-NOR, the delay of NOR is longer. Therefore, in LS_II, although INV1 and INV2 have been removed, the rising delay is longer than that of LS_I.

C. *Improvement III—Adding Self-Calibration Function*

Wide-bandgap devices have a lower parasitic capacitor and generate the huge *dV/dt* and EMI noise. Currently, the multilevel gate drivers have been put forward to weaken the EMI noise [23]. For the multilevel gate driver, the flag signal is needed to decide the multilevel driving capacity of the gate driver. Moreover, it is necessary to determine the flag signal according to the state of the power transistor. That needs a closed loop between the flag signal and the gate driver. In the whole closed-loop circuit, once the fault function is triggered during normal operation conditions, all subsequent switching actions would be wrong, which can significantly damage the drive circuit, power devices, and even the entire electronic system. Therefore, as the core block of the multilevel gate driver, the level shifter should have strong robustness and self-calibration to recover normal functions by itself. For many sub-ns delay level shifters, as shown in [12], [13], and [19], use the pulse-trigger mode. However, those level shifters have a fatal disadvantage, which is that the input signal must be a regular pulse signal. For the multilevel gate driver applications, an input flag signal of the level shifter is related to load and power transistor. Therefore, the input signal may not be a regular pulse signal; for example, it maintains a constant voltage during several periods. In the case of input signals at a constant voltage, the output logic of the pulse-trigger level shifter is determined by the previous output state. If the previous output state is wrong, then the pulse-trigger level shifter can always remain in the same wrong state, which is unacceptable.

The level shifter with self-calibration is demonstrated to solve the above problem, as shown in Fig. 10(a), which is referred to as LS_III. The enable signal EN of AND1 and AND2 is used in order to control whether the self-calibration technique is added. Only when EN is high, the self-calibration can be used in LS_III. It should be noted that the enable signal EN is just used to verify the self-calibration technique, and it can be removed in applications. The mechanism of LS_III is similar to LS_I or LS_II, but there is a little difference. The output of LS_III is determined by the signal-select circuit, which is the self-calibration technique. The input of LS_III can operate in two modes, a regular pulse signal, and a nonpulse signal, in which the level shifter can always maintain a right state. The following describes the mechanism of LS_III in detail.

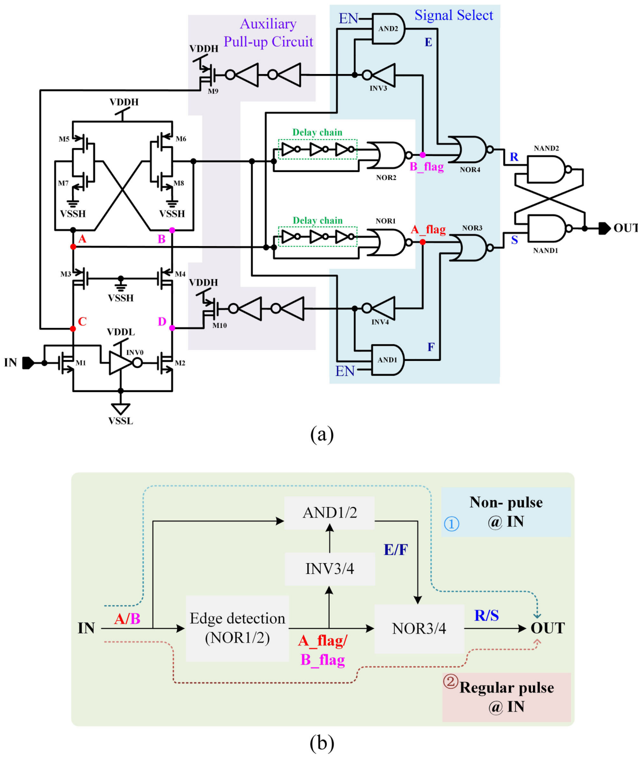

Fig. 10. Proposed level shifter improvement III – LS_III and operating modes. (a) LS_III. (b) Operating modes of LS_III.

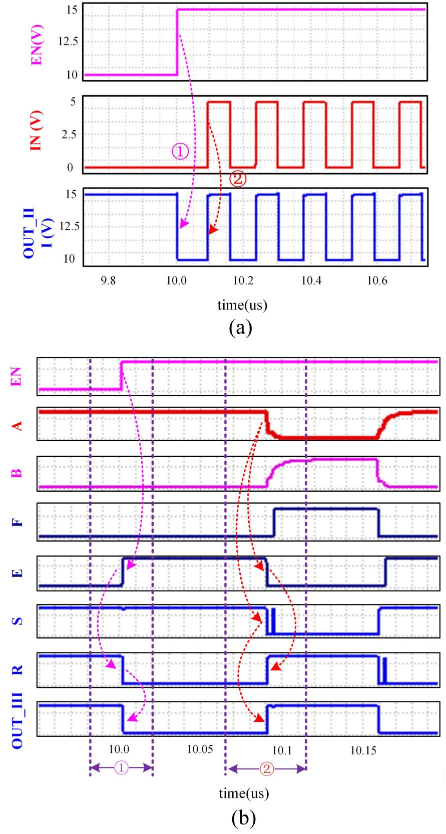

Fig. 11. Simulation results of the LS_III. (a) Whole operation waveform. (b) Detailed waveform.

Fig. 10(b) shows the two operating modes of LS_III. Assuming EN is high when IN is the nonpulse signal, there are no regular falling edges of nodes A and B. Then, A_flag and B_flag may remain low for some time. During this time, OUT of the level shifter still maintains the right state through the signal-select circuit (or path ①), as shown in Fig. 10(b). Due to the low A_flag/B_flag, two inputs of AND1/2 are high. Hence, nodes E and F are following nodes A and B. When IN is high, A is low, and B is high. So, E is low, and F is high. Then, NOR4 generates a high signal at node R, and NOR3 generates a low signal at node S. At last, the OUT can maintain high by the latch NAND1 and NAND2. When IN is low, the analysis is the same as above. For LS_III, whether the output is correct or not, a signal-select circuit can choose E/F to put the output in or recover to the correct state, which is the self-calibration technique. For the closed-loop control system, when the output of LS_III is wrong, it can be recovered in time to ensure the normal operation of the system.

For the regular pulse at IN, the level shifter can still realize a fast response speed by path ②, as shown in Fig. 10(b). Assuming EN is high, taking the IN from low to high as an example, when IN becomes high, as discussed in Section II, node A is low immediately, and node E is low by AND2. Because node B does not go low from high quickly, B_flag keeps low. At this moment, node R recovers high. Then, the edge detection circuit (Delay chain and NOR1) works, and the high short-pulse signal occurs at A_flag. Finally, NOR3 generates a low short-pulse signal at node S, and OUT becomes high. Thus, in this operating mode, the signal-select circuit chooses fast-changing signals, A_flag, guaranteeing the small propagation delay of LS_III.

From the analysis above, it can be seen that no matter what signal at IN, the signal-select circuit can ensure OUT is correct. At the same time, during the start-up stage, the LS_III has the right function, and a start-up circuit or enable signal is not needed, which is needed in [18]. Nevertheless, it should be noted that the LS_III has a shortcoming. Using the signal selection circuit, the propagation delay of LS_III increases about the delay of two logic gates NOR and AND. Of course, the beforementioned shortcoming is not critical to the entire gate driver, which is because the driver usually adopts a multistage driving chain, and the delay of two logic gates is relatively small. Moreover, as the process shrinks and the logic gate delay decreases, the above disadvantages are gradually reduced and even ignored. In a word, the self-calibration technique has an enormous advantage in engineering applications for wide-bandgap power devices.

A closed-loop test circuit with LS_III is needed to verify the self-calibration technique. In this article, the ring oscillator in [18] is utilized, in which LS_III can be as an up-shifter and a down-shifter adopt the convention level shifter without pulse-trigger circuit. LS_III can be better simulated in the closed-loop multi-level gate driver.

The simulation result is shown in Fig. 11. Fig. 11(a) demonstrates the operation of the level shifter from an abnormal state to a correct state. When EN is low, the output of LS_III is in error logic. When EN is high, the operation of the level shifter can

be divided into two parts. One is the self-calibration of LS_III (①), and the other is the regular pulse input signal of LS_III (②). Only the first switching waveform is analyzed, which represents the feedback signal in multilevel gate drivers. The detailed waveform in Fig. 11(b) is adopted to verify the above two modes. The explanation is as follows.

1) *The Nonpulse Signal at IN to Verify the Self-Calibration Technique:* As shown in Fig. 11(b), when EN changes from low to high, the signal-select circuit begins to take effect. Because V_A is high and V_B is low, V_E becomes high, and V_F maintains low. Then, V_R goes low, and V_S keeps high. Therefore, the output of the level shifter, OUT_III, goes low, which demonstrates that LS_III can recover normal function by itself. Hence, as described above, the self-calibration of the level shifter can be achieved through the signal-select circuit.
2) *The Regular Pulse Signal at IN:* As shown in Fig. 11(b), the EN keeps high, and the signal-select circuit can work properly, and the operation of LS_III is similar to the beforementioned level shifter. When IN goes high from low, V_A is low immediately. Then, V_A and V_S become low. At the moment, V_R becomes high. Thus, OUT_III goes high. Then, the conversion of signals has been completed. Of course, the low short-pulse signal occurs at node S due to the slow-response V_B, which is used for the self-calibration function. If the signal-select circuit is not used, the level shifter maintains an error state before the input signal switch. The level shifter in the wrong state affects the entire electronic system.

From the above simulation results, it can be seen that even if the level shifter has errors, it can recover by itself by using a self-calibration technique. The simulation results of LS_III's delay are not shown to make the article concise. Because of NOR3/4 and AND1/2, its delay increases by two logic gates, but the sub-ns delay can also be realized. It is worth noting that the propagation delay of the proposed level shifters can be significantly reduced under the smaller process size, as shown in Section II-C.

IV. *dV/dt* Immunity of the Proposed Level Shifters

As described in Section I, the *dV/dt* noise could be generated in half configuration, which is a challenge for the HV floating level shifter. So, the proposed level shifter not only needs to realize the sub-ns delay but also requires the ultrahigh *dV/dt* immunity, about hundreds of volts per nanosecond. This section mainly analyzes the *dV/dt* immunity of the proposed level shifter in the application of synchronous conversion circuits.

For the proposed level shifters, when there is a *dV/dt* noise at the HV power supply rail, the power supply rail conversion and pull-up circuits are greatly affected, which could lead to the wrong switch of the edge detection circuit. Then, the output of level shifters could be triggered by mistake. Whether IN is high or low, *dV/dt* of HV power supply rail results in a similar transient response owing to the symmetrical level shifter. So, *dV/dt* immunity can be analyzed under the condition that IN is high. Furthermore, nodes with larger parasitic capacitance are more disturbed by *dV/dt* noise. Thus, the parasitic capacitors of LDMOS transistors are mainly considered. Only the power supply rail conversion and the pull-up circuit are presented in order to simplify the analysis, as shown in Fig. 12, in which (a), (c), and (d) are transient operation during a positive *dV/dt,* and (b), (e), and (f) are transient operation during a negative *dV/dt*. The positive and negative *dV/dt* immunity is analyzed as follows.

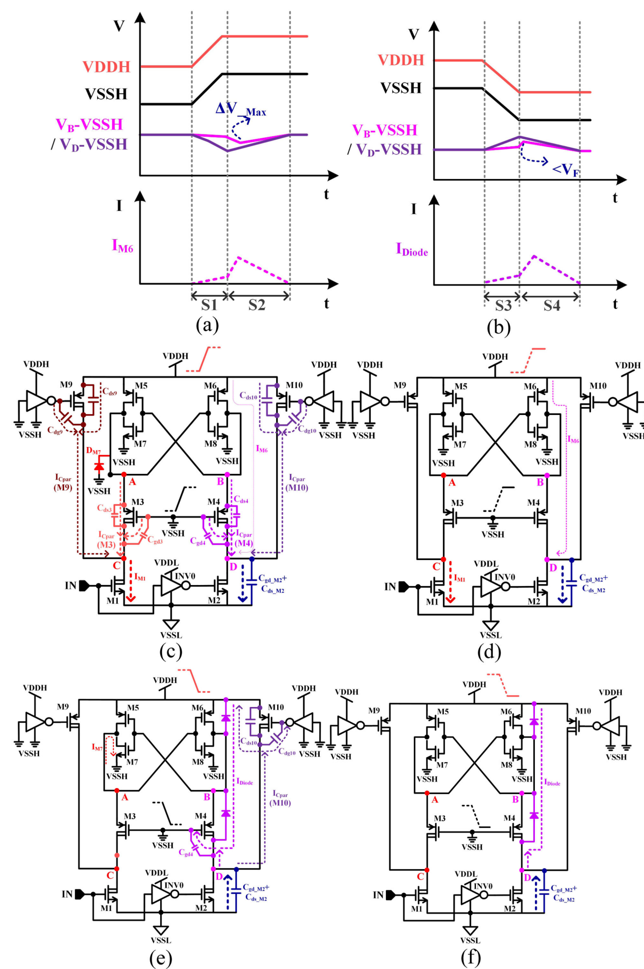

Fig. 12. Transient operation of essential waveform due to *dV/dt* of HV power supply rail, (a) during a positive *dV/dt,* (b) during a negative *dV/dt*, (c) in S1, (d) in S2, (e) in S3, and (f) in S4.

Case A: A Positive dV/dt *of VSSH and VDDH*

As described in Section II, when IN is high, the output of the level shifter could be triggered by mistake, only if node B dropped below the trigger voltage of logic gates. Hence, nodes B and D should be analyzed in detail. The cross-coupled structure formed by M5–M8 is a positive feedback loop, so node A would affect node B. The current could be generated on the C_{ds3} and C_{gd3} of M3 with VSSH and node A rising, which flows into M1. At the same time, due to the pull-up circuit at node C, M1 would have more current. Then, node C could be pulled up. Those current on parasitic capacitors could not increase current at the channel of M3. Therefore, node A keeps low. Besides, node A cannot be lower than a forward diode-drop below VSSH by the

clamping of the body diode of M7, D_{M7}. The above analysis is shown in Fig. 12(c). It can be concluded that when a positive *dV/dt* noise of the HV power supply rail occurs, node A always follows VSSH to rise and maintains low. Therefore, M6 is ON, and M8 is OFF, which can pull up node B to VDDH as far as.

For a positive *dV/dt* of the HV power supply rail, transient operation of nodes B and D can be divided into two stages, S1and S2, as shown in Fig. 12 (a), (c), and (d). S1 is the rising stage of the HV power supply rail, and S2 is the recovering stage of the level shifter. In S1, parasitic capacitors at node D are charged. Charging currents are generated by three paths, I_{M6}, I_{Cpar_M4}, and I_{Cpar_M10}.

I_{M6} is the current on M6 due to the voltage difference between V_B and VDDH. M6 is in the deep-linear state. So, the equation of I_{M6} is as follows:

$$I_{\mathrm{M6}} = \beta_n \times \left(\frac{W}{L}\right)_{\mathrm{M6}} \times (V_{gs} - V_{th}) \times (VDDH - V_{\mathrm{B}}) \tag{1}$$

where $(W/L)_{M6}$ is the width to length ratio of M6 and V_{gs} is equal to VDDH-V_A (the HV power supply rail voltage, 5 V).

I_{Cpar_M4} is generated on the C_{gd4} and C_{ds4}. The difference between dV_{VSSH}/dt and dV_D/dt could generate the current on $C_{gd4,}$ and the current on C_{ds4} is caused by the difference of dV_B/dt and dV_D/dt. Then, I_{Cpar_M4} is described by the following:

$$I_{Cpar_\mathrm{M4}} = C_{gd3} \times \left(\frac{dV_{\mathrm{VSSH}}}{dt} - \frac{dV_{\mathrm{D}}}{dt}\right) + C_{ds3} \times \left(\frac{dV_{\mathrm{B}}}{dt} - \frac{dV_{\mathrm{D}}}{dt}\right). \tag{2}$$

I_{Cpar_M10} is the current of C_{gd10} and C_{ds10}, which is produced owing to the difference of dV_{VDDH}/dt and dV_D/dt. The auxiliary pull-up circuit goes up with the HV power supply rail rise, so, the gate voltage of M10 is equal to VDDH. Then, the expression of I_{Cpar_M10} is shown in the following:

$$I_{Cpar_\mathrm{M10}} = (C_{gd10} + C_{ds10}) \times \left(\frac{dV_{\mathrm{VDDH}}}{dt} - \frac{dV_{\mathrm{D}}}{dt}\right). \tag{3}$$

At the first stage, S1, the gate voltage of M2 is VSSL. Then, node D could be pulled up by charging current on C_{ds2} and C_{dg2}. So, the following can be obtained:

$$(C_{ds2} + C_{dg2}) \times \frac{dV_D}{dt} = I_{\mathrm{M6}} + I_{Cpar_\mathrm{M4}} + I_{Cpar_\mathrm{M10}}. \tag{4}$$

VDDH and VSSH have the same rising rate, so *dV/dt* can represent dV_{VDDH}/dt and *dVSSH/dt*. Charging current on node D is mainly composed of I_{Cpar_M4} and I_{Cpar_M10} due to large parasitic capacitors at the drain of LDMOS. I_{M6} is very small and can be ignored. So, in the S1, dV_B/dt can also be expressed by *dV/dt*. Thus, (2) and (3) can be simplified by the following:

$$I_{Cpar_\mathrm{M4}} = (C_{gd3} + C_{ds3}) \times \left(\frac{dV}{dt} - \frac{dV_{\mathrm{D}}}{dt}\right) \tag{5}$$

$$I_{Cpar_\mathrm{M10}} = (C_{gd10} + C_{ds10}) \times \left(\frac{dV}{dt} - \frac{dV_{\mathrm{D}}}{dt}\right). \tag{6}$$

Then, according to (4)–(6), the expression between dV_D/dt and *dV/dt* is as follows:

$$\frac{dV_{\mathrm{D}}}{dt} = \frac{C_{gd3} + C_{ds3} + C_{ds10} + C_{gd10}}{C_{\mathrm{D2}} + C_{gd3} + C_{ds3} + C_{ds10} + C_{gd10}} \times \frac{dV}{dt} \tag{7}$$

where C_{D2} is the sum of C_{dg2} and C_{ds2}. ΔV_D can be written as follows, which is VDDH-V_D during the rising of VDDH

$$\Delta V_{\mathrm{D}} = \frac{C_{\mathrm{D2}}}{C_{\mathrm{D2}} + C_{gd3} + C_{ds3} + C_{ds10} + C_{gd10}} \times \Delta \mathrm{VDDH}. \tag{8}$$

As described earlier, M1–M4 could have large parasitic capacitors at the drain. When MOS transistors operate in weak inversion or cutoff, C_{gd} is close to zero because the inversion layer contains little charge [24]. In the triode region, C_{gd} reaches its maximum [25]. C_{ds} is the capacitance of the body diode and varies inversely with the square root of the drain–source bias. For the LDMOS transistor M2, when IN is high, Vgs is zero, and Vds is close to VDDH. So, C_{D2}, which includes C_{gd2} and C_{ds2}, has minimal value. M4 is in deep linear, and sizes of P-type MOSFET are more significant than that of N-type MOSFET under the condition of the same drain current. Therefore, compared to the other parasitic capacitors of node D, C_{D2} is very small. Then, (8) obtains a very small ΔV_D.

After the rising of VDDH and VSSH, node D does not increase significantly with VDDH and VSSH. Furthermore, the charging current on parasitic capacitors at node D would be significantly reduced, and I_{M6} is increased. Then, node B can be pulled down, in which logic gates are most likely to be triggered by mistake. The drop of node B is related to the value of V_D and the size of M6. Of course, because the parasitic capacitors of M4 and M10 are huge, the drop of node D is small. Therefore, the possibility of logic gates being triggered by mistake can be significantly reduced. The above operation is the recovering of the level shifter, which is the second stage, S2, as shown in Fig. 12(a) and (d).

According to the above transient operation analysis, the level shifter is the most prone to be triggered by mistake in the S2. Large parasitic capacitors of M4 and M10 would weaken the decline of nodes B and D. It should be noted that the positive d*V*/d*t* immunity of the level shifter can be enhanced by using the pull-up circuit.

Case B: A Negative dV/dt *of VSSH and VDDH*

For the level shifter, a negative *dV/dt* immunity is analyzed by using the same method as the above. The transient operation is described in Fig. 12(b), (e), and (f). Similarly, a negative *dV/dt* of VSSH and VDDH has a limited influence on nodes A and C. Node C is not lower than a forward drop of M1 body diode, and node A can be pull-down close to VSSH through M7 and M3. The transient operation of nodes B and D can also be divided into two stages, S3 and S4, as shown in Fig. 12(b).

During the fall of VSSH and VDDH, C_{gd2} and C_{ds2} discharge. The discharging current has I_{Cpar_M4}, I_{Cpar_M10}, and I_{Diode}. Node D could be pulled down through I_{Cpar_M4} and I_{Cpar_M10}. Hence, nodes B and D decrease with falling of VSSH and VDDH. Because *dV/dt* of nodes B and D is slower than that

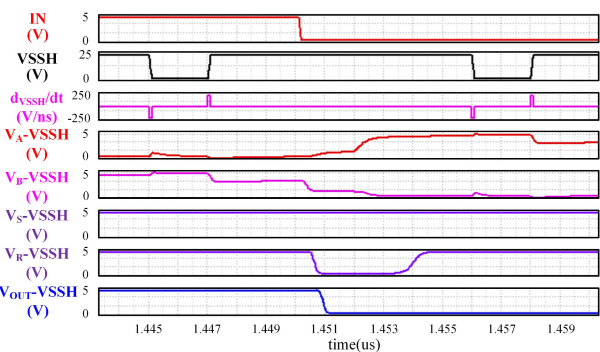

Fig. 13. Simulation results of LS_I with the ±250 V/ns slew rate of HV power supply rail at the 0.5 μm BCD process.

of the HV power supply rail, V_{B} and V_{D} would be higher than VDDH. That cannot make the level shifter to trigger by mistake. However, the more significant overshoot of nodes B and D may damage other devices. In the proposed level shifters, the overshoot of nodes B and D can be limited by a diode forward drop by body diode of M4 and M6, which can ensure that the voltage of devices is within a safe operating range. Furthermore, in this stage, I_{Cpar_M4} and I_{Cpar_M10} are large, so I_{Diode} is very small. Then, the overshoot of nodes B and D is tiny. The above transient operation is the third stage, S3, as demonstrated in Fig. 12(b) and (e). After the VSSH and VDDH drop, nodes B and D can recover to VDDH by the current on the body diode of M3 and M6. That is the fourth stage, S4, in Fig. 12(b) and (f).

To demonstrate the ultrahigh *dV/dt* immunity of the level shifter with the pull-up circuit, the ±250 V/ns slew rate of the HV power supply rail is simulated, as shown in Fig. 13. When the input signal of level shifters is high and low, respectively, ± 250 V *dV/dt* occurs in the HV power supply rail. Under the condition that IN is high when a negative 250 V/ns *dV/dt* occurs, node A is higher than VSSH, which has little influence on the function of the level shifter. However, the $\mathrm{V_B}$-VSSH has an overshoot, which is smaller due to the body-diode clamping. Thus, in this case, the level shifter cannot be triggered by mistake nor damage its devices. When IN is high and a positive 250 V/ns *dV/dt* occurs, the $\mathrm{V_B}$-VSSH has a large undershoot. In this situation, the level shifter may be triggered by mistake. However, due to the auxiliary pull-up circuit, M6, and logic gates with appropriate trigger voltage, the level shifter can maintain the correct state as discussed before. Therefore, when IN is high, the level shifter is always correct whether the positive or negative 250 V *dV/dt* noise occurs. The simulation result is consistent with the previous theoretical analysis. Meanwhile, as can be seen from Fig. 13, when IN is low, the transient response of the level shifter disturbed by *dV/dt* noise is similar to the above.

For some applications, *dV/dt* noise of the HV power supply rail may appear during the input of the level shifter switching. So, this scenario is verified at the 0.5 μm BCD process, as shown in Fig. 14. The operating frequency of input signals IN is more than 110 MHz. At the same time, according to Fig. 14, no matter how IN changes, the ±250 V/ns *dV/dt* noise does not make the level shifter in the wrong state.

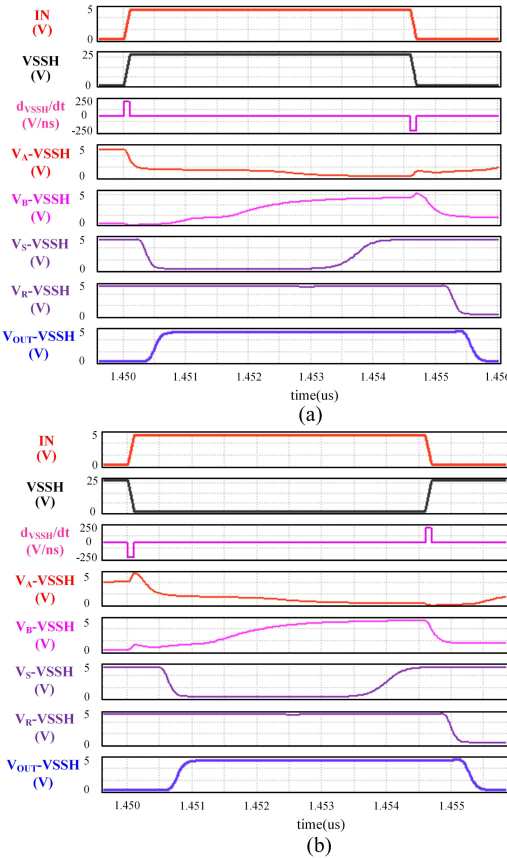

Fig. 14. ±250 V/ns *dV/dt* immunity simulation results of LS_I during the switching operation. (a) Positive 250 V/ns *dV/dt* occurs during the low-to-high transient of IN, and a negative 250 V/ns *dV/dt* happens during the high-to-low transient of IN, (b) is the opposite of (a).

In summary, for synchronous gate drivers in the half-bridge, when the HV power supply rail has ±250 V/ns *dV/dt* noises, the proposed level shifters can maintain normal function under any conditions. That means that the proposed level shifters can be applied to gate drivers that require ultrahigh d*V*/d*t* immunity.

V. Test Results and Comparison With Previous Work

In wide-bandgap applications, the response speed of a sub-ns level shifter is critical. Therefore, the propagation delay of the proposed level shifters is also verified. For the ps-level delay, the average delay could be measured by the ring oscillator circuit as described in Section V-A. LS_II and LS_I have different delay matching, but they have the same average delay. Thus, LS_II has been fabricated in the 0.5 μm BCD process and measured by the ring oscillator circuit. LS_III and LS_I have a similar circuit architecture, and the LS_III's delay is only two logic gates larger than LS_I. Therefore, this article illustrates the proposed sub-ns delay design technique by testing the average delay of LS_II. As for the verification of *dV/dt* immunity, as described in [13], it needs to be embedded in a high-speed, dual-channel gate driver. In the same way, post-simulation results are used to illustrate that the proposed level shifter has a high *dV/dt* immunity in Section IV.

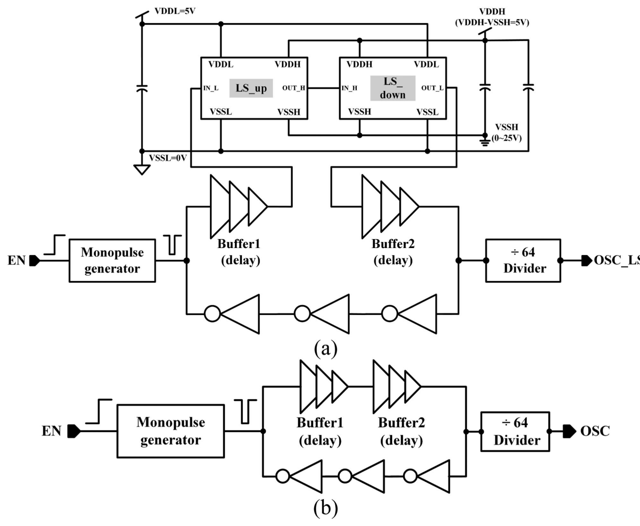

Fig. 15. Measurement circuit of the proposed level shifter. (a) Ring oscillator with LS_up (level up shifter) and LS_down (level down shifter). (b) Ring oscillator without LS_up and LS_down.

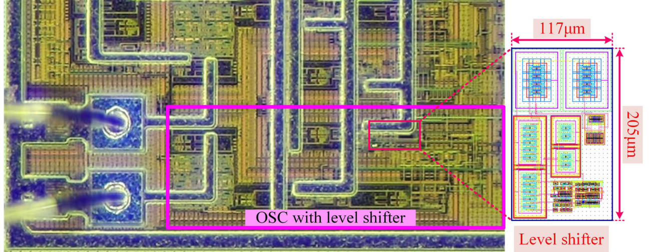

Fig. 16. Chip micrograph of the test circuit and the proposed LS_II.

A. Measurement Circuit

A sub-ns delay has been realized in the proposed HV floating level shifters, so the delay should be tested accurately. In general, the parasitic capacitor of chip IOs is about a few pF, which would make the inputs and outputs of the high-speed level shifters cannot be directly connected to chip IOs. Currently, there are two test methods for the level shifter. One is to use two buffer circuits, one with LS and the other with only the buffer circuit [26]. They have the same input pulse, and the difference between the output time of the two circuits is the delay of LS. This test method has a high requirement for testing, which requires strict matching of layout and test environment. For the sub-ns level shifter, this test method may increase the measurement error. The other is to use a ring oscillation circuit, as shown in [13] and [18]. For a ring oscillation circuit, an up level shifter, a down level shifter, and another inversion logic gate are in series, and a divider can obtain the output signal. The level-up shifter and level-down shifter use the same structure, so they can be assumed to have the same delay. However, in the ring oscillator, an inversion logic gate would affect the delay of the level shifter. In [18], the delay of an extra inversion logic gate is ignored, which is not suitable for the sub-ns level shifter. In [13], the delay of reverse logic needs to be adjusted, which is equal to the delay of the level shifter under test. However, it is difficult to match the propagation delay of different circuits.

In this article, an improved ring oscillator test method is adopted. As shown in Fig. 15, the test circuit has two ring oscillators, which one has the level shifter, and the other only has three inverters and two buffers. In Fig. 15(a), LS_up and LS_down use the proposed structure, and they have almost the same delay. Two oscillators period, T_{OSC} and $T_{\mathrm{OSC_LS}}$, are obtained by the 64 times divider to driving I/O pads. Then, the average delay of the LS_up and LS_down is described as follows:

$$T_{\mathrm{ave}} = \frac{T_{\mathrm{OSC}} - T_{\mathrm{OSC_LS}}}{4 \times 64}. \tag{9}$$

The test method proposed can avoid the influence of logic gates in the ring oscillator. The level shifter delay only depends on the difference between the two oscillators period. Therefore, to reduce the high-frequency requirement of an oscilloscope, the oscillator frequency can be designed smaller by using the buffer with the appropriate frequency divider circuit. Since some level shifters are pulse triggered, the initial state of an oscillator with the level shifter needs to be set. Then, a mono-pulse generator is added to the ring oscillator, as shown in Fig. 15. The two oscillators are better matched, both adding mono-pulse generators. The rising edge of enable signal EN produces a low one-shot pulse, which includes a rising edge signal and a falling edge signal. In the ring oscillator without initialization, only one of the LS_up and LS_down could have a logic error, or both are normal because there are three inverters. When LS_up has an error, those rising/falling edge signal could restore LS_up. When LS_down has an error, and LS_up is correct, those rising/falling edge signal could also cause the output of LS_up to generate a rising edge signal and a falling edge signal, making LS_down return to the normal state. Therefore, any error in LS_up and LS_down occurs, the function can be recovered through the rising and falling signals generated by EN. Then, the ring oscillator can work properly.

B. Measurement Results

As shown in Fig. 16, the chip micrograph of the test circuit is described. The chip area of LS_II is 117 μm × 205 μm. Although LS_II uses fewer devices, the layout occupies a large area due to the larger process nodes.

Measurement and postsimulation results are carried out for the test circuit in Fig. 15, which are shown in Fig. 17 and Fig. 18. All power supply rails are supplied through the external voltage sources during simulation and measurement. As shown in Fig. 15, VDDL is set to 5 V, VSSL is the reference, and VDDH-VSSH is equal to 5 V. Then, VSSH changes from 0 to 25 V with a 1 V step to observe the average delay of LS_II. Fig. 17 shows the transient measurement waveform of the two oscillators under VSSH = 25 V, in which channel 1 is the output of the ring oscillator without level shifters, and channel 2 is the output of the ring oscillator with level shifters. It can be calculated from Fig. 17 that the average delay of LS_II is only 664 ps.

Fig. 18 shows the average delay of LS_II varies with VSSH under postsimulation and measurement. Several phenomena can be observed in Fig. 18. First, the average delay of LS_II reduces

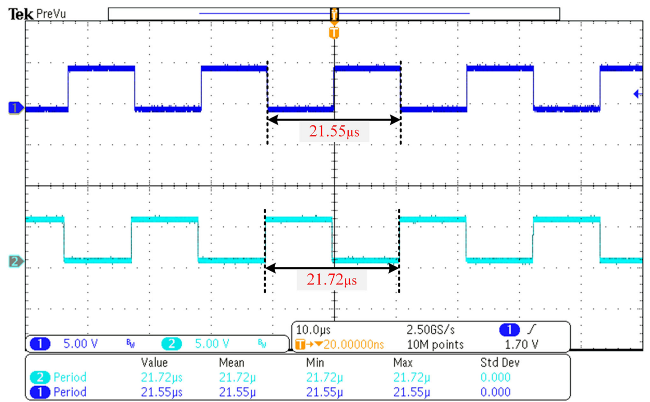

Fig. 17. Measured output waveform of the two oscillators under VSSH-25 V.

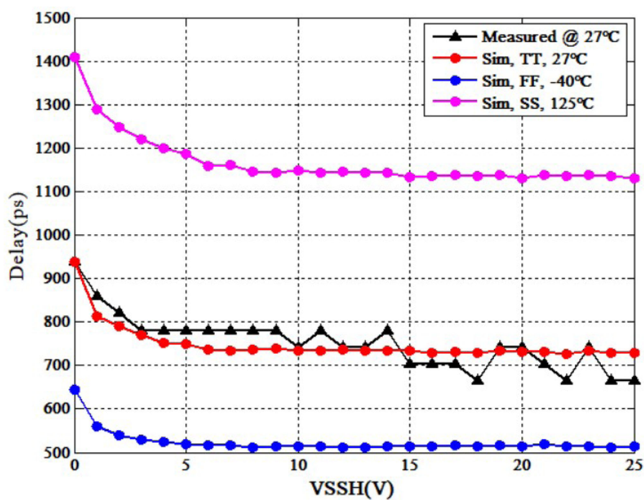

Fig. 18. Postsimulation and measurement results of the average delay for LS_II.

with the increase of VSSH. That is mainly because LDMOS transistors in LS_II have the channel modulation effect and parasitic capacitance. With the increase of VSSH, the pull-down current of n-type LDMOS (NLDMOS) gradually increases due to the channel modulation effect, and the parasitic capacitance of NLDMOS diode (the parasitic capacitance of nodes A and C) also decreases with VSSH increase. Therefore, the response speed of the A–C path or the B–D path of LS_II increases with the increase of VSSH, and the subsequent logic gate response also increases. So, the average delay of LS_II decreases with the increase of VSSH. When VSSH is relatively large, the parasitic capacitance of NLDMOS is small, and the variation is small. The delay of LS_II tends to be constant. Second, for the average delay of LS_II, the measurement results have a significant variation. Moreover, with the increase of VSSH, the measurement results show that the average delay of LS_II is lower than that of postsimulation results. That is mainly due to the finite simulation model accuracy of transistors. Overall, the deviation between measurement results and simulation results is within 10%, which is acceptable. Third, the average delay of LS_II in the test circuit is more considerable than that of single-module simulation in Fig. 9, above 100 ps. That is because the period of the ring oscillator includes the rise and fall time of the level shifter's input and output signals. Logic propagation delay measurement adopted in this article is the time from 50% of input signal amplitude to 50% of output signal amplitude. In general, compared with the logic propagation delay, the rise or fall time of the signal itself is very short, and the average delay obtained by using the ring oscillator is close to the actual delay. However, the proposed level shifter only has a sub-ns delay and uses a 0.5 μm BCD process. This process node is large, as mentioned above, so the rise or fall time of the logic gates in LS_II is not negligible compared with the delay of the proposed level shifter. Therefore, the average delay of LS_II could be increased by using the ring oscillation measurement circuit. In a word, it can be seen from the simulation and measurement results that the proposed level shifter can realize a sub-ns delay except in the case of high temperature at SS corner, which is affected by the process. The difference between the measurement results and the simulation results of LS_II is minimal, indicating that the level shifter architecture proposed is suitable for application in high-speed circuits.

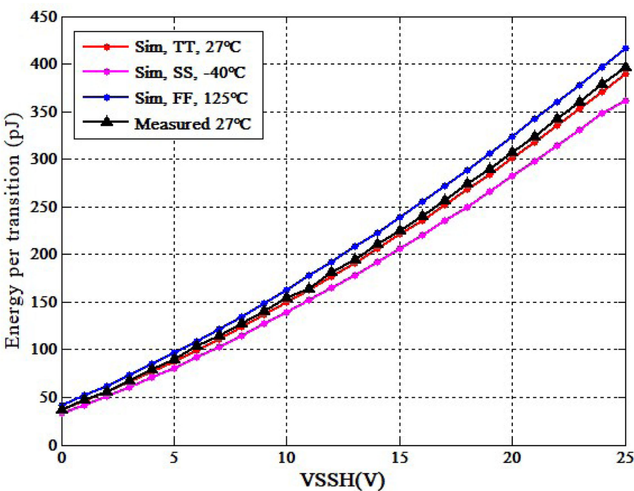

Fig. 19. Postsimulation and measurement results of energy per transition (ET) for LS_II.

Fig. 19 demonstrates the E_T of LS_II versus VSSH, which indicates that test results are very close to the simulation results. When the HV power supply rises, the average current of LS_II could remain constant, so E_T increases with VSSH.

C. Comparison With Previous Works

To compare the proposed level shifter with other previous works, Table I lists the main parameters of the HV floating level shifters, such as the propagation delay, *dV/dt* immunity, maximum operating voltage, process node, E_T, and chip area. For wide-bandgap applications, the propagation delay and *dV/dt* immunity of the level shifter is the most critical. However, the propagation delay is closely related to the process node.

In Table I, the level shifter only in [11]–[13], and this article can realize a sub-ns delay. The process node used by other sub-ns delay level shifters is just 0.18 μm, but the proposed level shifter uses a 0.5 μm BCD process. The FOM in [18] is used

TABLE I
COMPARISON WITH PREVIOUS WORKS

	Year	Process	Voltage (V)	Delay (ns)	Slew rate (V/ns)	E_T (pJ)	Chip area (mm^2)	FOM	FOM*
Z.Liu, et al.[10]	2015	0.5μm HV CMOS	40	2.0	40[1]	272[1]	0.22	0.1	108.8
A.Salimath, et al.[11]	2017	0.18μm BCD	50	0.5[1]	—	1212.5[1]	—	0.056	269.44[2]
D.Liu, et al.[12]	2016	0.18μm HV CMOS	20	0.37	30[1]	7.2[1]	0.005	0.1	23
D.Liu, et al.[13]	2019	0.18μm HV CMOS	50	0.53	200[1]	30.3	0.018	0.06	54
Y.Moghe, et al.[18]	2011	0.35μm HV CMOS	10	2.2	—	24	—	0.069	56
T.Lehmann, et al.[19]	2014	0.35μm HV CMOS	20	3	—	6[1]	—	0.43	21
J.Wittmann, et al.[20]	2014	0.18μm BiCMOS	50	<5	20	—	0.036	0.56	—
H.-A. Yang, et al.[22]	2015	0.5μm UHV	700	20	120	—	—	0.06	—
This work	**2020**	**0.5μm BCD**	**30**	**0.66**	**250**[1]	**397**	**0.024**	**0.044**	**6.8**[2]

Note: FOM from [18]: Delay/(Process node × Voltage). Unit: ns/(μm × V).
FOM$*$ from [12]: (E_T × Delay)/(Process node ^{3} × Voltage). Unit: (pJ × ns)/(μm^3 × V).
[1]Simulated, [2]FOM*: (E_T × Delay)/($L_{HV\text{-}MOS}{}^2$ × Process node × Voltage). Unit: (pJ × ns)/(μm^3 × V).

to evaluate the advantages of the level shifter architecture about the propagation delay. The proposed level shifter achieves the lowest FOM, only 0.044 ns/(μm $\times$ V).

E_T is another important parameter of the level shifter, which is greatly affected by parasitic capacitance. Large parasitic capacitors require more energy during level shifter transition. In [12], FOM$*$ can reflect both the propagation delay and energy per transition. The process node used in this article is 0.5 μm, but the minimum width allowed by NLDMOS is up to 1.6 μm, which greatly increases the parasitic capacitance and current consumption. Therefore, for the proposed level shifter's E_T, (E_T $\times$ Delay)/(Process node ^{3} $\times$ Voltage) in FOM$*$ should be (E_T $\times$ Delay)/ ($L_{HV\text{-}MOS}{}^2$ $\times$ Process node $\times$ Voltage), where $L_{HV\text{-}MOS}$ is the minimum width of NLDMOS. Compared with other works, the proposed level shifter consumes more energy due to the large process size. It can be seen from Table I that the proposed level shifter can still realize the better FOM$*$ without considering the influence of the process.

As for the *dV/dt* immunity, the proposed level shifter can achieve higher performance, exceeding 250 V/ns. Therefore, the proposed level shifter architecture can not only achieve a very high speed but also suppress a big *dV/dt* noise. Then, the proposed level shifter can be applied to drivers with high speed and tremendous *dV/dt* noise, especially in wide-bandgap applications.

VI. CONCLUSION

This article presents new design techniques to improve the performance of the HV floating level shifter. By utilizing the edge detection technique, the speed of signal conversion from the LV region area to the HV region area can be significantly improved, and the sub-ns delay level shifter can be realized. On this basis, various improvements are made to the level shifter for specific applications. For example, the auxiliary pull-up circuit in LS_I can not only reduce the switching time and dynamic power consumption but also improve the *dV/dt* immunity, which is very important for the application of high frequency and low duty cycle. In LS_II, the improvement of delay match can weaken the duty cycle distortion of the signal. The self-calibration technique enables LS_III to achieve a small delay and not to rely on the pulse triggering mode, which has a proper application in high-speed drive with a feedback mechanism.

In this article, LS_II was fabricated in the 0.5 μm BCD process. The experimental results show that the delay of LS_II is less than 1 ns and only 664 ps when VDDH is 30 V. Its FOM is the lowest among the previous sub-ns delay level shifters, only 0.044 ns/(μm $\times$ V). Postsimulation results demonstrate the proposed level shifters have a very high *dV/dt* immunity, over 250 V/ns, and are suitable for in any cases. The proposed level shifter is simulated at the 0.18 μm BCD process, and the propagation delay is improved by more than 60%. Therefore, the proposed level shifters are very suitable for ultrahigh-speed drivers, especially for wide-bandgap applications.

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