Current Limiting in Overload Conditions of an *LLC*-Converter-Based DC Transformer

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***Abstract*—The dc transformers based on an *LLC* converter operated in open loop near resonant frequency have several crucial advantages compared to other topologies. These advantages are the stiff voltage ratio with a natural power flow, the dc grid isolation via medium-frequency transformer, and the high efficiency due to the resonant converter nature. Despite these advantages, the open-loop operation does not provide any options to limit the transferred current during overload conditions in the dc grid. This is critical, since it prevents the grid from recognizing that either some local primary regulation or load shedding is required. This article proposes a closed-loop control method that utilizes variable duty cycles to limit the current once the overload situation is detected. An applicable control scheme is derived and implemented. Since the duty-cycle modulation increases the losses of the converter, an online thermal model is implemented to protect the dc transformer during the overload conditions. The proposed current-limiting mode with the thermal model are validated using an exemplary low-voltage dc transformer prototype, demonstrating the general feasibility and overall good performance.**

***Index Terms*—Control, DCX, dc transformer, duty cycle, *LLC* converter, overcurrent, resonant, solid-state transformer.**

I. Introduction

THE LLC resonant converter operated in open loop has been proposed for applications as a dc transformer several times in the literature, e.g., [1]–[9]. The topology is especially well-suited for this application, since it enables a load-independent voltage ratio and galvanic isolation through a compact medium-frequency transformer (MFT). Furthermore, high conversion efficiency is achieved due to zero-voltage and zero-current switching, characteristic for the topology. Nonetheless, the open-loop operation does not provide any current limiting in the case of overload, since it naturally delivers the power that is required to keep the voltage ratio constant. Thus, in the case of overload, the currents would rise and the zero-voltage switching can be lost, leading to significantly increased losses. Consequently, the dc transformer would be thermally overloaded after a short period of time and would have to be turned off for protection reasons. However, this is undesired, since this strategy suddenly cuts the power to the already overloaded grid. If the considered dc transformer is the main supplier of the overloaded dc grid, the voltage drops rapidly as dc links are discharged and the dc grid needs to be restarted in a "black start" procedure.

A better strategy is to limit the transferred current of the dc transformer by some additional means to slow down the drop rate of the dc-grid voltage. This way, the dc grid has a chance to recognize that it is overloaded by observing the slowly decreasing voltage and can take some regulating action, such as increasing the power supply from local energy storages or shedding some loads, in order to maintain its operation and restore the voltage.

In literature, several options were presented for current limiting in the *LLC* converter topology. Many of these options are hardware-based: resonant capacitor clamping by diodes [10], [11], additional notch filter in the resonant tank [12], and additional resistor that is connected in parallel to the resonant capacitor during overloads [13]. While the hardware solutions proved to be effective, they increase the footprint and the costs of the dc transformer. Hence, the software solutions are generally preferred, unless their performance is insufficient.

The traditional solution to limit the transferred power is to increase the switching frequency in order to increase the impedance of the resonant tank [10]. Nevertheless, with dc transformers that were designed for stiff voltage ratios, the applied switching frequency during heavy overload has to be up to one order of magnitude higher than the one applied during the normal open-loop operation. Hence, this current-limiting method is unfeasible for many switching devices (similar conclusions can also be found in [13]).

The second control option that enables current limiting at low voltage gains is to apply the duty-cycle control [13]–[15] or a combination of both switching-frequency and duty-cycle control [16], [17]. These solutions alter the current waveforms in the resonant tank and exhibit increased turn-OFF losses (zero-voltage turn on is maintained). Nevertheless, the losses are expected to be increased only moderately compared to pure frequency control and no significant hardware changes are required.

Hence, in this article, the solution based on the duty-cycle control is selected. To protect the dc transformer from damage due to increased losses, we propose to implement an online thermal model to supervise the converter semiconductor junction temperatures. This ensures that the switch losses during the current limiting can be higher than the rated losses for a transient

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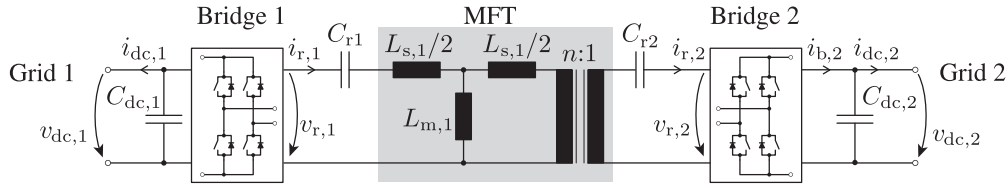


Fig. 1. Studied topology of the dc transformer connected between two dc grids. In the study, Grid 1 behaves as a source and Grid 2 represents a load. In this operation direction, only Bridge 1 is actively switched, while Bridge 2 operates as a passive rectifier.

period and thus, maximizes the time period for which the dc grid can be supported.

While the aforementioned papers [13], [16] study the general feasibility of the duty-cycle control for current limiting in steady state and [14], [15], [17] study current limiting for converter startup, there is currently no research that demonstrates how to implement a closed-loop control for this operation mode to improve the transient behavior and generally enable such current-limiting mode. This article demonstrates how the closed-loop current-limiting controller with an integrated thermal model can be designed for dc transformer applications. It answers the questions of which current should be controlled, what is a suitable model for the controller design, and how to address the nonlinear dependence of the converter voltage gain on the duty cycle.

This article is organized as follows. Section II presents the dc transformer topology and briefly explains the main idea of this article. In Section III, an example dc transformer is presented which will be used to demonstrate the practical design steps of the controller and later to experimentally validate the proposed current-limiting mode. The overview of the proposed current-limiting system is presented in Section IV with details explained in Sections V–VII. The experimental validation of the proposed current-limiting mode is in Section VIII. Finally, the conclusion is drawn in Section IX.

II. Problem Description and Proposed Solution

In the presented study, it is assumed that the dc transformer is connected between two dc grids, as depicted in Fig. 1. Grid 1 is assumed to be a relatively stiff grid that provides power to Grid 2. The dc transformer is implemented as an *LLC* converter operated at the resonant frequency with a symmetrically split tank ($C_{r1} = C_{r2}/n^2$) and full-bridge power stages. Since in the given scenario, the power is transferred from Grid 1 to Grid 2, only Bridge 1 is switching and Bridge 2 operates as a passive rectifier. Note that this direction was chosen solely for the purposes of the demonstration and the same principles apply to the other operating direction as well.

In the normal operation, the duty cycle is constant $\delta = 0.5$ and the dc transformer is operated in an open loop, guaranteeing almost constant voltage ratio independent of the transferred power. This is advantageous, since this converter operation mode acts as a passive dc transformer without any power setpoints. However, if the loading is increased beyond the rated one, the dc transformer naturally transfers more power and its currents are increased as well.

TABLE I
Example Prototype DC Transformer Parameters

Rated Power	P_N	5 kW
Rated Voltage Grid 1/Grid 2	$V_{dc,1}$, $V_{dc,2}$	200 V
Rated Current Grid 1/Grid 2	$I_{dc,1,N}$, $I_{dc,2,N}$	25 A
Switching Frequency	f_s	10.8 kHz
Measured Efficiency at Rated Power	η_N	$\approx$ 96 %
Rated Junction-to-Ambient Temperature	$\Delta\vartheta_{J-A,N}$	18.7 K
Rated Quality Factor	Q_N	0.12
Resonant Frequency	f_0	10.8 kHz
Transformer Ratio	n	1
Stray Inductance (incl. cables)	$L_{s,1}$	11.6 µH
Magnetizing Inductance	$L_{m,1}$	750 µH
Resonant Capacitances	C_{r1}, C_{r2}	37.5 µF
DC-link Capacitances	$C_{dc,1}$, $C_{dc,2}$	520 µF

During such overload conditions, we propose to limit the transferred current via a closed-loop duty-cycle controller. The design and the implementation of the controller will be the main focus of the following sections.

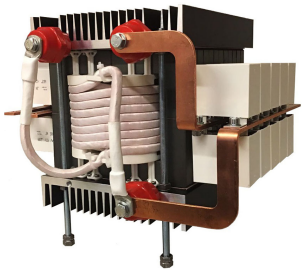
It is important to note that the *LLC* converter is further considered to be operated in the open-loop mode in normal conditions. The controller is only activated when the overload conditions are detected.

III. Considered Example of the DC Transformer

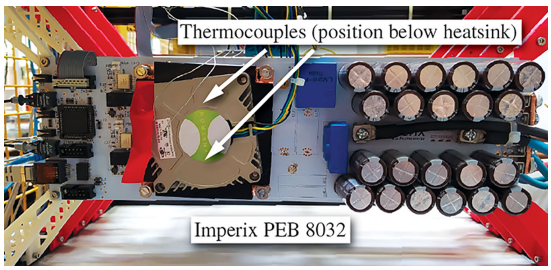
To demonstrate the steps for the derivation of the current-limiting control system in practice, an example of *LLC*-converter-based dc transformer is defined. The dc transformer is a downscaled 5 kW low-voltage prototype that was developed in [1] to demonstrate the design practices for high-power dc transformers for future dc grids. This dc transformer prototype is used for the experimental validation later in Section VIII. Although the parameters were selected carefully for desired properties in open-loop operation (as described in [1]), the hardware is not optimized by any means and it only serves to demonstrate operational principles. The parameters are listed in Table I and its components are presented in Fig. 2.

The resonant tank of the dc transformer is based on a 1:1 MFT with integrated resonant capacitors from [18] as shown in Fig. 2(a). The resonant tank is characterized by its resonant frequency

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{s,1} \cdot \frac{C_{r1} \cdot C_{r2}/n^2}{C_{r1} + C_{r2}/n^2}}} = 10.8\,\text{kHz} \qquad (1)$$



(a)



(b)

Fig. 2. Components of the example dc transformer. (a) 1:1 MFT with integrated resonant capacitors [18]. (b) Imperix half-bridge modules realizing the H-bridges.

and the quality factor at the rated power

$$Q_{\mathrm{N}} = \frac{Z_0}{R_{\mathrm{ac}}} = \frac{\sqrt{\frac{L_{\mathrm{s},1}}{\frac{C_{\mathrm{r}1}\cdot C_{\mathrm{r}2}/n^2}{C_{\mathrm{r}1}+C_{\mathrm{r}2}/n^2}}}}{\frac{8}{\pi^2}\cdot\frac{V_{\mathrm{dc},1}}{I_{\mathrm{dc},1,\mathrm{N}}}} = 0.12 \tag{2}$$

that is relatively low. In the open-loop operation of the dc transformer at the switching frequency near to the resonant frequency, such low value of Q_{N} guarantees a stiff loading characteristic (the voltage ratio is almost independent of the transferred power) [1].

The H-bridges are assembled using Imperix PEB 8032 half-bridge modules, shown in Fig. 2(b). To characterize and validate the thermal model later in Section VII, the sinks of the modules were milled and thermal sensors were placed onto the cases of the switches through the introduced grooves. It should be noted that the applied IGBTs (1200-V XPT GenX3 high-speed IGBT from IXYS [19]) are heavily oversized and that their junction-to-ambient temperature at the rated conditions is estimated to be only $\Delta\vartheta_{\mathrm{J-A,N}} = 18.7\,\mathrm{K}$. Assuming that in an optimized converter design the junction-to-ambient temperature at the rated power would be near the safety limit, the value $\Delta\vartheta_{\mathrm{J-A,N}}$ will be used in this article as a temperature limit that should not be exceeded during the current-limiting mode. The dc transformer is controlled using Imperix B-Box fast prototyping control platform.

IV. Proposed Control System for the Current-Limiting Mode

The proposed control system for the current-limiting mode is depicted in Fig. 3. It consists of several parts: a current estimation to determine the current delivered by the dc transformer, a controller to realize the closed-loop control of the estimated current, and a loss and thermal model that supervises the junction temperatures and determines what the maximum allowed current i^* that can be delivered by the dc transformer without exceeding system's safe operating area is.

The activation and deactivation of the current-limiting mode is handled by the "mode selection logic" block. The current-limiting mode is entered when the estimated dc transformer current exceeds its defined maximum value. During this mode, the duty cycle δ determined by the controller is forwarded to the setpoint duty-cycle value δ^* for the modulator. The current-limiting mode is deactivated when the setpoint duty cycle is $\delta = 0.5$ for several subsequent control periods (in the example implementation ten periods) which indicates that the delivered current naturally dropped below the current limit i^*. When the current limiting mode is inactive, the setpoint duty cycle is fixed at $\delta^* = 0.5$ for standard open-loop operation and the integrator of the PI controller within the "current-limiting controller" block is reset to prevent its wind-up.

As can be observed in Fig. 3, the inputs for the control are: the measured dc link voltages $v_{\mathrm{dc},1}$ and $v_{\mathrm{dc},2}$, the measured voltage $v_{C\mathrm{r}2}$ over the resonant capacitor $C_{\mathrm{r}2}$ to estimate the delivered current, and the ambient temperature ϑ_{A} for the thermal model. The only outputs are the setpoint duty cycle δ^* which is forwarded to a modulator to generate the switching signals for Bridge 1 and the signal "unsafe" that indicates that indicates that the switch junction temperatures have risen to dangerous levels and emergency shutdown is required.

The implemented modulator uses a special asymmetric modulation technique studied in [20] that equalizes the losses in the particular switches of the H-bridge converter stage. This is vital in order to increase the capabilities of the dc transformer to deliver the current with reduced duty cycles, since these conditions lead to increased losses (as will be demonstrated later). If other inverter stage than H bridge, e.g., half bridge, is applied, the modulator has to be replaced correspondingly.

In the following sections, the functionality of the particular blocks from Fig. 3 is presented.

V. Current Estimation

While it might seem as a natural choice to directly limit the current of the overloaded dc grid $i_{\mathrm{dc},2}$, it is not the best approach, since the dynamics of this current are impacted by the dc-link capacitance and the unknown time-variant impedances of the connected dc grid.

A significantly better option is to control the direct component of the current $i_{\mathrm{b},2}$ delivered by Bridge 2 to the dc link capacitor $C_{\mathrm{dc},2}$. This is advantageous, since this current component directly represents the current delivered by the dc transformer and its dynamics depend mainly on the well-known parameters of the resonant tank (the connected grids are decoupled by the dc-link capacitors). The only issue with this option is that it is impractical to measure this current directly in the low-inductive bus-bar part of the converter. Instead, it will be estimated indirectly as its value is identical to the mean value of the resonant current $i_{\mathrm{r},2}$ within the first or second half of the switching period $T_{\mathrm{s}}/2$

$$\langle i_{\mathrm{r},2}\rangle(k+1) = \frac{1}{T_{\mathrm{s}}/2}\int_{k\cdot T_{\mathrm{s}}/2}^{(k+1)\cdot T_{\mathrm{s}}/2} |i_{\mathrm{r},2}(t)|\,\mathrm{d}t. \tag{3}$$

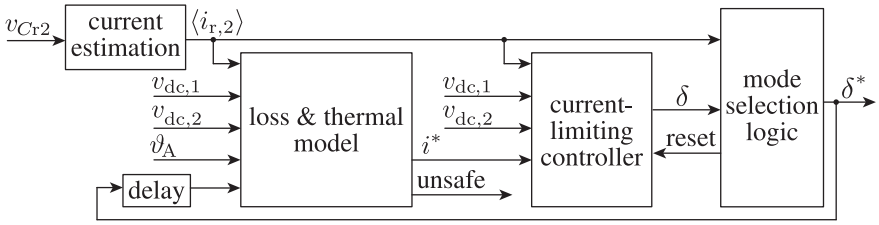


Fig. 3. Proposed control system for limiting the delivered currents during overload conditions. The current-limiting mode is activated and deactivated in the "mode selection logic" block. The transferred current $\langle i_{r,2}\rangle$ is estimated in "current estimation" block and it is closed-loop controlled in block "current-limiting controller" with the setpoint value i^* that is determined according to the estimated junction temperatures in block "loss & thermal model".

Nonetheless, it is neither easy to estimate the mean value of the current in the resonant tank, since during duty-cycle control, the shape of currents changes significantly, and thus, a high number of measured points would be needed for the waveform reconstruction. A solution is to estimate the current from the voltage

$$v_{Cr2}(t) = \frac{1}{C_{r2}} \cdot \int i_{r,2}(t)\,\mathrm{d}t \tag{4}$$

over the resonant capacitor C_{r2}, which is a function of the resonant current integral as well. Combining (3) and (4), it can be derived that the current value $\langle i_{r,2}\rangle$ can be estimated by subtracting the resonant voltage v_{Cr2} at the beginning of the half switching period $T_s/2$ from that in the end of the half switching period

$$\langle i_{r,2}\rangle(k+1) = \frac{C_{r2}}{T_s/2} \cdot |v_{Cr2}(k+1) - v_{Cr2}(k)| \quad . \tag{5}$$

Hence, for the estimation of the transferred current, two values of resonant capacitor voltages have to be measured in each switching period. Furthermore, this current estimation can be calibrated (considering that the exact capacitance value is usually unknown) by measuring the peak value of the resonant tank current during the open-loop operation (if these currents are sensed). Moreover, the sensor does not necessarily have to have a high precision, considering that the current-limiting mode is activated rarely and does not require highly precise regulation.

Note that the current can be theoretically estimated using the voltage drop v_{Cr1} over the capacitor C_{r1} as well, since the mean value of the magnetizing current is zero within each half period in steady state. Nevertheless, this practice can lead to light noise in the measurement when the "secondary" resonance between the magnetizing inductor $L_{m,1}$ and the resonant capacitor C_{r1} is excited and thus, it is not recommended as a preferred solution.

VI. Current-Limiting Controller Design

The derivation of the current-limiting controller is based on a simplified averaged model of the *LLC* converter as it is depicted in Fig. 4. Such averaged model of an *LLC* converter was first proposed in [21] and later studied extensively in [22] and [23]. These models generally neglect the impact of the magnetizing inductance $L_{m,1}$ and are valid only for frequencies sufficiently lower than the resonant frequency. Nevertheless, the neglection of $L_{m,1}$ proved to cause only minor errors as long as the ratio $L_{m,1}/L_{s,1}$ is sufficiently high [23] (which is usually the case

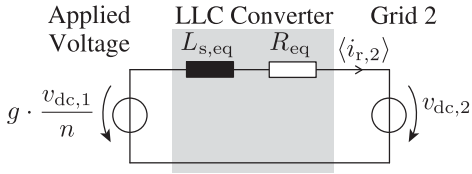


Fig. 4. Simplified linearized averaged model used for the design of the controller.

with *LLC* converters in dc transformer applications). Furthermore, for the design of the controller, the dc-link capacitors are simplified into ideal voltage sources. This simplification is valid, since the dynamic behavior of the capacitor voltages is typically significantly slower than that of the resonant tank. Since the voltage gain is impacted by the decreased duty cycle, the transformed dc-link voltage $v_{dc,1}/n$ is multiplied by the corresponding voltage gain value g. The nonlinear dependence $g(\delta)$ is studied further in Section VI-B.

According to [23], the equivalent inductance

$$L_{s,eq} = \frac{1}{n^2} \cdot \frac{\pi^2}{4} \cdot L_{s,1} \tag{6}$$

is determined purely by the stray inductance of the transformer, assuming that the dc transformer is switched at (or very near) its resonant frequency. The equivalent resistance R_{eq} represents the voltage drop due to load-dependent losses. This resistance can either be neglected for the controller design or it can be determined by measuring the dc-link voltages $v_{dc,1}$ and $v_{dc,2}$ and the transferred current $\langle i_{r,2}\rangle$ at the rated operating conditions offline, during commissioning, or online, during open-loop operation

$$R_{eq} = \frac{\frac{v_{dc,1}}{n} - v_{dc,2}}{\langle i_{r,2}\rangle} \quad . \tag{7}$$

In the example prototype, the equivalent inductance is $L_{s,eq} = 28.6\,\mu\mathrm{H}$ and the equivalent resistance was estimated to $R_{eq} = 0.24\,\Omega$.

Observing Fig. 4, it can be recognized that the averaged *LLC* converter model represents a (weakly-damped) first-order system with dc-link voltage $v_{dc,2}$ being a disturbance. Hence, a proportional-integral (PI) controller can be applied to robustly control the delivered current $\langle i_{r,2}\rangle$. To improve the transient behavior, feed-forward terms should be applied to compensate for the varying dc-link voltage $v_{dc,2}$ and the voltage drop over

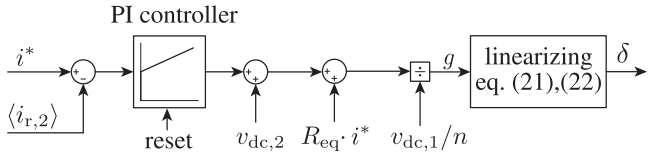


Fig. 5. Current-limiting closed-loop controller scheme.

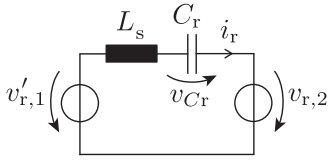


Fig. 6. Simplified model of the resonant tank for calculation of characteristic waveforms. The values are referred to the secondary side.

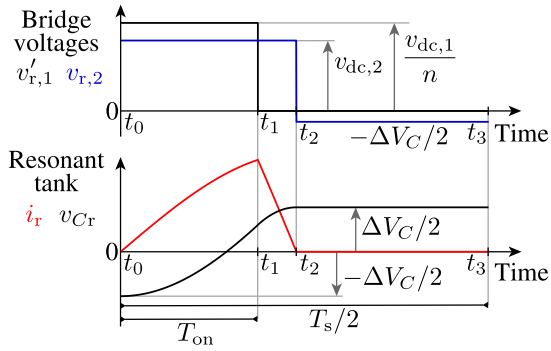


Fig. 7. Characteristic waveforms of the simplified model from Fig. 6 over half switching period $T_{\mathrm{s}}/2$.

the equivalent resistance R_{eq}. The utilized scheme of the closed-loop current-limiting controller is depicted in Fig. 5.

Fig. 5 shows that the current delivered by the dc transformer $\langle i_{\mathrm{r},2}\rangle$ is controlled by a PI controller to follow the setpoint value i^* determined by the thermal model (see Fig. 3). The controller output value is extended by the feed-forward term $v_{\mathrm{dc},2} + R_{\mathrm{eq}} \cdot i^*$ and divided by the transformed dc-link voltage $v_{\mathrm{dc},1}/n$ to obtain the setpoint voltage gain g. After that, a linearizing equation is applied that determines the required duty cycle δ to achieve the setpoint gain g. This linearizing equation is derived hereafter.

A. PI Controller Design

Considering that the losses of the dc transformer are typically low, the plant is weakly damped. Hence, the symmetric-optimum criterion [24] is a preferable method to tune the controller, since it is optimized for a good disturbance-rejection behavior and applicable for plants with a dominant integral part. For the tuning, the plant is assumed to behave purely as an inductor $L_{\mathrm{s,eq}}$, since all other parts are compensated for by the feed-forward terms. The total delay T_{d} can be approximated as a sum of the measurement acquisition delay ($\approx T_{\mathrm{s}}/2$), the calculation delay ($\approx T_{\mathrm{s}}/2$), and the modulation delay ($\approx T_{\mathrm{s}}/4$) – assuming the duty cycle is updated two times per period

$$T_{\mathrm{d}} = 1.25 \cdot T_{\mathrm{s}} \quad . \tag{8}$$

Finally, applying the symmetric-optimum criterion, the resulting gain and the time constant of the PI controller yield

$$G_{\mathrm{PI}} = \frac{L_{\mathrm{s,eq}}}{2 \cdot T_{\mathrm{d}}} \tag{9}$$

$$T_{\mathrm{PI}} = 4 \cdot T_{\mathrm{d}} \quad . \tag{10}$$

It should be noted that depending on the application and dc transformer parameters, an additional fine tuning of the controller might be required. Nevertheless, the controller parameters resulting from the symmetric-optimum criterion should give a good starting point for further optimization.

B. Linearizing Equation

As mentioned before, the relationship between the voltage gain of the converter g and the applied duty cycle δ is highly nonlinear due to the discontinuous operation in the duty-cycle control mode. To linearize the plant, this relationship can be derived analytically using a simplified piecewise linear model.

The simplified model of the resonant tank with concentrated elements, as depicted in Fig. 6, can be derived by neglecting the magnetizing inductance and the converter losses. This simplification is valid, since the magnetizing inductance does not take a significant part in energy transfer, and the losses of the converter are generally very low. In the model, all variables are referred to the secondary side. The values for concentrated elements can be determined as series connection of the elements (see Fig. 1)

$$C_{\mathrm{r}} = \frac{n^2 \cdot C_{\mathrm{r1}} \cdot C_{\mathrm{r2}}}{n^2 \cdot C_{\mathrm{r1}} + C_{\mathrm{r2}}} \tag{11}$$

$$L_{\mathrm{s}} = \frac{L_{\mathrm{s},1}}{n^2} \quad . \tag{12}$$

Generally, the behavior of the resonant circuit in Fig. 6 can be described by two differential equations

$$v'_{\mathrm{r},1}(t) - v_{\mathrm{r},2}(t) = L_{\mathrm{s}} \cdot \frac{\mathrm{d}i_{\mathrm{r}}(t)}{\mathrm{d}t} + v_{C\mathrm{r}}(t) \tag{13}$$

$$i_{\mathrm{r}}(t) = C_{\mathrm{r}} \cdot \frac{\mathrm{d}v_{C\mathrm{r}}(t)}{\mathrm{d}t} \quad . \tag{14}$$

In the following derivation steps, only the positive half-period of the operation, as demonstrated in Fig. 7, is studied. In the figure, it can be seen that the circuit is first excited by the transformed dc-link voltage $v'_{\mathrm{r},1}(t) = v_{\mathrm{dc},1}/n$ for the time duration

$$T_{\mathrm{on}} = \delta \cdot T_{\mathrm{s}} \tag{15}$$

determined by the duty cycle δ. After, the zero-voltage state is generated by Bridge 1 for the rest of the period, yielding $v'_{\mathrm{r},1}(t) = 0$. Since Bridge 2 is not actively switched, the voltage at its terminals depends on the resonant current. When positive current flows through the resonant tank, the rectifier of Bridge 2 connects the circuit to the second dc link: $v_{\mathrm{r},2}(t) = v_{\mathrm{dc},2}$. When the current i_{r} becomes zero, the rectifier stops conducting and

the voltage applied to the resonant circuit equals the opposite voltage of the resonant capacitor: $v_{\mathrm{r},2} = -v_{C\mathrm{r}}$.

The set of differential equations can be solved once the conditions for the energy storage components in the resonant tank are determined. Since only discontinuous duty-cycle operation is assumed, the conditions of the resonant current i_r at times t_0 and t_2 both equal zero

$$i_\mathrm{r}(t_0) = i_\mathrm{r}(t_2) = 0. \tag{16}$$

Furthermore, since the derivation assumes steady-state symmetric operation, the capacitor voltage changes from negative value $-\Delta V_C/2$ to positive value $\Delta V_C/2$ during positive half-period and from $\Delta V_C/2$ to $-\Delta V_C/2$ during negative half-period. As derived in Section V, the capacitor voltage change ΔV_C is directly proportional to the currently transferred current. This yields following conditions for the capacitor voltage:

$$v_{C\mathrm{r}}(t_0) = -v_{C\mathrm{r}}(t_2) = -\frac{1}{2}\cdot\Delta V_C \quad . \tag{17}$$

Additionally, the continuity of the capacitor voltage $v_{C\mathrm{r}}(t)$ and inductor current $i_\mathrm{r}(t)$ has to be ensured when the bridge voltage $v'_{\mathrm{r},1}(t)$ changes

$$i_\mathrm{r}(t_1^-) = i_\mathrm{r}(t_1^+) \tag{18}$$

$$v_{C\mathrm{r}}(t_1^-) = v_{C\mathrm{r}}(t_1^+) \quad . \tag{19}$$

Solving the system of (13)–(19) and applying the definition of the voltage gain

$$g = \frac{v_{\mathrm{dc},2}\cdot n}{v_{\mathrm{dc},1}} \tag{20}$$

it can be shown that the duty cycle

$$\delta = \frac{1}{2\cdot\pi}\cdot\frac{f_\mathrm{s}}{f_0}\cdot\left(\pi/2 - \ldots \right.$$
$$\left. \operatorname{atan}\left(\frac{(\frac{1}{2}-g)\cdot\Delta V_C + (1-g)\cdot\frac{v_{\mathrm{dc}1}}{n}}{\sqrt{(1-g)\cdot g\cdot\Delta V_C\cdot(\Delta V_C + 2\cdot\frac{v_{\mathrm{dc}1}}{n})}}\right)\right) \tag{21}$$

is a nonlinear function of the required voltage gain g, switching frequency to resonant frequency ratio f_s/f_0, the dc-link voltage $v_{\mathrm{dc},1}$, and the delivered current that is represented by the voltage difference ΔV_C at the equivalent single series capacitor C_r. The capacitor-voltage change within the half switching period

$$\Delta V_C = \frac{T_\mathrm{s}/2}{C_\mathrm{r}}\cdot\langle i_{\mathrm{r},2}\rangle \tag{22}$$

can be related to the mean value of the delivered current $\langle i_{\mathrm{r},2}\rangle$ via the switching period T_s and the concentrated resonant capacitance C_r [see (11)] based on the same principles as applied to derive (5).

Equations (21) and (22), are implemented for online calculation to determine the duty cycle δ for the required setpoint voltage gain g (see Fig. 5).

The resulting characteristic for the dc transformer prototype is displayed in Fig. 8 as an example calculated for its rated current and rated voltage. It was validated via switched simulations in Plexim PLECS, observing the steady-state voltage gains g at

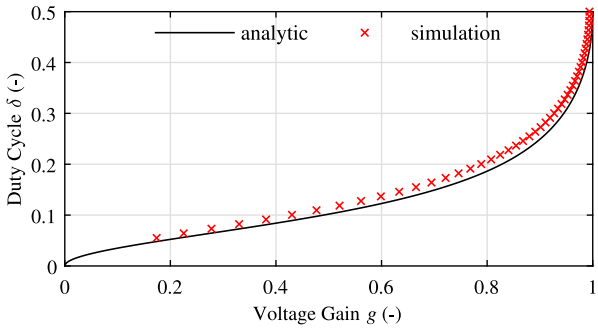


Fig. 8. Linearizing function for the used dc transformer prototype for rated current and rated voltage. The solid line represents the analytic solution according to (21) and (22). The crosses represent the characterization based on the PLECS switched simulation.

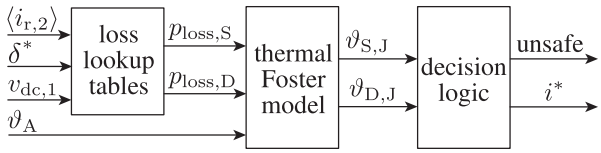


Fig. 9. Loss and thermal model overview.

a constantly set duty cycle δ and constant current source for current $i_{\mathrm{dc},2}$. Generally, a good match between the simulation results and the analytic equation can be concluded with only a small offset in x-axis caused by the converter losses that were not considered in the derivation. Note that this observable voltage drop over the equivalent resistance is partly considered in the proposed control system by feed-forward control, as depicted in Fig. 5.

Although [25] presents a more precise derivation without simplifications, the relationship $\delta(g)$ cannot be expressed analytically in the explicit form and thus, it is not suitable for online calculation.

VII. Loss and Thermal Model

The task of the loss and thermal model is to estimate and supervise the junction temperatures of the bridge semiconductor switches and diodes. The model determines whether the operation of the converter is safe and it determines what maximum current can be delivered by the dc transformer to the grid based on the current thermal conditions. An overview of the model is displayed in Fig. 9.

Based on the operating conditions, i.e., delivered current $\langle i_{\mathrm{r},2}\rangle$, duty-cycle setpoint δ^* delayed by one control step (see Fig. 3), and dc-link voltage $v_{\mathrm{dc},1}$, the mean losses within the last switching half-period are determined for the switches ($p_{\mathrm{loss,S}}$) and for the diodes ($p_{\mathrm{loss,D}}$). In the presented implementation, the losses are determined from a lookup table that was prepared offline in advance. These losses are fed into the thermal model that determines the junction temperature of the switches $\vartheta_{\mathrm{S,J}}$ and of the diodes $\vartheta_{\mathrm{D,J}}$. Based on the estimated junction temperatures, "decision logic" block recognizes if the operation is unsafe (initiating emergency stop) and determines the maximum

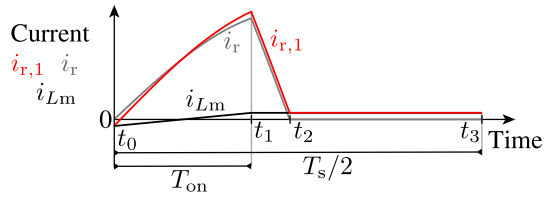


Fig. 10. Approximation of the bridge output current $i_{r,1}$. The current is a superposition of the simplified *LC* circuit current i_r and the linearized magnetizing current i_{Lm}.

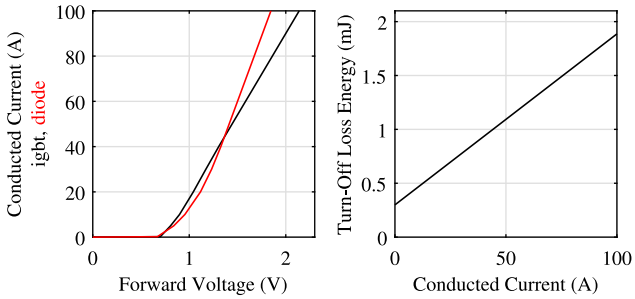


Fig. 11. Characterized conduction characteristic of the diode and the IGBT (left) and the turn-OFF energy loss characteristic of IGBT for 200 V dc-link voltage (right).

thermally feasible current that can be delivered under the current conditions by the dc transformer.

A. Loss Lookup Tables

Generally, it is too complex to determine the losses of the bridge online and thus, the lookup tables are utilized in the implementation. Since the loss-equalizing modulation technique is employed, the losses are distributed equally between the switches. Consequently, it is sufficient to implement a single lookup table for switches and another for the diodes.

The lookup tables are generated via repeating the following steps over all operating conditions of interest.

1) The steady-state output current waveform of Bridge 1 $i_{r,1}$ is determined for the given operating conditions.
2) The current $i_{r,1}$ is utilized to determine the conducted currents and the switched currents according to loss-equalizing modulation method, as described in [20].
3) The turn-OFF energies and conduction loss are determined according to switch and diode characteristics and the mean loss power is determined and saved into the lookup table.

The losses are calculated for three relevant varying parameters: delivered current $\langle i_{r,2} \rangle$, duty-cycle setpoint δ^*, and dc-link voltage $v_{dc,1}$.

The steady-state waveform of the bridge current $i_{r,1}$ can be generally determined either by switched simulations or by solving the equation system that describes the resonant tank, e.g., as presented in [25].

In this article, the current waveform $i_{r,1}(t)$ is approximated as a superposition of a series-resonant current waveform that is determined from the model in Fig. 6 using its analytic solution and the linear approximation of the magnetizing current i_{Lm} that changes from the negative value $-\hat{i}_{Lm}$ to the positive value

$$\hat{i}_{Lm} = \delta \cdot T_s \cdot \frac{v_{dc,1}}{2 \cdot L_m} \quad . \tag{23}$$

The decomposition of currents is displayed in Fig. 10. While this approximation proved to be sufficient to estimate losses in our application, its applicability needs to be carefully evaluated before utilizing it elsewhere.

Fig. 11 shows the characterized loss characteristics of the IXYS IGBT/diode module [19] that is utilized in the example dc transformer. Since zero-voltage switching is expected during the operation, the turn-ON loss energy of the IGBT and the reverse-recovery losses of the diode are not required. These characteristics are utilized to generate the lookup tables.

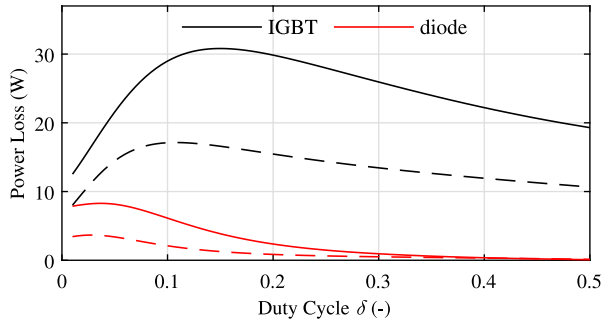


Fig. 12. Example showing a part of the loss lookup tables for $v_{dc,1} = 200$ V. The solid lines represents delivered current $i_{dc,2} = I_{dc,2,N}$, the dashed lines represent $i_{dc,2} = 0.5 \cdot I_{dc,2,N}$.

A part of the lookup tables is displayed in Fig. 12, showing the dependence of the IGBT and diode losses on the duty cycle at rated delivered current (solid lines) and half of the rated current (dashed lines). The figure clearly shows that the losses increase with decreased duty cycle and hence, the current-limiting operation with the rated current is expected to be possible only for a short period of time. A continuous operation is only feasible with reduced delivered current (with reduced losses).

B. Thermal Model

The thermal model is required to determine the junction temperatures of the switch and the diode. The implemented model consists of three separate Foster-network thermal models: The first is fed by the losses of the switch $p_{loss,S}$ to determine its junction-to-case temperature $\Delta\vartheta_{S,J-C}$. The second model uses the diode loss power $p_{loss,D}$ to determine the diode junction-to-case temperature $\Delta\vartheta_{D,J-C}$. Finally, the third model describes the sink that has two switches and two diodes on it. Hence, the losses applied to the cooler model are $2 \cdot p_{loss,S} + 2 \cdot p_{loss,D}$ leading to the case-to-ambient temperature $\Delta\vartheta_{C-A}$. If different configuration for the sink is applied, the model has to be adjusted accordingly.

All thermal models are implemented using identical generic three-section Foster-network models as depicted in Fig. 13. The Foster-network model has an advantage that the temperature of

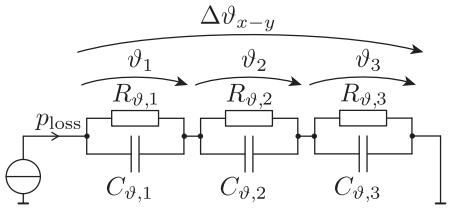


Fig. 13. Generic three-section Foster-network thermal model used for modeling of the diode, the switch, and the sink.

TABLE II
THERMAL PARAMETERS OF THE PROTOTYPE

	i	1	2	3
IGBT	$R_{\vartheta,i}$ (K/kW)	114.6	146	47.6
	$C_{\vartheta,i}$ (J/K)	2.399	0.198	0.03
diode	$R_{\vartheta,i}$ (K/kW)	124	228.7	181.4
	$C_{\vartheta,i}$ (J/K)	0.006	0.099	1.692
sink	$R_{\vartheta,i}$ (K/kW)	62.5	84.3	181.2
	$C_{\vartheta,i}$ (J/K)	1034.9	21.6	165.9

each section i ($i \in 1..3$)

$$\vartheta_i(k) = \vartheta_i(k-1) + \frac{T_\text{s}/2}{C_{\vartheta,i}} \cdot \left(p_\text{loss}(k) - \frac{\vartheta_i(k)}{R_{\vartheta,i}} \right) \tag{24}$$

can be calculated independently, assuming the thermal model is executed at each switching half-period $T_\text{s}/2$. Since the temperature changes very slowly, a simple backward-Euler integration leads to a sufficient precision. Finally, the total temperature drop over the generic Foster network

$$\Delta\vartheta_{x-y}(k) = \sum_{i=1}^{3} \vartheta_i(k) \tag{25}$$

is calculated as a sum of the temperatures of the individual sections.

The junction temperatures of the switch and of the diode

$$\vartheta_\text{S,J} = \Delta\vartheta_\text{S,J–C} + \Delta\vartheta_\text{C–A} + \vartheta_\text{A} \tag{26}$$

$$\vartheta_\text{D,J} = \Delta\vartheta_\text{D,J–C} + \Delta\vartheta_\text{C–A} + \vartheta_\text{A} \tag{27}$$

are calculated by summing the junction-to-case temperature, the case-to-ambient temperature, and the measured ambient temperature ϑ_A. If the measured ambient temperature is not available, a worst-case ambient temperature can be assumed instead. Nevertheless, this practice is not recommended, since it does not utilize the full potential of the dc transformer during the overload.

The thermal parameters for the experimental prototype of the dc transformer are summarized in Table II. The sink parameters were characterized experimentally by applying defined loss steps to the switches and measuring the temperature waveforms with the thermocouples [see Fig. 2(b)]. The parameters for the diode and the IGBT were obtained by fitting the transient thermal impedance from the datasheet [19].

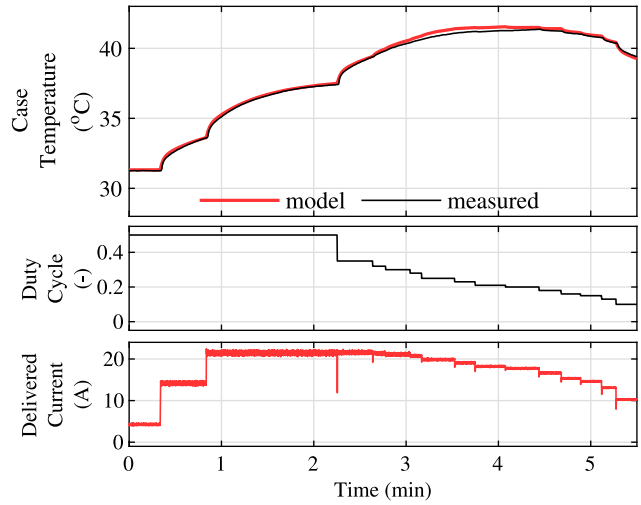


Fig. 14. Experimental validation of the thermal and loss model. The duty cycle is varied in an open-loop manner and the delivered current results from the conditions set up at Grid 2. The voltage at Grid 1 is constant at $v_{\text{dc},1} = 200$ V. The ambient temperature is $\vartheta_\text{A} = 27\,^\circ$C.

C. Validation of the Loss and Thermal Models

To validate the loss and thermal models, an open-loop experiment with varying duty cycle and delivered current was conducted. The captured waveforms are displayed in Fig. 14.

The figure compares how the case temperature measured directly by the thermocouple (plotted for the switch with the worst thermal resistance) and the temperature estimated from the online thermal model evolve. It can be seen that the estimated temperature matches the measured one very well. Therefore, both loss model and the thermal model can be concluded to be valid and sufficiently precise.

D. Decision Logic for Setpoint Current

The main idea of the article, as described in Section II, is to limit the transferred current of the dc transformer to its rated value in order to let the dc grid recognize that overload conditions are present. Hence, the setpoint value for the converter i^* is preferably set to the rated value $I_{\text{dc},2,\text{N}}$.

Nevertheless, the operation with reduced duty cycle and rated current leads to significantly increased losses (see example in Fig. 12) and thus, such operation is thermally sustainable only for a short period of time. Moreover, when the duty cycle is decreased, the turn-OFF current increases, possibly even above the safe-operating-area (SOA) limit.

When the temperatures or the turn-OFF currents rise to dangerous levels, an action needs to take place. One option is to activate an emergency state (signifying unsafe operating conditions) and turn off the bridge to protect the dc transformer. The other option is to slowly decrease the setpoint current i^* as the temperatures or turn-OFF currents are rising linearly to some safe value. Since the total thermal resistances are known, it is possible to calculate what loss values are long-term sustainable. Then, these losses can be cross-correlated with the given operating conditions (δ^* and $v_{\text{dc},1}$) in the loss lookup table to determine the maximum

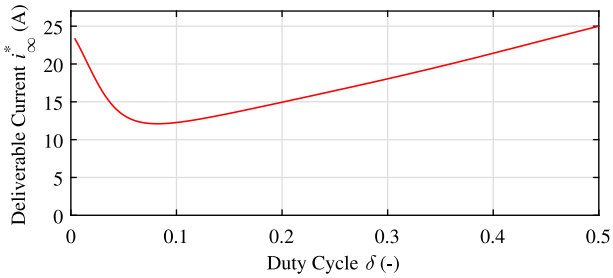


Fig. 15. Maximum steady-state current that is feasible with the dc transformer prototype as a function of duty cycle for $v_{\mathrm{dc},1} = 200$ V.

sustainable current. Although the second option is more complex to implement, it enables a possible restoration of the dc grid voltage even after a long-period heavy overload without an interruption of the dc transformer operation.

In the present implementation, the current setpoint is selected as the rated current: $i^* = I_{\mathrm{dc},2,\mathrm{N}}$, until the estimated junction-to-ambient temperature of the switch $\Delta\vartheta_{\mathrm{S,J-A}}$ reaches 95 % of the rated temperature $\Delta\vartheta_{\mathrm{J-A,N}}$. Once the estimated temperature is above this limit, the current setpoint i^* is gradually decreased with linear slope according to the rising temperature to the current value $i^*_\infty(v_{\mathrm{dc},1}, \delta)$ that is estimated as long-term feasible. The long-term feasible current i^*_∞ is determined as a current that causes the steady-state temperature rise of $\Delta\vartheta_{\mathrm{S,J-A}} = \Delta\vartheta_{\mathrm{J-A,N}}$. In the implementation, its value is determined from a dedicated lookup table. An example of the characteristic is plotted in Fig. 15.

The described practice maximizes the transferred current during the overload, which is ensured by the fact that the junction temperature increases monotonically for the increased transferred current.

E. Option to Vary the Switching Frequency

Considering the increased losses during current-limiting mode, it comes naturally as an idea to look for options how to lower these. An option would be to change the switching frequency together with decreasing duty cycle. Theoretically, an optimized characteristic of δ and f_{s} for each required voltage gain g can be found for the particular dc transformer to minimize its losses. This characteristic can then be added to the control scheme.

Nevertheless, the potential loss reduction is expected to be fairly low. Although the number of switching instants is lower for lower switching frequencies, the magnitude of the switched current has to be increased to deliver the same mean current with lower number of pulses. Moreover, the current form factor becomes worse as well for lower switching frequencies, leading to increased conduction losses.

This expectation is confirmed by calculating the total bridge losses (total losses of Bridge 1) for the dc transformer prototype at three switching frequencies: $f_{\mathrm{s}} = 0.8 \cdot f_0$, $f_{\mathrm{s}} = f_0$, and $f_{\mathrm{s}} = 1.2 \cdot f_0$. The results, plotted in Fig. 16, clearly demonstrate that the differences in losses are marginal. However, Fig. 16 also shows that by increasing the switching frequency, the turn-OFF current is reduced. Consequently, increasing the switching frequency can come in handy when the turn-OFF currents would be outside of the SOA of the semiconductor switch.

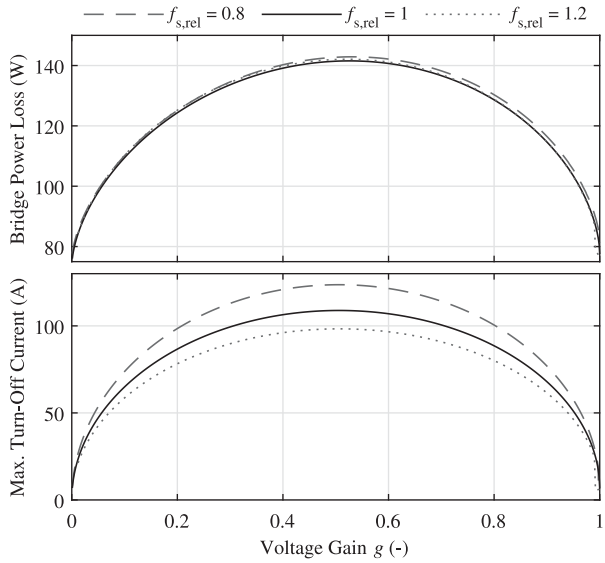


Fig. 16. Impact of the variation of the switching frequency ($f_{\mathrm{s,rel}} = f_{\mathrm{s}}/f_0$) on the total bridge losses and the maximum turn-OFF current, assuming the grid voltage $v_{\mathrm{dc},1} = 200$ V and the delivered current $\langle i_{\mathrm{r},2}\rangle = 25$ A.

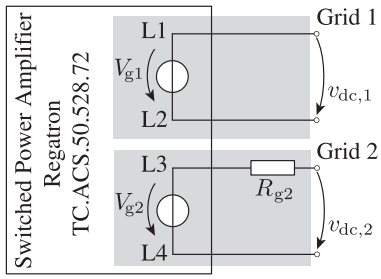


Fig. 17. Configuration of the dc grids for the experiments using the Regatron switched power amplifier.

Since the expected turn-OFF currents of the dc transformer prototype are well within the SOA and the utilized control platform does not currently support variable frequency operation, this option was not practically implemented.

VIII. Experimental Validation

To validate and demonstrate the proposed closed-loop current limiting method, experiments were conducted on the down-scaled 5 kW 1:1 dc transformer prototype presented at Section III (the prototype parameters are summarized in Table I). In the experiments, the dc grids are represented by the switched power amplifier Regatron TC.ACS. As shown in Fig. 17, lines L1 and L2 generate the voltage of Grid 1 which behaves as a very stiff grid with almost constant voltage $v_{\mathrm{dc},1} = V_{\mathrm{g1}}$. Grid 2 is a rather weak grid and is emulated as a series connection of the power amplifier voltage V_{g2} (lines L3 and L4 of the amplifier) and a resistor $R_{\mathrm{g2}} = 4.6\,\Omega$. The transferred power

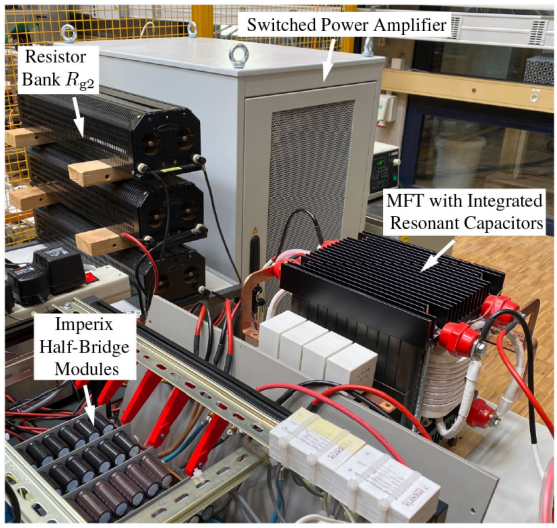


Fig. 18. Photograph of the experimental setup.

of the dc transformer is set by adjusting the voltage drop over the resistor R_{g2} via voltage V_{g2}. In Fig. 18, the photograph of the experimental setup is shown.

In the first experiment, performance of the current-limiting mode during short-time overload was studied. The overload was generated for time duration of 10 ms in Grid 2 by setting the voltage V_{g2} to zero, making the load purely resistive with resistance of $R_{g2} = 4.6\,\Omega$. Before and after the overload, the voltage V_{g2} is adjusted to achieve the transferred current $i_{dc,2} = 18$ A in steady state (this represents an operation at roughly 70 % of the rated power). The voltage of Grid 1 was set to $v_{dc,1} = 200$ V. The key waveforms of the operation are depicted in Fig. 19. The current and voltage waveforms were captured by an eight-channel oscilloscope "Yokogawa DLM 4058" using 10 MHz current probes and 100 MHz differential voltage probes, respectively. The duty cycle δ and the estimated relative junction-to-ambient temperatures

$$\begin{bmatrix} \Delta\vartheta_{\mathrm{S,J-A,rel}} \\ \Delta\vartheta_{\mathrm{D,J-A,rel}} \end{bmatrix} = \frac{1}{\Delta\vartheta_{\mathrm{J-A,N}}} \cdot \begin{bmatrix} \Delta\vartheta_{\mathrm{S,J-A}} \\ \Delta\vartheta_{\mathrm{D,J-A}} \end{bmatrix} \tag{28}$$

were captured by the logging function of the Imperix B-Box control platform. The synchronization between the scope waveforms and the logged data was achieved offline in Mathworks Matlab by the "limiting mode" signal, indicating the activation of the current-limiting mode, that was electrically coupled to the scope. The delivered current $\langle i_{r,2} \rangle$ waveform was determined in postprocessing from the measured current $i_{r,2}$.

Fig. 19(a) demonstrates the performance of the current limiting in the dc transformer during the short overload. At the beginning, the dc transformer is operated in steady state in open loop outside of the current limiting mode [see Fig. 19(b) for detailed view of the waveforms]. As can be seen, at time $t \approx 1$ ms, the overload condition occurs and the loading current at the secondary side is suddenly increased to $i_{dc,2} \approx 40$ A. Consequently, the voltage at the secondary side of the converter $v_{dc,2}$ starts to drop and the transferred current of the dc transformer $\langle i_{r,2} \rangle$ increases. Once it crosses the rated current value of $i_{dc,2,N} = 25$ A at the time $t \approx 1.5$ ms, the current limiting mode is activated and the duty cycle is decreased by the proposed closed-loop controller. Because there is a clear mismatch between the current required by the loads $i_{dc,2}$ and the current delivered by the transformer $\langle i_{r,2} \rangle$, the dc link voltage $v_{dc,2}$ is further decreasing. After 10 ms (at time $t \approx 11$ ms), the overload conditions are over and the loading current $i_{dc,2}$ is decreased. In practice, the overload conditions have either ended naturally or Grid 2 must have taken some action. Despite the decreased load, the dc transformer continues delivering the constant current until the steady-state value of the secondary-side voltage $v_{dc,2}$ is reached. First, when the duty cycle becomes steady at $\delta = 0.5$ for ten subsequent periods, the current limiting mode is deactivated and the open-loop operation with constant duty cycle $\delta = 0.5$ is entered again.

Fig. 19(a) shows that the controlled current $\langle i_{r,2} \rangle$ has a slight deviation from the setpoint value $i^* = 25$ A in the current limiting mode because the grid voltage $v_{dc,2}$ changes relatively fast. Nevertheless, it can be concluded that the current-limiting behavior is effective and sufficiently precise.

Fig. 19(b)–(e) shows detailed waveforms of the resonant tank in different conditions: Fig. 19(b) and (e) demonstrates the steady-state operation before and after the overload; Fig. 19(c) and (d) shows the detail of the operation in current-limiting mode during the overload as the grid voltage $v_{dc,2}$ is dropping (observable at the decreasing amplitude of $v_{r,2}$). Observing the current and voltage waveforms of the inverting stage i_{r1} and v_{r1}, it can be seen that by reducing the duty cycle during overload, the current waveforms are modified and significantly higher current is turned OFF by the IGBTs. Nevertheless, after a short analysis (similar as done in [20]), it can be recognized that the magnetizing current still ensures that the antiparallel diode is conducting while the IGBT turns ON. Hence, the zero-voltage switching is not affected by the reduced duty cycle (avoiding IGBT's turn-ON losses and diode's reverse-recovery losses). Observing the currents and voltages i_{r2} and v_{r2} on the rectifying side, it can be seen that the reduced duty cycle causes a discontinuous operation of the rectifier. Once the diodes stop conducting, oscillations caused by their parasitic capacitances occur that are observable in the voltage v_{r2}. Nevertheless, these oscillations do not have a negative impact on the operation.

The increased losses due to the modified current waveforms during current-limiting mode can be clearly seen at the rising relative junction-to-ambient temperatures of the IGBT $\Delta\vartheta_{\mathrm{S,J-A,rel}}$ and the diode $\Delta\vartheta_{\mathrm{D,J-A,rel}}$ in Fig. 19(a). Nevertheless, the thermal capacitances are sufficient for the temperature not to rise to any dangerous limits. Hence, during the short-time overload in the first experiment, the setpoint delivered current i^* was not reduced.

In the second experiment, the same overload conditions were repeated but for a longer overload time of 1 s to demonstrate the action of the thermal model. The key waveforms are plotted in Fig. 20.

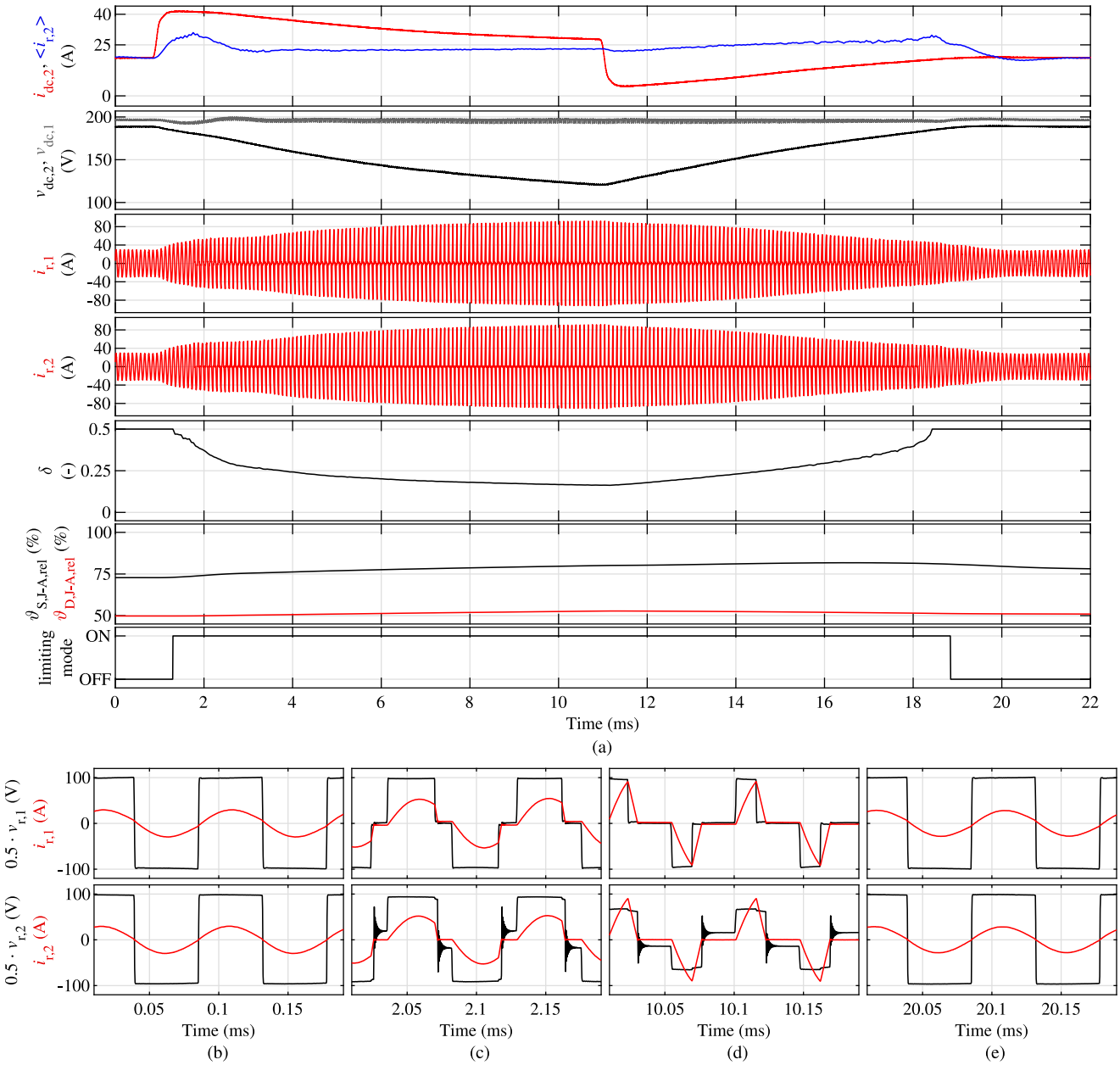


Fig. 19. Experimental results showing the current limiting during a short-time overload (duration of 10 ms). (a) Waveforms showing the activation of the current limiting mode and the behavior of the system. (b)–(e) Detailed view of the resonant tank waveforms at different operation points. The currents and voltages were captured by an eight-channel oscilloscope; the rest of the signals was recorded by the logging function of B-Box control platform. The waveforms are synchronized and postprocessed in Mathworks MATLAB.

As Fig. 20 shows, immediately after the overload was applied, the system responses identically as in the first experiment. However, since the overload conditions are applied for longer time, the energy from the dc link capacitor $C_{\mathrm{dc},2}$ is removed and its voltage $v_{\mathrm{dc},2}$ stabilizes at a new steady state according to the resistance $R_{\mathrm{g},2}$ and the delivered current $\langle i_{\mathrm{r},2} \rangle$. Since this operating point generates increased losses, the temperature rises accordingly.

At time $t \approx 180$ ms, the temperature reaches $95\,\%$ of the safe limit and thus, the setpoint current is decreased slowly towards the long-term feasible current i^*_∞. Because of the resistive nature of the load, the decreased current further decreases Grid 2 voltage $v_{\mathrm{dc},2}$ and consequently, the duty cycle is further reduced as well. As the results in Fig. 20 clearly demonstrate, the described practice effectively slowed down the temperature rise to an acceptable level and the temperature limit of 100% of the rated temperature was not exceeded.

After the overload conditions are cleared (at time $t \approx 1050$ ms), the voltage of the grid is restored in a procedure similar to that in Fig. 19(a). Subsequently, the dc transformer is operated in the open-loop mode again and the temperatures drop towards those of the original steady state.

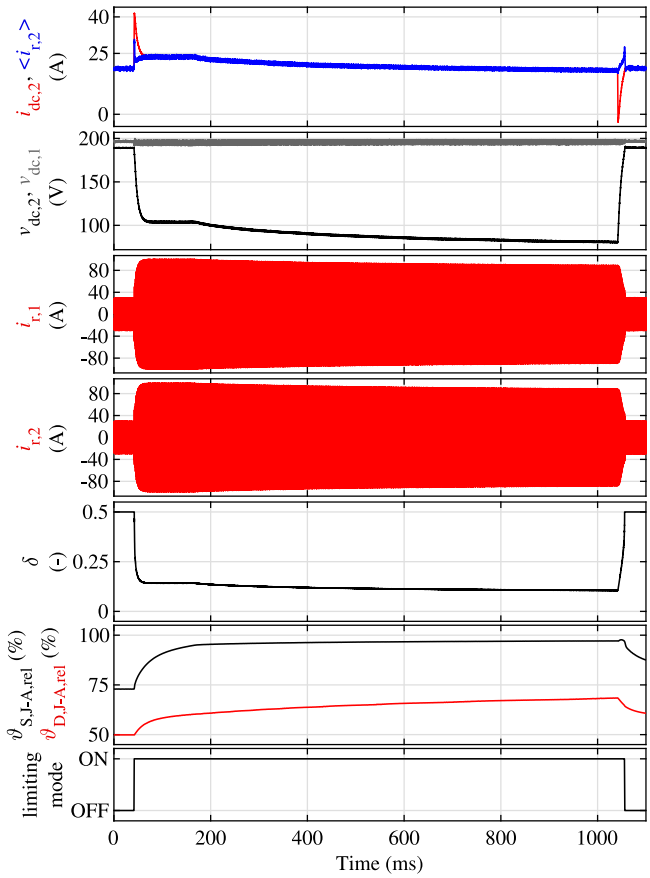


Fig. 20. Experimental results showing the current limiting during a long-time overload (duration of 1 s). The currents and voltages were captured by an eight-channel oscilloscope; the rest of the signals was recorded by the logging function of B-Box control platform. The waveforms are synchronized and postprocessed in Mathworks MATLAB.

IX. Conclusions and Outlook

This article has proposed a novel closed-loop control approach to limit the transferred current of *LLC*-converter-based dc transformers that utilizes a thermal model to ensure the safe operation. The proposed mode is an additional feature for the open-loop operated converter that is activated only during overload conditions. The design and implementation of the closed-loop controller and the thermal model was presented and discussed in detail. The effectiveness of the method has been demonstrated on a downscaled dc transformer prototype, showing the system behavior during both short-time and long-time overload conditions.

It can be concluded that the proposed current-limiting mode performs satisfactory and that the proposed thermal model is capable of supervising and limiting the junction temperatures.

Finally, the proposed current-limiting mode is a preferable solution for dc transformers, since it offers an option for the grid to recognize that overload conditions are present and to take some regulatory action, such as supply from an energy storage or load shedding. Moreover, since the proposed mode is based on the duty-cycle reduction, it does not require any major hardware changes, making it a cost-and-space-efficient add-on for *LLC*-converter-based dc transformers.

In the future research, the effectiveness and suitability of the proposed approach will be verified for a high-power medium-voltage dc transformer prototype.

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