Backstepping Control of High-Frequency Link Matrix Rectifier for Battery Chargers

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***Abstract*—High-frequency link matrix rectifier (HFLMR) is getting much interest in electric vehicle charger applications due to its high efficiency and compact volume. However, the inputs and outputs of HFLMR are highly coupled resulting in reduced system dynamic performance and robustness. This article proposes a dual closed-loop backstepping control (DCL-BSC) strategy to solve these problems, which consists of a dc output current outer-loop controller and a grid current inner-loop controller. First, the nonlinear mathematical model of HFLMR is established, and the six-segment space vector pulse width modulation scheme is used as the modulation method. Then, the DCL-BSC scheme is designed in detail based on the Lyapunov stability theory. And a compensation method based on the phase-shift angle is developed to realize the unity power factor. Compared with the conventional dual closed-loop PI control method, the proposed method has a better steady-state and dynamic performance, and robustness against system disturbances. Simulation and experimental results are used to verify the effectiveness of the proposed control scheme.**

***Index Terms*—Dual closed-loop backstepping control, high-frequency link matrix rectifier (HFLMR), output current regulation, power factor (PF) control.**

I. Introduction

ACCORDING to the prediction of [1], the global electric vehicle (EV) stock will expand from around 8 million in 2019 to 50 million by 2025 and close to 140 million vehicles by 2030, corresponding to an annual average growth rate close to 30%. The EV charger is a necessary equipment to supply energy of the battery, so it is the key infrastructure for EV promotion and application [2]. The two-stage topology has been widely utilized in the EV charger system, which is usually a three-phase pulsewidth modulation (PWM) rectifier followed by an isolated dc–dc converter. The *LLC* resonant converter, which has the advantages of soft switching and high efficiency is commonly used as the isolated dc–dc stage [3]. The two-stage topology has the merits of decoupling control for the two-stage converter and simple control algorithm [4]–[6]. However, the dc-link film capacitors increase the system volume and decrease power density and reliability [7]. High-frequency link matrix rectifier (HFLMR) without the dc-link capacitor is one kind of single-stage converter. So, HFLMR has the advantages of high efficiency, compact volume, and tight dc output regulation capability, which has been a preferred choice for EV chargers [8], [9].

In order to obtain higher efficiency and adjustable output current, several modulation methods were studied in recent years. The modulation methods are mainly divided into three categories, including line-to-line voltage modulation [10], sinusoidal carrier-based PWM [11] and space vector pulsewidth modulation (SVPWM) [12], [13]. Compared with the former two methods, the SVPWM scheme is easier to implement in the digital processor, consequently it is widely used for HFLMR. In order to improve the efficiency and reduce the total harmonic distortion (THD) of HFLMR, a six-segment SVPWM scheme with reduced switching losses was proposed in [14]. A soft-switching modulation scheme and derived closed form solutions to calculate switching times, which reduce conduction losses were proposed in [15]. A dual-period-decoupled space vector phase-shifted modulation was proposed in [16] to eliminate the grid-side current distortion. A PWM scheme was proposed for one phase loss of three-phase power grid in [17], where the zero-voltage switching can be realized for one phase loss operation. Among of the abovementioned modulations, the six-segment SVPWM scheme in [14] is widely used for HFLMR due to the simplicity of implementation.

Although the abovementioned objectives can be achieved by modulation methods, control strategies are also required to satisfy the requirements of the dynamic performance and robustness. In the EV charger applications, HFLMR is required to simultaneously satisfy the control requirements of grid-side and battery-side. For the grid side, the unity power factor (PF) is difficult to guarantee without any modification because of the input LC filters. For the battery-side, fast charging strategies, such as the sinusoidal-ripple-current (SRC) charging strategy [18]–[20], require the output current of HFLMR to track charging command with fast dynamic response and strong robustness. A proportional integral (PI) control strategy was proposed in [21], but it has steady-state errors when tracking the SRC reference value. Thus, several advanced control strategies

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for ac–dc and dc–dc converters have been proposed for the better steady-state and dynamic performance, as well as greater robustness. A model-predictive controller (MPC) is proposed in [22] for a three-phase ac–dc converter to realize a better stability and transient performance. However, the model-based MPC is sensitive to system parameter variations. A finite-time disturbance observer-based nonsingular terminal sliding-mode controller (SMC) was proposed in [23] for buck converters to suppress load disturbances. But the intermediate variables in SMC systems may result in the chattering problem. A backstepping control (BSC) method was designed for the direct power control of a three-phase PWM rectifier in [24], which achieves a good input/output performance with the ability to suppress the system parametric uncertainties.

In the abovementioned control schemes, the BSC is a method to control the strict-feedback nonlinear systems with unmatched disturbances (disturbances that appear on different coordinates than the input control signal), which is one of the most challenging problems in controller design [25]. According to the Lyapunov stability theory, the tracking errors of the BSC scheme exponentially converge to zero, and the output rapidly and precisely tracks reference value. The BSC scheme design procedure can be separated into a sequence of smaller design problems for low-order cascade subsystems, which simplifies controller design procedure of the BSC method [26]. Due to the abovementioned merits, the BSC scheme has been widely employed in the fields of motor drive and multiple manipulator control [27]–[29]. In addition, the applications of BSC scheme in power converters are emerging in recent years [24], [30], [31], [33]. In [30], a BSC scheme for a fuel cell stack/boost power converter system was proposed to guarantee the great output voltage regulation performance. A common dc-bus voltage BSC scheme was constructed for islanded dc microgrids within the acceptable limits under different operating conditions in [31]. Based on the abovementioned advantages, the BSC method is extremely suitable for the multivariable higher order nonlinear HFLMR system.

The specific contributions of this article are follows.

1) A dual closed-loop backstepping control (DCL-BSC) strategy is proposed for the HFLMR, where an inner grid currents loop and an outer current loop are designed.

2) The proposed control strategy provides the better steady-state and dynamic performance, and robustness for the HFLMR.

3) A compensation method based on the phase-shift angle is developed to realize the unity PF.

This article is organized as follows. In Section II, the model of HFLMR is established and the six-segment SVPWM scheme is described. The DCL-BSC scheme and phase-compensation method are designed in Section III. Simulation and experimental results are presented in Sections IV and V, respectively. Finally, the conclusion is given in Section VI.

II. Modeling and Modulation of HFLMR

As shown in Fig. 1, the HFLMR is composed of three-phase input LC filters, six bidirectional switches, high-frequency transformer (turns ratio is $n:1$ and leakage inductance is $L_{\rm lk}$), single-phase uncontrolled diode rectifier and output LC filter ($L_{\rm dc}$ and $C_{\rm dc}$). The input LC filters are used to eliminate the high-frequency harmonics of three-phase grid currents. The line-frequency three-phase voltages are transformed into bipolar high-frequency voltage by the six bidirectional switches, and the adjustable output voltage is obtained by properly controlling six bidirectional switches. The high-frequency transformer isolates the input side and output side. The single-phase uncontrolled diode rectifier converts the bipolar voltage to dc voltage. The output LC filter is used to eliminate ripples of output voltage and current.

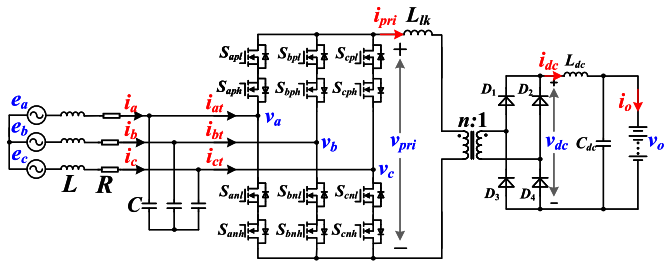


Fig. 1. Topology of HFLMR.

A. Modeling of HFLMR

It is assumed that the grid voltages e_x $(x = a, b, c)$ with angular frequency ω and amplitude E_m are symmetrical, and they are expressed as

$$\begin{cases} e_a = E_m \cos \omega t \\ e_b = E_m \cos\left(\omega t - \dfrac{2\pi}{3}\right) \\ e_c = E_m \cos\left(\omega t + \dfrac{2\pi}{3}\right). \end{cases} \tag{1}$$

The input LC filters cause a displacement angle φ of grid voltages and currents. Therefore, the grid currents i_x $(x = a, b, c)$ can be expressed as

$$\begin{cases} i_a = I_m \cos(\omega t - \varphi) \\ i_b = I_m \cos\left(\omega t - \dfrac{2\pi}{3} - \varphi\right) \\ i_c = I_m \cos\left(\omega t + \dfrac{2\pi}{3} - \varphi\right). \end{cases} \tag{2}$$

The mathematical model of the HFLMR is given as

$$L\frac{di_x}{dt} = e_x - v_x - i_x R \tag{3}$$

$$C\frac{dv_x}{dt} = i_x - i_{xt} \tag{4}$$

$$i_{xt} = \frac{i_{\rm dc}}{n} m_x \tag{5}$$

where $x = a, b, c$, and i_{xt} are the high-frequency input currents of the six bidirectional switches, v_x are input voltages of the six

bidirectional switches, $i_{\rm dc}$ is the output current of diode rectifier, m_x are the modulation ratio indices of HFLMR in the abc frame.

In order to design the BSC scheme, the active components in the dq frame are described as

$$\frac{di_d}{dt} = \frac{e_d - v_d - i_d R}{L} + \omega i_q \tag{6}$$

$$\frac{dv_d}{dt} = \frac{i_d - i_{dt}}{C} + \omega v_q \tag{7}$$

$$i_{dt} = \frac{i_{\rm dc}}{n} m_d. \tag{8}$$

To simplify the dc-side analysis, the effect of the output capacitance is ignored (i.e., yields $i_{\rm dc} \approx i_o$, where i_o is the output current of HFLMR). So, the differential equation on dc side can be written as

$$v_{\rm dc} = L_{\rm dc}\frac{di_o}{dt} + v_o \tag{9}$$

where $v_{\rm dc}$ is the output voltage of diode rectifier and v_o is the dc output voltage of HFLMR.

To integrate the model of ac and dc sides, the power balance expression can be written as follows, when the converter losses are ignored for simplification

$$P_{\rm dc} = P_{\rm ac} = v_{\rm dc} i_o = \frac{3}{2}(e_d i_d + e_q i_q). \tag{10}$$

In the dq frame, it can be deduced that $e_d = E_m$ and $e_q = 0$. Then, combining (9) and (10), and considering system disturbances, the model of HFLMR can be expressed as

$$\frac{di_o}{dt} = \frac{3E_m i_d}{2L_{\rm dc} i_o} - \frac{v_o}{L_{\rm dc}} + d(t) \tag{11}$$

where $d(t)$ is the system parameter perturbation, lumped uncertainty terms of the comprehensive model, whose bound is given as $|d(t)| < \rho$, and ρ is a positive real number.

B. Six-Segment SVPWM Scheme

The six-segment SVPWM scheme in [14] is used for controlling the six bidirectional switches of the HFLMR. The modulation of the HFLMR should guarantee that 1) a path must be provided for the output inductor current and 2) short circuit must not occur in the grid filter capacitors. Considering the abovementioned constraints, one of the three bidirectional switches at upper or lower bridge arms must be ON at any time. In consequence, the HFLMR has six active vectors $\vec{I}_a (a = 1, \ldots, 6)$ and three zero vectors $\vec{I}_b (b = 7, \ldots, 9)$ (turn-ON switches on the same bridge), which are summarized in Table I.

Then, the space distribution of the abovementioned nine vectors is shown in Fig. 2, where six sectors N are divided as Table II according to grid phase θ. In sector I, the current reference vector $\vec{i}^*$ is synthesized by two adjacent active vectors ($\vec{I}_1$ and $\vec{I}_2$) and their opposite active vectors ($\vec{I}_4$ and $\vec{I}_5$) and the zero vector ($\vec{I}_7$). According to the volt-second balance principle, their relationship can be expressed as

$$\vec{i}^* T = \vec{I}_1 t_1 + \vec{I}_2 t_2 + \vec{I}_7 t_7 + \vec{I}_4 t_4 + \vec{I}_5 t_5 + \vec{I}_7 t_7. \tag{12}$$

TABLE I
SIX ACTIVE VECTORS AND THREE ZERO VECTORS OF HFLMR

S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	Vector
1	0	0	0	1	0	$\vec{I}_1$
1	0	0	0	0	1	$\vec{I}_2$
0	1	0	0	0	1	$\vec{I}_3$
0	1	0	1	0	0	$\vec{I}_4$
0	0	1	1	0	0	$\vec{I}_5$
0	0	1	0	1	0	$\vec{I}_6$
1	0	0	1	0	0	$\vec{I}_7$
0	1	0	0	1	0	$\vec{I}_8$
0	0	1	0	0	1	$\vec{I}_9$

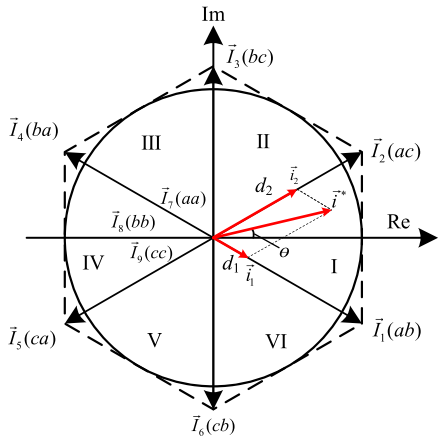


Fig. 2. Space vector diagram of HFLMR.

TABLE II
SECTORS ACCORDING TO GRID PHASE θ

Range of θ	Sector N
$11\pi/6 \le \theta < \pi/6$	$N = 1$
$\pi/6 \le \theta < \pi/2$	$N = 2$
$\pi/2 \le \theta < 5\pi/6$	$N = 3$
$5\pi/6 \le \theta < 7\pi/6$	$N = 4$
$7\pi/6 \le \theta < 3\pi/2$	$N = 5$
$3\pi/2 \le \theta < 11\pi/6$	$N = 6$

The dwell times of active vectors and zero vectors are

$$\begin{cases} t_1 = t_4 = m_d T_s \sin(\pi/6 - \theta)/2 \\ t_2 = t_5 = m_d T_s \sin(\pi/6 + \theta)/2 \\ t_7 = T_s/2 - t_1 - t_2 \end{cases} \tag{13}$$

where T_s is the switching period. The modulation ratio m_d can be defined as

$$m_d = \frac{2i_m^*}{\sqrt{3} I_{am}} \tag{14}$$

where i_m^* and I_{am} are the magnitude of the current reference vector $\vec{i}^*$ and six active vectors $\vec{I}_a$, respectively.

Compared with the conventional SVPWM method, the output current of the six-segment SVPWM scheme has both positive and negative components. Thus, the ac current can pass through

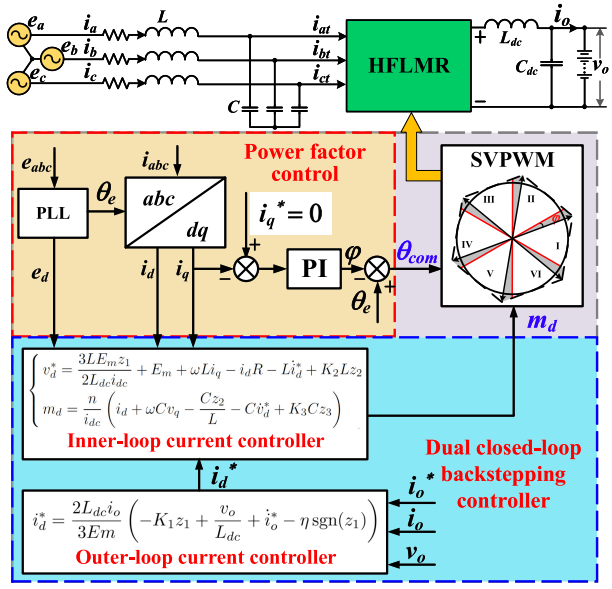


Fig. 3. Control block diagram of HFLMR system.

the high-frequency isolation transformer. The greatest benefit of the six-segment SVPWM scheme is that the output current can be regulated by only changing the modulation ratio m_d.

III. Controller Design

The control block diagram of the HFLMR in this article is shown in Fig. 3. The control objectives are to rapidly and precisely regulate output current at the dc side, and achieve unity PF at the grid side. To meet the requirement of dc side, a DCL-BSC scheme is designed, which consists of a dc output current outer-loop controller and a grid current inner-loop controller. The global large-signal stability is proved based on the Lyapunov stability theory. To meet the requirement of grid side, a phase-compensation method is implemented to realize unity PF. Finally, the six-segment SVPWM scheme is adopted to generate corresponding switch gate signals.

A. DCL-BSC Scheme Design

To design the DCL-BSC scheme, the tracking errors of the outer-loop and inner-loop controller are defined as

$$\begin{cases} z_1 = i_o - i_o^* \\ z_2 = i_d - {i_d}^* \\ z_3 = v_d - {v_d}^* \end{cases} \tag{15}$$

and their derivatives can be represented as

$$\begin{cases} \dot{z}_1 = \dot{i}_o - \dot{i}_o^* \\ \dot{z}_2 = \dot{i}_d - \dot{i}_d^* \\ \dot{z}_3 = \dot{v}_d - \dot{v}_d^*. \end{cases} \tag{16}$$

1) *BSC Design for DC Output Current:* The objective of the outer-loop controller is to ensure that the output current i_o tracks the reference i_o^* under system perturbations.

The Lyapunov function is designed as $V_1 = z_1^2/2$. Based on (11) and (15)–(16), the derivative of V_1 is

$$\begin{aligned} \dot{V}_1 &= z_1 \dot{z}_1 = z_1(\dot{i}_o - \dot{i}_o^*) \\ &= z_1 \left(\frac{3E_m i_d^*}{2L_{\rm dc} i_o} + \frac{3E_m z_2}{2L_{\rm dc} i_o} - \frac{v_o}{L_{\rm dc}} - \dot{i}_o^* + d(t) \right) \\ &\le z_1 \left(\frac{3E_m i_d^*}{2L_{\rm dc} i_o} + \frac{3E_m z_2}{2L_{\rm dc} i_o} - \frac{v_o}{L_{\rm dc}} - \dot{i}_o^* \right) + \rho |z_1|. \end{aligned} \tag{17}$$

The stability of the outer-loop controller can be guaranteed when the derivative of Lyapunov function $\dot{V}_1$ is negative definite. So designing the control law for output current as follows:

$$i_d^* = \frac{2L_{\rm dc} i_o}{3Em} \left(-K_1 z_1 + \frac{v_o}{L_{\rm dc}} + \dot{i}_o^* - \eta \,\mathrm{sgn}(z_1) \right) \tag{18}$$

where $\mathrm{sgn}(\cdot)$ is a sign function, and K_1 and η are positive real numbers. K_1 is the control gain of outer-loop controller, and η is uncertainty bound estimation. The term of i_d^* in (18) can be viewed as a virtual control variable, which is also the reference value of the input of the inner-loop controller.

Substitute the controller (18) into (17), we have

$$\begin{aligned} \dot{V}_1 &\le -K_1 z_1^2 + \frac{3E_m z_2 z_1}{2L_{\rm dc} i_o} - \eta z_1 \mathrm{sgn}(z_1) + \rho |z_1| \\ &= -K_1 z_1^2 + \frac{3E_m z_2 z_1}{2L_{\rm dc} i_o} - (\eta - \rho)|z_1|. \end{aligned} \tag{19}$$

When z_2 converges to zero, $\dot{V}_1 \le -K_1 z_1^2$ can be satisfied (i.e., z_1 can converge to zero with $\rho < \eta$). Next, the inner-loop controller is designed to ensure that z_2 converges to zero.

Another important issue is that the $\mathrm{sgn}(\cdot)$ in output current control law (18) may cause chattering problem, which degrades the system dynamic performance. So we replace $\mathrm{sgn}(\cdot)$ with $\mathrm{sat}(\cdot)$

$$\mathrm{sat}(z_1) = \frac{z_1}{|z_1| + \varepsilon} \tag{20}$$

where ε is the boundary layer thickness.

2) *BSC Design for Three-phase Grid Currents:* The objective of inner-loop controller is to ensure that the i_d and v_d track the reference values i_d^* and v_d^* precisely.

The inner-loop subsystem is a second-order system and the Lyapunov function candidate of the whole closed-loop system can be defined as

$$V = V_1 + {z_2}^2/2 + {z_3}^2/2. \tag{21}$$

Substitute (15)–(16) and (19) into (21), the derivative of V can be obtained as (22) shown at bottom of the next page.

To guarantee the stability of the whole closed-loop control system, the derivative of Lyapunov function $\dot{V}$ must be negative definite. So designing the control law for grid current as follows:

$$\begin{cases} v_d^* = \dfrac{3\,LE_m z_1}{2L_{\rm dc} i_o} + E_m + \omega L i_q - i_d R - L\dot{i}_d^* + K_2\, L z_2 \\ m_d = \dfrac{n}{i_o} \left(i_d + \omega C v_q - \dfrac{C z_2}{L} - C\dot{v}_d^* + K_3 C z_3 \right) \end{cases} \tag{23}$$

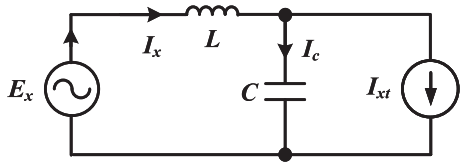


Fig. 4. Simplified equivalent circuit of HFLMR.

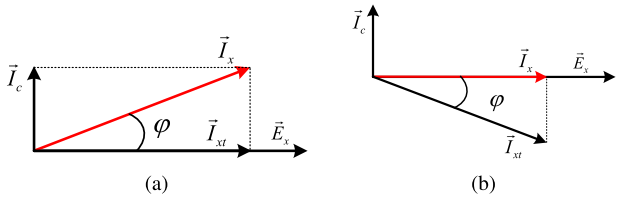


Fig. 5. Phase diagram of grid side. (a) Before compensation. (b) After compensation.

where K_2 and K_3 are positive real numbers of control gains for inner-loop controller.

Substitute the grid current inner-loop control law (23) into (22), we have

$$\begin{aligned}\dot{V} &= -K_1 z_1^2 - (\eta-\rho)|z_1| - K_2 z_2^2 - K_3 z_3^2 \\ &\le -KV - (\eta-\rho)|z_1|\end{aligned} \tag{24}$$

where the coefficient $K = \min\{2K_1, 2K_2, 2K_3\}$.

When $\rho < \eta$, $\dot{V}$ is a negative-definite function. Thus, the global large-signal stability of the DCL-BSC scheme can be guaranteed.

According to the Lyapunov stability theory, z_i $(i = 1, 2, 3)$ converge to zero exponentially. So, the output current is guaranteed to track the reference current rapidly and precisely.

B. Phase-Compensation Method Design

Fig. 4 shows the simplified equivalent circuit of HFLMR at the grid side. The three-phase grid voltages and currents are given as (1) and (2). The voltages across the filter capacitor C in ac side are assumed to be the same as the grid voltages. In consequence, the high-frequency currents $\vec{I}_{xt}$ are in phase with grid voltages without the phase-compensation method [34]. However, the capacitor current $\vec{I}_c$ is leading 90° to the grid voltages. So the phase of grid currents is ahead of grid voltages, especially at light load condition, as shown in Fig. 5(a).

The objective of PF control is to ensure that the i_q converges to zero. As shown in Fig. 5(b), if the phase-shift angle φ can be compensated by shifting the input currents of the six bidirectional switches $\vec{I}_{xt}$ with the same angle, the grid currents $\vec{I}_x$ will be in phase with grid voltages $\vec{E}_x$. A PI compensation method based on the phase-shift angle is proposed to compensate the angle φ. First, the tracking error of PI controller is defined as

$$e = i_q^* - i_q. \tag{25}$$

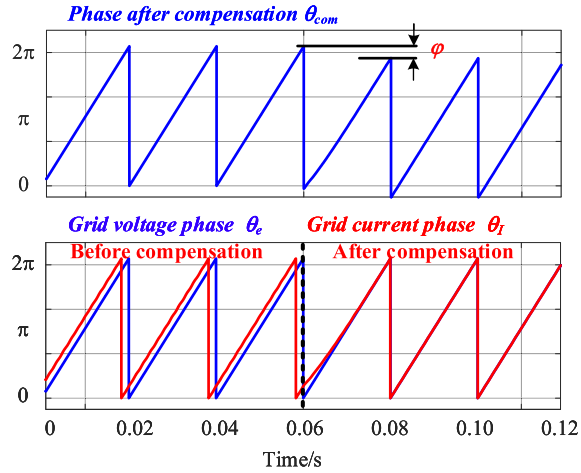


Fig. 6. Waveforms of phase after compensation θ_{com}, grid voltages phase θ_e, and grid currents phase θ_I.

A PI controller is used to generate compensating angle $-\varphi$. Then, the grid voltages phase θ_e adds the compensating angle $-\varphi$. Finally, the angle after compensation $\theta_{\text{com}} = \theta_e - \varphi$ is obtained, which is used to generate the sector N, as shown in Table II.

Fig. 6 shows the waveforms of phase after compensation θ_{com}, grid voltages phase θ_e, and grid currents phase θ_I. It can be seen that θ_I is ahead of θ_V because of the three-phase input LC filters. After phase compensation, θ_I is in phase with θ_e, and θ_{com} decreases by angle φ. Then the θ_{com} is used to generate new sector N of six-segment SVPWM scheme. Therefore, the unity PF can be realized by the phase-compensation method.

$$\begin{aligned}
\dot{V} &\le \dot{V}_1 + z_2\dot{z}_2 + z_3\dot{z}_3 \le -K_1 z_1^2 + \frac{3E_m z_2 z_1}{2L_{\text{dc}} i_o} - (\eta-\rho)|z_1| + z_2\dot{z}_2 + z_3\dot{z}_3 \\
&\le -K_1 z_1^2 - (\eta-\rho)|z_1| + z_2\left(\frac{e_d - v_d - i_d R}{L} + \omega i_q + \frac{3E_m z_1}{2L_{\text{dc}} i_o} - \dot{i}_d^*\right) + z_3\left(\frac{i_d - i_{dt}}{C} + \omega v_q - \dot{v}_d^*\right) \\
&\le -K_1 z_1^2 - (\eta-\rho)|z_1| + z_2\left(\frac{E_m - v_d^* - z_3 - i_d R}{L} + \omega i_q + \frac{3E_m z_1}{2L_{\text{dc}} i_o} - \dot{i}_d^*\right) + z_3\left(\frac{i_d}{C} - \frac{m_d i_o}{nC} + \omega v_q - \dot{v}_d^*\right) \\
&\le -K_1 z_1^2 - (\eta-\rho)|z_1| + z_2\left(\frac{E_m - v_d^* - i_d R}{L} + \omega i_q + \frac{3E_m z_1}{2L_{\text{dc}} i_o} - \dot{i}_d^*\right) + z_3\left(\frac{i_d}{C} - \frac{m_d i_o}{nC} + \omega v_q - \dot{v}_d^* - \frac{z_2}{L}\right)
\end{aligned} \tag{22}$$

TABLE III
PARAMETERS OF SIMULATIONS AND EXPERIMENTS

Parameters	Values
AC grid voltage (RMS)	110 V
Grid frequency	50 Hz
Switching frequency(f_s)	25 kHz
Sampling period	100 μs
Transformer turns ratio($n:1$)	1 : 1
Transformer leakage inductance(L_{lk})	2 μH
LC input filter	L = 1 mH, C = 30 μF
LC output filter	L_{dc} = 1 mH, C_{dc} = 47 μF
LiNCM Battery load	130 V
Resistor load	20 Ω/15 Ω

IV. SIMULATION RESULTS

In order to validate the effectiveness of the proposed control scheme, simulations are performed utilizing MATLAB/Simulink. The key parameters for simulations are summarized in Table III. The switching frequency of HFLMR is chosen as 25 kHz to obtain higher efficiency [35]. Due to the HFLMR is a converter of EV charger, a battery is used as the load to verify the dynamic response of the proposed DCL-BSC strategy. To simulate stronger disturbances, we use resistance as the load to verify the robust performance of the proposed DCL-BSC strategy.

For the proposed DCL-BSC control strategy, the inner-loop control gains are $K_2 = 15\,000$ and $K_3 = 1500$, the outer-loop control gain is $K_1 = 18\,000$, and the uncertainty bound estimation is $\eta = 20\,000$.

A. Simulation Results of Dynamic Performance

Three cases of output current reference are set up to verify the dynamic tracking performance of the conventional DCL-PIC and the proposed DCL-BSC strategy. In these three cases, the open-circuit voltage (OCV) of the LiNCM battery load are all 130 V. In case I, the dc output current reference value increases from 7.5 to 10 A at 0.045 s and then returns to 7.5 A at 0.07 s. In cases II and III, the output current reference value is composed of a dc component and a sinusoidal component, which is $[7.5 + 2.5\sin(20\pi t)]$ A and $[7.5 + 2.5\sin(100\pi t)]$ A, respectively.

Case I: $i_o^* = 7.5\text{ A} \rightarrow 10\text{ A} \rightarrow 7.5\text{ A}$

Fig. 7 shows the dynamic performance of HFLMR in case I, where the waveforms of dc output current reference i_o^*, output current i_o, output voltage v_o, and three-phase currents i_x ($x = a, b, c$) are shown.

Fig. 7(a) shows the dynamic performance under the DCL-PIC strategy. The output current transient response rise time is 7 ms and fall time is 6 ms, respectively. Fig. 7(b) shows the dynamic performance under the proposed DCL-BSC strategy. The output current has little overshoot and immediately reaches steady state. The output current transient response rise time is 2 ms and fall time is 1 ms, respectively.

Compared with the conventional DCL-PIC strategy, the rise time and fall time decrease by about 75% under the proposed DCL-BSC strategy. Thus, it can be seen from Fig. 7 that the proposed DCL-BSC strategy has a better dynamic performance in case I.

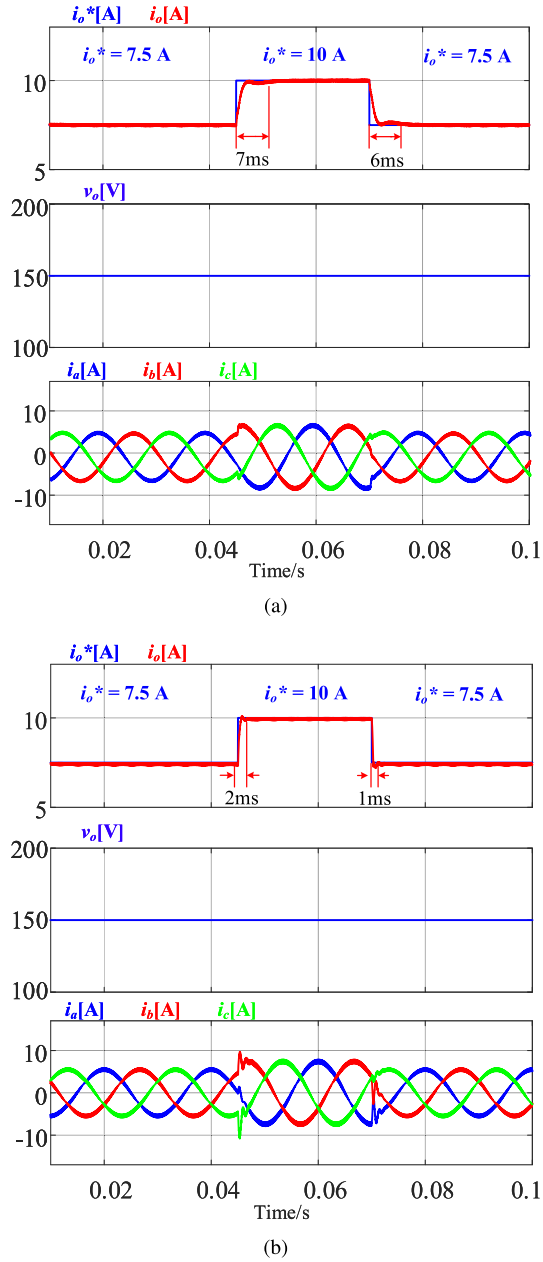


Fig. 7. Dynamic tracking performance of output current i_o in case I. (a) Under the DCL-PIC strategy. (b) Under the DCL-BSC strategy.

Case II: $i_o^* = [7.5 + 2.5\sin(20\pi t)]$ A

Fig. 8 shows simulation results of active current component reference i_d^* and active current component i_d under the DCL-PIC strategy and the proposed DCL-BSC strategy. It can be seen that the amplitude ratio of i_d/i_d^* is 0.95 while the phase of i_d lags behind i_d^* 21.8° under the DCL-PIC strategy. In contrast, the amplitudes of i_d^* and i_d are equal and i_d is in phase with i_d^* under the proposed DCL-BSC strategy.

Fig. 9 shows the dynamic performance of HFLMR in case II. The output current reference i_o^* and output current i_o under

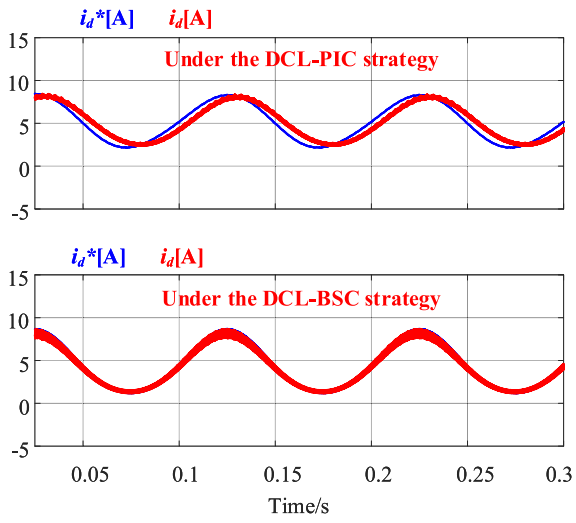


Fig. 8. Dynamic tracking performance of active current component i_d under the DCL-PIC strategy and the DCL-BSC strategy in case II.

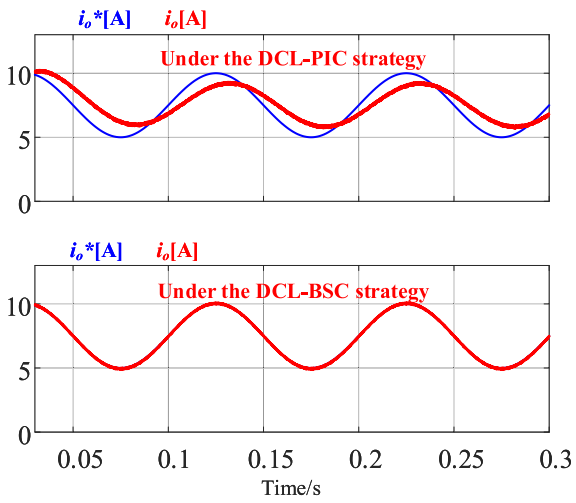


Fig. 9. Dynamic tracking performance of output current i_o under the DCL-PIC strategy and the DCL-BSC strategy in case II.

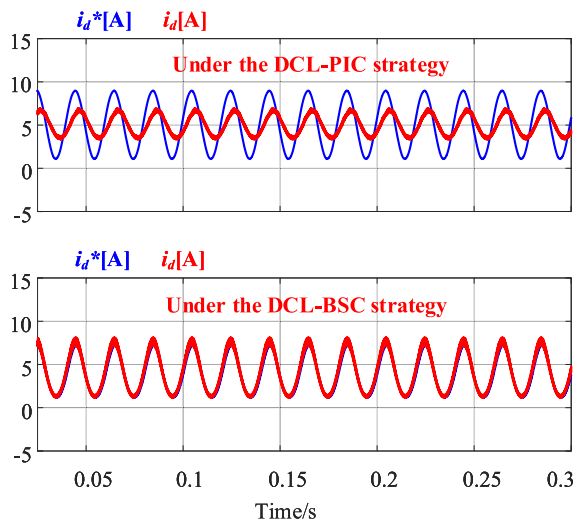


Fig. 10. Dynamic tracking performance of active current component i_d under the DCL-PIC strategy and the DCL-BSC strategy in case III.

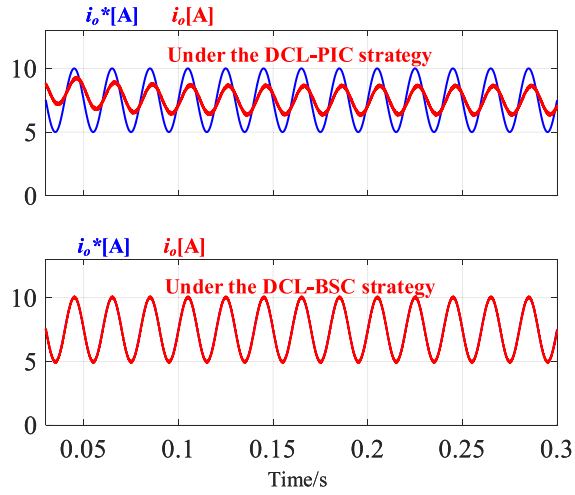


Fig. 11. Dynamic tracking performance of output current i_o under the DCL-PIC strategy and the DCL-BSC strategy in case III.

the DCL-PIC strategy and the proposed DCL-BSC strategy are shown. It can be seen that the amplitude ratio of i_o/i_o^* is 0.92 and the phase of i_o lags behind i_o^* 18° under the DCL-PIC strategy. In contrast, under the DCL-BSC strategy, the amplitudes of i_o^* and i_o are equal and i_o is in phase with i_o^*. Thus, the i_o tracks the reference value i_o^* well under the proposed DCL-BSC strategy.

Case III: $i_o^* = [7.5 + 2.5\sin(100\pi t)]$ A

Fig. 10 shows simulation results of active current component reference i_d^* and active current component i_d under the DCL-PIC strategy and the proposed DCL-BSC strategy. It can be seen that the amplitude ratio of i_d/i_d^* is 0.75 and the phase of i_d lags behind i_d^* 25° under the DCL-PIC strategy. In contrast, under the proposed DCL-BSC strategy, the amplitude ratio of i_d/i_d^* is 1.04 and i_d lags behind i_d^* −9°.

Fig. 11 shows the dynamic performance of HFLMR in case III. The output current reference i_o^* and output current i_o under the DCL-PIC strategy and the proposed DCL-BSC strategy are shown. It can be seen that the amplitude ratio of i_o/i_o^* is 0.88 and the phase of i_o lags behind i_o^* 36° under the DCL-PIC strategy. In contrast, under the DCL-BSC strategy, the amplitudes of i_o^* and i_o are equal and i_o lags behind i_o^* 5°. Thus, the i_o tracks the reference value i_o^* well under the proposed DCL-BSC strategy.

The tracking results under the conventional DCL-PIC strategy and the proposed DCL-BSC strategy are summarized in Table IV.

The tracking performance of i_d^* indicates the dynamic performance of inner-loop controller. The tracking performance of i_o^* indicates the dynamic performance of dual closed-loop controller. It can be concluded from Figs. 8–11 that the DCL-BSCs inner-loop and outer-loop controllers have a better tracking performance than the DCL-PIC strategy to track ac charging current reference.

TABLE IV
COMPARISONS OF AC CURRENT REFERENCE TRACKING PERFORMANCE

Frequency	Amplitude and phase	Conventional method (DCL-PIC)	Proposed method (DCL-BSC)
10 Hz	i_d lags i_d^*	21.8°	0°
	i_d/i_d^*	0.95	1
	i_o lags i_o^*	18°	0°
	i_o/i_o^*	0.92	1
50 Hz	i_d lags i_d^*	25°	−9°
	i_d/i_d^*	0.75	1.04
	i_o lags i_o^*	36°	5°
	i_o/i_o^*	0.88	1

B. Simulation Results of Robust Performance

Three cases of disturbances are set up to verify the robust performance of the conventional DCL-PIC and the proposed DCL-BSC strategy. In these three cases, the output current reference is constant $i_o^* = 10$ A. In case I, the resister load decreases from 20 Ω to 15 Ω at 0.045 s and then returns to 20 Ω at 0.07 s. In case II, the magnitude of phase voltage increases from 155 to 180 V at 0.045 s and then returns to 155 V at 0.07 s. In case III, the controller parameters are $L/2$ and $C/2$, and the actual converter parameters are the same as that in Table III.

Case I: Load variations 20 Ω → 15 Ω → 20 Ω

Fig. 12 shows the robust performance of the HFLMR against load variations, where waveforms of output current i_o, output voltage v_o, and three-phase grid currents i_x $(x = a, b, c)$ are shown. Due to load variations, the i_o has a current fluctuation of 4 A and returns to 10 A after 6 ms, and the v_o reaches 150 V in 6 ms under the DCL-PIC strategy. In contrast, i_o has little overshoot and reaches the steady state in 1 ms, and v_o reaches 150 V in 1 ms under the DCL-BSC strategy. In addition, the grid currents are sinusoidal with THD 2.28% and 2.14% during load variations under the DCL-PIC strategy and the DCL-BSC strategy, respectively. The results of the comparison show that the proposed DCL-BSC strategy has better robustness than the DCL-PIC strategy against load variations.

Case II: Grid variations 155 V → 180 V → 155 V

Fig. 13 shows the robust performance of the HFLMR against grid variations, where waveforms of three-phase grid voltages e_x $(x = a, b, c)$, grid currents i_x $(x = a, b, c)$, output current reference i_o^*, output current i_o are shown. Under the DCL-PIC strategy, the i_o has a current fluctuation of 1.2 A and returns to 10 A after 6 ms, as shown in Fig. 13(a). In contrast, i_o has a small fluctuation of 0.3 A and reaches the steady state in 2 ms under the DCL-BSC strategy, as shown in Fig. 13(b). The results of the comparison show that the proposed DCL-BSC strategy has better robustness than the DCL-PIC strategy against grid variations.

Case III: Parameter uncertainties

To verify the robustness of the proposed DCL-BSC scheme against parameter uncertainties, we choose controller parameters $L/2$ and $C/2$, and the actual converter parameters are the same as that in Table III. Fig. 14 shows the robust performance of the HFLMR against parameter uncertainties, where waveforms of three-phase grid current i_x $(x = a, b, c)$, a-phase voltage and current, output current reference i_o^*, output current i_o are shown. The THD of the input current is 2.54%. The a-phase current is in phase with a-phase voltage. The output current i_o tracks the reference i_o^* stably. As a result, the proposed BSC scheme still works well under the condition of parameter uncertainties.

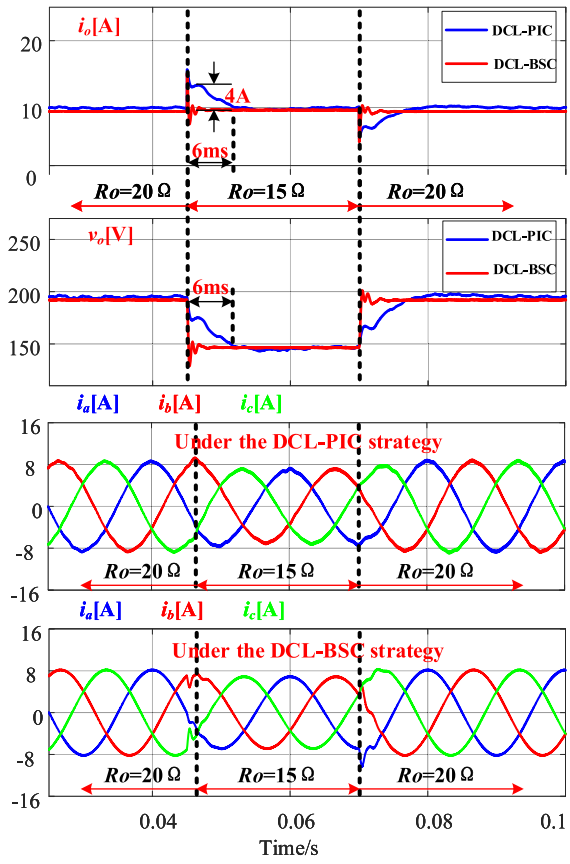


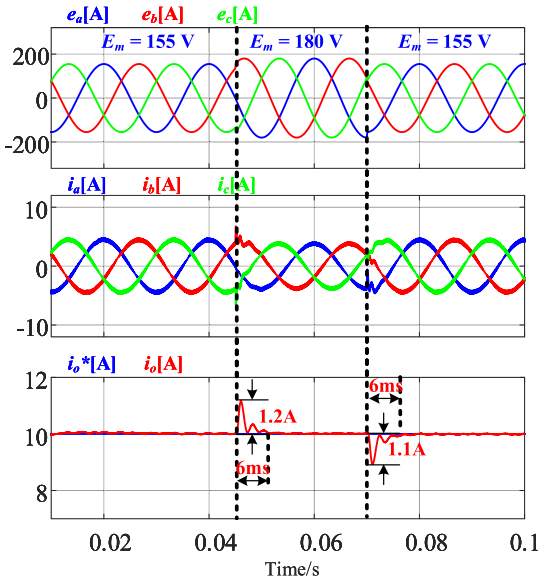
Fig. 12. Robust performance of output current i_o, output voltage v_o, and three-phase grid currents i_x $(x = a, b, c)$ against load variations under the DCL-PIC strategy and the DCL-BSC strategy.

According to the comparison of the abovementioned three cases, the proposed DCL-BSC strategy has better robustness than the DCL-PIC strategy against system disturbances.

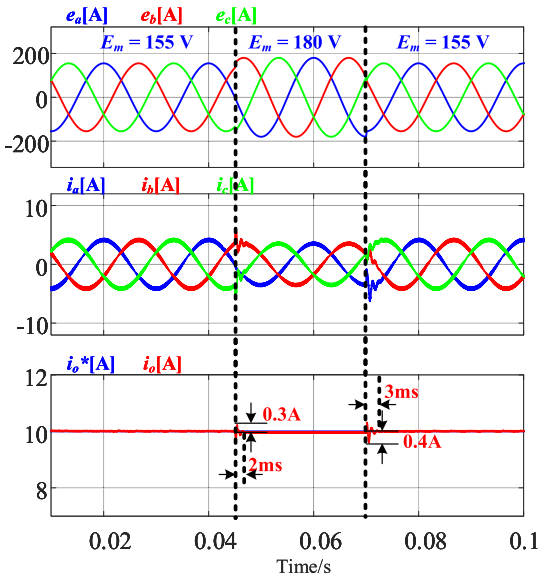
C. Simulation Results of PF Control Performance

To verify the effectiveness of the phase-compensation method, the output current reference is constant 10 A and the load is 20 Ω.

Fig. 15 shows simulation results of a-phase with the phase compensation method. The a-phase voltage e_a, a-phase current i_a, midpoint voltage of bridge A v_a, and high-frequency current of bridge A i_{at} are shown. Before 0.1 s, i_a is ahead of the e_a without the phase-compensation method due to the effects of input LC filters. Meanwhile, i_{at} is in phase with v_a because the voltage across the filter capacitor C is equal to the grid voltages. After 0.1 s, the i_a is in phase with e_a while the high-frequency current i_{at} is behind of the v_a due to the phase compensation. So the unity PF is realized with the phase-compensation method, which coincides with the analysis in Section III-B.



(a)



(b)

Fig. 13. Robust performance of three-phase grid currents i_x $(x = a, b, c)$ and output current i_o against grid variations under the DCL-PIC strategy and the DCL-BSC strategy.

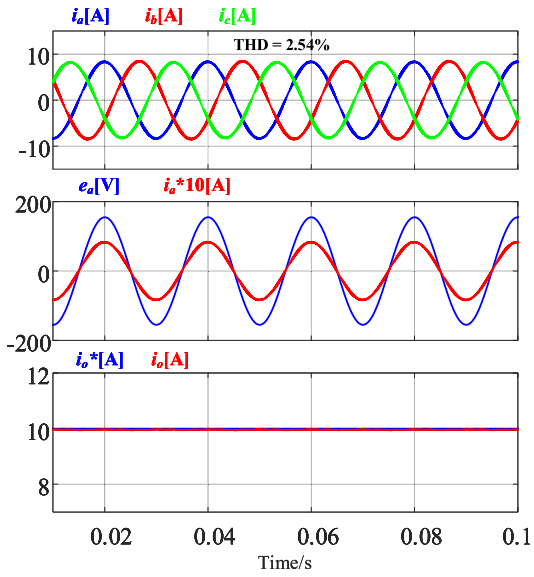


Fig. 14. Simulation results of three-phase currents i_x $(x = a, b, c)$, a-phase voltage/current (e_a, i_a), output current reference i_o^*, and output current i_o under the DCL-BSC strategy during parameter uncertainties.

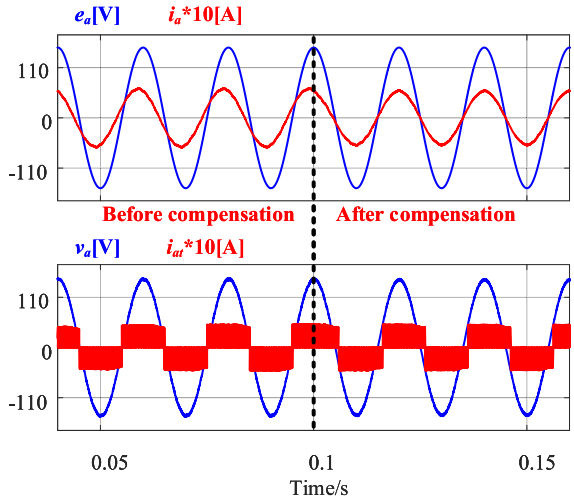


Fig. 15. Simulation results of PF control of a-phase.

V. Experimental Results

An experimental prototype system of an HFLMR has been set up with the power rating of 2 kW as shown in Fig. 16. The control scheme is implemented with the dSPACE 1007 digital control system. Parameters of experiments are identical with those of simulations, which are shown in Table III. For the proposed DCL-BSC control strategy, the inner-loop control gains are $K_2 = 15\,000$ and $K_3 = 1500$, the outer-loop control gain is $K_1 = 18\,000$, and the uncertainty bound estimation is $\eta = 20\,000$, which are the same as the simulations.

Fig. 17 shows the steady-state experimental results of HFLMR when the modulation ratio m is set to 0.8 with the six-segment SVPWM scheme [14]. The gate-to-source voltage $v_{\rm gs}$, drain-to-source voltage $v_{\rm ds}$ of MOSFET $S_{\rm anl}$, and primary voltage of transformer $v_{\rm pri}$ are shown. As shown in Fig. 17(a), the envelope curve of transformer primary voltage $v_{\rm pri}$, which has a six orders fluctuation is the same as the envelope curve of line-to-line grid voltage. It can be seen from Fig. 17(b), the switch $S_{\rm anl}$ turns ON and OFF without spikes. As a result, the six-segment SVPWM scheme realizes the great steady-state performance.

A. Experimental Results of Dynamic Performance

Four cases of output current references are set up to verify the dynamic tracking performance of the conventional DCL-PIC

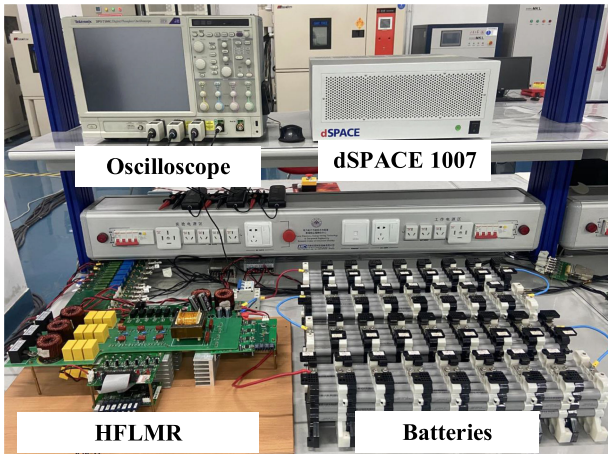


Fig. 16. Experimental prototype of HFLMR.

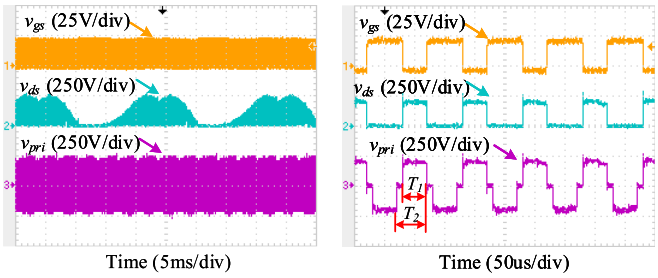


Fig. 17. Experimental waveforms under the six-segment SVPWM scheme. (a) In large time scale. (b) In small time scale.

and the proposed DCL-BSC strategy. In these four cases, the OCV of the LiNCM battery load are all 130 V. In case I, the dc output current reference value increases from 7.5 to 10 A. In case II, the dc output current reference value decreases from 10 to 7.5 A. In case III, the output current reference value is composed of a dc component and a sinusoidal component, which is $[7.5 + 2.5\sin(20\pi t)]$ A. In case IV, the output current reference value is $[7.5 + 2.5\sin(100\pi t)]$ A.

Case I: ($i_o^* = 7.5 \rightarrow 10$ A) and case II: ($i_o^* = 10 \rightarrow 7.5$ A)

Fig. 18 shows the dynamic performance of HFLMR in cases I and II, where the waveforms of dc output current reference i_o^*, output current i_o, output voltage v_o, and a-phase current i_a are shown.

Fig. 18(a) and (b) shows the dynamic performance in these two cases under the DCL-PIC strategy. The output current transient response rise time in case I is 20 ms and fall time in case II is 15 ms, respectively. Fig. 18(c) and (d) shows the dynamic performance in these two cases under the proposed DCL-BSC strategy. The output current has little overshoot and immediately reaches steady state. The output current transient response rise time in case I is 2 ms and fall time in case II is 1 ms, respectively.

Compared with the conventional DCL-PIC strategy, the rise time and fall time decrease by about 90% under the proposed DCL-BSC strategy. As a result, the proposed DCL-BSC strategy

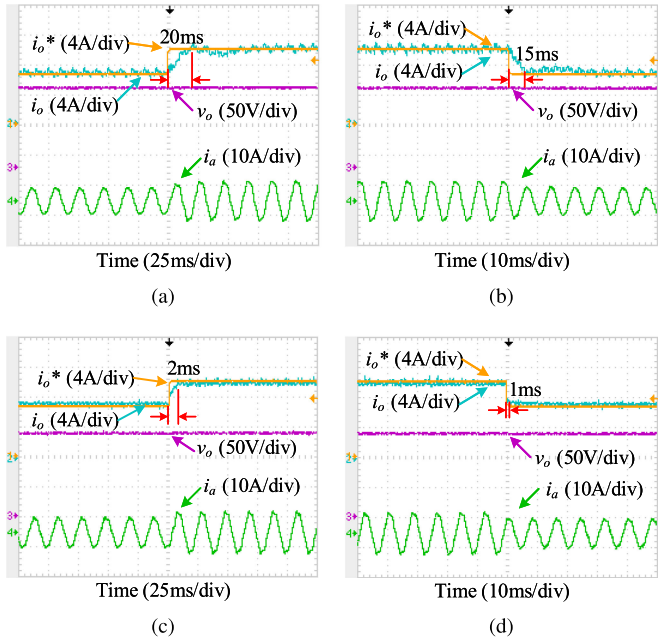


Fig. 18. Dynamic tracking performance of output current i_o. (a) Under the DCL-PIC strategy in case I. (b) Under the DCL-PIC strategy in case II. (c) Under the DCL-BSC strategy in case I. (d) Under the DCL-BSC strategy in case II.

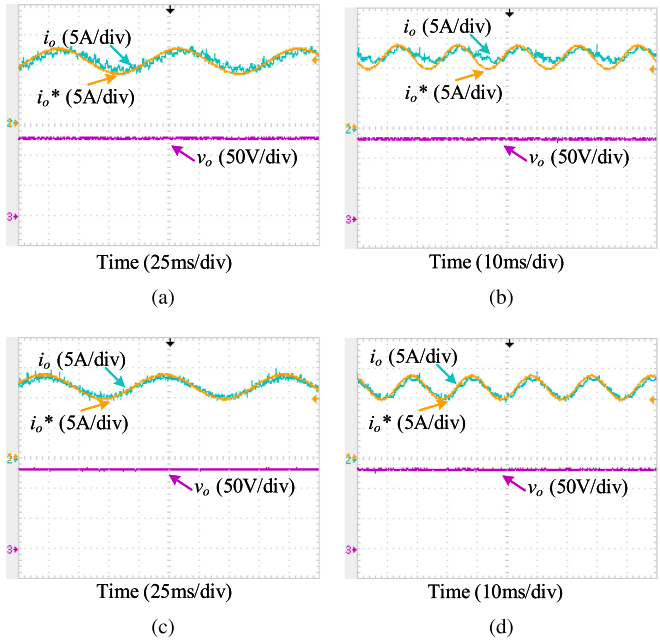


Fig. 19. Dynamic tracking performance of output current i_o. (a) Under the DCL-PIC strategy in case III. (b) Under the DCL-PIC strategy in case IV. (c) Under the DCL-BSC strategy in case III. (d) Under the DCL-BSC strategy in case IV.

achieves a better dynamic performance than the conventional DCL-PIC strategy when the output currents have mutations.

Case III: ($i_o^* = [7.5 + 2.5\sin(20\pi t)]$ A) and *Case IV:* ($i_o^* = [7.5 + 2.5\sin(100\pi t)]$ A)

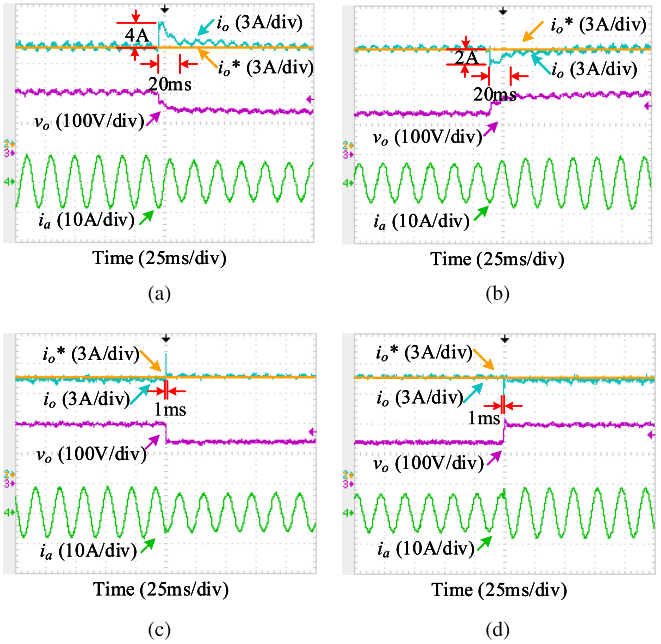


Fig. 20. Robust performance of output current i_o, output voltage v_o and a-phase current i_a. (a) Load decreases from 20 Ω to 15 Ω under the DCL-PIC strategy. (b) Load increases from 15 Ω to 20 Ω under the DCL-PIC strategy. (c) Load decreases from 20 Ω to 15 Ω under the DCL-BSC strategy. (d) Load increases from 15 Ω to 20 Ω under the DCL-BSC strategy.

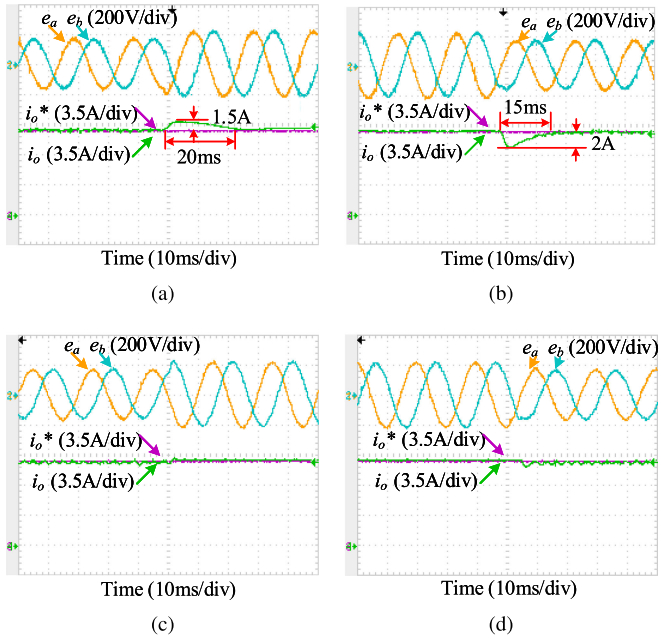


Fig. 21. Robust performance of two-phase voltages (e_a, e_b), output current reference i_o^*, and output current i_o. (a) Grid voltage increases from 155 to 180 V under the DCL-PIC strategy. (b) Grid voltage decreases from 180 to 155 V under the DCL-PIC strategy. (c) Grid voltage increases from 155 to 180 V under the DCL-BSC strategy. (d) Grid voltage decreases from 180 to 155 V under the DCL-BSC strategy.

Fig. 19 shows the dynamic performance of HFLMR in cases III and IV, where waveforms of dc output current reference i_o^*, output current i_o are shown.

Fig. 19(a) and (b) shows the dynamic performance in these two cases under the conventional DCL-PIC strategy. It can be seen that the amplitude of i_o is less than i_o^* and the phase of i_o lags behind i_o^* especially in case IV. Fig. 19(c) and (d) shows the dynamic performance in these two cases under the proposed DCL-BSC strategy. It can be seen that i_o can track i_o^* smoothly in these two cases.

Compared with the conventional DCL-PIC strategy, the proposed DCL-BSC strategy has a faster dynamic response rate. As a result, the proposed DCL-BSC strategy achieves a better dynamic performance than the conventional DCL-PIC strategy when the output currents have sinusoidal components.

B. Experimental Results of Robust Performance

In this part, the robust performance of the DCL-PIC and the proposed DCL-BSC strategy against the load, grid, and parameter variations are investigated. In case I, the resister load decreases from 20 Ω to 15 Ω and then returns to 20 Ω. In case II, the magnitude of phase voltage increases from 155 to 180 V and then returns to 155 V. In case III, the controller parameters are $L/2$ and $C/2$, and the actual converter parameters are the same as that in Table III. In these three cases, the output current reference is constant $i_o^* = 10$ A.

Case I: Load variations 20 Ω → 15 Ω and 15 Ω → 20 Ω

Fig. 20 shows the robust performance of HFLMR against load variations. The output current reference i_o^*, output current i_o, output voltage v_o, and a-phase current i_a are shown.

Fig. 20(a) and (b) shows the robust performance when load decreases and increases under the conventional DCL-PIC strategy. It can be seen that i_o has a current fluctuation of 4 A and returns to 10 A after 20 ms, and the v_o reaches steady state in 20 ms under the DCL-PIC strategy. Fig. 20(c) and (d) shows the robust performance when load decreases and increases under the proposed DCL-BSC strategy. It can be seen that i_o has little overshoot and reaches the steady state in 1 ms, and v_o reaches steady state in 1 ms under the proposed DCL-BSC strategy. In addition, the grid currents are sinusoidal without distortion during load variations under the DCL-PIC strategy and the DCL-BSC strategy, respectively. As a result, the proposed DCL-BSC strategy has a great robust performance than the conventional DCL-PIC strategy against load variations.

Case II: Grid variations 155 V → 180 V and 180 V → 155 V

Fig. 21 shows the robust performance of the HFLMR against grid variations. The waveforms of two-phase grid voltages (e_a, e_b), output current reference i_o^*, and output current i_o are shown.

Fig. 21(a) and (b) shows the robust performance when grid voltage increases and decreases under the conventional DCL-PIC strategy. It can be seen that i_o has a current fluctuation of 1.5 A and returns to 10 A after 20 ms when grid voltage increases, and i_o has a current fluctuation of 2 A and returns to 10 A after 15 ms when grid voltage decreases under the DCL-PIC strategy. In contrast, i_o has little overshoot and reaches the steady state in 1 ms under the proposed DCL-BSC strategy as shown

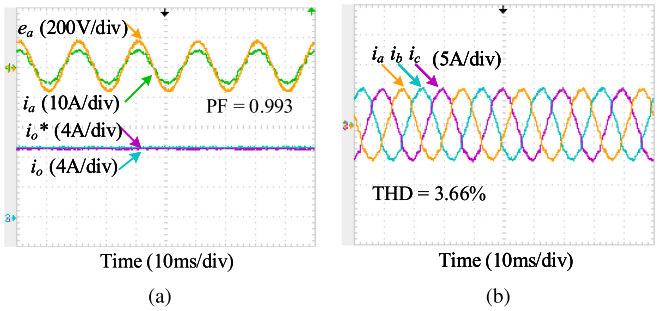


Fig. 22. Robust performance of the HFLMR under the proposed DCL-BSC strategy when the controller parameters are L/2 and C/2. (a) a-phase voltage e_a and current i_a, output current reference i_o^*, and output current i_o. (b) Three-phase current i_x $(x = a, b, c)$.

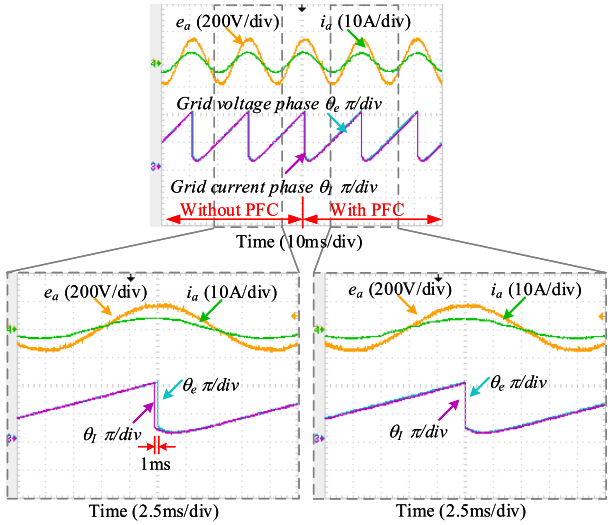


Fig. 23. Experimental results of PF control of a-phase.

in Fig. 21(c) and (d). The results of the comparison show that the proposed DCL-BSC strategy has better robustness than the DCL-PIC strategy against grid variations.

Case III: Parameter uncertainties

Fig. 22 shows the robust performance of the HFLMR under the proposed DCL-BSC strategy when the controller parameters are $L/2$ and $C/2$, and the actual converter parameters are the same as that in Table III. The waveforms of two-phase grid voltages (e_a, e_b), output current reference i_o^*, output current i_o are shown. The PF of a-phase is 0.993. The THD of the input current is 3.66%. The output current i_o tracks the reference i_o^* without steady-state error. As a result, the proposed BSC scheme still works well under the condition of parameter uncertainties.

According to the comparison of the abovementioned three cases, the proposed DCL-BSC strategy has better robustness than the DCL-PIC strategy against system disturbances.

C. Experimental Results of PF Control Performance

To verify the effectiveness of the phase-compensation method, the output current reference value is constant 10 A.

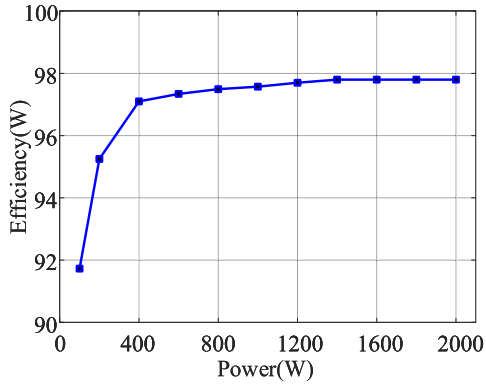


Fig. 24. Experimental efficiency of HFLMR.

Fig. 23 shows experimental results of a-phase with the phase-compensation method. The a-phase voltage e_a, a-phase current i_a, grid voltages phase θ_e, and grid currents phase θ_I are shown.

The i_a is ahead of the e_a and the θ_I is ahead of the θ_V 1 ms without the phase-compensation method because of the input LC filters. After compensation, the i_a is in phase with the e_a and the θ_I is in phase with the θ_V with the phase-compensation method. In conclusion, the unity PF is realized with the phase-compensation method.

The efficiency of the HFLMR has been measured by the WT1806E precision power analyzer. The measurements are conducted on the experimental prototype with a constant R-load ($R = 20\,\Omega$). The magnitude of phase voltage is constant 155 V, while the dc output current is changed. The efficiency curve is shown in Fig. 24. It can be seen that the efficiency increases with higher power, up to 97.8%.

VI. Conclusion

In this article, a dual closed-loop backstepping control (DCL-BSC) strategy is proposed for HFLMR to ensure the better steady state and dynamic performance, and robustness against system disturbances. The proposed strategy realizes superior characteristics of accurate current tracking performance in steady state and fast and nonovershoot response in transient state. Meanwhile, to realize accurate unity PF, this article proposes a compensation method based on the phase-shift angle. The simulation and experimental results confirm that the dynamic and robust performance of the proposed strategy is better than the conventional DCL-PIC strategy. Especially, the proposed strategy is simple in structure and requires no additional hardware, so it can be easily implemented in engineering. This scheme has great potential to be applied to EV charger, battery test system, active power filter.

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