Accurate and Stable Hardware-in-the-Loop (HIL) Real-Time Simulation of Integrated Power Electronics and Power Systems

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***Abstract*—Power hardware-in-the-loop (PHIL) technology allows for the testing of physical equipment in a real-time simulation environment. An important role is attributed to the power interface (PI). This PI connects a power system model, which is implemented on a digital computer, to physical hardware under test, such as a power electronic converter. Several hardware-in-the-loop (HIL) test setups with distinct PIs are proposed and compared. Based on detailed modeling of the different interfaces, system analysis is performed for each HIL test setup with respect to overall stability and accuracy. To verify stability for PHIL simulation systems, transfer function representations of the entire PHIL simulation processes are developed, and all involved time delays are quantified. The Nyquist stability criterion is applied to analyze all considered interfacing methods to enhance PHIL simulation stability, and the accuracy is evaluated. Moreover, experimental test results are given to demonstrate both the applicability and the functioning of the proposed interfacing methods. A particular focus is laid on the interfacing of physical power electronic inverters tested as part of a network in a PHIL real-time simulation.**

***Index Terms*—Digital real-time simulation, electrical power system, power electronic converter, power hardware-in-the-loop (PHIL), power interface (PI), simulation, system theory.**

NOMENCLATURE

Principle Variables

f	Frequency
I	Electric current
i	Iteration counter
L	Inductance
N	Number of partitioned subsystems
t	Time
U	Electric voltage
Z	Impedance
ε	Relative error
τ	Duration
τ_{S}	Time step size of subsystem
ω	Angular frequency

Functions

F_{O}	Open-loop transfer function
T	Transfer function

Operators

j	Imaginary unit
s	Operator variable in Laplace domain

Subscript Indicators

A	Analog
C	Current measurement
D	Digital
d	Delay
di	Delay at input
do	Delay at output
eq	Equivalent
FB	Feedback
FW	Feedforward
id	Ideal
HS	Hardware-to-software
LL	Line-to-line
L1, L2, L3	Phase 1, 2, and 3
MIN	Minimum
MRP	Multi-rate partitioning
nom	Nominal
rated	Rated
S	Source
SH	Software-to-hardware
SR	Single-rate
sh	Shifting
SYS	System
VA	Voltage-type amplification
VI	Virtual interface
Z	Impedance
Z1	Impedance on software side
Z11	Impedance of software subsystem S_{11}
Z12	Impedance of software subsystem S_{12}
Z2	Impedance on hardware side

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I. INTRODUCTION

THE STRUCTURE and architecture of electric power systems has changed significantly in recent years. The

increase in the number of power electronic inverters as key components of modern generation units implies challenges as well as opportunities at all voltage levels [1]. The increasing system complexity asks for accurate and efficient simulation techniques for the analysis of electric power systems [2]–[4]. In this context, real-time simulation and in particular power hardware-in-the-loop (PHIL) simulation have already been applied for the validation and testing of system behavior, closely emulating the behavior of power electric and electronic systems [5]–[14].

In this article, a set of novel power interface (PI) techniques for the stabilization of PHIL simulation systems is introduced, implemented, and validated. All methods presented are augmentation methods for PHIL simulation, which may be applied independently or jointly with existing common interface algorithms [5], [15]. In comparison with other existing stabilization methods [15], [16], the proposed techniques show enhancements related to the achievable overall bandwidth. The latter translates into an increased accuracy and better system stability when evaluating power hardware in electric networks during fast transients.

Following this introduction, a thorough background on PHIL simulation with a basic interface is given in Section II. In Section III, existing methods to stabilize PHIL systems referred to as the hardware inductance addition (HIA) method, the feedback current filtering (FCF), and the multi-rate partitioning (MRP) method are presented. The partial shifting impedance (PSI) represents a novel method to stabilize PHIL systems. In Section IV, analytical approaches are given for the determination of stability and accuracy. In Section V, two selected methods are validated in a laboratory experiment, where a physical power electronic inverter is connected to a low-voltage distribution grid in a PHIL setup. Finally, Section VI concludes this article.

II. System Analysis of PHIL Simulation With Single-Rate (SR) Interfaces

The PHIL simulation process involves two main constraints. First, the real-time constraint is to be met. Thus, the duration needed to perform all computations of a single time step must never exceed the time step size τ_{S}. Second, the simulation process is to be stable. Even if stable numerical integration methods are applied, the involved feedback loop may compromise stability. For the purpose of analyzing the latter, the entire digital PHIL simulation system may be modeled by means of a continuous-time system equivalent, making use of transfer functions in the Laplace domain. In particular, all involved time delays and phase shifts as well as modifications of the amplitude are to be captured accurately. Details on this approach, resulting in models and block diagrams for interfaces, software systems, and hardware systems are given in [17]. System stability can then be determined by evaluating the open-loop transfer function $F_{\mathrm{O}}(s)$ according to the Nyquist stability criterion.

In addition to stability, the accuracy of PHIL simulation systems is relevant. Transfer function analysis also serves as a useful starting point for accuracy analysis. As an example, the model and the block diagram of transfer functions for a SR PHIL system are given in Fig. 1. As opposed to the multi-rate case, a

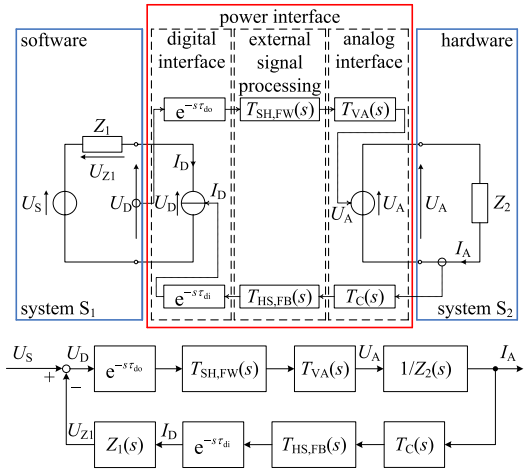

Fig. 1. Model and block diagram for analysis of PHIL simulation with SR transformer model PI.

PHIL simulation with SR interface only involves a single time step size. Fig. 1 shows the transformer model PI of voltage type. In what follows, the relative error of the voltage U_{A} of system S_2 for PHIL simulation system with SR interface is determined. The voltage U_{A} is calculated as

$$U_{\mathrm{A}}(s) = T_{\mathrm{SYS,A}}(s) U_{\mathrm{S}}(s) \tag{1}$$

where U_{S} is the source voltage of system S_1, and $T_{\mathrm{SYS,A}}(s)$ is the corresponding system transfer function of the PHIL system. The system transfer function is defined by

$$T_{\mathrm{SYS,A}}(s) = \frac{T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}}}{1 + F_{\mathrm{O}}(s)} \tag{2}$$

obtained by combining the following equations

$$U_{\mathrm{A}}(s) = T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}} U_{\mathrm{D}}(s) \tag{3}$$

$$U_{\mathrm{D}}(s) = U_{\mathrm{S}}(s) - U_{\mathrm{Z1}}(s) \tag{4}$$

$$U_{\mathrm{Z1}}(s) = U_{\mathrm{D}}(s) F_{\mathrm{O}}(s) \tag{5}$$

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) T_{\mathrm{C}}(s) T_{\mathrm{HS,FB}}(s) Z_1(s) \mathrm{e}^{-s\tau_{\mathrm{d}}}}{Z_2(s)} \tag{6}$$

with definitions as shown in [17]

$$\tau_{\mathrm{d}} = \tau_{\mathrm{do}} + \tau_{\mathrm{di}} \tag{7}$$

$$\tau_{\mathrm{do}} = \tau_{\mathrm{S}} \tag{8}$$

$$\tau_{\mathrm{di}} = \tau_{\mathrm{S}}. \tag{9}$$

In the above equations, $T_{\mathrm{SH,FW}}(s)$ and $T_{\mathrm{HS,FB}}(s)$ are transfer functions describing the external signal processing stages in the forward and in the feedback path, respectively, $T_{\mathrm{VA}}(s)$ is the transfer function of the power amplification unit in voltage-type mode, $T_{\mathrm{C}}(s)$ is the transfer function of the current measurement, τ_{d} is the overall delay, τ_{do} is the output delay, τ_{di} is the input delay, and τ_{S} is the time step size.

A special case is the ideal PI. An ideal PI for PHIL simulation has delay-free signal transfer, unity gain, zero time delay, and infinite bandwidth, therefore, the transfer functions $T_{\mathrm{SH,FW}}(s)$,

$T_{\mathrm{VA}}(s)$, $T_{\mathrm{C}}(s)$, and $T_{\mathrm{HS,FB}}(s)$ satisfying the following:

$$T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)\mathrm{e}^{-s\tau_{\mathrm{d}}} = 1. \tag{10}$$

Under this assumption, the interface of Fig. 1 becomes an ideal transformer model. The system transfer function $T_{\mathrm{SYS,A,id}}(s)$ for the PHIL system with such a notional ideal PI is given by

$$T_{\mathrm{SYS,A,id}}(s) = \frac{Z_2(s)}{Z_1(s) + Z_2(s)}. \tag{11}$$

The relative difference between the system transfer functions obtained by the PHIL simulation and the system transfer functions of the ideal system can be calculated as the corresponding relative error $\varepsilon_{\mathrm{SYS,A}}(s)$ of the voltage U_{A}:

$$\varepsilon_{\mathrm{SYS,A}}(s) = |T_{\mathrm{SYS,A}}(s) - T_{\mathrm{SYS,A,id}}(s)|/|T_{\mathrm{SYS,A,id}}(s)|. \tag{12}$$

Based on the definition of the Laplace transform and for reasons of convergence [18], the complex Laplace variable $s = \sigma + \mathrm{j}\omega$ must include $\sigma = 0$ to allow for the transition from $\varepsilon_{\mathrm{SYS,A}}(s)$ to the frequency response $\varepsilon_{\mathrm{SYS,A}}(\mathrm{j}\omega)$. Alternatively, the determination of the absolute error between respective PHIL simulation systems and the ideal system may be used for accuracy analysis.

III. Methods to Enhance PHIL Simulation Stability

In this section, methods to achieve stability of PHIL simulation systems with voltage type PIs are presented. Similar to the work in [15], open-loop transfer functions of the closed-loop PHIL system are derived for the determination of stability according to the Nyquist stability criterion. As a review of the state of the art in PHIL simulation, the well-known HIA method and the FCF method are discussed in Sections III-A and III-B. The novel PSI method is introduced in Section III-C, representing an innovative and effective SR interface to enhance stability. For the purpose of allowing a quantitative comparison, the MRP interfacing method is also included in Section III-D.

A. HIA Method

As an introduction representing the state of the art, the HIA method is reviewed as a basic technique to improve the stability of PHIL simulation. Hereby, an inductance L_2 is added as a hardware part and connected in series with the hardware impedance $Z_2(s)$. The principle architecture and the corresponding model are given in [5]. Referring to the model of PHIL simulation with SR interface shown in Fig. 1, the open-loop transfer function results in

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)Z_1(s)\mathrm{e}^{-s\tau_{\mathrm{d}}}}{sL_2 + Z_2(s)}. \tag{13}$$

Details on the derivation of the open-loop transfer function as well as the system transfer function of PHIL simulation with SR HIA method are given in Appendix A.

B. FCF Method

The FCF method introduces one or multiple filter blocks described by the generalized transfer function $T_{\mathrm{F,FB}}(s)$ in series to the external signal processing in the feedback signal path given by $T_{\mathrm{HS,FB}}(s)$ in Fig. 1. Filter blocks are implemented in software for reasons of flexibility regarding variation of topology, order, magnitude, and phase. The stabilization effect is largely obtained by a reduction of the overall bandwidth by the operation of the filter.

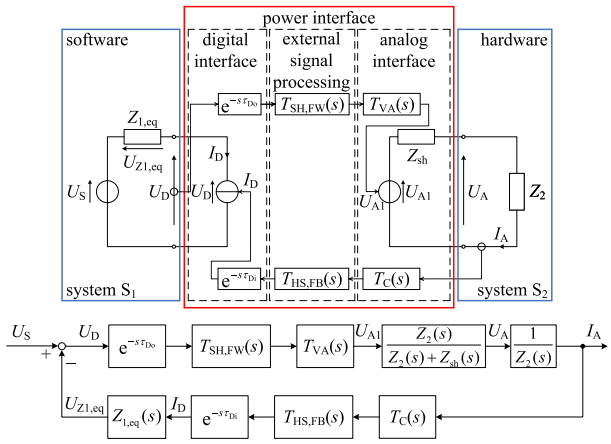

Fig. 2. Model and block diagram for analysis of PHIL simulation with SR PSI PI.

For the purpose of system modeling, the transfer function of the external signal processing block $T_{\mathrm{HS,FB}}(s)$, depicted in Fig. 1, is multiplied by the transfer function of the filter block $T_{\mathrm{F,FB}}(s)$. Thus, the corresponding open-loop transfer function of the closed-loop system of a PHIL simulation with SR FCF method and voltage-type PI becomes

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{F,FB}}(s)T_{\mathrm{HS,FB}}(s)Z_1(s)\mathrm{e}^{-s\tau_{\mathrm{d}}}}{Z_2(s)}. \tag{14}$$

The open-loop transfer function as well as the system transfer function of PHIL simulation with the SR FCF method are derived in Appendix B. Different types such as low-pass, Butterworth, or Chebyshev filters are suitable for application with the FCF methodology. Corresponding transfer functions are given in [19] and [20]. Based on this concept, signal filters may also be implemented and applied to the feedforward signal path. Hereby, the filters would be connected in series to the external signal processing in the feedforward signal path given by $T_{\mathrm{SH,FW}}(s)$ in Fig. 1.

C. PSI Method

The PSI method is characterized by the idea to, respectively, modify the impedances on the hardware and software sides in order to obtain stability for PHIL simulation. System stability is attained by means of shifting and variation of system impedances.

Fig. 2 shows the model of PHIL simulation with SR interface for the PSI methodology with introduced shifting impedance $Z_{\mathrm{sh}}(s)$. The shifting impedance $Z_{\mathrm{sh}}(s)$ and the existing hardware impedance $Z_2(s)$ are connected in series. Compared with the original PHIL system of Fig. 1, this results in a new equivalent

hardware impedance $Z_{2,\mathrm{eq}}(s)$ as

$$Z_{2,\mathrm{eq}}(s) = Z_2(s) + Z_{\mathrm{sh}}(s). \tag{15}$$

To compensate the effect of the hardware side, the equivalent system impedance of S_1 representing the equivalent software impedance $Z_{1,\mathrm{eq}}(s)$ is formulated as

$$Z_{1,\mathrm{eq}}(s) = Z_1(s) - Z_{\mathrm{sh}}(s). \tag{16}$$

The introduction of the shifting impedance $Z_{\mathrm{sh}}(s)$ results in a modification of $Z_1(s)$ and $Z_2(s)$ to $Z_{1,\mathrm{eq}}(s)$ and $Z_{2,\mathrm{eq}}(s)$, respectively. Taking into account the PI as shown in Fig. 2, $U_{\mathrm{A}}(s)$ and $U_{\mathrm{D}}(s)$ are now related as follows:

$$U_{\mathrm{A}}(s) = T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)\mathrm{e}^{-s\tau_{\mathrm{do}}}\frac{Z_2(s)}{Z_2(s)+Z_{\mathrm{sh}}(s)}U_{\mathrm{D}}(s). \tag{17}$$

Shown in the lower part of Fig. 2 is the block diagram representation in the form of a single-input-single-output (SISO) closed-loop PHIL simulation system. The corresponding open-loop transfer function of the closed-loop system defined by

$$F_{\mathrm{O}}(s) = \frac{U_{Z1,\mathrm{eq}}(s)}{U_{\mathrm{D}}(s)} \tag{18}$$

becomes

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)Z_{1,\mathrm{eq}}(s)\mathrm{e}^{-s\tau_{\mathrm{d}}}}{Z_{2,\mathrm{eq}}(s)}. \tag{19}$$

With (15) and (16), the open-loop transfer function of the closed-loop PHIL simulation system with SR PSI methodology and voltage type PI becomes

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)(Z_1(s)-Z_{\mathrm{sh}}(s))\mathrm{e}^{-s\tau_{\mathrm{d}}}}{Z_2(s)+Z_{\mathrm{sh}}(s)}. \tag{20}$$

Using

$$U_{\mathrm{D}}(s) = U_{\mathrm{S}}(s) - U_{Z1,\mathrm{eq}}(s) \tag{21}$$

and relations in (1), (17), (18), the system transfer function $T_{\mathrm{SYS,A}}(s)$ for PHIL simulation systems with SR PSI interface method becomes

$$T_{\mathrm{SYS,A}}(s) = \frac{Z_2(s)}{Z_{\mathrm{sh}}(s)+Z_2(s)}\frac{T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)\mathrm{e}^{-s\tau_{\mathrm{do}}}}{1+F_{\mathrm{O}}(s)}. \tag{22}$$

The important advantage of this technique consists in the transformation of the system impedance ratio to a certain value such as to guarantee system stability according to the Nyquist stability criterion.

A minimum value of the shifting impedance $Z_{\mathrm{sh,MIN}}$ may be calculated in order to obtain overall stability for PHIL simulation with the PSI method. The PSI method is well compatible with the FCF method of Section III-B. In Fig. 2, the joint application may be modeled by integrating the transfer function $T_{\mathrm{F,FB}}(s)$ contributed by the FCF with the block $T_{\mathrm{HS,FB}}(s)$.

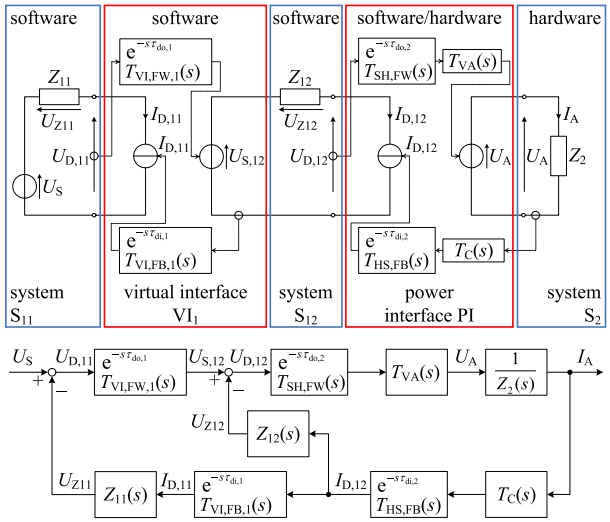

Fig. 3. Model and block diagram for analysis of PHIL simulation with MRP interface.

D. MRP Method

In the MRP method, the original simulation system is decomposed into multiple subsystems using different time step sizes for different subsystems [17]. For the subsystem next to the PI, it is the aim to achieve a comparatively small time step size to boost stability. The creation of different partitions generates software subsystems S_{11}, S_{12}, …, S_{1N}, which are represented by system impedances $Z_{11}(s)$, $Z_{12}(s)$, …, $Z_{1N}(s)$, respectively. Subsystems with differing time step sizes are linked through a virtual interface (VI). Internal signal processing stages in the VI are described by transfer functions $T_{\mathrm{VI,FW},i}(s)$ for the forward signal and by $T_{\mathrm{VI,FB},i}(s)$ for the feedback signal. Hardware system S_2 is linked with software subsystem S_{1N} through the PI. The total number of partitioned subsystems N depends on the size of the simulated network and the given possibility to create partitions from an engineering and system theoretic point of view. In general, the higher the necessity on increased system bandwidth is, the smaller the time step sizes of the partitioned subsystems must be in order to track transients.

Fig. 3 shows the model and block diagram of an MRP interface of the order $N = 2$ with two partitioned subsystems and corresponding impedances $Z_{11}(s)$ and $Z_{12}(s)$. The system impedances for PHIL simulation with MRP interface are partitioned as

$$Z_1(s) = Z_{11}(s) + Z_{12}(s). \tag{23}$$

The open-loop transfer function of the closed-loop system is defined by

$$F_{\mathrm{O}}(s) = \frac{U_{\mathrm{Z11}}(s)}{U_{\mathrm{D},11}(s)} \tag{24}$$

and is derived according to analysis in Appendix C as (25) shown at the bottom of the next page. Equation (1) relates the voltages U_{A} and U_{S} and defines the system transfer function $T_{\mathrm{SYS,A}}(s)$ for the SR interface. For the multi-rate case, (1) is still applicable for the voltages U_{A} and U_{S}. According to the model and the

block diagram in Fig. 3, the calculation of the system transfer function starts by combining

$$U_{\mathrm{A}}(s) = T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)\mathrm{e}^{-s\tau_{\mathrm{do},2}}U_{\mathrm{D},12}(s) \tag{26}$$

with

$$U_{\mathrm{D},12}(s) = U_{\mathrm{S},12}(s) - U_{\mathrm{Z}12}(s) \tag{27}$$

$$U_{\mathrm{S},12}(s) = T_{\mathrm{VI,FW},1}(s)\mathrm{e}^{-s\tau_{\mathrm{do},1}}U_{\mathrm{D},11}(s) \tag{28}$$

$$U_{\mathrm{Z}12}(s) = Z_{12}(s)I_{\mathrm{D},12}(s) \tag{29}$$

$$I_{\mathrm{D},12}(s) = T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)\mathrm{e}^{-s\tau_{\mathrm{di},2}}I_{\mathrm{A}}(s) \tag{30}$$

$$I_{\mathrm{A}}(s) = \frac{U_{\mathrm{A}}(s)}{Z_2(s)}. \tag{31}$$

Substituting (27) to (31) in (26) and extracting the voltages U_{A} and $U_{\mathrm{D},11}$ results in

$$U_{\mathrm{A}}(s) = T_{\mathrm{SYS,FW}}(s)U_{\mathrm{D},11}(s) \tag{32}$$

with

$$T_{\mathrm{SYS,FW}}(s) = \frac{T_{\mathrm{VI,FW},1}(s)T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)Z_2(s)T_{\mathrm{d,FW}}(s)}{Z_2(s) + T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)Z_{12}(s)T_{\mathrm{d},2}(s)} \tag{33}$$

and definitions

$$T_{\mathrm{d,FW}}(s) = \mathrm{e}^{-s\tau_{\mathrm{d,FW}}} \tag{34}$$

$$\tau_{\mathrm{d,FW}} = \tau_{\mathrm{do},1} + \tau_{\mathrm{do},2}. \tag{35}$$

Here, $T_{\mathrm{SYS,FW}}(s)$ is the forward system transfer function of the PHIL system with MRP interface, $T_{\mathrm{d,FW}}(s)$ is the transfer function of the discretization time delay due to the VI connecting S_{11} and S_{12} and the PI connecting S_{12} and S_2.

Using

$$U_{\mathrm{D},11}(s) = U_{\mathrm{S}}(s) - U_{\mathrm{Z}11}(s) \tag{36}$$

and relations in (1), (24), (32), the system transfer function $T_{\mathrm{SYS,A}}(s)$ for PHIL simulation systems with MRP interface method becomes

$$T_{\mathrm{SYS,A}}(s) = \frac{T_{\mathrm{SYS,FW}}(s)}{1 + F_{\mathrm{O}}(s)}. \tag{37}$$

The corresponding system transfer function $T_{\mathrm{SYS,A,id}}(s)$ for the MRP method with ideal PI and the resulting relative error $\varepsilon_{\mathrm{SYS,A}}(s)$ can be calculated as given in (11) and (12) in Section II. The MRP method is well compatible with the FCF method. A joint application may be accomplished by applying the additional filtering in the feedback path, as also considered for the PSI method in Section III-C.

The introduction of the system transfer function for the MRP method is necessary to enable a comprehensive, comparative analysis of PHIL system accuracy. While in [17] open-loop transfer functions for system stability analysis were developed, here the theoretical foundation of this framework is extended by a set of system transfer functions allowing for accuracy analysis. Based on this concept, system stability and accuracy of PHIL simulation with SR and MRP interfaces can be assessed in a consistent way.

In general, all methods to enhance stability of PHIL simulation systems introduced in Sections III-A–D have their own specific characteristics and can be dealt with independently in terms of implementation. However, several of these methods may be used jointly and simultaneously if their combination is applicable and feasible for given PHIL simulation systems. As an example, and as also done in Sections IV and V because of its practical relevance for experimental PHIL test setups, the FCF method may be applied in combination with the HIA method, the PSI method, or the MRP method.

IV. Analytical Comparison of Accuracy of Interfaces for PHIL Simulation System

In this section, PHIL simulation setups are analyzed for the purpose of accuracy evaluation. Following the introduction of the methodology applied, the modeling of the PHIL setups is explained. Finally, results pertaining to the accuracy of the four PHIL simulation setups are discussed and analyzed.

A. Methodology

The following discussions serve to explain the comparative analysis of the techniques to enhance PHIL simulation stability, as given in Sections III-A–D. The quality of the PHIL simulation setups is evaluated based on transfer function models of the setups. In the following, the principle steps of the methodology are introduced.

The first stage of the methodology is dedicated to the modeling of the PHIL simulation setups of interest. For each PHIL simulation setup, the model covers the software side, the PI, and the hardware side. Four different PHIL setups to enhance stability are considered: the SR interfaces HIA, FCF, and PSI, as well as the multi-rate interface MRP. For the SR interfaces, all share the same software and hardware sides. They just differ in terms of PI design. The MRP also has the same hardware side, but the network on the software side is decomposed into two subsystems as explained in Section III-D. This approach of referring to the same hardware sides and identical networks on the software side lays the basis for starting a comparison with regard to the quality of the PIs.

The quality of a PI refers to its impact on stability and accuracy. Here, for the purpose of comparison, all PIs are adjusted by applying appropriate filters for $T_{\mathrm{HS,FB}}(s)$ as explained in Section III.B to limit the system bandwidth and to yield the same stability margin given by the Nyquist criterion. With the same stability margin given, the accuracy of the results can be compared. The simulation considered here is challenging because without the application of a method to enhance PHIL

$$F_{\mathrm{O}}(s) = \frac{T_{\mathrm{VI,FW},1}(s)T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)T_{\mathrm{VI,FB},1}(s)Z_{11}(s)T_{\mathrm{d}}(s)}{Z_2(s) + T_{\mathrm{SH,FW}}(s)T_{\mathrm{VA}}(s)T_{\mathrm{C}}(s)T_{\mathrm{HS,FB}}(s)Z_{12}(s)T_{\mathrm{d},2}(s)} \tag{25}$$

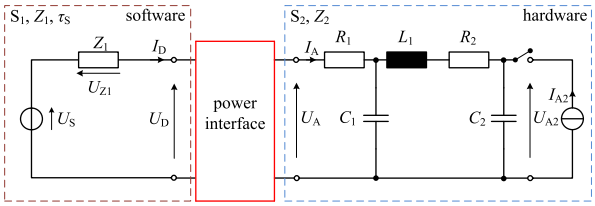

Fig. 4. Circuits on software and hardware sides for model-based analysis of PHIL simulation system with SR interface.

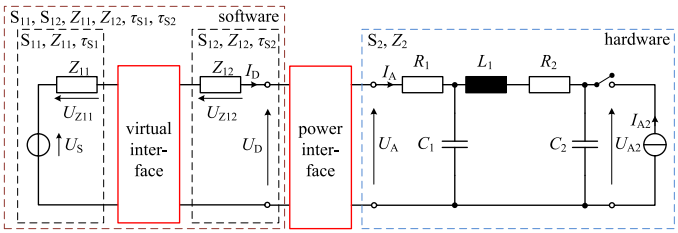

Fig. 5. Circuits on software and hardware sides for model-based analysis of PHIL simulation system with MRP interface.

simulation stability as part of the PI, stability would not be given. A setup with the notional ideal PI of Section II is modeled to serve as the reference. At the end of the modeling stage, transfer function models of all PHIL simulation setups are available.

In the second stage, a frequency response analysis is performed. The results are compared in terms of the accuracy obtained, the setup with the notional ideal PI is used as reference.

B. Modeling

Fig. 4 and Fig. 5 show the circuits on software and hardware sides for the model-based analysis of a PHIL simulation setup with respective SR and MRP interfaces. A grid-connected inverter is linked to a cable in a single-phase distribution network. System S_1 consists of a distribution network voltage source U_S and a distribution cable [21], [22] with a cable length of 1.2 km represented by its impedance $Z_1(s)$:

$$Z_1(s) = 0.7392\ \Omega + s0.002246\ \Omega\text{s}. \tag{38}$$

System S_2 represents a distributed generation unit as shown in Fig. 4 [23]. It consists of a grid-connected inverter model with current source I_{A2} and an output filter. The values of resistive, inductive, and capacitive output filter components are given as follows: $R_1 = 0.1\ \Omega$, $R_2 = 2.54\ \Omega$, $L_1 = 12$ mH, $C_1 = 1\ \mu$F, and $C_2 = 2.2\ \mu$F. Systems S_1 and S_2 are linked through the corresponding PI. Key components of the PI are modeled by the transfer function of the power amplification unit $T_{VA}(s)$ as well as the transfer function of the current sensor $T_C(s)$ [17]:

$$T_{VA}(s) = \frac{1}{s^2 2.9 \cdot 10^{-7}\mu\text{s}^2 + s\,0.8\,\mu\text{s} + 1} e^{-s4.2\mu\text{s}} \tag{39}$$

$$T_C(s) = \frac{1}{s\,0.8\,\mu\text{s} + 1}. \tag{40}$$

First, the HIA method of Section III-A at a time step τ_S of 12.5 µs is applied, resulting in a delay time τ_d of 25 µs according to [17], and the inductance $L_2 = 1.0$ mH is introduced to S_2. For the HIA method, as given in Section III.A, a first-order unity gain Butterworth filter with a corner frequency $f_{C,SR}$ of 3.05 kHz is applied for $T_{HS,FB}(s)$ in (13), as indicated in Table I, respectively. Second, the FCF method is applied, as given in Section III-B. The following transfer function for stabilization filters $T_{F,FB}(s)$ is applied in (14): a third-order unity gain Butterworth filter with a corner frequency of $f_{C,SR}$ of 5.7 kHz is used for the SR interface at a time step τ_S of 12.5 µs; for comparison, the SR interface is also implemented at a time step of 1 µs and with a third-order unity gain Butterworth filter whose corner frequency $f_{C,SR}$ is 7.8 kHz. Third, the PSI method of Section III-C at a time step τ_S of 12.5 µs is applied. The introduced shifting impedance $Z_{sh}(s)$ in Fig. 2 amounts to $Z_{sh}(s) = 0.037\ \Omega + s0.000107\ \Omega$s. For the PSI method, as given in Section III.C, a third-order unity gain Butterworth filter with a corner frequency $f_{C,SR}$ of 3.9 kHz is applied for $T_{HS,FB}(s)$ in (20).

TABLE I
PHIL SIMULATION PARAMETRIZATION FOR SR AND MULTI-RATE PARTITIONING (MRP) INTERFACES

setup	$\tau_S;\tau_d$	$\tau_{S1};\tau_{d1}$	$\tau_{S2};\tau_{d2}$	$f_{C,SR}$	$f_{C,MRP}$	L_2	Z_{sh}
unit	(µs; µs)	(µs; µs)	(µs; µs)	(kHz)	(kHz)	(mH)	(Ω)
HIA	12.5; 25	-;-	-;-	3.05	-	1.0	-
FCF (slow)	12.5; 25	-;-	-;-	5.7	-	-	-
FCF (fast)	1; 2	-;-	-;-	7.8	-	-	-
PSI	12.5; 25	-;-	-;-	3.9	-	-	0.037+s0.000107s
MRP	-;-	12.5; 25	1; 2	-	6.45	-	-

Finally, the MRP interface in Fig. 3 of Section III-D is applied. Regarding MRP, the system impedance $Z_1(s)$ of system S_1 is partitioned into $Z_{11}(s)$, which belongs to system S_{11} at a time step τ_{S1} of 12.5 µs, and $Z_{12}(s)$, which belongs to system S_{12} at a time step τ_{S2} of 1 µs. As shown in [17], corresponding delay times for S_{11} and S_{12} are given by τ_{d1} and τ_{d2} in Table I, respectively. In analogy to the determination of $Z_1(s)$, (38) is used for the calculation of the system impedances $Z_{11}(s)$ and $Z_{12}(s)$. For PHIL simulation with MRP interface, the cable lengths are set to 1.0 and 0.2 km, respectively. For the MRP method, as given in Section III-D, a third-order unity gain Butterworth filter with a corner frequency $f_{C,MRP}$ of 6.45 kHz is applied for $T_{HS,FB}(s)$ in (25), and $T_{VI,FB,1}(s)$ is equal to 1.

For all applied methods, the transfer functions of filters $T_{SH,FW}(s)$ and $T_{VI,FW,i}(s)$ in the feedforward signal paths are set equal to 1, respectively. Table I summarizes the simulation parametrizations for different PHIL systems in accordance with models defined in Sections II and III.

Upon completion of the settings made above, the open-loop transfer function of the PHIL simulation setups all show the same stability margin. The minimum distance of the Nyquist plot to the Nyquist point (–1,0) is set to 0.08. To formally distinguish the open-loop transfer functions $F_O(s)$, the subscripts HIA, FCF, PSI, and MRP are introduced: $F_{O,HIA}(s)$, $F_{O,FCF}(s)$, $F_{O,PSI}(s)$, and $F_{O,MRP}(s)$.

In order to perform the accuracy evaluations, the transfer functions according to (1) are determined. For models of PHIL simulation setups with SR interfaces, this is done in Appendices A and B as well as in Section III-C leading to (22). For the PHIL setup with MRP interface, (37) of Section III-D is adopted.

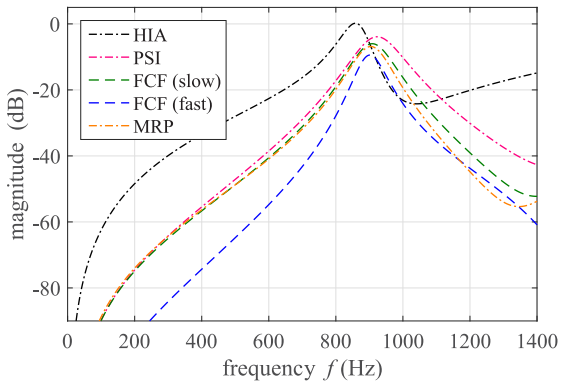

Fig. 6. Relative error of voltage U_{A} of the simulated PHIL setup with varying interfaces and different methods for PHIL system stability applied.

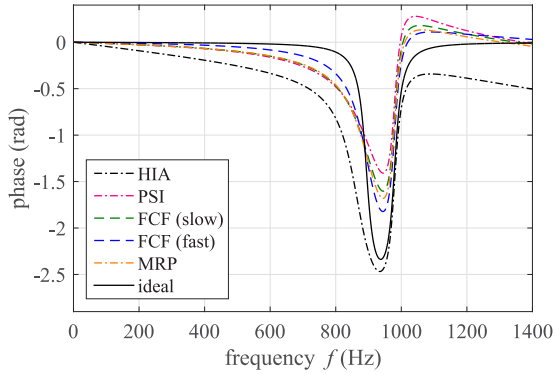

Fig. 7. Phase angle of voltage U_{A} of the simulated PHIL setup with varying interfaces and different methods for PHIL system stability applied.

Again, the subscripts HIA, FCF, PSI, and MRP are added to the system transfer function $T_{\mathrm{SYS,A}}(s)$ to relate $U_{\mathrm{A}}(s)$ and $U_{\mathrm{S}}(s)$, respectively:

$$T_{\mathrm{SYS,A,HIA}}(s) = \frac{Z_2(s)}{sL_2 + Z_2(s)} \frac{T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}}}{1 + F_{\mathrm{O,HIA}}(s)} \tag{41}$$

$$T_{\mathrm{SYS,A,FCF}}(s) = \frac{T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}}}{1 + F_{\mathrm{O,FCF}}(s)} \tag{42}$$

$$T_{\mathrm{SYS,A,PSI}}(s) = \frac{Z_2(s)}{Z_{\mathrm{sh}}(s) + Z_2(s)} \frac{T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}}}{1 + F_{\mathrm{O,PSI}}(s)} \tag{43}$$

$$T_{\mathrm{SYS,A,MRP}}(s) = \frac{T_{\mathrm{SYS,FW}}(s)}{1 + F_{\mathrm{O,MRP}}(s)} \tag{44}$$

where $T_{\mathrm{SYS,A,HIA}}(s)$, $T_{\mathrm{SYS,A,FCF}}(s)$, $T_{\mathrm{SYS,A,PSI}}(s)$, and $T_{\mathrm{SYS,A,MRP}}(s)$ denote the system transfer functions for the models of PHIL simulation setups with the HIA, FCF, PSI, and MRP interface methods, respectively.

C. Results and Analysis

Fig. 6 shows the magnitudes of the relative errors $\varepsilon_{\mathrm{SYS,A}}(\mathrm{j}\omega)$. The latter are given by (12), which relates to the voltage U_{A} according to (1). By definition, the relative error considers the size of the quantity involved. This allows for a practical estimation of accuracy properties throughout the frequency range of interest for PHIL simulation systems. Therefore, the use of the relative error is appropriate for this given use case. For use cases such as short-circuit fault scenarios at which the hardware impedance $Z_2(s)$ may approximate zero, the calculation of the absolute error represents a suitable alternative measure.

The curves are obtained with functions (41), (42), (43), and (44) relating $U_{\mathrm{A}}(s)$ and $U_{\mathrm{S}}(s)$ for different interfacing methods. The chain-dotted black line is the relative error of the PHIL simulation with HIA method, the chain-dotted magenta line shows the PSI method, and the dashed green line represents the FCF method at a time step of 12.5 µs. For the purpose of comparison with the MRP interface, the FCF method is also run at a smaller time step of 1 µs, represented by the dashed blue line. The chain-dotted orange line represents the PHIL system with MRP method. The same conventions apply to Fig. 7, which depicts the phase angles of the voltages U_{A}. Furthermore, the solid black line in Fig. 7 represents the phase angle of the fictitious ideal system assuming an ideal PI.

The bandwidth of accuracy of each model of PHIL simulation setup is defined as the frequency up to which the magnitude of the relative error is lower than –20 dB. The HIA method gives the smallest bandwidth at less than 650 Hz. The bandwidth of the FCF method at a time step size of 12.5 µs amounts to 790 Hz. The PSI method with shifting impedance reaches a bandwidth of 775 Hz. The FCF method with SR interface and a time step size of 1 µs reaches a higher bandwidth of 840 Hz, while the bandwidth of the MRP interface amounts to 800 Hz.

In Fig. 7, for low frequencies up to approximately 200 Hz, the phase angle deviation from the ideal system is low for all PHIL setups. For frequencies higher than 200 Hz and lower than 900 Hz, a significant phase angle deviation from the ideal system can be observed for the HIA method. Compared with the HIA method, the phase angle of the FCF method with a time step size of 12.5 µs shows a lower deviation from the phase angle of the ideal system up to a frequency of about 850 Hz. Further improvements in that frequency range are accomplished by the MRP method and the FCF method at a time step size of 1 µs. Just like the MRP method, the PSI method shows a low phase angle deviation from the ideal system up to a frequency of about 850 Hz.

The joint analysis of the plots of magnitude and phase in Figs. 6 and 7 shows that best accuracy is obtained with the FCF method at a time step size of 1 µs and the MRP method. Regarding this usage of the FCF method, the real-time constraint as indicated in Section II is to be kept in mind. Compared with the also considered time step size of 12.5 µs, the number of computations that can be performed within an interval of 1 µs is sharply reduced. Thus, the size of the network that can be simulated while respecting the real-time constrained is reduced, too. The MRP method here introduces flexibility to the real-time constraint as the network is partitioned to allow for diverse time step sizes in different subsystems. In practice, only a small

subdivision close to the PI would use the comparatively small time step size. If the MRP method is not available, then the PSI method offers an attractive tradeoff. It supports a particularly accurate simulation of the phase and a good performance regarding the magnitude.

The FCF method at 12.5 µs stands out as it is straightforward to implement and of high relevance in practical implementation. Its ability to set the bandwidth allows to ensure stability in a convenient way. This makes the FCF method a compelling candidate when setting up physical PHIL experiments in the laboratory, and it can also be well combined with the interfaces based on the HIA, PSI, or MRP methods.

V. Experimental Validation

In this section, the proposed analysis technique for PHIL systems is validated experimentally. The experimental study includes the implementation of an inverter-dominated low-voltage network with active generation units, nonlinear load profiles, and different types of cables in a laboratory environment.

A. Methodology

Based on the promising outcome of the analysis in Section IV-C, the SR PSI method and the MRP method were selected for implementation and verification as experimental PHIL simulation setups. A further hardware-only test setup was established to serve as the reference. While all three setups are of identical hardware side, the experimental PHIL simulation setups also involve PIs and software sides as explained in Section III.

Compared with the arrangement of the analytical evaluations performed in Section IV-A, the preparation of the experiments is more challenging. This relates to the certain degree of uncertainty when physical equipment is connected to the hardware interface for the first time. While instability in a theoretical analysis is acknowledged through the respective results of calculations, instability of an experimental PHIL simulation setup could lead to serious damage of equipment. It is thus recommended to start with conservative settings that ensure stability. Gradually, the settings can be adjusted. The steps of this iterative processes are described in the following.

In a first step, the experimental PHIL simulation setups are modeled to obtain open-loop transfer functions as described in Section IV-B, applied to the actual configuration. From Figs. 8 and 9, it can be seen that the hardware side of this configuration mainly consists of a grid-connected inverter. Therefore, the inverter model from Section IV-B was used again in this first step of modeling the transfer functions.

In the following step, the obtained approximate open-loop transfer functions are used to quantify the stability characteristics of each experimental PHIL simulation setup. Given a certain degree of uncertainty affiliated with the results, it is recommended to integrate the FCF method with the used PSI and MRP methods. The role of the FCF method is to limit the bandwidth of the open-loop transfer function and so enforcing stability, as discussed in Section III-B. Although not explicitly

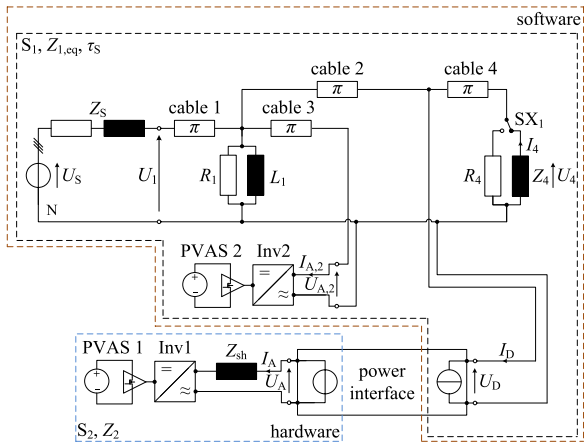

Fig. 8. Circuits on software and hardware sides for experimental analysis of PHIL simulation with SR interface.

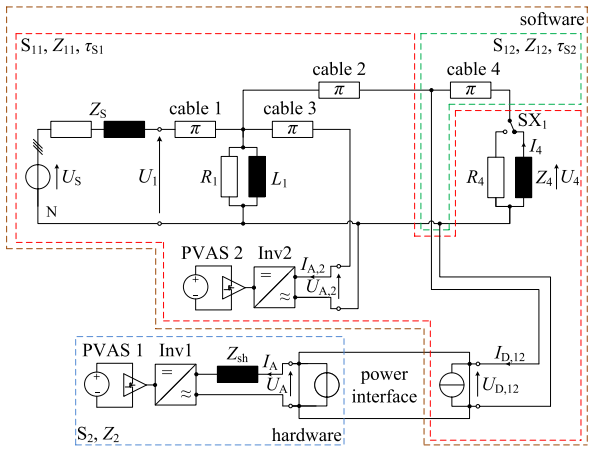

Fig. 9. Circuits on software and hardware sides for experimental analysis of PHIL simulation with MRP interface.

stated below, whenever the PSI and MRP methods are mentioned within the context of laboratory experiments, the usage of those methods implies a combination with the FCF method.

In a further step, the stability property is verified by moving from transfer function analysis to laboratory-scale PHIL experimentation. This is done by running PHIL simulations using the experimental PHIL simulation setups. Conservative settings are used initially. Then, in an iterative process, the prior and present steps are repeated with less conservative settings until the desired stability limit is attained. To allow for a comparison of the accuracy, PHIL setups with PSI and MRP interface methods both need to be at the same stability limit. The desired stability margin in the experimental PHIL setup is obtained when the differences in oscillatory behavior of the interface signals between the experimental PHIL simulation setup and the corresponding model of PHIL simulation of Section IV have become very small in the iterative process.

In a final step, the accuracy is considered. For the two experimental PHIL simulation setups with SR PSI method and the MRP method, the accuracies are analyzed by considering

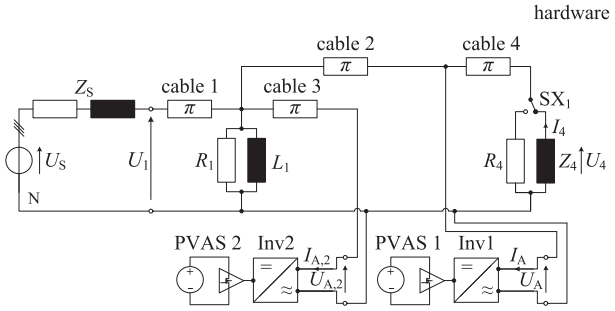

Fig. 10. Circuits for experimental analysis of hardware-only electric network.

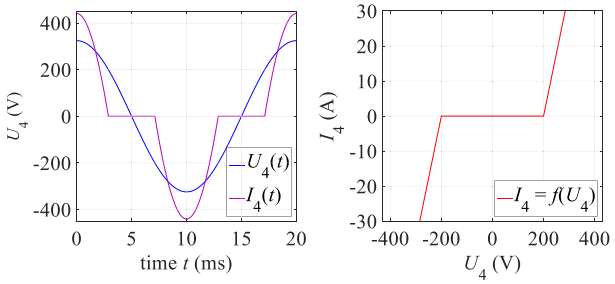

Fig. 11. Voltage and current characteristics for nonlinear load connected to PHIL simulation setup.

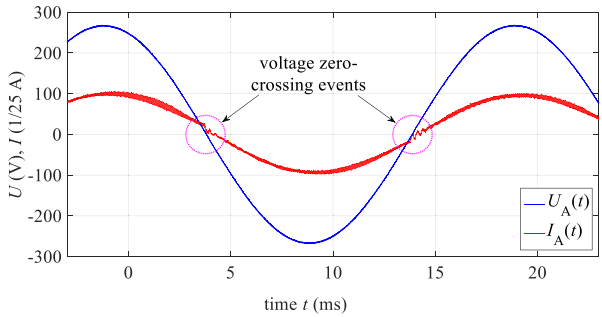

Fig. 12. Full wave of signal waveforms of Inv1 with connected linear load for hardware-only test setup.

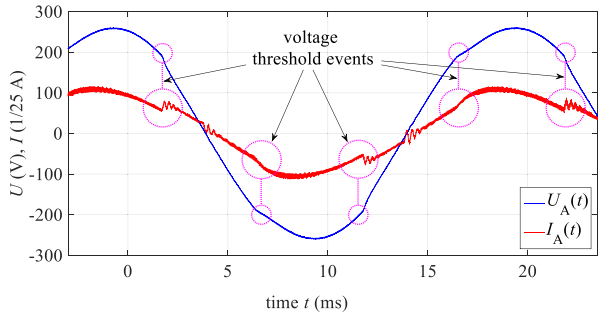

Fig. 13. Full wave of signal waveforms of Inv1 with connected nonlinear load for hardware-only test setup.

the resulting voltage and current waveforms of the hardware sides and comparing them with the waveforms obtained with the hardware-only setup.

B. Modeling and Experimental Setup

The schematic of the PHIL simulation setup with SR interface is shown in Fig. 8. The setup with the SR interface covers software side S_1 and hardware side S_2. When using the MRP interface, the software side is further partitioned into subsystems S_{11} and S_{12} marked by dashed lines in red and green colors in Fig. 9, respectively. Fig. 10 gives the hardware-only testing setup referring to the same integrated low-voltage power electric and electronic system. This setup allows for comparison of results from real-time based PHIL simulation and hardware-only tests.

As part of the setups, three single-phase voltage sources with a nominal line-to-line ac voltage value of $U_{\mathrm{LL}} = 400$ V at a nominal frequency of $f_{\mathrm{nom}} = 50$ Hz have an internal source impedance of $Z_S = 0.3\ \Omega + \mathrm{j}0.25\ \Omega$. Each of cables 1, 2, and 3 has a length of 1.2 km, while cable 4 is set to 0.5 km. The network includes the resistive load $R_1 = 18\ \Omega$ as well as the inductive load $L_1 = 85$ mH. As depicted in Fig. 8, either the resistive load R_4 or the nonlinear load Z_4 is connected to cable 4 via the switch SX_1. The nonlinear load Z_4 consists of a rectifying bridge feeding a linear load. Its characteristics are shown in Fig. 11. The magenta line on the left graph of Fig. 11 is the resulting current in response to an ideal sinusoidal voltage marked by the blue line. The red line on the right graph of Fig. 11 shows the nonlinear characteristics relating voltage and current of Z_4.

Inverters Inv1 and Inv2 are components of a rated, active output power of $P_{\mathrm{AC,rated}} = 4.0$ kW, respectively. In Fig. 8, Inv 1 is the hardware device connected to the PI, and Inv2 is a software model as explained in Section IV-B. More information referring to the software part, the hardware part, and the PI is given in Appendix D.

For the hardware-only test setup of Fig. 10, inverters Inv1 and Inv2 are physical hardware components sourced by the dc power supplies PVAS 1 and PVAS 2, respectively. Fig. 19 in Appendix D shows a photographic illustration of the setup.

C. Results and Analysis

Figs. 12 and 13 give, respectively, voltage U_{A} and current I_{A} of inverter Inv1 for the hardware-only test setup with and without nonlinear load connected. Fig. 12 shows waveforms where the linear load R_4 is connected to the network. Fig. 13 presents waveforms where the nonlinear load Z_4 is connected via the switch SX_1, which can be actuated during the running PHIL simulation. In these graphs, the solid blue line represents the voltage U_{A}, and the current I_{A} is marked by the solid red line, respectively. Voltage zero-crossing events and voltage threshold events triggering fast transients are highlighted by magenta circles in Figs. 12 and 13, respectively.

Fig. 14 shows details of voltage and current waveforms of Inv1 for the hardware-only test setup. Fig. 15 shows details of those waveforms of Inv1 for PHIL simulation with SR interface and applied PSI method, while Fig. 16 shows the corresponding waveforms for PHIL simulation with MRP interface. In these graphs, the solid blue line represents the voltage U_{A}. The current I_{A} is marked by the solid red line for the hardware-only setup,

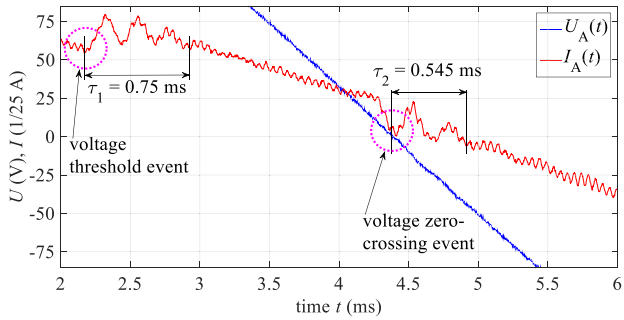

Fig. 14. Detailed view of voltage and current waveforms of Inv1 with connected nonlinear load for hardware-only test setup.

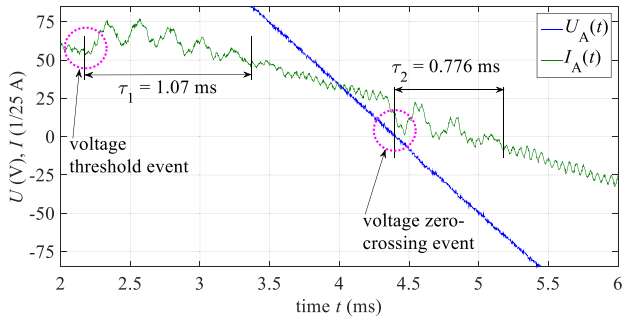

Fig. 15. Detailed view of voltage and current waveforms of Inv1 with connected nonlinear load for PHIL simulation with applied SR PSI interface.

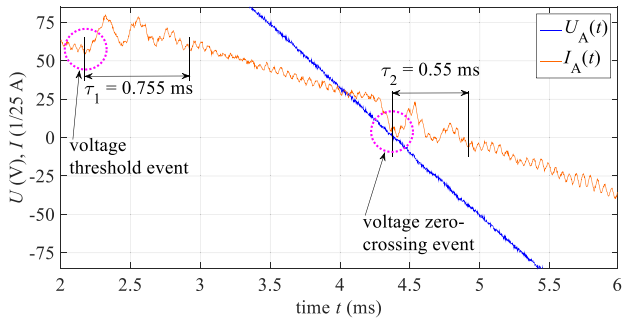

Fig. 16. Detailed view of voltage and current waveforms of Inv1 with connected nonlinear load for PHIL simulation with applied MRP interface.

the solid green line for the SR PSI method, and the solid orange line for the MRP interfacing method, respectively. Voltage zero-crossing events and voltage threshold events are highlighted by magenta circles in Figs. 14–16.

The waveforms of the hardware-only test setup in Fig. 14 and of the PHIL test setup with MRP interface in Fig. 16 show a quasi-identical behavior. For waveforms obtained with respective SR and MRP PHIL setups in Figs. 15 and 16, quantitative differences are observed for fast transients that appear just after $t = 2.2$ ms and $t = 4.4$ ms. Such fast transients are triggered here whenever the slope of the nonlinear load characteristic $I_4 = f(U_4)$ changes abruptly, as shown in Fig. 11, or whenever a zero-crossing of the voltage U_A occurs. The threshold voltages

TABLE II
MEASURED INTERVALS OF DECAY FOR HARDWARE-ONLY SETUP AND PHIL SIMULATION WITH SR AND MRP INTERFACES

setup	duration τ_1 (ms)	duration τ_2 (ms)
hardware-only setup	0.75	0.545
SR PHIL with PSI	1.07	0.776
PHIL with MRP	0.755	0.55

of the nonlinear load characteristics are observed at 200 V and – 200 V. The beginning of the fast transients at $t = 2.2$ ms is consistent with a crossing of the 200-V threshold. For the starting time at $t = 2.2$ ms, oscillations with the hardware-only setup have largely decayed by $t = 2.95$ ms. In comparison to that, oscillations of the inverter current are observed until $t = 3.27$ ms for the PHIL setup with SR PSI interface. For the PHIL setup with MRP interface, oscillations end at $t = 2.955$ ms. For voltage zero-crossing events starting at $t = 4.4$ ms, respectively, oscillations with the hardware-only setup end at $t = 4.945$ ms. Oscillations of the inverter current are observed until $t = 5.176$ ms for the PHIL setup with SR PSI interface. For the PHIL setup with MRP interface, oscillations end at $t = 4.95$ ms.

Table II summarizes the results for the measured transients' durations τ_1 and τ_2 for the hardware-only test setup, for PHIL simulation with SR PSI interface, and for PHIL simulation with MRP interface. The average duration for PHIL simulation with MRP interface slightly exceeds that for the hardware-only setup. For the PHIL setup with applied SR PSI method, the average duration is larger. Results show that the PHIL setup with MRP interface gives a better representation of the transients when comparing both MRP and SR tests with the hardware-only test. This can be attributed to the higher bandwidth attained for the MRP method.

For both PHIL simulation setups, results of practical relevance are achieved at identical stability properties. However, differences related to the dynamic performance between PHIL simulation setups are identified for conditions of fast transients. Given the differences in the used interfacing methods, such an observation is plausible. The observation is also consistent with the outcome of the analytical comparison in Section IV. On the one hand, the MRP method is more accurate than the SR method. In terms of accuracy, the MRP process of the network into subsystems is beneficial. On the other hand, this implementation is also more sophisticated, involving a higher application effort compared with the SR technique.

VI. CONCLUSION

Novel techniques for interconnecting physical equipment in power hardware-in-the-loop (PHIL) real-time simulation were developed, implemented, and validated. Particular attention was attributed to the connection of power electronic converters as physical equipment. Three main contributions were made. First, a framework for comparative analysis of PHIL system stability and accuracy was developed. For this purpose, all processes

involved in the signal processing and signal transfer from the software to the hardware side and vice versa were modeled and represented as block diagrams. Each block comprises a transfer function covering important information such as a block's influence on time delay and bandwidth. The modeling readily lends itself to application of the Nyquist criterion for stability analysis and the evaluation of accuracy. As an ideal reference for the purpose of comparison, the model of a notional ideal PI was formulated. The latter has no restriction on bandwidth, nor does it involve delays of signals.

The impact achieved through this development of the framework of comparative analysis is very high for PHIL users. Thanks to the framework, users are enabled to assess stability and accuracy and exploit this knowledge in planning for a PHIL experiment. Given the type of power hardware to be tested and the types of transients to be considered, users can determine the kind of interface that is most appropriate to interconnect physical hardware with the digital real-time simulator. Users are enabled to determine all relevant simulation parameters including time step sizes, bandwidths, and stability margins. The ability to clearly define simulation setups is indispensable for those who operate comprehensive PHIL laboratories and who need to estimate the efforts involved and to plan for upcoming PHIL tests for own purposes or on behalf of external clients.

The second contribution concerns the formulation and testing of a set of PHIL interfacing methods, making use of the above framework for comparative analysis. This includes the novel development of the PSI method as well as the extension and parametrization of the existing FCF and MRP methods. The existing HIA method was also included. Each method was applied to a model of a test setup covering an inverter model connected to a distribution network model.

The impact of this second contribution directly relates to the resulting recommendation that identifies the FCF, PSI, and MRP methods as practical alternatives, clearly outperforming the HIA method. With these recommendations, PHIL engineers have practical options readily at hand. While the PSI method performs best in SR simulation, the MRP method outperforms other techniques if multi-rate simulations are possible. The FCF method in turn can be combined with other methods to enhance stability.

As a third contribution, it is shown how to set up laboratory experiments that make use of the proposed PHIL interfaces. A power electronic inverter was physically connected to a PHIL real-time simulator in a laboratory environment and to a hardware-only test setup. A nonlinear load was modeled and connected as physical hardware as part of the setup.

The impact of this exercise is twofold. One the one hand, it was possible to validate the performance of the PHIL interfaces and to confirm the recommendations given. On the other hand, the offered explanations also give a user guideline on how to proceed with PHIL experiments without compromising stability.

Thanks to the described methods to stabilize PHIL systems, it has become possible to perform equipment testing at an enhanced level of accuracy at a specified stability margin. Given the increasing importance of power electronics as part of power systems when integrating renewable energy, the proposed methods will be beneficial for all manufacturers, network operators, consultants, and researchers who need to verify and validate the impact of such physical equipment in the network.

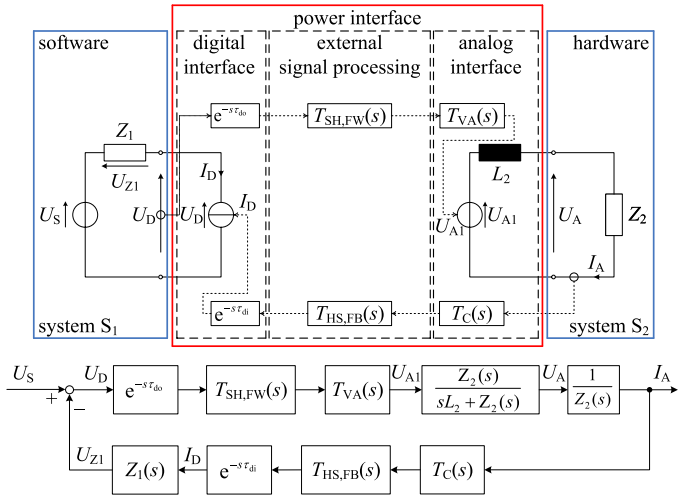

Fig. 17. Model and block diagram for analysis of PHIL simulation with SR HIA PI.

APPENDIX

A. Details on Transfer Functions of HIA Interfacing Method

Fig. 17 shows the model and the block diagram representation of PHIL simulation with SR HIA method in the form of a SISO closed loop. The corresponding open-loop transfer function defined by

$$F_{\mathrm{O}}(s) = \frac{U_{\mathrm{Z1}}(s)}{U_{\mathrm{D}}(s)} \tag{45}$$

becomes (13) with definition τ_{d} given by (7).

Using relations in (1) and (4), definitions given by (7), (45), and the relation

$$U_{\mathrm{A}}(s) = \frac{Z_2(s)}{sL_2 + Z_2(s)} T_{\mathrm{SH,FW}}(s) T_{\mathrm{VA}}(s) \mathrm{e}^{-s\tau_{\mathrm{do}}} U_{\mathrm{D}}(s) \tag{46}$$

the system transfer function $T_{\mathrm{SYS,A}}(s)$ for PHIL simulation systems with SR HIA interface method becomes (41).

B. Details on Transfer Functions of FCF Interfacing Method

Fig. 18 shows the model and the block diagram representation of PHIL simulation with SR FCF method in the form of a SISO closed loop. The corresponding open-loop transfer function defined by (45) becomes (14) with definition τ_{d} given by (7).

Using relations in (1), (3), (4), (7)–(9), and (14), the system transfer function $T_{\mathrm{SYS,A}}(s)$ for PHIL simulation systems with SR FCF interface method becomes (42).

C. Details on Transfer Functions of MRP Interfacing Method

In analogy to analysis presented for PHIL simulation with SR interface in Section II, the definition of the open-loop transfer function of the closed-loop system of the MRP interfacing

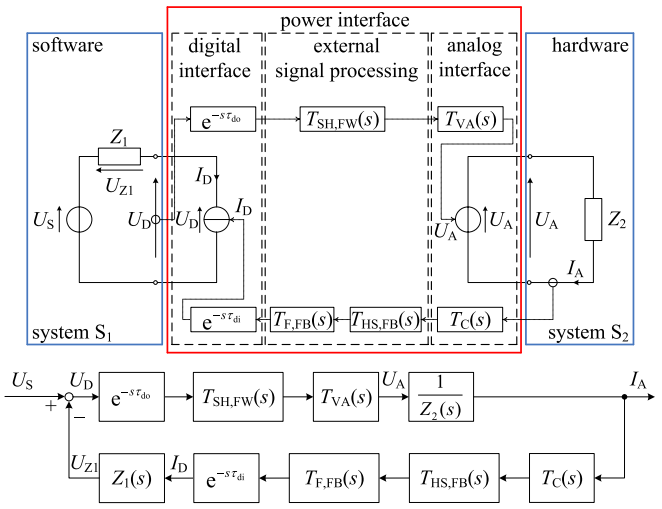

Fig. 18. Model and block diagram for analysis of PHIL simulation with SR FCF PI.

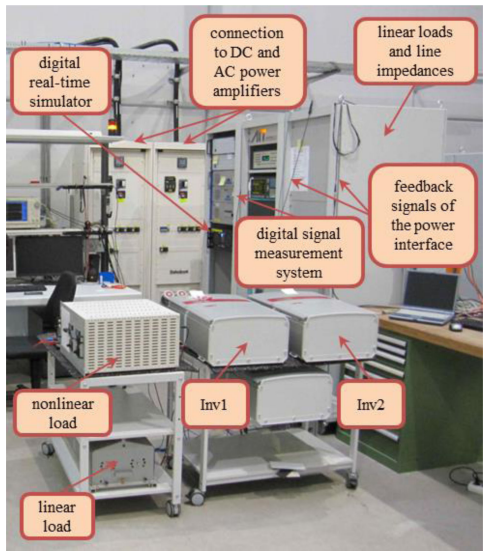

Fig. 19. Photograph of laboratory test setup for PHIL simulation and hardware-only test.

method is given by (24). The model for analysis of PHIL simulation with MRP interface and the corresponding block diagram is presented by Fig. 3 in Section III-D.

Based on the MRP concept, the following relations are defined for involved time delays:

$$T_{\mathrm{d},1}(s) = \mathrm{e}^{-s\tau_{\mathrm{d}1}} \tag{47}$$

$$T_{\mathrm{d},2}(s) = \mathrm{e}^{-s\tau_{\mathrm{d}2}} \tag{48}$$

$$T_{\mathrm{d}}(s) = \mathrm{e}^{-s\tau_{\mathrm{d}}} \tag{49}$$

$$\tau_{\mathrm{d}1} = \tau_{\mathrm{do},1} + \tau_{\mathrm{di},1} \tag{50}$$

$$\tau_{\mathrm{d}2} = \tau_{\mathrm{do},2} + \tau_{\mathrm{di},2} \tag{51}$$

$$\tau_{\mathrm{d}} = \tau_{\mathrm{d}1} + \tau_{\mathrm{d}2} \tag{52}$$

where $T_{\mathrm{d},1}(s)$ is the transfer function of the discretization time delay due to the VI connecting S_{11} and S_{12}, $T_{\mathrm{d},2}(s)$ is the transfer function of the discretization time delay due to the PI connecting systems S_{12} and S_2, and $T_{\mathrm{d}}(s)$ is the transfer function of the cumulative total time delay due to discretization. According to [17], the open-loop transfer function of the MRP interfacing method becomes (25).

D. Details on Experimental Setup in Laboratory

Following the methodological concept of Section V-A, the following settings were made for the PHIL simulation setups and for the hardware-only test setup in Section V-B. For the SR interface with PSI method, a minimum time step size of $\tau_{\mathrm{S}} = 50$ µs could be achieved while complying with the real-time constraint. Stability for the PHIL setup with PSI method can be reached when applying a shifting impedance of $Z_{\mathrm{sh}}(s) = 0.12\ \Omega + \mathrm{j}0.003\ \Omega$ to the analog interface, as described in Section III-C. At the same time, a low-pass filter component is applied to the feedback path, as introduced in Section III-B. The corner frequency of this feedback filter is varied based on the methodological process explained in Section V-A.

At an initial stage of PHIL experiments, conservative settings are chosen to ensure system stability as a primary objective. At further stages of the validation process, those setups are modified step by step with the objective of exploring the stability limit. As part of this process, filter corner frequencies are varied, as explained in Section V-A. The maximum achievable system bandwidth of the PHIL setup with the SR PSI method is so shown to be 0.8 kHz.

For the multi-rate interface with the MRP method, the settings of the PHIL simulation setup have to be configured in such a way that the results can be compared to those of the PHIL setup with the SR PSI method. For the MRP interface, the primary subsystem S_{11} with the impedance $Z_{11}(s)$ as defined in Fig. 8 is given the time step size of $\tau_{\mathrm{S}1} = 50$ µs. For subsystem S_{12} with the impedance $Z_{12}(s)$, a minimum time step size of $\tau_{\mathrm{S}2} = 25$ µs is reached. As a consequence of this setting, the maximum achievable system bandwidth of PHIL simulation with MRP interface setup is 2.5 kHz. In analogy to the SR case, the system bandwidth of the PHIL simulation system with MRP interface may be adjusted by defining the feedback filter represented by $T_{\mathrm{HS,FB}}(s)$ and $T_{\mathrm{VI,FB},i}(s)$, as explained in [17].

For both PHIL simulation setups, a linear amplifier is used for the purpose of voltage amplification, and a current probe is applied for the current measurement. The dynamics of the power amplifier and the current probe are described by $T_{\mathrm{VA}}(s)$ in (39) and $T_{\mathrm{C}}(s)$ in (40), respectively.

Fig. 19 shows a photographic image of the laboratory setup consisting of components and connections. In addition to performing PHIL simulation, the shown setup also allows for hardware-only tests, as described in Section V-A.

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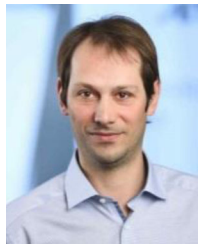

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