

Accurate Online Junction Temperature Estimation of IGBT Using Inflection Point Based Updated I–V Characteristics

Abhinav Arya^{1b}, Student Member, IEEE, Abhishek Chanekar^{2b}, Student Member, IEEE, Pratik Deshmukh, Amit Verma, Member, IEEE, and Sandeep Anand^{3b}, Senior Member, IEEE

Abstract—The junction temperature (T_j) estimation of the insulated gate bipolar transistor (IGBT) is important for reliable operation of the power converters in various applications. For T_j estimation, ON-state collector-emitter voltage (v_{ce}) at higher collector currents (i_c) is widely used temperature sensitive electrical parameter (TSEP). For real-time T_j estimation, this TSEP is calibrated using the I–V characteristics of the new IGBT. Due to bond-wire degradation, the original I–V characteristics of IGBT changes resulting in inaccurate T_j estimation. In this article, a technique is proposed to update the I–V characteristics of the degraded IGBT, without affecting the normal operation of the power converter. It is achieved by estimating the increment in bond-wire resistance (ΔR_{con}) by using real-time samples of v_{ce} and inductor current. The mathematical analysis is also presented to find an error in estimated ΔR_{con} . The major contributions of this article are as follows: a) it enables the accurate T_j estimation of the IGBT throughout its lifetime; and b) it also provides the parameter ΔR_{con} , which could be utilized in condition monitoring of the IGBT. Further no additional circuitry is required. The proposed technique is validated on experimental setup, which is developed in the laboratory. The error in T_j estimation is observed within 1 °C the degraded IGBT, which shows the effectiveness of the proposed scheme.

Index Terms—Bond-wire degradation, insulated gate bipolar transistor (IGBT), junction temperature, ON-state collector emitter voltage.

I. INTRODUCTION

AN IGBT is the most commonly used power semiconductor device in medium/high power conversion applications. Though widely used, the reliability of insulated gate bipolar

transistor (IGBT) is a major concern in the industrial applications. The study reveals that around 34% of the converter failures are due to failure of the IGBTs [1], [2]. Besides, around 55% failures of IGBTs are related to its junction temperature (T_j). For reliable operation of an IGBT, the information of T_j has various applications such as its: 1) CM [3]–[8], 2) active thermal control (ATC) [9]–[12], 3) protection against thermal runaway [13], 4) power curtailment [14], etc. The T_j is an average value of temperature distribution within the chip/die of an IGBT and is a virtual value. In general, the accuracy of 1°C in estimated T_j is desired for successful implementation of the abovementioned applications [1], [9].

To obtain the T_j of an IGBT, the methods presented in the literature are categorised into direct and indirect methods. The comparison of these methods are provided in Table I. The direct methods include the measurement of T_j by using the optical temperature sensors, thermistors, etc. Generally, the measurement of T_j by using the direct methods is limited due to packaging of the IGBT. There are some commercial solutions available on the direct measurement of temperature inside the IGBT package. The temperature sensor (generally thermistor or diode) is integrated on the substrate layer of the IGBT package [15]. However, there is a nonuniform distribution of temperature inside the IGBT package [9]. Due to this, the temperatures are different at the junction of IGBT chip and at the sensor. Thus, the temperature sensor would fail to measure the T_j of the IGBT.

There are indirect methods available in the literature to estimate the T_j by using the thermal impedance models (Cauer/Foster) or temperature sensitive electrical parameters (TSEPs) of the IGBT. First, the literature on T_j estimation by using the thermal impedance models is presented. The lumped RC parameter values of conventional Foster model are provided in datasheet of the IGBT. By using the thermal model parameters and estimated power loss of the IGBT, the T_j could be estimated. However, the model parameters provided in the datasheet are calculated for worst scenarios, thus, not suitable for accurate real time T_j estimation [9]. In [16], a method for estimation of an accurate lumped RC thermal model parameters is presented. It enables the T_j estimation with reduced error as compared to the conventional thermal model. However, the thermal properties of different packaging layers varies with the temperature. This results in the temperature dependency of the thermal model,

Manuscript received October 28, 2020; revised January 30, 2021; accepted March 3, 2021. Date of publication March 17, 2021; date of current version June 1, 2021. Recommended for publication by Associate Editor A. Lindemann. (Corresponding author: Abhinav Arya.)

Abhinav Arya, Abhishek Chanekar, and Amit Verma are with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India (e-mail: abhinav.ieee1920@gmail.com; abhichanekar26@gmail.com; akv3900@gmail.com).

Pratik Deshmukh is with the Intel Technology India Pvt, Ltd., Bangalore 560001, India (e-mail: pratikd18@gmail.com).

Sandeep Anand is with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India (e-mail: me.sandeep.anand@gmail.com).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2021.3066287>.

Digital Object Identifier 10.1109/TPEL.2021.3066287

TABLE I
COMPARISON OF DIFFERENT METHODS TO OBTAIN JUNCTION TEMPERATURE OF IGBT

| Methods | Parameter | Accuracy | Complexity | Real-time | Independent of Operating Conditions | Independent of Ageing |
|--------------------------------------|--|----------|------------|-----------|-------------------------------------|-----------------------|
| Direct | Optical sensor, thermistor, etc. | High | High | No | Yes | Yes |
| Indirect (Thermal Model Based) | RC Parameters from datasheet [9] | Low | Low | No | No | No |
| | Estimated RC Parameters of Cauer thermal model [16] | Low | Low | No | No | No |
| | Temperature dependent Cauer thermal model [17], [18] | Moderate | Moderate | No | No | No |
| | Lumped RC 3-D thermal model [19] | High | High | No | Yes | No |
| Indirect (TSEP) | Short-circuit current [20] | High | High | Yes | No | No |
| | t_{off} [21] | Low | Moderate | Yes | No | Yes |
| | $V_{GE,np}$ [22] | Low | Moderate | Yes | No | No |
| | Gate resistance [23] | Low | Low | Yes | Yes | No |
| | v_{ce} at low i_c [6] | Low | High | Yes | Yes | Yes |
| | v_{ce} at high i_c [24] | Moderate | Low | Yes | Yes | No |
| | v_{ce} at high i_c with updated I-V characteristics (proposed) | Moderate | Low | Yes | Yes | Yes |

which is not incorporated in [16]. The temperature dependent thermal model for T_j estimation is presented in [17]. The RC parameters of the thermal model are obtained by using the temperature dependent equations of thermal conductivity and specific heat capacity of different packaging layers of IGBT. In [18], RC parameters of temperature dependent thermal model are obtained by finite element method (FEM) simulations. In both [17] and [18], the thermal models do not incorporate the cross coupling of power losses among different semiconductor chips inside the packaged IGBT. In [19], the presented 3-D thermal model incorporates this cross coupling. The parameters of 3-D thermal model is obtained by using FEM simulations, which are utilized in real time T_j estimation of IGBT. The major limitation of the thermal model based techniques is that the model parameters changes with the ageing of the IGBT. This is due to voids or cracks formation in the package layers with degradation. Thus, the accurate temperature estimation in real applications is not possible through these techniques.

For indirect T_j estimation of IGBT, it is advantageous to use a TSEP due to its faster response and its feasibility during the operation of power converters. However, the proper selection of a TSEP is crucial for 1) accuracy in the estimated temperature and 2) not affecting the actual operation and life of the converter. In [6], ON-state collector-emitter voltage (v_{ce}) at low collector current (i_c) is used as TSEP. The calibration of v_{ce} versus T_j is done in order to estimate the real time T_j of the IGBT. The drawback of the technique is that the sensitivity of v_{ce} with T_j is poor at low collector currents. This would require a precise voltage and current measurements and would increase the cost of the system. In [20], the short-circuit current is used as TSEP for online T_j estimation of IGBT. The short-circuit current has good sensitivity with T_j . However, the large short circuit current would increase the stress on IGBT. Thus, reducing the operational life of the device. The techniques discussed in [6]

and [20], would also affect the normal converter operation and require an additional circuitry for the T_j estimation. In [21] and [22], turn-OFF time (t_{OFF}) and gate-emitter negative peak voltage during turn-OFF ($V_{GE,np}$) of IGBT are used as TSEPs, respectively. The presented techniques do not affect the normal operation and life of the converter. However, for real time T_j estimation, the high ADC sampling rate is required to obtain t_{OFF} and the measurement of $V_{GE,np}$ is prone to noise. Also, the dependence of t_{OFF} and $V_{GE,np}$ on operating parameters such as load current and blocking voltage, limits their use in T_j estimation of the IGBT. In [23], a technique is proposed in which the internal gate resistance of MOS devices is used as TSEP. The presented technique is immune to circuit operating conditions. The drawback of the technique is that the calculation of internal gate resistance includes the resistance of bond-wire, which increases due to its degradation with ageing. The effect of device aging on this TSEP results in inaccurate T_j estimation over a lifetime of IGBT. In [24], v_{ce} at higher collector currents (i_c) of IGBT is used as TSEP. The real time T_j is estimated by mapping the sampled v_{ce} and i_c on the I-V characteristics of the IGBT. The drawback of the technique is that the I-V characteristics change due to bond-wire degradation of an IGBT, which results in an inaccurate T_j estimation. The general limitations of the TSEP-based techniques such as their dependence on device ageing, poor sensitivity of TSEPs, interference with normal circuit operation and requirement of additional circuitry are overcome in the proposed technique of this article.

In this article, a technique is proposed to real time update the I-V characteristics of an IGBT with its bond-wire degradation. The T_j of an IGBT is estimated by using the v_{ce} at high i_c of I-V characteristics as TSEP. The novelty of proposed technique is that it enables the accurate T_j estimation even for degraded IGBT. The implementation of technique does not require any additional circuitry and does not affect the actual operation.

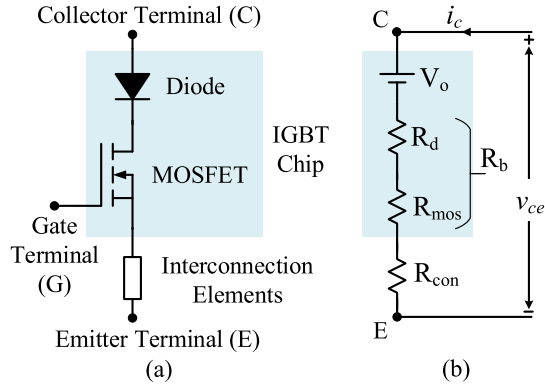


Fig. 1. ON-state model of IGBT. (a) Series combination of different elements. (b) Representation in terms of electrical parameters.

Furthermore, the proposed technique also provide the increment in bond-wire resistance due to its degradation, which could be utilized for condition monitoring of the IGBT. The article is organized as follows. In Section II, the sensitivity of v_{ce} with T_j at different i_c is presented, which helps in selection of operating point ($v_{ce}-i_c$) for T_j estimation. In this section, the effect of bond-wire degradation on I–V characteristics is also discussed. The detailed explanation of the proposed technique with mathematical analysis is presented in Section III. The results on experimental validation of the proposed technique is presented in Section IV. Finally, Section V concludes this article.

II. SENSITIVITY AND ACCURACY OF v_{ce} AS TSEP

A. Sensitivity of v_{ce} With T_j

In this section, the sensitivity of v_{ce} with T_j for different collector currents is presented. During ON-state, IGBT chip is modeled as series combination of diode and metal-oxide semiconductor field effect transistor, as shown in Fig. 1 [25]–[27]. The electrical connection to the IGBT chip is made by using interconnection elements such as chip metallization, substrate metallization, bond-wires, and terminals. The interconnection elements are also incorporated in the ON-state model of the IGBT. By using this model, the temperature dependent ON-state collector emitter voltage of healthy IGBT, v_{ce}^{hl} is given by [6], [24]

$$v_{ce}^{hl} = V_o + \alpha_o \Delta T_j + i_c R_b (1 + \alpha_b \Delta T_j) + i_c R_{con} (1 + \alpha_{con} \Delta T_j) \quad (1)$$

where ΔT_j is the difference between operating T_j and its base value (T_{j0}), V_o is the ON-state zero-current forward voltage drop at T_{j0} , and α_o is its temperature coefficient. R_b is the addition of resistances R_d and R_{mos} at T_{j0} , α_b is the temperature coefficient of R_b , R_{con} is the resistance of interconnecting elements at T_{j0} , and α_{con} is its temperature coefficient. From (1), the sensitivity (S) of v_{ce} with T_j is given by

$$S = \frac{\partial v_{ce}}{\partial T_j} = \alpha_o + i_c (R_b \alpha_b + R_{con} \alpha_{con}). \quad (2)$$

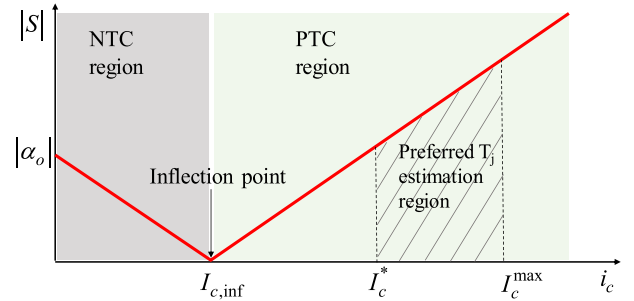


Fig. 2. Sensitivity of v_{ce} with T_j at different i_c .

The trench gate field stop IGBTs (FS-IGBTs) are widely used in the power applications, as they combine the advantages of conventional nonpunch through and punch through structures [28]. For FS-IGBTs, the value of α_o is negative, whereas, the values of α_b and α_{con} are positive [29]. At lower values of i_c , the sensitivity of v_{ce} with T_j is negative. This region is known as negative temperature coefficient (NTC) region, as shown in Fig. 2. The magnitude of S keeps on reducing as the i_c increases in NTC region. At a certain value of i_c ($I_{c,inf}$), the value of S reaches to zero. This operating point is known as the inflection point, at which the value of v_{ce} is independent of T_j . Abovementioned inflection point, the sensitivity of v_{ce} with T_j is positive and the value of S increases with an increase in i_c . This region is known as positive temperature coefficient (PTC) region. From Fig. 2, it is observed that the value of S is low in NTC region with maximum of α_o at zero collector current. The magnitude of α_o is around $1 - 1.5 \text{ mV}/^\circ\text{C}$, [4], which is also verified in Section IV-A. On the other side, in the PTC region, the high value of S could be achieved at higher collector currents. Based on the abovementioned discussion, it is suggested to estimate the T_j at higher collector currents of the IGBT. For T_j estimation, it is preferred to define the threshold value of i_c (I_c^*), which is near to maximum operating current of the IGBT (I_c^{\max}), as shown in Fig. 2.

B. Effect of Bond-Wire Degradation on I–V Characteristics

With the ageing of IGBT, the degradation of bond-wire results in an increase in the interconnection resistance (ΔR_{con}). The ON-state collector emitter voltage for a degraded IGBT, v_{ce}^{deg} is given by

$$v_{ce}^{\text{deg}} = V_o + \alpha_o \Delta T_j + i_c R_b (1 + \alpha_b \Delta T_j) + i_c (R_{con} + \Delta R_{con}) (1 + \alpha_{con} \Delta T_j). \quad (3)$$

From (1) and (3), for a given T_j and i_c , the increment in v_{ce} due to ΔR_{con} is written as

$$\Delta v_{ce} = i_c \cdot \Delta R_{con} (1 + \alpha_{con} \Delta T_j). \quad (4)$$

Generally, for an IGBT the value of R_{con} is below $10 \text{ m}\Omega$ [24]. Over the life span of IGBT, the value of ΔR_{con} is not more than 5% to 10% of the R_{con} of healthy IGBT [1], [3]. The change in ΔR_{con} would be very small due to variation in temperature. Therefore, the temperature dependence of ΔR_{con} could be

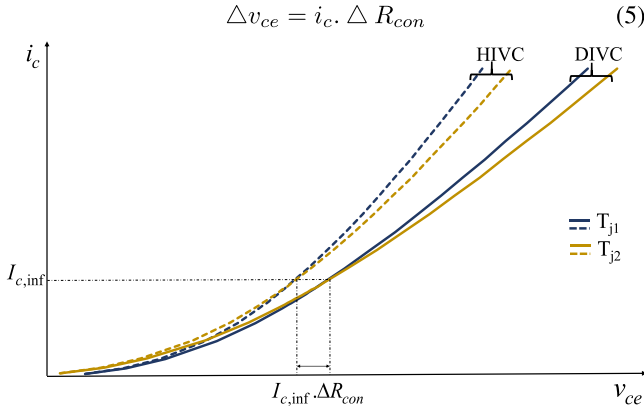


Fig. 3. Shift in I–V characteristics due to bond-wire degradation.

neglected. This assumption is justified later on in Section IV. With this assumption, (4) is written as

$$\Delta v_{ce} = i_c \cdot \Delta R_{con}. \quad (5)$$

The increment in v_{ce} due to ΔR_{con} shifts the healthy I–V characteristics (HIVC) to the degraded I–V characteristics (DIVC), as shown in Fig. 3. It is assumed that the value of i_c at inflection point of HIVC and DIVC would not change due to bond-wire degradation. Therefore, the inflection point would shift horizontally by $I_{c,inf} \cdot \Delta R_{con}$, as marked in Fig. 3. The increment in v_{ce} at $I_{c,inf}$ is utilized in forming DIVC from HIVC for an accurate real time T_j estimation, which is discussed in the following section.

III. PROPOSED TECHNIQUE

In this section, a detailed explanation of the proposed technique on online T_j estimation of IGBT is presented. The mathematical analysis is also carried out to determine the efficacy of the proposed technique and included in this section.

A. Explanation of Proposed Technique

The proposed technique is explained in detail by using the modules, as shown in Fig. 4.

1) *Module 1 (Prerequisites)*: Prior to application of the IGBT, its ON-state I–V characterization is carried out by using the methodology presented in [30]. During characterization, the case temperature of healthy device under test (DUT) is controlled by placing it inside the thermal chamber. To ensure the junction temperature of DUT nearly equal to the case temperature, a current pulse of short duration flows through it by using a single pulse test circuit. At a particular junction temperature, the current pulses of different magnitudes are provided to the DUT and the respective v_{ce} is measured. The process is repeated to obtain the I–V characteristics at different junction temperatures. The obtained I–V characteristics of IGBT is termed as healthy I–V characteristics (HIVC). The HIVC provide the collector current ($I_{c,inf}$) at inflection point and corresponding collector-emitter voltage $V_{ce,inf}^{hl}$, which are used in updating the I–V characteristics of the aged IGBT as discussed in the following.

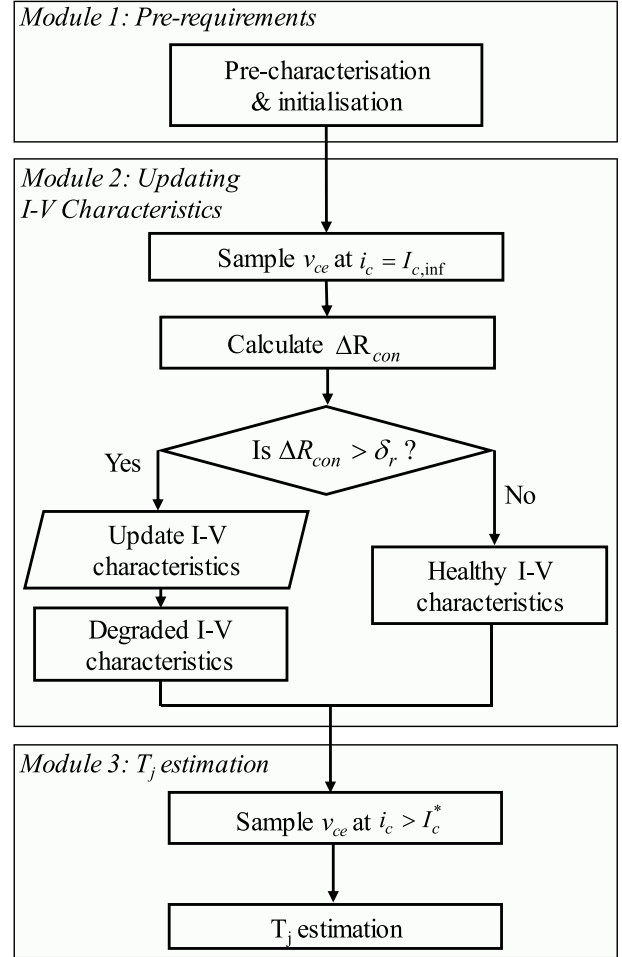
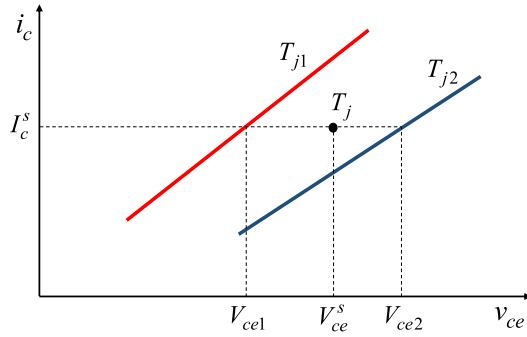


Fig. 4. Different modules of the proposed technique.

2) *Module 2 (Updating I–V Characteristics)*: As discussed in Section II-B, the value of $I_{c,inf}$ is assumed to be same for HIVC and DIVC. This property is utilized in estimating the value of ΔR_{con} due to bond-wire degradation. During actual operation of IGBT, the v_{ce} is sampled at the collector current equals to the $I_{c,inf}$, which is obtained from HIVC, as discussed in Module 1. By using the sampled v_{ce} , the value of ΔR_{con} is calculated by

$$\Delta R_{con} = \frac{V_{ce,inf}^s - V_{ce,inf}^{hl}}{I_{c,inf}} \quad (6)$$

where $V_{ce,inf}^s$ is the sampled v_{ce} at $I_{c,inf}$. An error in sampling of v_{ce} and the collector current introduces an error in the estimation of ΔR_{con} . The maximum value of this error is used as a tolerance (δ_r) for ΔR_{con} to decide the updation of I–V characteristics. If the value of ΔR_{con} is greater than δ_r , then this implies that the bond-wire of IGBT is degraded and the characteristics should be updated. The value of δ_r should be kept nearer to zero for detection of even a small change in R_{con} due to bond-wire degradation. For degraded IGBT, the DIVC is obtained by updating the values of v_{ce} of HIVC (v_{ce}^{hl}) at different i_c and T_j . The updated values of v_{ce} of DIVC is given by

Fig. 5. Linear interpolation for T_j estimation.

$$V_{ce}^{\text{deg}}[m, n] = V_{ce}^{\text{hl}}[m, n] + I_c[n] \cdot \Delta R_{con}$$

$$\forall m = 1, 2, \dots, M \ \& \ \forall n = 1, 2, \dots, N \quad (7)$$

where N is the total number of I-V points in an I-V curve at a particular T_j of HIVC and n is an index term representing each I-V point of that I-V curve at a particular T_j , M is the number of I-V curves of HIVC at different T_j and m is the index term representing each I-V curve of HIVC at a particular T_j . For the degraded IGBT, the DIVC obtained from the abovementioned method is used in module-3 for T_j estimation. If the value of ΔR_{con} is within the tolerance δ_r , then this implies that the bond-wire of IGBT is healthy. Thus, it is not required to update the values of v_{ce} of the HIVC. For the healthy IGBT, the HIVC is used in module-3 for T_j estimation.

3) *Module 3 (T_j Estimation)*: In module-2, based on the health status of the IGBT, the I-V characteristics is determined for T_j estimation. In this module, the method of T_j estimation of IGBT is presented using the I-V characteristics. During actual operation of IGBT, the values of v_{ce} are sampled at the i_c greater than the I_c^* , which is obtained from HIVC, as discussed in Module 1. The sampled v_{ce} (V_{ce}^s) and i_c (I_c^s) are mapped on the I-V characteristics to estimate the T_j . In practice, the I-V characteristics are available at finite discrete temperature values within the operating range of T_j of an IGBT. In that case, the V_{ce}^s and I_c^s may not intersect the characterized curves, as shown in Fig. 5. The T_j lies in between the two temperature curves, which can be obtained by linear interpolation as given by

$$T_j = T_{j1} + \frac{T_{j2} - T_{j1}}{V_{ce2} - V_{ce1}} \times (V_{ce}^s - V_{ce1}) \quad (8)$$

where T_{j1} and T_{j2} are the two nearest temperature curves where the sampled I-V point lies in-between, V_{ce1} and V_{ce2} are the values of v_{ce} at I_c^s at temperatures T_{j1} and T_{j2} , respectively. The effectiveness of linear interpolation is validated in Section IV.

B. Mathematical Analysis of the Proposed Technique

In the proposed technique, the estimation of ΔR_{con} is based on assumption that the value of $I_{c,\text{inf}}$ is same for HIVC and DIVC. In this section, the shift in $I_{c,\text{inf}}$ due to bond-wire degradation is estimated and the abovementioned assumption is validated. Also, an error is estimated in calculating ΔR_{con} by using the $I_{c,\text{inf}}$ of HIVC.

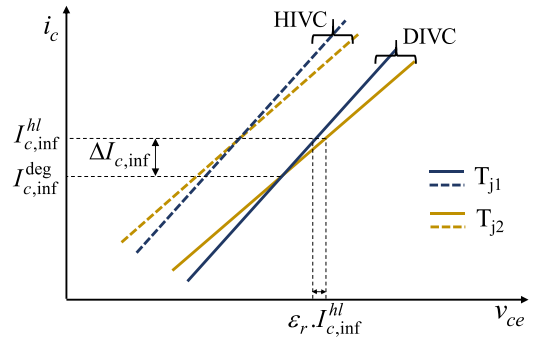


Fig. 6. Shift in inflection point due to bond-wire degradation.

1) *Shift in $I_{c,\text{inf}}$ Due to Bond-Wire Degradation*: For a healthy IGBT, the value of v_{ce} at inflection point, $V_{ce,\text{inf}}^{\text{hl}}$ is given by

$$V_{ce,\text{inf}}^{\text{hl}} = V_o + \alpha_o \Delta T_j + I_{c,\text{inf}}^{\text{hl}} R_b (1 + \alpha_b \Delta T_j)$$

$$+ I_{c,\text{inf}}^{\text{hl}} R_{con} (1 + \alpha_{con} \Delta T_j) \quad (9)$$

where $I_{c,\text{inf}}^{\text{hl}}$ is the collector current at inflection point of HIVC. As discussed in Section II-A, the v_{ce} at inflection point is independent of T_j . Therefore, the T_j dependent terms in (9) cancel each other as given by

$$\alpha_o + I_{c,\text{inf}}^{\text{hl}} (R_b \alpha_b + R_{con} \alpha_{con}) = 0. \quad (10)$$

From (10), the $I_{c,\text{inf}}^{\text{hl}}$ is written as

$$I_{c,\text{inf}}^{\text{hl}} = \frac{-\alpha_o}{k} \quad (11)$$

where $k = R_b \alpha_b + R_{con} \alpha_{con}$. From (11), it observed that the increment in R_{con} due to bond-wire degradation would decrease the current at inflection point of HIVC. This results a shift in $I_{c,\text{inf}}$ between HIVC and DIVC, as shown in Fig. 6. For a degraded IGBT, the value of v_{ce} at shifted inflection point, $V_{ce,\text{inf}}^{\text{deg}}$ is given by

$$V_{ce,\text{inf}}^{\text{deg}} = V_o + \alpha_o \Delta T_j + I_{c,\text{inf}}^{\text{deg}} R_b (1 + \alpha_b \Delta T_j)$$

$$+ I_{c,\text{inf}}^{\text{deg}} (R_{con} + \Delta R_{con}) (1 + \alpha_{con} \Delta T_j) \quad (12)$$

where $I_{c,\text{inf}}^{\text{deg}}$ is the collector current at inflection point of DIVC. Similar to (11), the $I_{c,\text{inf}}^{\text{deg}}$ is given by

$$I_{c,\text{inf}}^{\text{deg}} = \frac{-\alpha_o}{k + \Delta R_{con} \alpha_{con}}. \quad (13)$$

By using (11) and (13), a shift in collector current at the two inflection points, $\Delta I_{c,\text{inf}}$ is given by

$$I_{c,\text{inf}}^{\text{deg}} - I_{c,\text{inf}}^{\text{hl}} = \Delta I_{c,\text{inf}} = \frac{\alpha_o \alpha_{con} \Delta R_{con}}{k \cdot (k + \Delta R_{con} \alpha_{con})}. \quad (14)$$

By using the HIVC of an IGBT, the value of k is calculated from (11). The value of k is typically less than $1 \text{ m}\Omega/\text{C}$ whereas, the product of ΔR_{con} and α_{con} is in order of few $\mu\Omega/\text{C}$. Thus, the product $\Delta R_{con} \cdot \alpha_{con}$ is neglected as compared to k and (13) is

rewritten as

$$\Delta I_{c,\text{inf}} = \frac{\alpha_o \alpha_{con} \Delta R_{con}}{k^2} = B \cdot \Delta R_{con}. \quad (15)$$

It is observed that the shift in $I_{c,\text{inf}}$ is proportional to the bond-wire degradation. However, the product of B and ΔR_{con} is small which limits the $\Delta I_{c,\text{inf}}$ in order of milli-Amperes, where the value of $I_{c,\text{inf}}$ is in order of few to 10's of Amperes. Though the shift in $I_{c,\text{inf}}$ is small for a degraded IGBT, but it is important to estimate an error in calculating ΔR_{con} due to this shift.

2) *Error in Estimation of ΔR_{con}* : For a healthy IGBT, by using (9) and (10), the $V_{ce,\text{inf}}^{hl}$ is written as

$$V_{ce,\text{inf}}^{hl} = V_o + I_{c,\text{inf}}^{hl}(R_b + R_{con}). \quad (16)$$

Due to bond-wire degradation, the value of $I_{c,\text{inf}}^{hl}$ is shifted to $I_{c,\text{inf}}^{\text{deg}}$, as discussed in the following section. Therefore, for a degraded IGBT, the value of v_{ce} at $I_{c,\text{inf}}^{hl}$ is no more T_j independent. For a degraded IGBT, the temperature dependent value of v_{ce} at $I_{c,\text{inf}}^{hl}$, V_{ce}^{deg} is given by

$$V_{ce}^{\text{deg}} = V_o + \alpha_o \Delta T_j + I_{c,\text{inf}}^{hl} R_b (1 + \alpha_b \Delta T_j) + I_{c,\text{inf}}^{hl} (R_{con} + \Delta R_{con}) (1 + \alpha_{con} \Delta T_j). \quad (17)$$

By subtracting (16) from (17)

$$V_{ce}^{\text{deg}} - V_{ce,\text{inf}}^{hl} = (\alpha_o + I_{c,\text{inf}}^{hl} (R_b \alpha_b + R_{con} \alpha_{con})) \Delta T_j + I_{c,\text{inf}}^{hl} \Delta R_{con} (1 + \alpha_{con} \Delta T_j). \quad (18)$$

By using (10), (18) is simplified as given by

$$V_{ce}^{\text{deg}} - V_{ce,\text{inf}}^{hl} = I_{c,\text{inf}}^{hl} \Delta R_{con} (1 + \alpha_{con} \Delta T_j). \quad (19)$$

From (19), the value of ΔR_{con} is estimated as given by

$$\Delta R_{con} = \frac{V_{ce}^{\text{deg}} - V_{ce,\text{inf}}^{hl}}{I_{c,\text{inf}}^{hl}} - \varepsilon_r \quad (20)$$

where $\varepsilon_r = \Delta R_{con} \cdot \alpha_{con} \cdot \Delta T_j$. The ε_r in (20) is the error in estimation of ΔR_{con} due to bond-wire degradation. The product of $\Delta R_{con} \cdot \alpha_{con}$ is very small, in order of few $\mu\Omega/^\circ\text{C}$. Thus, the value of ε_r is very small for an operating range of junction temperature of the IGBT.

IV. EXPERIMENTAL VALIDATION OF PROPOSED TECHNIQUE

In this section, the experimental results on the discussion made in the previous sections is presented. The I–V characterization of the IGBT is carried out on the characterization setup, which is developed in the laboratory. By using the characterized IGBT, the hardware setup of H-bridge inverter is also developed in the laboratory. The proposed technique on updating the I–V characteristics of degraded IGBT and T_j estimation is implemented along with the inverter operation.

A. Calibration in Voltage and Current Measurement

In this article, v_{ce} and i_c of the DUT are measured by using the voltage measurement circuit (VMC) and current measurement circuit (CMC), as suggested in [30]. The measured voltage and current are sampled in the digital signal processor (DSP). An

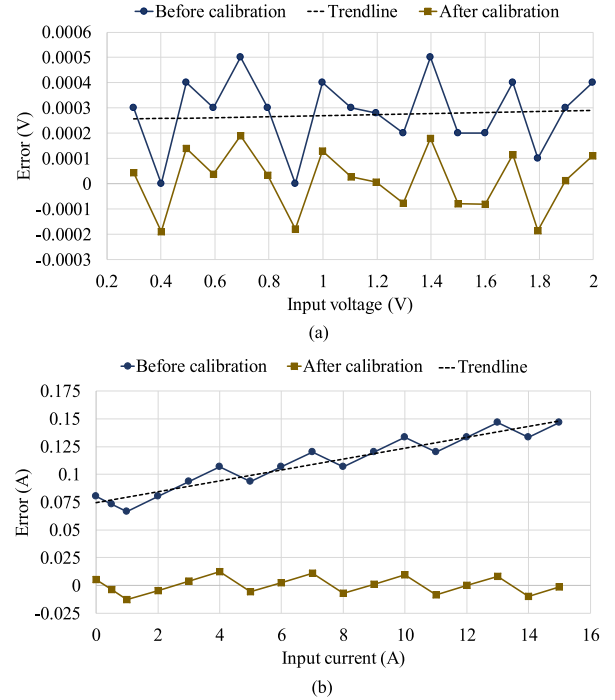


Fig. 7. Calibration in (a) voltage measurement and (b) current measurement.

experimentation is performed in order to obtain an error in sampling the voltage and current.

1) *Voltage Measurement Calibration*: For voltage, a regulated dc power supply is connected at the input of the VMC. During the operation of this setup, the derived input voltage in the DSP is compared with the true input voltage, which is obtained by using Fluke multimeter (model: 87 V). The error in sampling the voltage at different input voltage is shown in Fig. 7(a). The trend of the error is utilized in the calibration of v_{ce} measurement in real-time operation. The error in voltage measurement after calibration is also plotted in Fig. 7(a). It is observed that the error is below ± 0.2 mV.

2) *Current Measurement Calibration*: The current is swept (0 A to 15 A) through the Hall effect current sensor and is sampled in the DSP via scaling circuit. The derived current in DSP is compared with the true current, which is obtained by using Fluke multimeter (model: 87 V). The error in current measurement at different current is calculated, as shown in Fig. 7(b). The trend of the error is utilized in the calibration of CMC in its real time operation. The error in current measurement after the calibration is also plotted in Fig. 7(b). It is observed that the error is below 15 mA for different currents.

B. I–V Characterization of a Healthy IGBT

The characterization setup is developed in the laboratory, as discussed in [30]. By using the characterization setup, the HIVEC of IGBT (A1P25S12M3, 1200 V, 25 A) is obtained, as shown in Fig. 8. The value of $I_{c,\text{inf}}$ is 4.95 A. It is found that the value of α_o is 1.3 mV/ $^\circ\text{C}$. This validates the low sensitivity of v_{ce} with T_j in NTC region, as discussed in Section II-A. However,

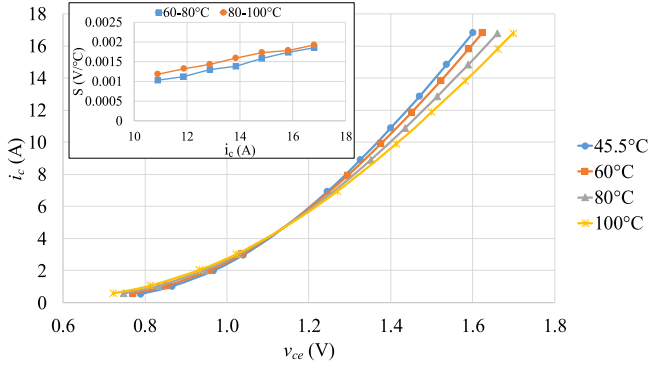


Fig. 8. HVIC of an IGBT (A1P25S12M3, 1200 V, 25 A). Inset shows sensitivity (S) at different collector currents.

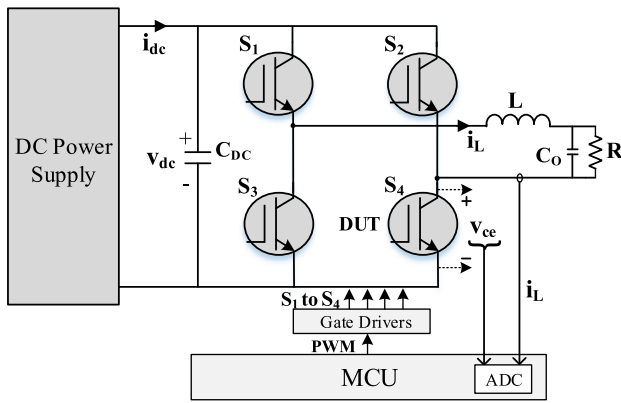


Fig. 9. Circuit diagram of H-bridge setup developed in laboratory.

TABLE II
LIST OF MAJOR COMPONENTS USED IN INVERTER SETUP

| Components | Specifications | Company |
|------------------|----------------------------|--------------------|
| DC Power Supply | (SGI: 600V/25A) | AMETEK |
| IGBT Module | 1200V, 25A | STMicroelectronics |
| MCU | TMS320F28379D | Texas Instruments |
| Gate Driver IC | FOD8316 | ON-Semiconductors |
| Inductor | $L = 3\text{mH}$ | — |
| Output Capacitor | $C_O = 3.3\mu\text{F}$ | — |
| DC Capacitor | $C_{DC} = 1000\mu\text{F}$ | — |
| Current Sensor | LA 25-P (25A) | LEM |

the sensitivity of v_{ce} with T_j is increased at higher collector currents in PTC region, as shown in inset Fig. 8. The value of I_c^* is chosen to be 14 A, above which the value of S is greater than $1.5\text{ mV}/^\circ\text{C}$.

C. Inverter Operation

The H-bridge inverter prototype is developed in the laboratory as per the circuit diagram shown in Fig. 9. The list of components used in the inverter setup is given in Table II. During the inverter operation, the waveforms of inductor current, DUT gate pulses and collector-emitter voltage of DUT are captured and shown in Fig. 10. The i_c of DUT is obtained by using the sensed inductor current (i_L) and the information of gate pulse to the DUT (S_{DUT}),

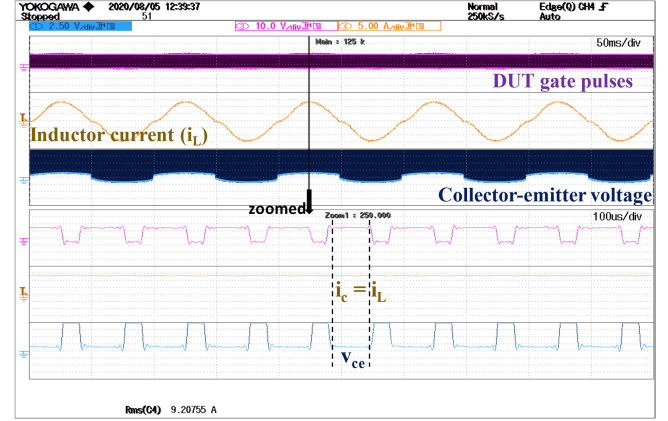


Fig. 10. Voltage and current waveforms during inverter operation (DUT gate pulse: 10 V/div , inductor current: 5 A/div , collector-emitter voltage: 2.5 V/div , time normal: 50 ms/div , time zoomed: $100\mu\text{s/div}$).

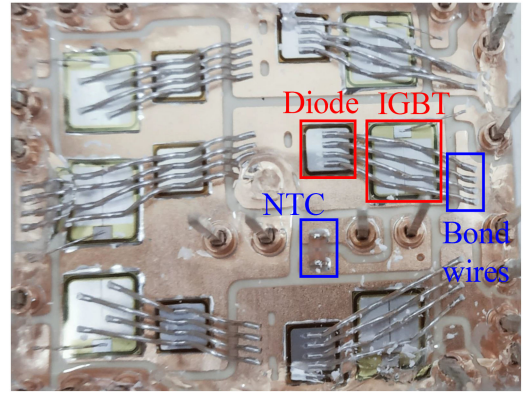


Fig. 11. Open IGBT (A1P25S12M3, 1200 V, 25 A) in the laboratory.

as given by

$$i_c = i_L \cdot S_{DUT} \quad \text{if } i_L \geq 0 \\ = 0 \quad \text{if } i_L < 0. \quad (21)$$

The value of i_c and corresponding v_{ce} are sampled in the DSP. The sampled voltage and currents are utilized in updating the I–V characteristics of the degraded DUT and the T_j estimation, as presented in the following section.

D. Updating I–V Characteristics of Degraded IGBT

In this section, the proposed technique of updating the I–V characteristics of degraded IGBT is implemented during operation of the inverter. The degradation of bond-wire is emulated by cutting the two out of four bond-wires manually of the open IGBT module (A1P25S12M3, 1200 V, 25 A), as shown in Fig. 11. During operation of the inverter with degraded IGBT, the value v_{ce} is measured when i_c equals to the $I_{c,inf}$. To ensure the sampling of v_{ce} at $I_{c,inf}$, i) the loading of inverter is maintained such that peak value of i_L is greater than $I_{c,inf}$, ii) the sampling frequency (f_s) of v_{ce} and i_c is kept much greater than the fundamental frequency (f_o), i.e., $f_s \gg f_o$. By using the sensed v_{ce} at $I_{c,inf}$ the value of ΔR_{con} is estimated by setting

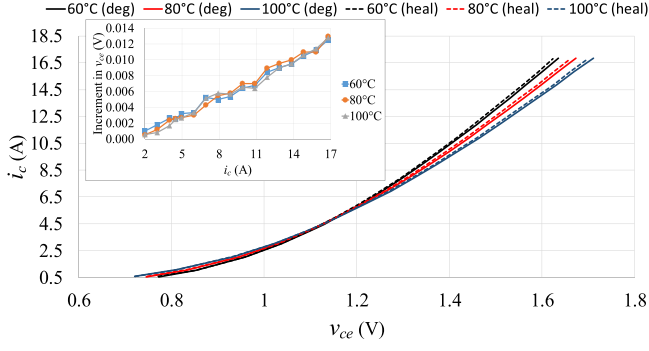


Fig. 12. Updating I–V characteristics by using proposed scheme. Inset shows increment in v_{ce} due to degradation at different collector currents. (Tolerance: voltage= ± 0.2 mV, current = ± 15 mA).

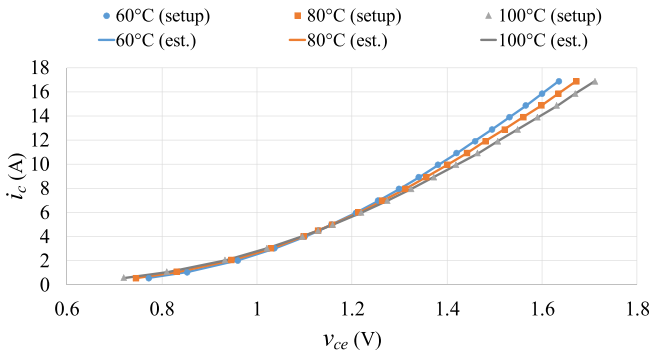


Fig. 13. Validation of estimated DIVC from characterization setup.

$\delta_r = 0.16$ m Ω . The estimated value of ΔR_{con} is found to be 0.65 m Ω . The value of ΔR_{con} is used in updating the HIVC to form DIVC, as shown in Fig. 12. It is observed that for a given temperature the shift in v_{ce} is large at higher values of i_c . The accuracy in DIVC of DUT, which is obtained from the proposed method is verified by using the characterization setup. The DIVC obtained from the proposed method and the characterization setup are shown in Fig. 13. It is observed that the I–V curves at different temperatures are almost overlapping with an average error of 0.3, 0.4, and 0.7 mV at T_j of 60°C, 80°C, and 100°C, respectively. This validates the assumption of neglecting effect of temperature on ΔR_{con} , as mentioned in Section II-A. The shift in $I_{c,inf}$ due to the degradation of IGBT is shown in Fig. 14(a). It is observed that the value of $\Delta I_{c,inf}$ is around 30 mA and the value of ϵ_r is 0.1 m Ω . The value of ϵ_r would introduce an error in v_{ce} ($i_c \cdot \epsilon_r$) when updating the I–V characteristics of the degraded IGBT (DIVC). Due to an error in v_{ce} , an error in T_j estimation, (ϵ_{T_j}) is given by

$$\epsilon_{T_j} = \frac{v_{ce}}{S_{i_c}} = \frac{i_c \cdot \epsilon_r}{S_{i_c}} \quad (22)$$

where S_{i_c} (V/ $^\circ$ C) is the sensitivity of v_{ce} with temperature at a particular i_c . By using (22), the value of ϵ_{T_j} is less than 1 $^\circ$ C.

The expected error in T_j estimation due shift in $I_{c,inf}$ is also evaluated for an IGBT with larger current rating (Infineon, FF75R12RT4, 1200 V, 75 A). From the HIVC, it is observed

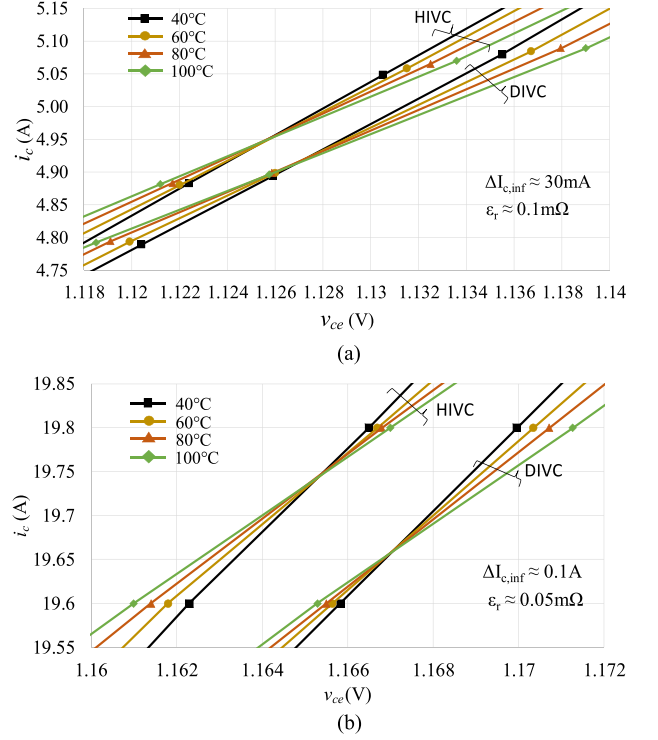


Fig. 14. Shift in $I_{c,inf}$ due to bond-wire degradation of IGBT. (a) With 25 A current rating (STMicroelectronics, A1P25S12M3). (a) with 75 A current rating (Infineon, FF75R12RT4).

that the current at inflection point is around 19.75 A, as shown in Fig. 14(b). The degradation of bond-wire is emulated by cutting the four out of eight bond-wires manually of the open IGBT module. From the DIVC, it is observed that the value of $\Delta I_{c,inf}$ is around 0.1 A and the value of ϵ_r is 0.05 m Ω . The expected value of ϵ_{T_j} is around 1 $^\circ$ C, which is similar for the IGBT of lower current rating (A1P25S12M3, 1200 V, and 25 A). Therefore, the proposed scheme would provide an estimated T_j with an accuracy of around 1 $^\circ$ C of the degraded IGBT, irrespective of the current rating.

E. T_j Estimation of an IGBT

The T_j of a healthy DUT is estimated within the power cycle of the inverter operation in steady state, as shown in Fig. 15. To validate the accuracy in methodology of T_j estimation, the in-built NTC thermistor of an IGBT is used, which is marked in Fig. 11. The difference between the T_j of DUT and NTC thermistor, ΔT_{j-NTC} is given by

$$\Delta T_{j-NTC} = Z_{th(DUT-NTC)} \cdot P_{DUT} \quad (23)$$

where $Z_{th(DUT-NTC)}$ is the thermal impedance between DUT and NTC thermistor and P_{DUT} is the power loss in the DUT [31]. When the device is healthy, the value of $Z_{th(DUT-NTC)}$ is almost constant. Therefore, the percentage increase in ΔT_{j-NTC} is same as the percentage increase in P_{DUT} . In the H-bridge inverter with unipolar PWM switching, all the IGBTs have equal electrical stresses and each IGBT contributes equally in the total power loss of the inverter (P_L). Therefore, the percentage increase in

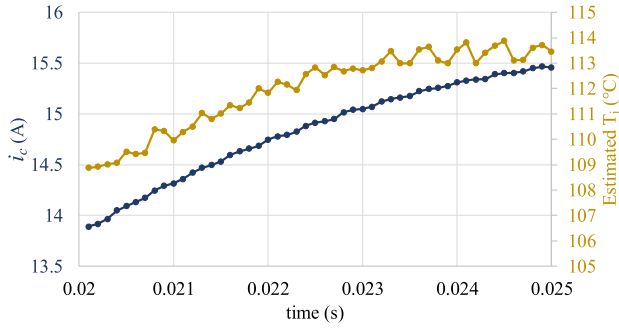


Fig. 15. Estimated T_j of the IGBT during inverter operation (inverter power loss, $P_L = 31.4$ W).

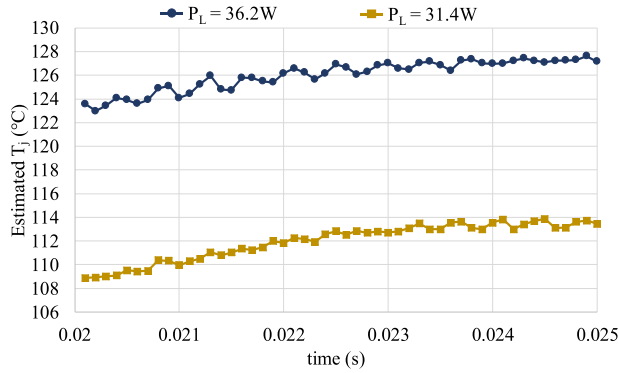
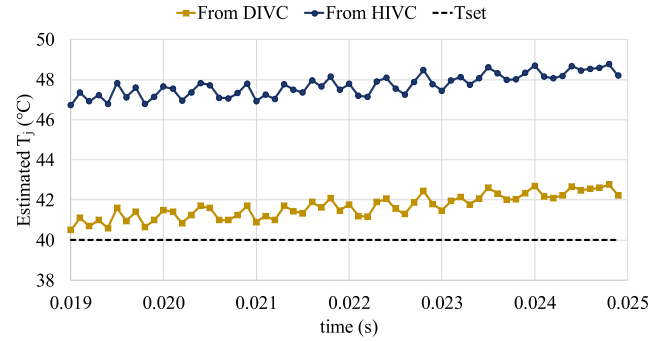


Fig. 16. Estimated T_j at different inverter power loss.

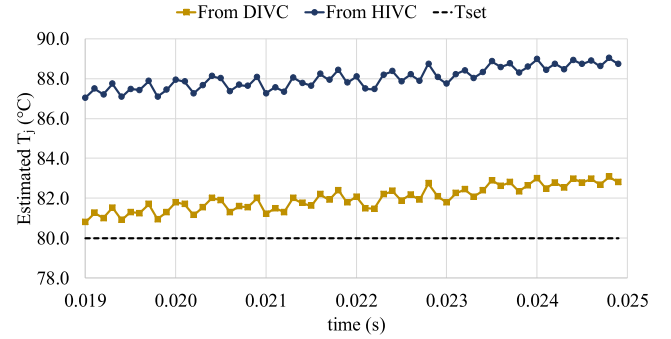
TABLE III
JUNCTION AND NTC TEMPERATURE AT DIFFERENT POWER LOSS

| P_L (W) | $T_{j,avg}$ ($^{\circ}C$) | T_{NTC} ($^{\circ}C$) | ΔT_{j-NTC} ($^{\circ}C$) |
|-----------|-----------------------------|---------------------------|------------------------------------|
| 31.4 | 112 | 79 | 33 |
| 36.2 | 126 | 88 | 38 |

the P_L is equals to the percentage increase in P_{DUT} and, hence, equals to the percentage increase in ΔT_{j-NTC} . The inverter is operated at two different power losses of the inverter. At each power loss the inverter is operated for a time till the NTC thermistor temperature is settled and then the T_j is estimated, as shown in Fig. 16. The average of estimated T_j ($T_{j,avg}$) and measured temperature of NTC thermistor (T_{NTC}) at different values of P_L are given in Table III. It is observed that the increase in ΔT_{j-NTC} is 15.15% due to the 15.2% increment in P_L . The fulfillment of necessary condition given in (23) implies the accuracy in methodology used in T_j estimation of the IGBT. To further validate the accuracy of the proposed scheme, the H-bridge inverter is assembled containing the degraded DUT (A1P25S12M3, 1200 V, 25 A), with cutoff two bond-wires. When the inverter is not under operation, it is kept in the temperature controlled chamber (TCC) for a long duration. This ensures that the T_j of the DUT becomes equal to the set temperature of the TCC (T_{set}). Then, the operation of the inverter is started. The i_c and v_{ce} of the degraded DUT are measured in the first power cycle from the start of the inverter operation. This avoids self-heating of the DUT. The measured values of i_c and v_{ce}



(a)



(b)

Fig. 17. Estimated T_j of degraded IGBT by using HIVC and DIVC (inverter power loss, $P_L = 40$ W). (a) At $T_{set} = 40^{\circ}C$. (b) At $T_{set} = 80^{\circ}C$.

TABLE IV
ESTIMATED T_j USING HIVC AND PROPOSED METHOD

| T_{set} ($^{\circ}C$) | Estimated T_j ($^{\circ}C$) | |
|---------------------------|---------------------------------|-----------------|
| | HIVC | proposed method |
| 20 | 27.8 | 21.5 |
| 40 | 47.2 | 41.0 |
| 60 | 67.8 | 61.5 |
| 80 | 87.4 | 81.3 |

are used in estimating the T_j by using the HIVC as well as DIVC, as shown in Fig. 17. It is observed that the estimated T_j by using DIVC is close to T_{set} at the starting of the inverter operation, with an error of around $1^{\circ}C$ and $1.3^{\circ}C$ for T_{set} equals to $40^{\circ}C$ and $80^{\circ}C$, respectively. If the T_j is estimated by using the HIVC, error is around $7.2^{\circ}C$ and $7.4^{\circ}C$ for T_{set} equal to $40^{\circ}C$ and $80^{\circ}C$, respectively. The estimated T_j by using HIVC and proposed method at different values of T_{set} is given in Table IV. It is found that there is substantial increment in accuracy of estimated T_j by using the DIVC. This accuracy is important in the condition monitoring applications and other temperature critical applications, as discussed in Section I.

V. CONCLUSION

This article presented a technique for an accurate T_j estimation of the IGBT, irrespective of its extent of ageing. The important findings of this article are listed as follows.

- 1) The HVC of IGBT changes due to bond-wire degradation. Therefore, it is required to update the DIVC for an accurate T_j estimation.
- 2) In the proposed technique, real-time estimation of ΔR_{con} at $I_{c,inf}$ of HVC is utilized in updating DIVC. A mathematical analysis of the proposed technique is also presented. It is derived that for a bond-wire degraded IGBT, the shift in $I_{c,inf}$ and error in estimation of ΔR_{con} are small. Thus, the proposed technique provides a good accuracy in T_j estimation of the IGBT.
- 3) The proposed scheme is validated during real-time operation of the H-bridge inverter. The shift in $I_{c,inf}$ is found to be around 0.6% for the degraded IGBT.
- 4) Due to small shift in $I_{c,inf}$, an error in estimation of ΔR_{con} (ϵ_r) is observed to be around 15% for a variation in T_j of 60°C. Due to this, the expected error in T_j estimation is within 1°C.
- 5) The information of real-time ΔR_{con} of the degraded IGBT could be utilized for its condition monitoring.

REFERENCES

- [1] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.
- [2] U. Choi, F. Blaabjerg, and K. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015.
- [3] U. M. Choi, F. Blaabjerg, S. Munk-Nielsen, S. Jorgensen, and B. Rannestad, "Reliability improvement of power converters by means of condition monitoring of IGBT modules," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7990–7997, Oct. 2017.
- [4] A. Singh, A. Anurag, and S. Anand, "Evaluation of VCE at inflection point for monitoring bond wire degradation in discrete packaged IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2481–2484, Apr. 2017.
- [5] P. Sun, C. Gong, X. Du, Y. Peng, B. Wang, and L. Zhou, "Condition monitoring IGBT module bond wires fatigue using short-circuit current identification," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3777–3786, May 2017.
- [6] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.
- [7] B. Ji *et al.* "In situ diagnostics and prognostics of solder fatigue in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1535–1543, Mar. 2015.
- [8] Z. Hu, M. Du, and K. Wei, "Online calculation of the increase in thermal resistance caused by solder fatigue for IGBT modules," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 785–794, Dec. 2017.
- [9] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 17–27, Sep. 2014.
- [10] D. Murdock, J. Torres, J. Connors, and R. Lorenz, "Active thermal control of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 552–558, Mar./Apr. 2006.
- [11] M. N. Marwali, J. W. Jung, and A. Keyhani, "Control of distributed generation systems- part II: Load sharing control," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1551–1561, Nov. 2004.
- [12] K. Ma, M. Liserre, and F. Blaabjerg, "Reactive power influence on the thermal cycling of multi- MW wind power inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 922–930, Mar./Apr. 2013.
- [13] J. Chen *et al.*, "A smart IGBT gate driver IC with temperature compensated collector current sensing," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4613–4627, May 2019.
- [14] M. Du, Y. Tang, M. Gao, Z. Ouyang, K. Wei, and W. G. Hurley, "Online estimation of the junction temperature based on the gate pre-threshold voltage in high-power IGBT modules," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 3, pp. 501–508, Sep. 2019.
- [15] E. R. Motto and J. F. Donlon, "IGBT module with user accessible on-chip current and temperature sensors," in Proc. Appl. Power Electron. Conf. Expo., Orlando, FL, USA, Feb. 5–9, 2012, pp. 176–181.
- [16] Z. Wang and W. Qiao, "A physics-based improved cauer-type thermal equivalent circuit for IGBT modules," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6781–6786, Oct. 2016.
- [17] T. K. Gachovska, B. Tian, J. L. Hudgins, W. Qiao, and J. F. Donlon, "A real-time thermal model for monitoring of power semiconductor devices," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3361–3367, Jul./Aug. 2015.
- [18] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3306–3314, Jul./Aug. 2016.
- [19] A. S. Bahman, K. Ma, and F. Blaabjerg, "A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.
- [20] Z. Xu, F. Xu, and F. Wang, "Junction temperature measurement of IGBTs using short-circuit current as a temperature-sensitive electrical parameter for converter prototype evaluation," *IEEE Trans. Ind. Appl.*, vol. 62, no. 6, pp. 3419–3429, Jun. 2015.
- [21] D. W. Brown and M. Abbas, "Turn-off time as an early indicator of insulated gate bipolar transistor latch-up," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 479–489, Feb. 2012.
- [22] Y. Peng and L. Zhou, "Junction temperature estimation of IGBT module via a bond wires lift-off independent parameter V_{gE-Np} ," *IET Power Electron.*, vol. 11, no. 2, pp. 320–328, Feb. 2017.
- [23] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3784–3793, May 2016.
- [24] U. M. Choi, F. Blaabjerg, F. Iannuzzo, and S. Jorgensen, "Junction temperature estimation method for a 600 V, 30 A IGBT module during converter operation," *Microelectron. Rel.*, vol. 55, no. 9–10, pp. 2022–2026, 2015.
- [25] B. Jayant Baliga, *Fundamental of power semiconductor devices*. New York, NY, USA: Springer, 2008, pp. 776–777.
- [26] *STMicroelectronics Application Note AN604*. Accessed: Jan. 15, 2021. [Online]. Available: https://www.st.com/resource/en/application_note/cd00003894-calculation-of-conduction-losses-in-a-power-rectifier-stmicroelectronics.pdf
- [27] *International Rectifier Power MOSFET Basics*. Accessed: Jan. 15, 2021. [Online]. Available: <https://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f>
- [28] T. Laska, M. Munzer, F. Pfirsich, C. Schaeffer, and T. Schmidt, "The field stop IGBT (FS IGBT). A new power device concept with a great improvement potential," in Proc. 12th Int. Symp. Power Semicond. Devices ICs, Toulouse, France, 2000, pp. 355–358.
- [29] R. Perret, *Power Electronics Semiconductor Devices*. Hoboken, NJ, USA: Wiley, Mar. 2013, pp. 94–95.
- [30] A. Arya, P. Kumar, and S. Anand, "Methodology of an accurate static I-V characterization of power semiconductor devices," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7703–7715, Oct. 2020.
- [31] P. Liu, C. Chen, X. Zhang, and S. Huang, "Online junction temperature estimation method for SiC modules with built-in NTC sensor," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 94–99, Mar. 2019.



Abhinav Arya (Student Member, IEEE) received the B.Tech. degree in electrical and electronics from Babu Banarasi Das National Institute of Technology and Management, Lucknow, India, in 2012, and the M.Tech. degree in power and control in 2015 from the Indian Institute of Technology Kanpur, Kanpur, India, where he is currently working toward the Ph.D. degree with the Department of Electrical Engineering.

He was with Mahindra and Mahindra Ltd., Chennai, India. His research interests include fault diagnostics and condition monitoring of power elec-

tronic converters used in renewable energy systems.



Abhishek Chanekar (Student Member, IEEE) received the B.Tech. degree in electrical engineering from Walchand College of Engineering Sangli, Sangli, India, in 2014, and the M.Tech. degree in power electronics and drives from the Visvesvaraya National Institute of Technology Nagpur, Nagpur, India, in 2017. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, India.

His research interests include reliability analysis and active thermal control of power semiconductor devices.



Amit Verma (Member, IEEE) received the Integrated M.Tech. degree in engineering physics from Indian Institute of Technology (BHU), Varanasi, India, in 2010, and the Ph.D. degree in electrical engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2015.

After working as a Postdoc with Cornell University, USA, he joined the Indian Institute of Technology Kanpur, Kanpur, India, where he is currently an Assistant Professor with the Department of Electrical Engineering. His research interests include fabrication, characterization, and modeling of semiconductor devices based on wide-bandgap semiconductors and phase-change materials.



Pratik Deshmukh received the B.Tech. degree in electrical engineering from the Walchand College of Engineering Sangli, Sangli, India, in 2015, and the M.Tech degree in power engineering from the Indian Institute of Technology Kanpur, Kanpur, India, in 2018.

He is currently with the Intel Technology India Pvt., Ltd., Bengaluru, India, as an SoC Design Engineer. His research interest includes condition monitoring of power semiconductor devices.



Sandeep Anand (Senior Member, IEEE) received the B.Tech. and Ph.D. degrees in electrical engineering from the Indian Institute of Technology Bombay, Mumbai, India, in 2007 and 2013, respectively.

He was previously with Emerson Network Power, Mumbai, and Cosmic Circuits Pvt., Ltd., Bengaluru, India. From 2013 to 2020, he was an Assistant Professor with the Indian Institute of Technology Kanpur, Kanpur, India. He is currently an Associate Professor with the Indian Institute of Technology, Bombay, India. His research interests include reliability of power electronic circuits, gallium nitride based converters, and control of converters interfacing alternate sources of energy.