A New Dead Time Regulation Synchronous Rectification Control Method for High Efficiency *LLC* Resonant Converters

SangCheol Moon, *Member, IEEE*, ChengSung Chen, *Member, IEEE*, and Ren-Jye Wang, *Member, IEEE*

***Abstract*—In low output voltage and high output current *LLC* resonant converter applications, a synchronous rectification (SR) is essential component for high efficiency and high power density. However, stray inductances in MOSFET package and printed circuit board (PCB) pattern make premature turn-OFF of SR gate and large SR dead time. To compensate the stray inductance effect and increase system efficiency, a hysteresis band dead time regulation control method is proposed. In the proposed control method, SR dead time is regulated to predetermined dead time target regardless of the stray inductances by using a mixed signal, which includes instantaneous drain voltage information and previous cycle dead time information. As a result, the proposed control method can provide lower conduction losses by the dead time regulation and better transient characteristic by the instantaneous drain voltage information. To verify the validity of the proposed control method, 234-W prototype is built and experimented with the proposed controller, which is implemented with 0.25-μm BCDMOS technology.**

***Index Terms*—*LLC* resonant converter, synchronous rectification.**

I. Introduction

AMONG many resonant type converters, an *LLC* resonant converter has been the most popular topology and there are many recent studies [1]–[7] since this topology has many advantages over other resonant type topologies; it can regulate the output over entire load condition with a relatively small switching frequency variation, it can achieve zero-voltage switching (ZVS) for the primary-side switches and zero-current switching for the secondary-side rectifiers. In the *LLC* resonant converter, rectifier diodes are typically used to obtain dc output voltage from the secondary-side winding of a transformer. However, the conduction loss of the diode rectifier contributes significantly to the overall power losses in the *LLC* resonant converter; especially in low-voltage and high-output current applications, because the conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the average current. In addition, a large size heatsink may be required to avoid thermal issue of the diode rectifier. On the other hand, in a synchronous rectification (SR), which replaces the rectifier diodes as MOSFETs with a small ON-resistance r_{DS_ON}, the forward-voltage drop of the synchronous rectifier is much lower than that of the diode rectifier so that the rectifier conduction loss is dramatically reduced. Consequently, the heatsink size for the rectifier can be minimized and higher power density can be achieved.

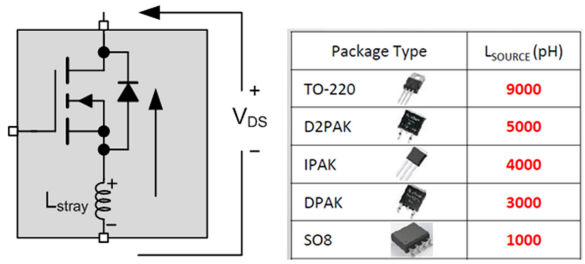

Fig. 1. Stray inductance of MOSFET package.

In the conventional SR control method, instantaneous drain-source voltage sensing type [8]–[10] is the most practical and widely used due to simplicity. In the SR MOSFET, an SR body diode conducts first as normal diode rectifier. After SR gate is turned ON, the drain-source voltage is determined by the product of r_{DS_ON} and instantaneous SR current. As SR current decreases to zero, the drain-source voltage V_{DS} also approaches zero. When V_{DS} reaches the turn-OFF threshold voltage, SR gate is turned OFF. If the turn-OFF threshold is set as close as possible to zero, the turn-OFF dead time can be minimized in this control method.

However, in the practical power supply system, the stray inductances of MOSFET package and printed circuit board (PCB) pattern prevent exact drain-source voltage sensing while SR is turning ON. The typical stray inductance of the MOSFET packages are summarized in Fig. 1 and the stray inductance effect is described in Figs. 2 and 3. If there is no stray inductance, V_{DS} becomes negative phase sine-wave, which follows SR current shape while SR gate is turning ON in Fig. 2. However, in a practical MOSFET having the stray inductance as shown in Fig. 3, the offset voltage $v_{LS}(t)$ is induced by

$$v_{LS}(t) = -L_{\mathrm{Stray}} \times \frac{di_{\mathrm{SR}}}{dt} \tag{1}$$

Manuscript received October 11, 2020; revised December 29, 2020; accepted February 9, 2021. Date of publication February 22, 2021; date of current version June 1, 2021. This paper was presented in part at the Applied Power Electronics Conference and Exposition, Anaheim Convention Center, Anaheim, CA, USA, Mar. 17–21, 2019. Recommended for publication by Associate Editor X. Wu. *(Corresponding author: SangCheol Moon.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3060793.

Digital Object Identifier 10.1109/TPEL.2021.3060793

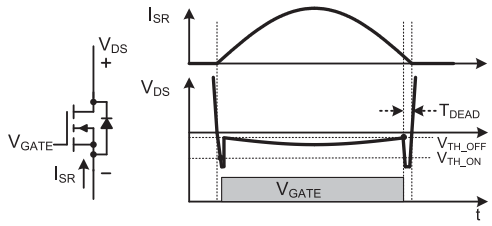

Fig. 2. SR current and gate waveform without $L_{\rm stray}$.

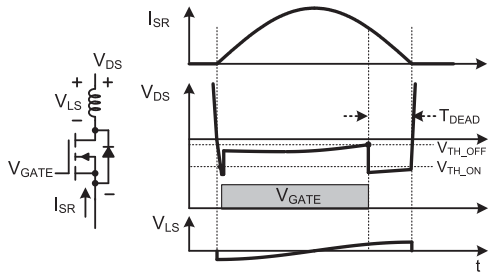

Fig. 3. SR current and gate waveform with $L_{\rm stray}$.

across the stray inductance. The induced voltage makes drain-source sensing voltage of MOSFET higher than the product of $r_{DS\_\,\rm ON}$ and instantaneous SR current, when SR current decreases. It results in premature turn-OFF of SR gate and large body diode conduction time $T_{\rm DEAD}$, as shown in Fig. 3. As a result, the conduction loss increases.

To overcome the stray inductance effect and increase SR conduction time, a capacitive network circuit is presented in [11]. In the study, the time delay circuit is designed to cancel the inductive voltage offset. However, the induced voltage v_{LS} is varied with the output load condition, and $r_{DS\_\rm ON}$ of SR MOSFET can be selected by the power system specifications. Hence, optimal design of the capacitive network is difficult. In a similar study [12], a zero-crossing noise filter scheme is introduced. The method is simplified from [11] and effective for heavy load condition. But, in the light load condition, it may lead to late turn-OFF and inversion current due to the time delay.

In other research, a digitally implemented adaptive control methods [13]–[18] are proposed. In the control scheme, the SR gate turn-ON is synchronized with the primary-side gate signal with small delay, so that additional galvanic isolation devices are required. When SR is turned OFF, the control scheme detects the body diode conduction, and the digital controller would increase or decrease the SR conduction time in the next switching cycle. In the steady state, the controller will jitter between two conditions of SR conduction with the body diode and without the body diode. It may induce large dead time variation in the steady state. In addition, when the operating frequency increases, if SR turn-ON stays the condition without the body diode conduction, the adaptive ON-time control cannot reduce SR gate pulse width properly. In that case, the SR inversion current makes huge drain voltage spike to occur, because the adaptive turn-OFF control scheme is only based on the body diode detection signal in the previous cycle to compensate the stray inductance effect. In the commercialized IC, the work in [19]–[21] utilize the adaptive control method.

In another type of SR controller, the work in [22]–[24] adopt a drain voltage regulation control method, which regulates the drain sensing voltage by lowering a gate driving voltage at around SR turn-OFF. It can prolong gate turn-OFF instant when compared to the control method of [8]–[10]. However, the SR MOSFET cannot be fully turned ON and has a higher $R_{DS\_\rm ON}$ due to lower gate voltage during drain regulation. Therefore, it cannot minimize the conduction loss with the stray inductance in high output current applications.

In alternative approaches, a dual-edge tracking control method [25], a self-driven gate driver [26], a resonant capacitor voltage method [27], and a prediction method [28] are proposed. Choi [25] used rising edge and falling edge of the only one channel drain sensing voltage and the primary-side gate signal information to generate two channel SR gate signals. However, one channel drain sensing voltage cannot represent both channel information properly, which makes the drain edge detection difficult.

Another publication [26] proposes a self-driven gate driver with auxiliary passive components. Those create another resonant tank to extract the fundamental signal of the drain sensing voltage with a 180° out of phase for the SR gate driver. However, sinusoidal SR gate signal may increase $r_{DS\_\rm ON}$ of SR MOSFET at around turn ON and turn OFF.

In [27], an SR driving strategy based on the resonant capacitor voltage V_{Cr} is presented. Since V_{Cr} is a large signal, this method has higher noise immunity compared to the drain sensing method and provides accurate turn-OFF SR gate signal to maximized efficiency. However, the method requires input and output voltage information of the *LLC* resonant converter, as well as V_{Cr}. In addition, the SR conduction time error will increase under light load condition.

In [28], according to the body diode conduction time of the previous cycle, a reference voltage is increased or decreased. Then, the reference voltage is compared with an internal ramp signal to determine the SR gate pulsewidth. Since this method uses only the previous cycle information and has only single feedback loop like the voltage mode control of the feedback theory, a transient performance is not good. Especially, this method may induce an inversion current in the frequency controlled converters such as *LLC* resonant converter.

To overcome the disadvantages of the previous works and maximize the SR turn-ON time without the SR inversion current, this article proposes an advanced dead time regulation control method.

II. Analysis of the Proposed Dead Time Regulation Control Method

A. System Block Diagram

Fig. 4 shows the system block diagram of the proposed control method. For easy explanation, *LLC* control and GATE2 control blocks are depicted as a simple rectangular block. The SR gate turn-ON method is the same as the conventional control method. Simply, a drain sensing voltage V_{D1} is compared with a turn-ON

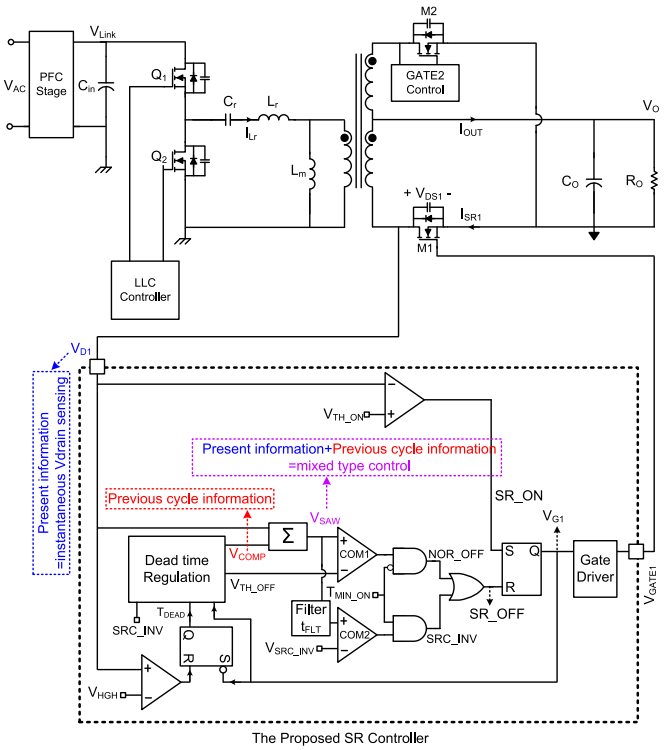

Fig. 4. System block diagram of the proposed control method.

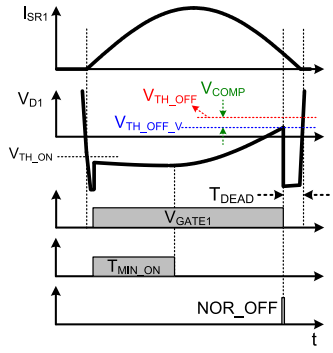

Fig. 5. SR gate turn-OFF by normal turn-OFF signal.

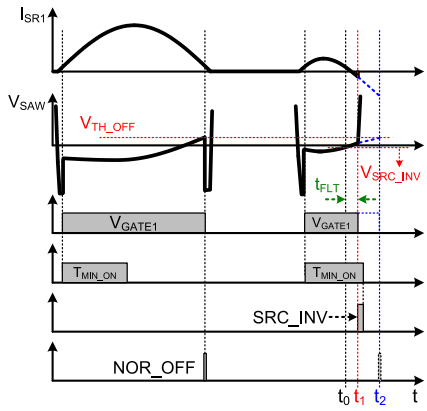

Fig. 6. SR gate turn-OFF by current inversion detection signal.

threshold voltage V_{TH_ON}. As V_{D1} is lower than V_{TH_ON} by body diode conduction of *M1*, a gate driver's output V_{GATE1} becomes high and SR gate is turned ON. However, unlike the conventional control, there are two methods to turn-OFF SR gate. First, in a normal switching cycle, a mixed signal V_{SAW} is compared with a turn-OFF threshold voltage V_{TH_OFF} in a comparator COM1. When V_{SAW} is higher than V_{TH_OFF}, COM1 outputs high. The condition is given by

$$V_{\mathrm{SAW}} = V_{D1} + V_{\mathrm{COMP}} \geq V_{TH\_OFF}. \tag{2}$$

In V_{SAW}, the drain sensing voltage V_{D1}, which has instantaneous drain voltage information, is combined with the compensation voltage V_{COMP}, which is determined by previous cycle dead time information to compensate the stray inductances in a dead time regulation block. Rearranging (2) with respect to V_{D1}, COM1 is high, when V_{D1} is higher than a virtual turn-OFF threshold voltage $V_{TH\_OFF\_V}$ as follows:

$$V_{D1} \geq V_{TH\_OFF} - V_{\mathrm{COMP}} = V_{TH\_OFF\_V}. \tag{3}$$

Then, a normal turn-OFF signal *NOR*_OFF determines gate turn-OFF after a minimum ON-time signal $T_{\mathrm{MIN\_ON}}$ goes low. $T_{\mathrm{MIN\_ON}}$ can be a 0%–50% time of the previous cycle SR conduction time and it is used for preventing turn-OFF mistrigger by drain sensing noise. Fig. 5 shows key waveforms of the normal gate turn-OFF.

In the other gate turn-OFF method by a comparator COM2, when SR inversion current occurs during fast load transient from heavy load to light load condition, as shown in Fig. 6, V_{SAW} can be higher than a current inversion detection threshold voltage $V_{\mathrm{SRC\_INV}}$ at t_0 for a filter time t_{FLT}. If this event happens during high of $T_{\mathrm{MIN\_ON}}$, a current inversion detection signal SRC_INV becomes high at t_1 and it turns OFF SR gate immediately. Unless *SRC_INV* turns OFF at t_1, SR gate will be turned OFF at t_2 by *NOR*_OFF. It will induce large inversion current and huge drain spike. Therefore, the second turn-OFF method helps reducing inversion current during the load transient.

As explained, the proposed control method utilizes V_{SAW} signal, which has both V_{D1} of instantaneous drain voltage information and V_{COMP} of previous cycle dead time information, to turn-OFF SR gate. As a result, the proposed control method can provide lower conduction losses by the stray inductance compensation and better transient characteristic by the current inversion detection.

B. Hysteresis Band Dead Time Regulation Control

In the SR control, minimized SR dead time and the body diode conduction time are required to maximize the system efficiency. However, very small dead time may increase the possibility of the inversion current during transient condition. To optimize the dead time, a hysteresis band dead time regulation control is proposed in this section.

In the dead time regulation block, V_{COMP} is generated based on previous cycle SR dead time T_{DEAD}, which is measured from V_{GATE1} falling edge to where V_{D1} is higher than a drain high threshold voltage V_{HGH}. In the hysteresis band dead time

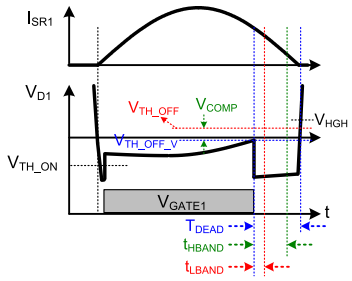

Fig. 7. $T_{\mathrm{DEAD}} > t_{\mathrm{HBAND}}$.

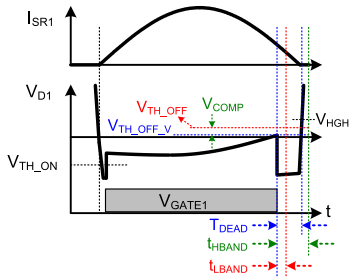

Fig. 8. $t_{\mathrm{LBAND}} < T_{\mathrm{DEAD}} < t_{\mathrm{HBAND}}$.

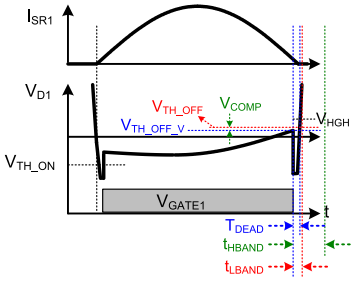

Fig. 9. $T_{\mathrm{DEAD}} < t_{\mathrm{LBAND}}$.

regulation control, there are two dead time targets: a dead time lower band t_{LBAND} and a dead time upper band t_{HBAND}. If the dead time is larger than the upper band t_{HBAND}, as shown in Fig. 7, the virtual turn-OFF threshold voltage $V_{TH\_\mathrm{OFF}\_V}$ is increased by decreasing V_{COMP} in the next switching cycle to reduce T_{DEAD}. After several switching cycles are repeated, if T_{DEAD} is between t_{LBAND} and t_{HBAND}, as described in Fig. 8, the dead time regulation control is paused. Then, $V_{TH\_\mathrm{OFF}\_V}$ is kept until T_{DEAD} is out of the bands.

In another load condition, if the dead time T_{DEAD} is smaller than t_{LBAND} in Fig. 9, $V_{TH\_\mathrm{OFF}\_V}$ is decreased by increasing V_{COMP} in the next switching cycle to enlarge T_{DEAD}. As a result, T_{DEAD} is always placed between t_{LBAND} and t_{HBAND} in the steady state. By this regulation algorithm, the proposed control method provides optimal SR dead time. If V_{COMP} has saturated to a maximum value $V_{\mathrm{COMP\_MAX}}$ or a minimum value $V_{\mathrm{COMP\_MIN}}$, V_{TH_OFF} changes one step-up or one step-down in accordance with the V_{COMP} saturation level. In the dead time regulation block, V_{COMP} is for fine tuning of T_{DEAD} and V_{TH_OFF} is used for the coarse dead time control.

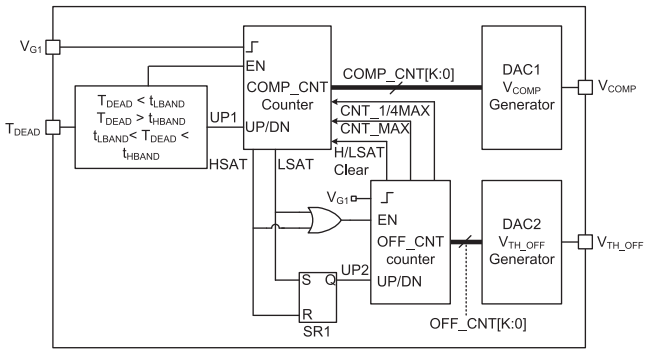

Fig. 10. Hysteresis band dead time regulation control block.

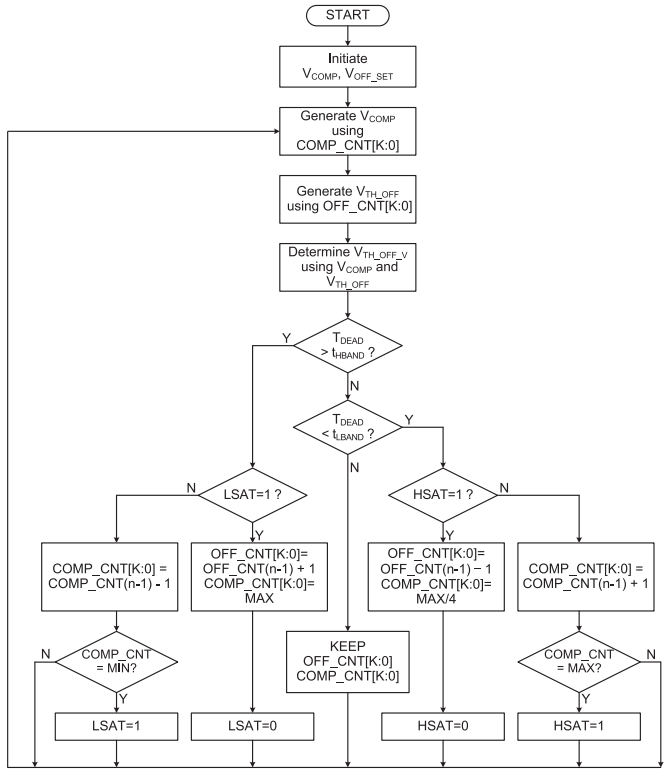

Fig. 11. Proposed dead time regulation algorithm.

Figs. 10 and 11 illustrate the proposed hysteresis band dead time regulation block and the control algorithm, respectively. When the control algorithm starts, V_{COMP} and V_{TH_OFF} are initiated with maximum value and minimum value, respectively, which provide the lowest value of $V_{TH\_\mathrm{OFF}\_V}$ for the dead time soft-start. If T_{DEAD} is larger than t_{HBAND}, up/down flag *UP1* of a COMP_*CNT* counter, which outputs a digital value COMP_*CNT[K:0]* corresponding to V_{COMP}, becomes low. So, the counter is set as a down counter. Then, if the counter is not saturated by minimum value, which means *LSAT* is low, COMP_*CNT* is updated by

$$\mathrm{COMP}\_CNT(n) = \mathrm{COMP}\_CNT(n-1) - 1 \qquad (4)$$

at next rising edge of V_{G1}, which is a logic level signal of V_{GATE1}. Then, the counter checks updated COMP_*CNT* whether it is minimum value or not. Thereby, a digital to analog converter DAC1 generates V_{COMP} according to COMP_*CNT[K:0]*. On the other hand, if *LSAT* is high in previous cycle and *UP1* is low, SR latch *SR1* is set and a OFF_*CNT* counter, which generates a digital value of V_{TH_OFF}, is enabled. Then, up/down flag *UP2* becomes high and the counter is set as a up counter. As a result, OFF_*CNT* is updated by

$$\mathrm{OFF}\_CNT(n) = \mathrm{OFF}\_CNT(n-1) + 1. \tag{5}$$

At the same time, the counter sends a LSAT clear signal and a counter max signal *CNT_MAX* to COMP_*CNT*. Finally, a digital to analog converter DAC2 increases V_{TH_OFF} to make virtual turn-OFF threshold voltage $V_{TH\_\mathrm{OFF}\_V}$ increase and dead time decrease.

On the other hand, if T_{DEAD} is smaller t_{LBAND}, the up/down flag *UP1* of the COMP_*CNT* counter is set to high. Then, if the counter has not maximum saturation level, which means HSAT is low, COMP_*CNT* is increased at next rising edge of V_{G1} by

$$\mathrm{COMP}\_CNT(n) = \mathrm{COMP}\_CNT(n-1) + 1. \tag{6}$$

After then, updated COMP_*CNT* is compared with maximum value. Finally, V_{COMP} is increased by the digital to analog converter DAC1. If HSAT is high in the previous cycle and *UP1* is high, SR latch *SR1* is reset. Then, the up/down flag *UP2* of the OFF_*CNT* counter goes low and the counter is set as a down counter and OFF_*CNT* is calculated by

$$\mathrm{OFF}\_CNT(n) = \mathrm{OFF}\_CNT(n-1) - 1. \tag{7}$$

At a result, V_{TH_OFF} changes one step down, and the counter sends a HSAT clear signal and a COMP_*CNT* counter one fourth signal *CNT_1/*4MAX. It decreases virtual turn-OFF threshold voltage $V_{TH\_\mathrm{OFF}\_V}$ and increases dead time.

In the steady state, the proposed control method provides the optimized dead time between t_{LBAND} and t_{HBAND} regardless of the stray inductance. In the condition, the COMP_*CNT* counter and the OFF_*CNT* counter are both disabled and the counters keep previous cycle value to minimize the dead time variation. It lowers the conduction loss of SR MOSFET so that the proposed control method can achieve higher efficiency when compared to the conventional control method.

Fig. 12 shows simulation result of V_{COMP}, V_{TH_OFF}, and $V_{TH\_\mathrm{OFF}\_V}$ transition under soft load changing. When the output load is increased at t_0, the induced offset voltage $v_{LS}(t)$ by stray inductance of SR MOSFET is also increased due to steep I_{SR1} slope. It leads SR dead time T_{DEAD} increases. Therefore, the proposed control algorithm operates with (4) and (5) during t_0–t_2. When V_{COMP} has minimum value and LSAT becomes high at t_1, V_{TH_OFF} is increased by one step and V_{COMP} is reset to maximum value. If T_{DEAD} is regulated between t_{LBAND} and t_{HBAND}, the proposed control method keeps V_{COMP} and V_{TH_OFF} during t_2–t_3. As the output load is decreased at t_3, the dead time is reduced below t_{LBAND} by lower I_{SR1}. Then, V_{COMP} and V_{TH_OFF} is controlled by (6) and (7). When V_{COMP} becomes maximum value and HSAT is high at t_4, V_{TH_OFF} is decreased by one step and V_{COMP} is set to 1/4 of the maximum value.

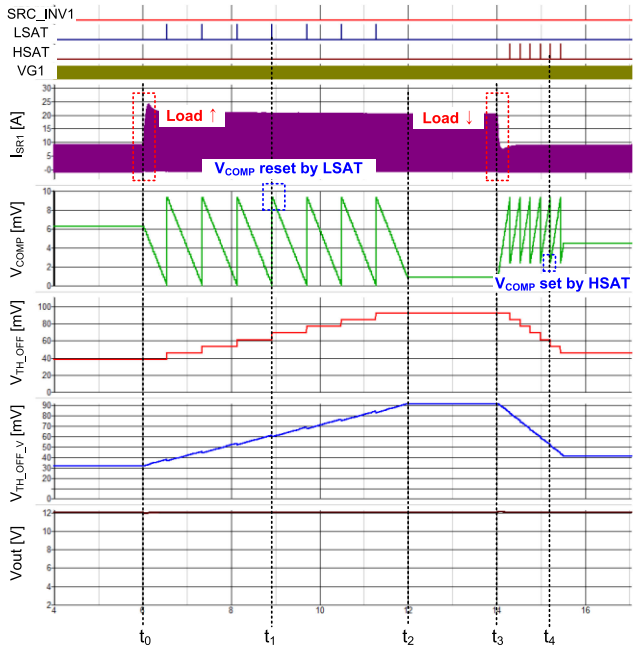

Fig. 12. Simulation results of V_{COMP} and V_{TH_OFF} variation, while soft the output load change.

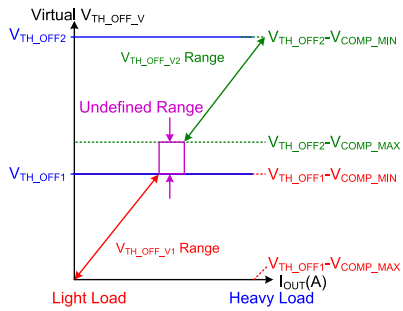

Fig. 13. Virtual $V_{TH\_\mathrm{OFF}\_V}$ range with small $V_{\mathrm{COMP\_STEP}}$.

III. Design Considerations

In this section, the compensation voltage step size design, the virtual turn-OFF threshold voltage trajectory, the current inversion detection, and the light load operation are discussed for proper implementation of the proposed hysteresis band dead time regulation control method.

A. Compensation Voltage V_{COMP} Step Size Design

In the proposed control method, V_{COMP} step size $V_{\mathrm{COMP\_STEP}}$ should be properly selected for stable V_{TH_OFF} transition. If small $V_{\mathrm{COMP\_STEP}}$ is designed, it is good for the dead time fine tuning. However, it brings narrow $V_{TH\_\mathrm{OFF}\_V}$ range. It results in undefined $V_{TH\_\mathrm{OFF}\_V}$ range between two consecutive V_{TH_OFF} levels, as shown in Fig. 13. When the output load moves to the undefined range, T_{DEAD} can jump from the state of $T_{\mathrm{DEAD}} > t_{\mathrm{HBAND}}$ to the state of $T_{\mathrm{DEAD}} < t_{\mathrm{LBAND}}$ without the state of $t_{\mathrm{LBAND}} < T_{\mathrm{DEAD}} < t_{\mathrm{HBAND}}$. Then, the proposed control method repeats V_{TH_OFF} step-up and V_{TH_OFF} step-down to regulate SR dead time. It may induce

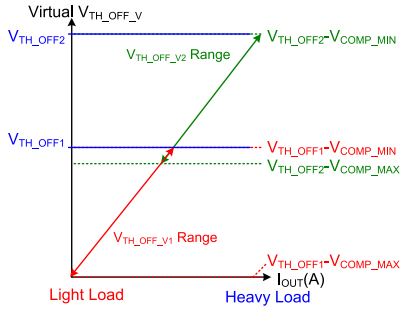

Fig. 14. Virtual $V_{TH\_OFF\_V}$ range with large $V_{\mathrm{COMP\_STEP}}$.

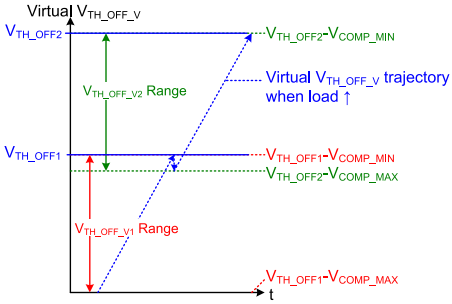

Fig. 15. Virtual $V_{TH\_OFF\_V}$ trajectory when load increases.

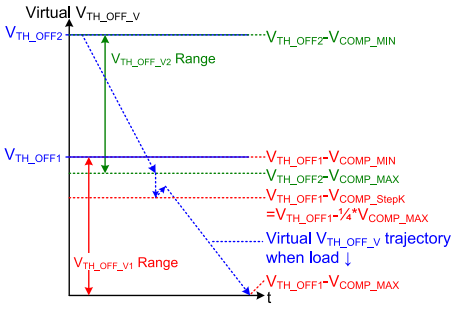

Fig. 16. Virtual $V_{TH\_OFF\_V}$ trajectory when load decreases.

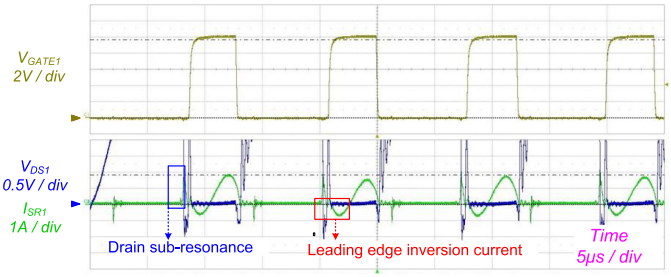

Fig. 17. Leading edge inversion current.

large dead time variation and stimulate the system feedback loop of the *LLC* resonant converter. In this condition, the output current oscillation and audible noise may occur so that the system becomes unstable. To avoid the unstable operation and to achieve soft-transition of V_{TH_OFF}, $V_{\mathrm{COMP\_STEP}}$ needs a minimum value to make range overlap between two consecutive $V_{TH\_OFF\_V}$ ranges such as $V_{TH\_OFF\_V2}$ and $V_{TH\_OFF\_V1}$ ranges, as shown in Fig 14. Therefore, $V_{\mathrm{COMP\_STEP}}$ is recommended as small as possible with 15% of the range overlap satisfying

$$V_{TH\_OFF2} - V_{TH\_OFF1} < 0.85 \cdot V_{\mathrm{COMP\_MAX}} = 0.85 \cdot M \cdot V_{\mathrm{COMP\_STEP}} \tag{8}$$

where *M* is maximum value of the COMP_*CNT* counter output and represents total number of V_{COMP} step.

B. Virtual Turn-OFF Threshol Voltage $V_{TH\_off\_V}$ Trajectory

When V_{TH_OFF} is changed by LSAT or HSAT high signal, V_{COMP} should be set or reset to a proper value which provides soft-transition between two consecutive V_{TH_OFF} such as from V_{TH_OFF1} to V_{TH_OFF2}. If it is not considered, $V_{TH\_OFF\_V}$ is severely changed at V_{TH_OFF} transition. It may induce the SR dead time jumping and the output current oscillation.

To prevent the situation, in the output load increasing condition, V_{COMP} should be reset to maximum value $V_{\mathrm{COMP\_MAX}}$ at V_{TH_OFF} one step-up. In Fig. 15, when $V_{TH\_OFF\_V}$ equals $(V_{TH\_OFF1} - V_{\mathrm{COMP\_MIN}})$, V_{TH_OFF} is increased by high of LSAT, and V_{COMP} is reset to $V_{\mathrm{COMP\_MAX}}$. It makes $V_{TH\_OFF\_V}$ cutback to $(V_{TH\_OFF2} - V_{\mathrm{COMP\_MAX}})$. As a result, $V_{TH\_OFF\_V}$ follows dotted line trajectory for V_{TH_OFF} soft-transition.

On the other hand, when the output load is decreasing and V_{TH_OFF} is reduced from V_{TH_OFF2} to V_{TH_OFF1} by HSAT signal, V_{COMP} needs an optimal set value $V_{\mathrm{COMP\_STEPK}}$ satisfying

$$V_{TH\_OFF2} - V_{\mathrm{COMP\_MAX}} \geq V_{TH\_OFF1} - V_{\mathrm{COMP\_STEPK}}. \tag{9}$$

Using (8), (9) is rearranged as

$$V_{\mathrm{COMP\_STEPK}} \geq 0.15 \cdot V_{\mathrm{COMP\_MAX}}. \tag{10}$$

In real design, $V_{\mathrm{COMP\_STEPK}}$ can be $1/4 - V_{\mathrm{COMP\_MAX}}$ with additional 10% margin of $V_{\mathrm{COMP\_MAX}}$. In this load condition, $V_{TH\_OFF\_V}$ decreasing trajectory is illustrated in Fig. 16. In the trajectory, when $V_{TH\_OFF\_V}$ reaches $(V_{TH\_OFF2} - V_{\mathrm{COMP\_MAX}})$, $V_{TH\_OFF\_V}$ changes to $(V_{TH\_OFF1} - ¼{*}V_{\mathrm{COMP\_MAX}})$ for the dead time margin and soft transition. After then, $V_{TH\_OFF\_V}$ is determined by the dead time regulation control algorithm.

C. Current Inversion Detection

There are two types of current inversion in the SR MOSFET. First, the leading edge current inversion occurs under light load condition, as shown in Fig. 17. The drain voltage subresonance makes SR turn-ON mistrigger, which causes the current inversion. In heavy load condition, the body diode of SR MOSFET starts conducting right after the primary-side switching transition. However, when the resonance capacitor voltage amplitude is not large enough in light load condition, the voltage across the magnetizing inductance of the transformer is smaller than the reflected output voltage. Thus, in the secondary side, body diode is reverse biased until the magnetizing inductor voltage builds up to the reflected output voltage. If SR gate is turned ON before the body diode conduction, the inversion current flows SR MOSFET.

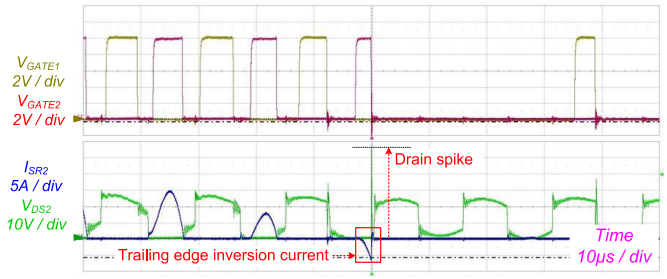

Fig. 18. Trailing edge inversion current.

To prevent it, the proper turn-ON delay is provided in the light load condition. It will be discussed following section.

The other type of current inversion is the trailing edge current inversion caused by the minimum ON-time described in Fig. 4 under fast load transient. If the minimum ON-time is longer than the powering time in the primary side, a regular gate turn-OFF trigger signal is prohibited by the minimum ON-time, which leads the trailing edge inversion current and huge drain spike, as shown in Fig. 18. Thus, the current inversion detection function should turn-OFF SR gate as soon as possible even in minimum ON-time. In the proposed control method, it is easily implemented by using V_{SAW} signal. Therefore, the inversion current can be minimized.

D. Light Load Operation

In the *LLC* resonant converter, light load operation with the synchronous rectifier is quite different from the conventional diode rectifier due to large output capacitance $C_{\mathrm{oss\,SR}}$ of SR MOSFET. To control SR in the light load condition, it is important to understand light load condition behavior. For the light load operation analysis, the switching period is subdivided into five modes. The main equivalent circuits for operation modes are shown in Fig. 19. Operational waveforms in light load condition are depicted in Fig. 20.

Mode 1 (t_0 – t_1)*: Mode 1* begins at t_0 when the primary switch Q_1 is turned OFF. An equivalent circuit is shown in Fig. 19(a). In this mode, C_{oss1} and $C_{\mathrm{oss}\,SR1}$ are charged, and C_{oss2} and $C_{\mathrm{oss}\,SR2}$ are discharged by the resonant current I_{Lr}. In addition, the magnetizing inductor voltage V_{Lm} increases. After the transition of drain voltages V_{DS1}, V_{DS2}, $V_{SR1\,DS}$, $V_{SR2\,DS}$, this mode ends. In the practical *LLC* resonant converter system, the transition of V_{DS1} and V_{DS2} may end earlier than that of $V_{\mathrm{SR1}\,DS}$ and $V_{\mathrm{SR2}\,DS}$. ZVS of Q_2 and M_2 can be guaranteed during this mode.

Mode 2 (t_1–t_2)*:* When *Mode 1* ends, the body diodes of Q_2 and M_2 are conducted. The resonant inductor voltage V_{Lr} is still determined by the resonant capacitor voltage V_{Cr} and V_{Lm}. However, since V_{Cr} is not larger enough to build up I_{Lr}, and V_{Lm} is smaller than the reflected output voltage, the *LLC* converter cannot transfer power to the secondary side. The SR current I_{SR2} decreases with a slope of $n^2 * (V_o + V_F)/L_m$, where n is the turns ratio of the transformer and V_F is the forward voltage drop of the body diode. At t_1, the body diode of M_1 is reverse biased so that I_{SR1} is added to I_{SR2}. It results in a sudden increase of

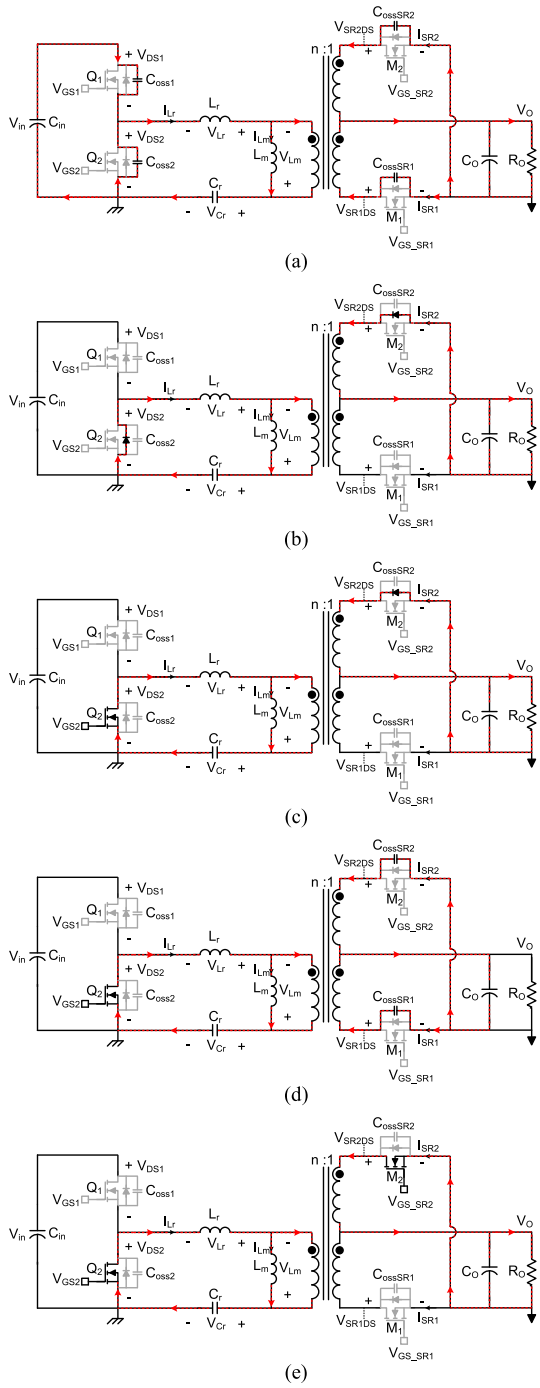

Fig. 19. *LLC* converter equivalent circuits in light load condition. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

I_{SR2}, which is called capacitive current spike at t_1. At the same time, $V_{\mathrm{SR2}\,DS}$ becomes $-V_F$, which generates SR gate turn-ON trigger signal of M_2. However, the turn-ON trigger signal should be ignored, because there is no power transfer from the primary side until when V_{Lm} equals the reflected output voltage $n * (V_o + V_F)$. If the turn-ON trigger signal is not prevented, it induces the leading edge inversion current of M_2 from the output capacitor. *Mode 2* ends when Q_2 is turned ON.

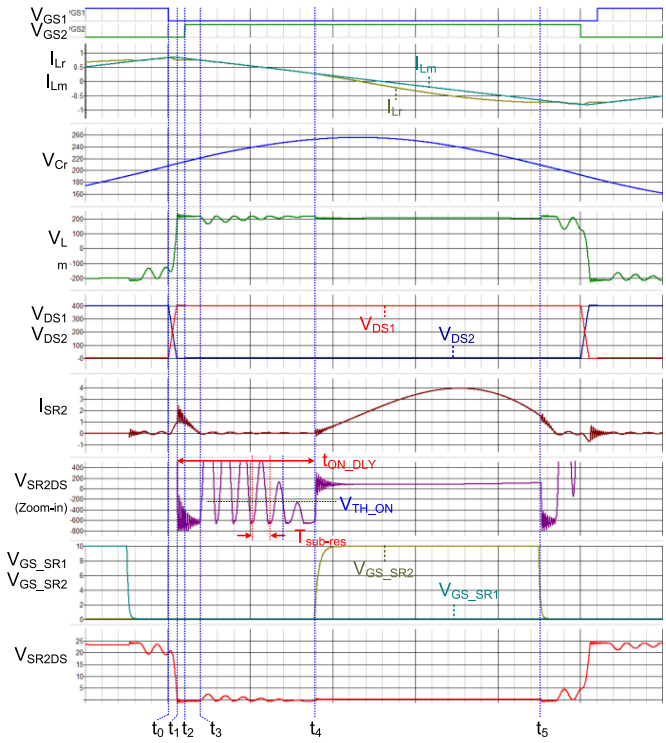

Fig. 20. Operational waveforms in light load condition.

Mode 3 ($t_2 - t_3$)*:* In this mode, I_{Lm} decreases with the same slope as in *Mode 2* until when I_{SR2} becomes zero. In the primary side, V_{Cr} is charged by I_{Lm}. The equivalent circuit is shown in Fig. 19(c).

Mode 4 (t_3–t_4)*:* In the primary side, since V_{Lm} is not clamped by the reflected output voltage, V_{Cr} is applied to V_{Lm} and V_{Lr} in accordance with their inductance ratio

$$V_{Lm} = V_{Cr} \cdot L_m/(L_r + L_m) \tag{11}$$

$$V_{Lr} = V_{Cr} \cdot L_r/(L_r + L_m). \tag{12}$$

In the secondary side, since I_{SR2} is zero at t_3, subresonance starts between $C_{\mathrm{oss}SR1}$, $C_{\mathrm{oss}SR2}$, L_r, and L_m. The subresonance period $T_{\mathrm{sub\text{-}res}}$ is given by

$$T_{\mathrm{sub-res}} = 2\pi\sqrt{(L_r||L_m) \cdot n^2(C_{oss\mathrm{SR1}} + C_{oss\mathrm{SR2}})}. \tag{13}$$

Under the oscillation, as shown in Fig. 20, I_{Lr} cannot transfer power to the secondary side. Finally, when V_{Lm} reaches the reflected output voltage, the body diode of M_2 is turned ON and V_{Lm} is clamped by $n * (V_o + V_F)$, and I_{SR2} starts increasing. To prevent the leading edge inversion current, turn-ON delay $t_{\mathrm{ON\_DLY}}$ should be longer than t_4 of the subresonance end.

Mode 5 (t_4–t_5)*:* After the turn-ON delay finishes, M_2 is turned ON so that $V_{\mathrm{SR2}\,DS}$ is determined by the product of r_{DS_ON} of M_2 and instantaneous SR current I_{SR2}. When $V_{\mathrm{SR2}\,DS}$ is higher than turn-OFF threshold voltage at t_5, M_2 is turned OFF and this mode ends.

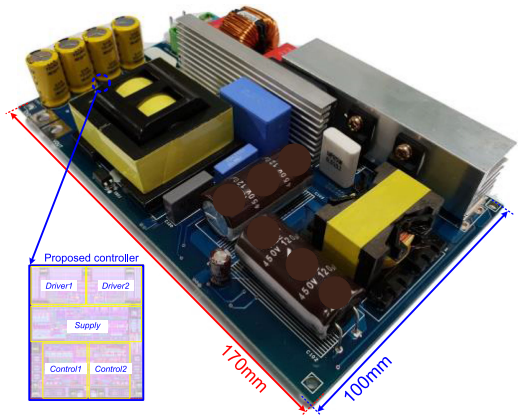

Fig. 21. Prototype with the proposed controller.

TABLE I
SYSTEM SPECIFICATIONS

Parameters	Value
Input voltage V_{in}	230 Vac
PFC output voltage V_{Link}	392 Vdc
Output voltage V_O	19.5 V
Output current I_{OUT}	12 A
Output Power P_o	234 W
Switching frequency f_s @ full load condition	101 kHz
Resonant inductance L_r	80 µH
Magnetizing inductance L_m	650 µH
Resonant capacitance C_r	33 nF
LLC transformer turns ratio	31 : 3
Dead time target t_{LBAND}	100 ns
Dead time target t_{HBAND}	200 ns
SR MOSFET	FDB045AN08A0

IV. EXPERIMENTAL RESULTS

A prototype for the 234 W ac–dc power system, which is configured by a boost PFC and an *LLC* resonant converter with the proposed controller, is built and experimented on to verify the validity of the proposed control method, as shown in Fig. 21. The proposed control method is implemented with 0.25-μm BCDMOS technology. In the system specifications, as shown in Table I, the input voltage V_{in} is 230 Vac, the output voltage V_O is 19.5 V, and the maximum output current I_{OUT} is 12 A.

The operating frequency f_s of the *LLC* resonant converter is 101 kHz under full load condition. In the resonant tank design, the resonant inductance and magnetizing inductance are 80 and 650 μH, respectively, and the resonant capacitance is 33 nF. For the proposed hysteresis dead time regulation control, 100 ns of the dead time lower target t_{LBAND} is designed by considering 20–30 ns of turn-OFF signal propagation delay and the input capacitor C_{ISS} discharging time of SR MOSFET.

In t_{HBAND} design, the dead time variation guard band, which is time difference from t_{HBAND} to t_{LBAND}, can be selected as 1% of the switching period of the *LLC* resonant converter

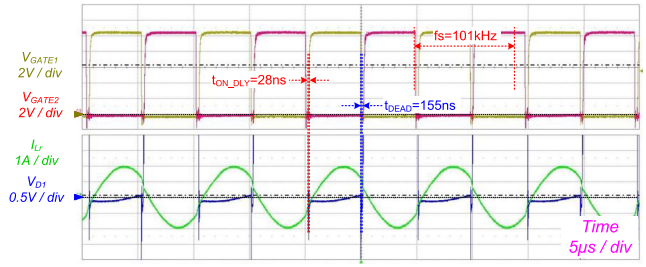

Fig. 22. SR waveforms, when $I_{\mathrm{OUT}} = 12$ A load condition.

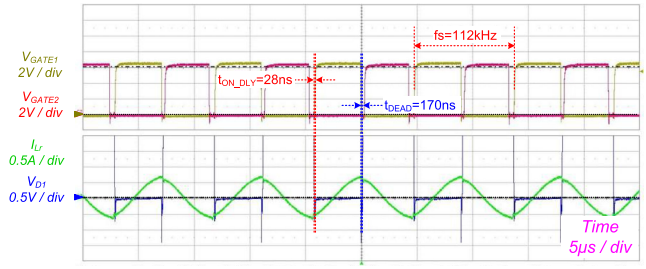

Fig. 23. SR waveforms, when $I_{\mathrm{OUT}} = 1$ A load condition.

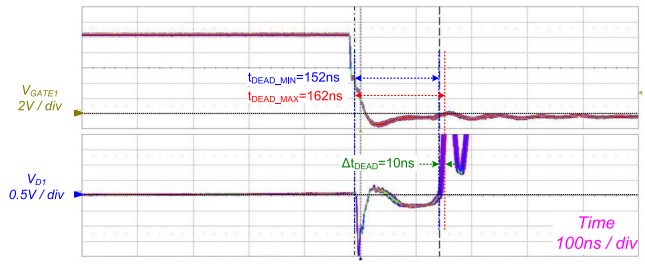

Fig. 24. SR dead time variation, when $I_{\mathrm{OUT}} = 12$ A load condition.

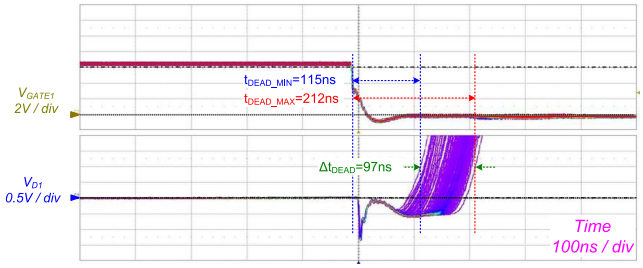

Fig. 25. SR dead time variation, when $I_{\mathrm{OUT}} = 1$ A load condition.

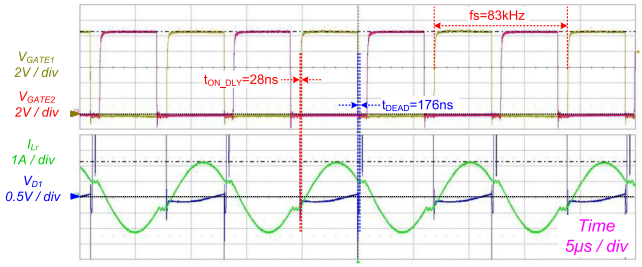

Fig. 26. Below resonance operation, when $I_{\mathrm{OUT}} = 12$ A load condition.

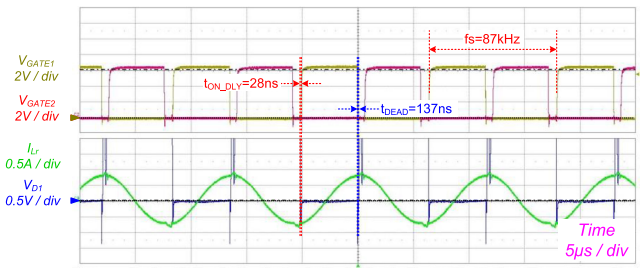

Fig. 27. Below resonance operation, when $I_{\mathrm{OUT}} = 1$ A load condition.

to prevent stimulating the feedback loop for the output voltage regulation. Thereby, 200 ns of t_{HBAND} is used in the experiment.

Figs. 22 and 23 show waveforms of steady-state operation under heavy load and light load conditions, respectively. Under heavy load condition, the primary current I_{Lr} shows abovemintioned resonance operation. In this condition, the SR gate V_{GATE1} is turned ON with 28 ns of turn-ON delay after the body diode conduction. The gate turn-OFF is determined by the proposed dead time regulation control method with 155 ns of SR dead time. Thus, the SR MOSFET turn-ON time is optimized and it provides maximized efficiency under the heavy load condition. Under the light load condition, the operating frequency is increased from 101 to 112 kHz and the primary side current is reduced a lot. The drain sensing voltage V_{D1} is almost flat near zero voltage while SR gate is turning ON. It makes the turn-OFF control difficult. However, the proposed control method well finds a new steady state and regulates T_{DEAD} at around 170 ns.

Fig. 24 shows the SR dead time variation with persistence mode of an oscilloscope under 12-A load condition. The dead time T_{DEAD} is measured from 2 V of V_{GATE1} falling to 0.8 V of V_{D1} rising. Maximum T_{DEAD} is 162 ns and minimum T_{DEAD} is 152 ns. It verifies that T_{DEAD} is well regulated between t_{LBAND} and t_{HBAND} in the proposed control method. It also shows only 10 ns of the SR dead time variation. In Fig. 25, the dead time variation is measured under 1-A load condition. Since the output current is reduced, the induced voltage by the stray inductance, which is determined by (1), is also decreased. In addition, V_{D1} becomes noise sensitive under this condition. It increases dead time variation by changing one step of V_{COMP}. Therefore, the variation is larger than that under the heavy load condition. However, it is not serious and still within the dead time regulation target. Maximum and minimum T_{DEAD} are 212 and 115 ns, respectively.

In Figs. 26 and 27, the waveforms of below resonance operation are shown by reducing PFC output voltage V_{Link} to 365 Vdc. The operating frequency is changed to 83 and 87 kHz under heavy load condition and light load condition, respectively. In both conditions, T_{DEAD} is properly regulated between t_{LBAND} and t_{HBAND}. Thus, the proposed control method can be applied to both abovementioned resonance *LLC* design and below resonance *LLC* design.

Under 0.3 A of load condition in Fig. 28, the leading edge inversion current is detected by using the method described in

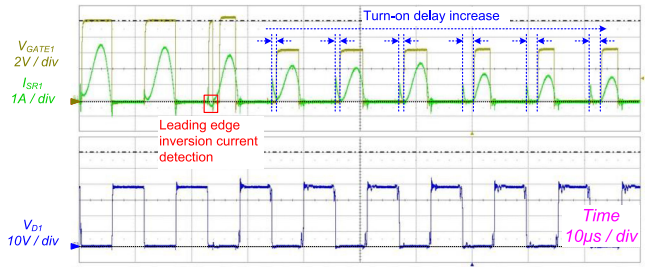

Fig. 28. Leading edge inversion current detection and turn-ON delay increase.

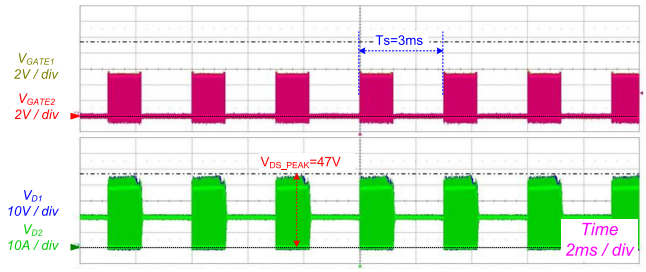

Fig. 29. SR waveforms under 10 A of load ON and OFF condition.

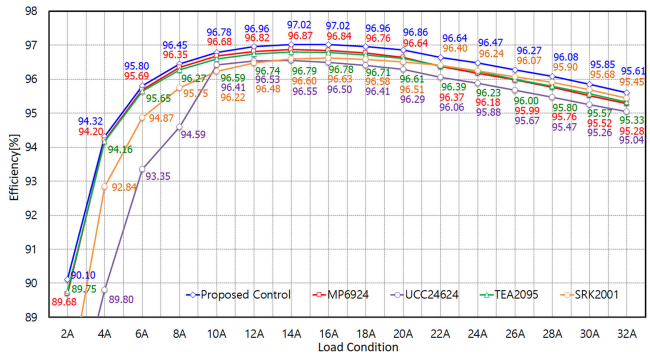

Fig. 30. Efficiency comparison.

Fig. 4 and Section III-C. Then, the proposed controller increases turn-ON delay to prevent additional inversion current.

Fig. 29 shows the SR gate and the drain voltage waveforms under the fast output load transient condition. The output load is changed between 0 and 10 A with 333 Hz of load ON–OFF frequency. When the output load is decreased from 10 to 0 A, V_{GATE1} and V_{GATE2} are stopped without the drain spike. On the other hand, when the output load is increased to 10 A, the proposed controller resumes operation and outputs V_{GATE1} and V_{GATE2}. Under this severe load transient condition, stable SR operation is verified.

In order to verify the key advantage of the proposed control method, *LLC* resonant tank is redesigned with 100 μH of L_r, 475 μH of L_m, and 55 nF of C_r for low-voltage and high-output current application, which has 12 V of V_O and 32 A of I_{OUT}. The efficiency is measured without PFC stage and compared with the conventional SR controllers [20], [22]–[24], as shown in Fig. 30. In the result, the proposed control method shows at least 0.16% higher efficiency than that of the conventional control methods under 32 A of the load condition. It means that more than 600 mW of conduction loss in SR MOSFET is reduced when compared with the convention turn-OFF methods. Thereby, the proposed control method can provide better thermal performance. As the output load decreases, the proposed control method still shows higher efficiency in the entire load range.

V. Conclusion

In this article, a novel hysteresis band dead time regulation control method for *LLC* synchronous rectification was proposed to maximize SR conduction time and the system efficiency. In the proposed control method, instantaneous drain voltage information and previous cycle dead time information were used for SR dead time regulation and better transient characteristic. The virtual turn-OFF threshold voltage control algorithm for compensating the stray inductance of MOSFET package and PCB pattern is discussed in Section II. In design considerations, the compensation voltage and the virtual turn-OFF threshold voltage trajectory were discussed. In addition, the light load SR operation was explained in Section III. To verify the validity of the proposed control method, a 234-W prototype was experimented with the proposed controller, which is implemented with 0.25-μm BCDMOS technology. In the result, the proposed control method showed the dead time regulation at around dead time target, which provides optimized SR conduction time under heavy and light load conditions. Under the load transient condition, the proposed controller well provided gate drive signals without any problem. In the efficiency comparison with low-voltage and high-output current application, the proposed control method proved higher efficiency compared to that of the conventional control method. Therefore, the proposed SR control method can be a good candidate for high-efficiency *LLC* resonant converter.

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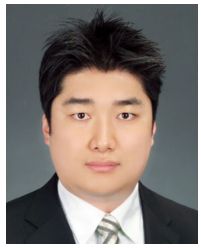

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