A New Current Source Converter Using AC-Type Flying-Capacitor Technique

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***Abstract*—Entering the new millennium, current source converters (CSCs) have drawn increasing attention not only for high-power but also some emerging low-power applications which prefer the inherent voltage boosting nature and low dv/dt on ac-side. However, the dc-link quality of CSC has not been well improved and is rarely discussed in literature. To fill this gap, a new type of CSC topology is proposed in this article through the isomorphic theory. It utilizes the ac-type flying capacitors in each phase leg and provides alternative commutation loops, which can reduce the dc-side dv/dt and improve the common-mode voltage simultaneously. Besides, this technique can increase the withstand voltage of the converter without series connections of switching devices. Different from the voltage-source converter type, the flying capacitor voltage in CSC should be maintained as ac voltage, thus, active voltage regulation is necessary. To deal with such a challenge, carrier-based pulsewidth modulation with flying capacitor voltage regulation is also developed in this work. Compared with the traditional device-series-connected CSC topologies, the numbers of active switches and the device blocking voltage can remain the same, while the ac-type flying capacitors are added in the proposed topology to gain all the above merits. Simulation and experiment results are obtained to verify the advantages of this new type of CSC topology.**

***Index Terms*—Carrier-based pulse width modulation (PWM), current source converter (CSC), DC-link ripple, flying-capacitor-clamped converter.**

I. Introduction

CURRENT source converters (CSCs) have been successfully implemented in high-power motor drives (medium voltage), power grid transmission system (high voltage) [1], and drawing increasing attention in some emerging applications with lower voltage/power ratings, e.g., solar photovoltaics, wind turbine generation, electrical vehicle, etc. [2]–[4]. CSCs enjoy some well-acknowledged merits like the inherent low dv/dt on its ac-side, the bidirectional power flow control capability, short-circuit fault tolerance, and voltage boost features. In addition to these advantages, the advanced device, control, design, and manufacture improvements all together make the CSC technique competitive with the voltage-source converter (VSC) in these areas [4]–[8].

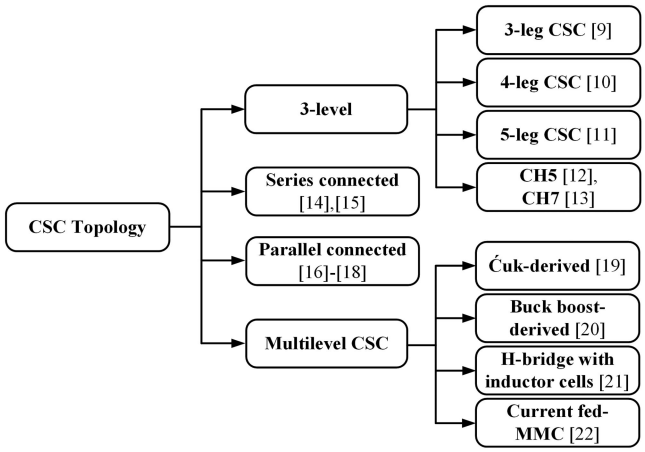

Fig. 1. General topology classification of existing CSCs.

As one of the most important driving forces of this technique, CSC topologies have been evolved since the beginning of power electronics, which results in a large number of different types as shown in Fig. 1. The conventional CSCs are classified into 3-level type since they can only generate three current levels in each phase (line current) [9]–[13]. Series and parallel configurations are also found in practice to increase the power handling capability of the CSCs [1], [14]–[18]. Besides, to further increase the ac-link output power quality and reduce the current ratings of the device, many multilevel CSCs are proposed [19]–[22]. It can be noted that great research efforts have been devoted to load/grid side serving quality. However, dc-link issues are rarely discussed in the topology research domain. In fact, opposed to VSCs, the dc-link of CSCs contains a large volume of voltage pulses which may lead to high dv/dt [23]. This could be more severe if the dc choke is not large, and the utilized switch has a very small turn-ON/OFF time constant. Furthermore, the large dv/dt may also lead to increased common-mode voltage (CMV), which will degrade the insulation materials and cause leakage current problems with transformer-less configuration [12], [24].

From a topological point of view, there could be several ways to deal with this challenge: 1) use energy buffer on dc-link, e.g., increase dc-choke value, add auxiliary pulse absorption equipment; 2) limits the switching speed to a certain level. However, both solutions 1) and 2) could easily lead to obvious negative effects on the converter performance. Alternatively, we

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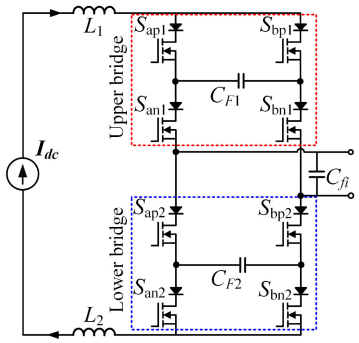

Fig. 2. Proposed single-phase flying-capacitor-clamped CSC (FCC-CSC).

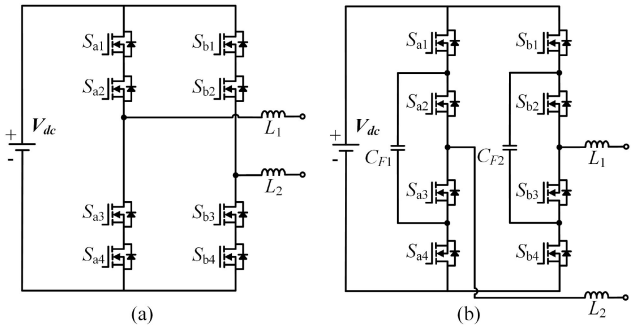

Fig. 3. Single-phase VSC topology. (a) VSC with series connected device. (b) 3-level flying-capacitor-clamped VSC evolved from (a).

introduce the third solution: Develop new commutation loops to suppress dv/dt.

In practice, the flying-capacitor-clamped (FCC) techniques are commonly implemented in the VSC for decades to solve ac dv/dt issues [25]. It could be beneficial if the same concept can also be used for CSC, which has never been studied in literature. Thanks to the recently discovered isomorphic relationships between CSC and VSC [26], the FCC concept can be transformed into the CSC version (Fig. 2). In particular, the resulting new type of CSC can naturally reduce the dc-side dv/dt with all similar benefits in VSCs. Basically, it utilizes the ac-type flying capacitors in each phase leg and provides alternative commutation loops, resulting in a new type of CSCs. With the ac-type flying capacitors technique, the proposed CSC enjoys several good features: 1) better dc output power quality with low dv/dt exposed on the dc-side inductors, 2) reduced CMV, 3) higher voltage rating of the converter without device-series connection, and 4) a modular structure that is easy to scale up.

The rest of the article is organized as follows: The topology of the proposed FCC-CSC with ac-type flying capacitor is introduced in Section II, the operation principle of the proposed CSC is analyzed in Section III, the modulation design, and flying capacitor clamping voltage regulation are presented in Section IV. Simulation and experiment results are presented in Section V. Finally, Section VI concludes the article.

II. Topology Derivations of the Proposed FCC-CSC Through Isomorphic Theory

A. Flying capacitor Technique in VSC

In practice, multilevel VSC-based topologies have been proposed and successfully implemented. One typical example is the 3-level flying-capacitor-clamped VSC [in Fig. 3(b)] which was evolved from the conventional VSC with series-connected devices [in Fig. 3(a)] by adding a dc-type flying capacitor in each phase leg [25]. With the dc-type flying capacitor technique, the VSC enjoys several good features: 1) better ac output power quality with low dv/dt exposed on the ac-side inductors, 2) higher voltage rating of the converter without device-series connection, 3) a modular structure that is easy to scale up, etc.

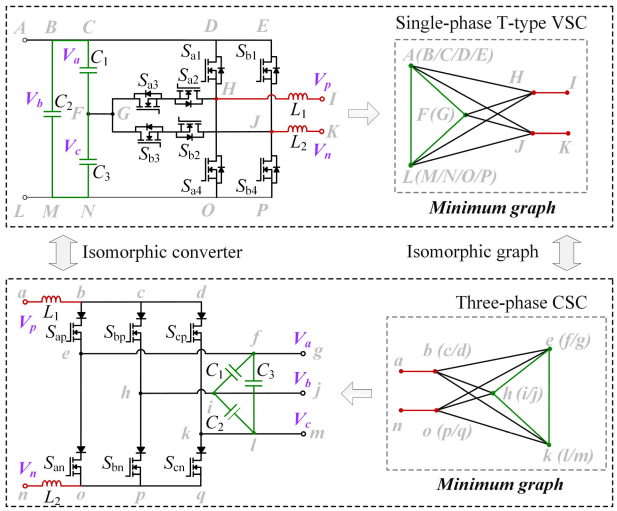

Fig. 4. Topology transformation example from single-phase three-level T-type VSC to three-phase CSC [26].

B. Proposed FCC-CSC Topology

From the graphical view, the CSC and VSC topologies can share the same configurations in a fundamental way. In fact, dual and isomorphic principles can be considered as powerful tools to establish such fundamental links among various converters [26]. Furthermore, it is possible to utilize such relationships to generalize the FCC concept in VSC into the CSC-based system.

Based on the isomorphic theory, these two different types of converters can be transformed into each other by the following three steps [27]: 1) the first step is to derive the isomorphic CSC of the original VSC is to draw the minimum graphs as shown in the top of Fig. 4; 2) the second step is to reverse the input and output of the converter, therefore, the dc (ac) link of VSC should be changed into the ac (dc) link of the CSC, while the passive components and all the connections are maintained the same; 3) the third step is to implement the right switches in the derived converter, e.g., from MOSFET with antiparallel diode into MOSFET with a series diode as shown in Fig. 4.

Based on the same steps, the FCC-VSC can be transformed into FCC-CSC by the isomorphic theory as shown in Fig. 5. Through the isomorphic relationship [26], [27], not only the

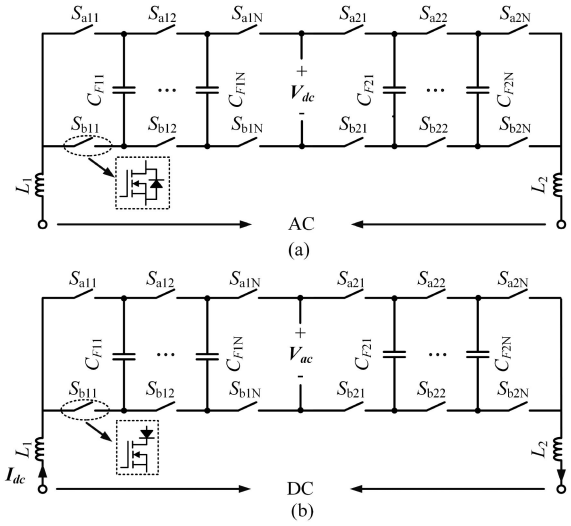

Fig. 5. Topology derivation of FCC-CSC from FCC-VSC by isomorphic theory. (a) N-stage FCC-VSC. (b) N-stage FCC-CSC.

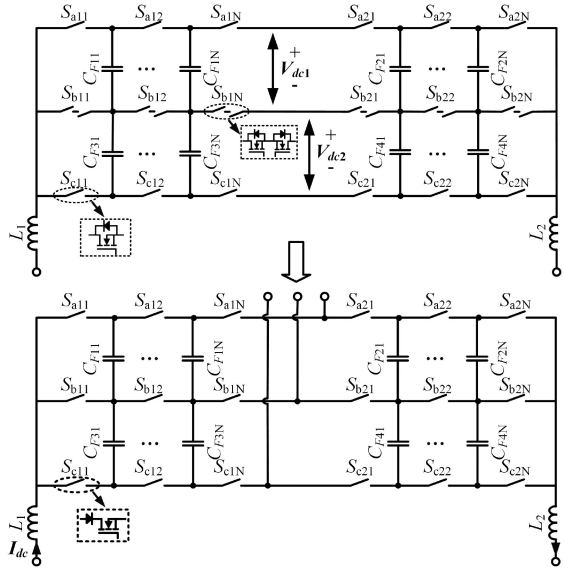

Fig. 6. Derivation of three-phase FCC-CSC from the stacked multilevel VSC.

circuit appearances but also operation features are linked with each other, and can be predicted as follows: 1) the ac-side voltages of FCC-VSC become the dc-side voltages of the FCC-CSC, i.e., multilevel waveforms; 2) the dc-type flying capacitors in FCC-VSC become ac-type capacitors in FCC-CSC; 3) the flying capacitor voltage can be regulated by the active control of redundant states; 4) the FCC-VSC can be generalized by modularly staking the basic cells, so as FCC-CSC; 5) carrier-based PWM can be utilized for both converters with similar increased equivalent frequency phenomenon.

C. Other Derivates of FCC-CSC Topology

Due to the inherent scalability and modularity of the new topology, it can be easily extended into a modular or multiphase CSC system for higher power scenarios. For instance, as indicated in Fig. 5(b), the proposed converter can be generalized by using N flying capacitors for the upper/lower bridge. In such a way, 2N devices in each leg are clamped into 1/N of line voltage and series connections are avoided.

Different from the scaling rules of FCC-VSC, the proposed FCC-CSC cannot be simply generalized into multiphase versions by adding the same leg in a single-phase circuit. To derive the multiphase FCC-CSC, the isomorphic theory can be implemented. It turns out that a back-to-back single-phase leg stacked multilevel VSC [28] can be transformed into its isomorphic version, which is the three-phase FCC-CSC as shown in Fig. 6. Similarly, the four-phase FCC-CSC should be transformed from the corresponding scaled-up stack multilevel VSC and enjoys corresponding features. It can be expected that, for each FCC VSC topology, there is an FCC-CSC accordingly. Since this article is mainly focused on the conceptual introduction of the ac-type flying capacitor techniques and its verifications, therefore, the following sections will be concentrated on the single-phase version of the FCC-CSC.

D. Comparison of FCC-CSC With Existing CSC Topologies

Several existing CSC topologies shown in Fig. 1 are discussed to give a detailed comparison between the existing CSC topologies and the proposed FCC-CSC. Their main features and isomorphic pairs are summarized as follows.

1) Multiphase CSCs can realize a better dc-link dv/dt. The conventional N-phase CSCs are isomorphic with the single-phase T-type N-level VSCs [26], where the ac-link output quality can be improved with the increased number of voltage levels. Based on their isomorphic relationships, the multiphase CSCs could provide more voltage potentials on the dc-link and have better dc-link quality.
2) AC-link parallel-connected CSCs can realize a better ac-link output quality by providing multilevel current PWM waveforms as well as some other multilevel CSCs. They are thoroughly summarized in the literature [16]–[18].
3) DC-link series-connected CSCs can realize a better dc-link quality. The dc-link series-connected CSCs are isomorphic with the cascaded H-bridge (CHB) VSCs. With a higher number of the cascaded modules, CHB VSCs can achieve a better ac-side quality; however, following the similar constraints of CHB VSCs, the dc-link series-connected CSCs require the ac independent power supplies, e.g., the ac-side isolated transformer, which could be unfavorable in certain applications, where galvanic isolation is not mandatory.
4) Device-series-connected (DSC) CSC topologies have the same input and output performance as the conventional six-switch CSC. The major advantage of this topology is the increased voltage blocking capability by using series-connected devices, which has been the industrial common sense for higher voltage applications. However, under such higher voltage cases, the dc-link dv/dt tends to be quite high if not attenuated.

TABLE I
SUMMARY OF THE EXISTING CSC TOPOLOGIES AND THE PROPOSED FCC-CSC

CSC Topology	Multiphase structure	AC-link parallel-connected topology	DC-link series-connected topology	Device-series-connected topology [8]	Proposed FCC-CSC
Isomorphic topology	Single-phase T-type *N*-level VSC	DC-link parallel-connected VSC	Cascaded H-bridge VSC	Device series-connected VSC	Flying-capacitor-clamped VSC
AC-side power quality	Similar	Better	Same	Same	Same
DC-side power quality	Better	Same	Better	Same	Better
Common mode voltage	Similar	Better	Better	Same	Better
Voltage blocking capability	Same	Same	Higher	Higher	Higher
Current handling capability	Same	Better	Same	Same	Same
Operation challenges	Trick AC current modulation and control	Require circulating current control	Require AC independent power supplies	Require voltage sharing of the device	Require active control of flying-capacitor voltages
Potential applications	Multiphase system or multiphase load, e.g. five-phase motor drive	High power/current applications where modular design is preferred	Higher voltage rating applications where galvanic isolation is mandatory	Higher voltage rating applications, e.g. high-power motor drive	Higher voltage rating applications requiring low DC-side dv/dt, e.g. transformer-less PV inverter

Table I summarizes the CSC topologies including existing ones and the proposed FCC-CSC in terms of their features in various aspects. The comments on them are made based on the benchmark of the conventional six-switch three-phase CSC. Since only the DSC CSC and the proposed FCC-CSC are developed to achieve higher voltage rating without using bulky isolated transformers, more comparisons between them in terms of dc-link quality and CMV will be provided in the article.

III. OPERATION PRINCIPLE ANALYSIS OF THE PROPOSED FCC-CSC TOPOLOGY

In this section, the operation principles of the proposed FCC-CSC are introduced. The single-phase one-stage FCC-CSC (Fig. 2) can be divided into two full-bridge building blocks, which can be analyzed separately. Based on the commutation principle of CSC, only one switch should be turned ON from the upper/lower leg at any time instance. Therefore, there are four switching states for each bridge, which are identified as S_1: [0101]; S_2: [0110]; S_3: [1001], and S_4: [1010]. The four digitals represented the gating signals in the order of [$S_{\rm ap}$ $S_{\rm bp}$ $S_{\rm an}$ $S_{\rm bn}$], where "1" means switching turn ON while "0" means switching turn OFF. Fig. 7 shows the commutation paths of the upper and lower bridge under different switching states. Since the upper and lower bridges both have four switching states, there are 16 switching state combinations in total. The device blocking voltages are changed with the switching states. Table II summarizes the device blocking voltages of the upper bridge under the four different switching states, which indicates that the device blocking voltages of the upper/lower bridge are related to the output voltage (V_{ab}) and the upper/lower flying capacitor clamping voltage (V_{c1} or V_{c2}).

To reduce the device blocking voltage and make them equal to half of the output voltage, it is critical that the capacitor clamping voltage is well regulated, otherwise, the blocking voltages of devices are unequal and may exceed the voltage ratings of devices. To achieve this target, the capacitor clamping voltage should fulfill the equation as

$$V_{c1} = V_{c2} = 0.5V_{ab}. \tag{1}$$

Once the capacitor clamping voltages are regulated to half of the output voltage, the blocking voltage of each device is the envelope line of $0.5V_{ab}$ under an arbitrary switching state according to Table II.

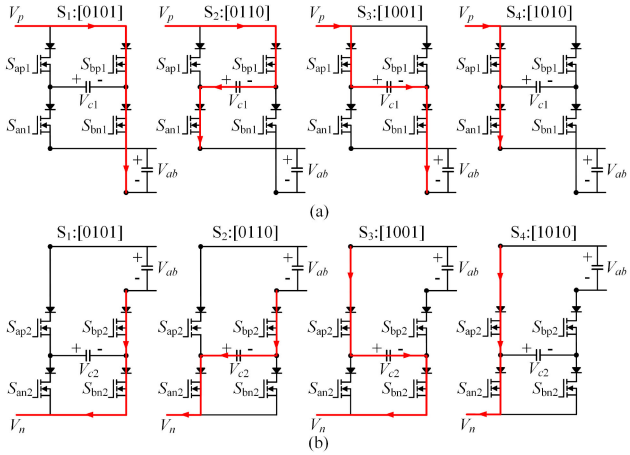

Fig. 7. Switching state of FCC-CSC. (a) Upper bridge. (b) Lower bridge.

TABLE II
DEVICE BLOCKING VOLTAGE OF UPPER BRIDGE

	S_1	S_2	S_3	S_4
S_{ap1}	$-V_{c1}$	$-V_{c1}$	0	0
S_{bp1}	0	0	V_{c1}	V_{c1}
S_{an1}	$V_{c1}-V_{ab}$	0	$V_{c1}-V_{ab}$	0
S_{bn1}	0	$-V_{c1}+V_{ab}$	0	$-V_{c1}+V_{ab}$

TABLE III
DC-LINK VOLTAGE AND COMMON-MODE VOLTAGE VALUES OF SINGLE-PHASE ONE-STAGE FCC-CSC

		S_1	S_2	S_3	S_4
S_1	V_{c1}	-	↓	↑	-
	V_{c2}	-	-	-	-
	V_{pn}	0	V_{ab}-V_{c1}	V_{c1}	V_{ab}
	CMV	0	0.5·(V_{ab}-V_{c1})	0.5V_{c1}	0.5V_{ab}
S_2	V_{c1}	-	↓	↑	-
	V_{c2}	↓	↓	↓	↓
	V_{pn}	-V_{c2}	V_{ab}-V_{c1}-V_{c2}	V_{c1}-V_{c2}	V_{ab}-V_{c2}
	CMV	0.5V_{c2}	0.5·(V_{ab}-V_{c1}+V_{c2})	0.5·(V_{c1}+V_{c2})	0.5·(V_{ab}+V_{c2})
S_3	V_{c1}	-	↓	↑	-
	V_{c2}	↑	↑	↑	↑
	V_{pn}	-V_{ab}+V_{c2}	-V_{c1}+V_{c2}	V_{c1}+V_{c2}-V_{ab}	V_{c2}
	CMV	0.5·(V_{ab}-V_{c2})	0.5·(2V_{ab}-V_{c1}-V_{c2})	0.5·(V_{ab}+V_{c1}-V_{c2})	0.5·(2V_{ab}-V_{c2})
S_4	V_{c1}	-	↓	↑	-
	V_{c2}	-	-	-	-
	V_{pn}	-V_{ab}	-V_{c1}	V_{c1}-V_{ab}	0
	CMV	0.5V_{ab}	0.5·(2V_{ab}-V_{c1})	0.5·(V_{ab}+V_{c1})	V_{ab}

Since the current flows of CSC switching devices are unidirectional and constant, therefore, the current following through the flying capacitor is only determined by the switching state. For example, the flying capacitor voltage will increase when the switching state is S_3, while it will decrease under switching state S_2, and the zero switching states S_1 and S_4 have no effect on flying capacitor voltage. The complete conduction paths are determined by the combination of the switching states of upper and lower bridges, which results in different dc-link voltage as well as CMV values.

The complete list of switching state combinations is shown in Table III, where the dc-link voltage (V_{pn}), CMV, and flying capacitor voltage influence under different switching states are summarized (row: Upper bridge; column: Lower bridge). The symbols "↑," "↓," and "-" represent an increase, decrease, and no change, respectively. The capacitor voltage influence status is only determined by the switching states of the corresponding bridge. Multilevel dc-link voltages ($\pm V_{ab}$, $\pm 0.5V_{ab}$, and 0) can be achieved, which can reduce dv/dt and ripples of dc-link voltage, thus, results in a smaller dc-link filter potentially. Meanwhile, the number of available CMV levels can be greater compared to the DSC CSC topologies [8], which will provide more flexibility to deal with the CMV issues.

IV. CARRIER-BASED MODULATION DESIGN WITH FLYING CAPACITOR VOLTAGE REGULATION SCHEMES

Based on the analysis in Section III, the modulation method of the proposed FCC-CSC should guarantee sinusoidal outputs and regulated capacitor clamping voltages simultaneously. To fulfill these targets, a carrier-based PWM with capacitor clamping voltage control is introduced in this section.

A. Unipolar Carrier-Based PWM

To produce sinusoidal outputs, the output current PWM should fulfill the theorem of impulse. According to the FCC-CSC topology, the output current can only be regulated by the four switches connected to the output terminals (S_{an1}, S_{bn1}, S_{ap2}, and S_{bp2}). Other devices (S_{ap1}, S_{bp1}, S_{an2}, and S_{bn2}) can be utilized to regulate the voltages of flying capacitors.

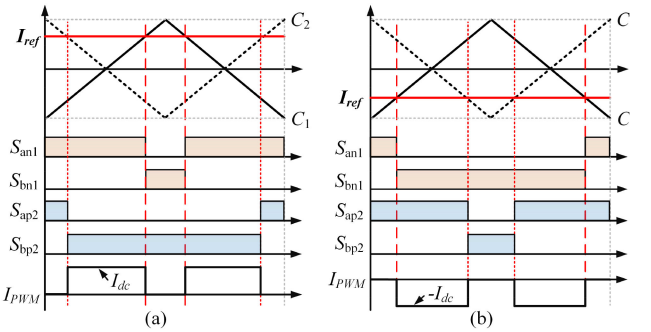

Fig. 8. Unipolar modulation of single-phase CSC. (a) Positive fundamental cycle. (b) Negative fundamental cycle.

Based on the operation principle of CSC, one and only one switch among the upper and lower leg switches should be ON at the same time, which can be restricted by $S_{an1} + S_{bn1} = 1$ and $S_{ap2} + S_{bp2} = 1$. Taking unipolar carrier-based PWM as an example, the gating signals of S_{an1} and S_{bn1} are generated by comparing the current reference with carrier C_1, while the gating signals of S_{ap2} and S_{bp2} are produced by comparing the current reference with lower carrier C_2. The logical relationship can be expressed as

$$S_{an1} = \bar{S}_{bn1} = \begin{cases} 1, & I_{ref} \geq C_1 \\ 0, & I_{ref} < C_1 \end{cases}; \; S_{ap2} = \bar{S}_{bp2} = \begin{cases} 1, & I_{ref} < C_2 \\ 0, & I_{ref} \geq C_2 \end{cases} \quad (2)$$

where I_{ref} is the sinusoidal current reference, C_1 and C_2 are the symmetrical carriers, which are shifted 180° as shown in Fig. 8. The reference is assumed to be constant in each carrier period. It shows that the PWM waveform is 5-segment symmetrical for both positive and negative fundamental cycles and the average switching frequency is the same as the carrier frequency.

B. Flying Capacitor Voltage Regulation Schemes

Based on the above analysis, the gating signals of S_{an1}, S_{bn1}, S_{ap2}, and S_{bp2} are generated by comparing the current reference and carriers to guarantee sinusoidal ac outputs, meanwhile, the gating signals of S_{ap1}, S_{bp1}, S_{an2}, and S_{bn2} are determined to regulate the capacitor clamping voltage actively. An example of the flying capacitor voltage regulation process is shown in Fig. 8(a), where both flying capacitor voltages are assumed to be higher than half of ac voltage in the beginning. For the upper bridge, since S_{an1} is turned ON, S_{bp1} will be turned ON to discharge the flying capacitor C_{F1}. For the lower bridge, S_{an2} needs to be turned ON to form a short-circuit with S_{ap2}, otherwise, the voltage flying capacitor C_{F2} will be charged to much higher. To regulate the flying capacitor voltage, the gating signals of S_{ap1}, S_{bp1}, S_{an2}, and S_{bn2} can be

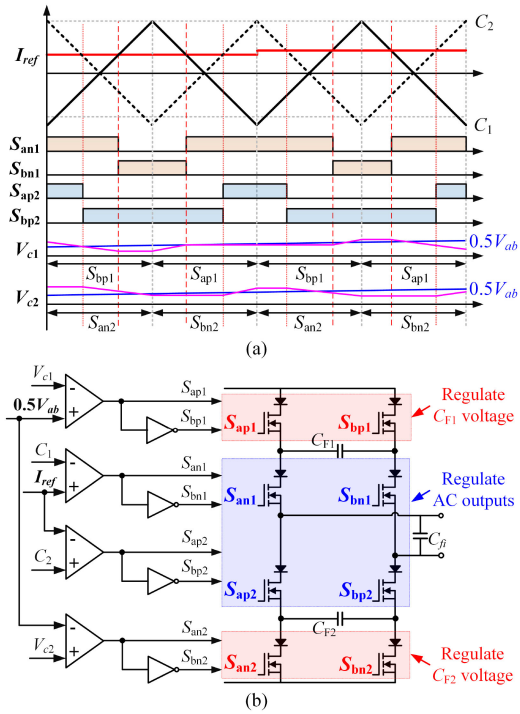

Fig. 9. Flying capacitor clamping voltage regulation. (a) Gating signal generation. (b) Digital implement process.

determined as

$$S_{\mathrm{ap1}} = \bar{S}_{\mathrm{bp1}} = \begin{cases} 1, & 0.5V_{ab} \geq V_{c1} \\ 0, & 0.5V_{ab} < V_{c1} \end{cases}; \; S_{\mathrm{an2}} = \bar{S}_{\mathrm{bn2}} = \begin{cases} 1, & 0.5V_{ab} < V_{c2} \\ 0, & 0.5V_{ab} \geq V_{c2}. \end{cases} \tag{3}$$

In this article, open-loop control is adopted for ac output regulation, a given current reference I_{ref} is generated by a digital controller. It is worth mentioning that the closed-loop control strategies developed for traditional CSC topology can be adopted for FCC-CSC to control the ac outputs. While the flying capacitor voltage control is achieved with simple feedback tracking by comparing the flying capacitor voltage and half of the ac voltage. The overall digital control process is shown in Fig. 9(b), where the ac output regulation and capacitor clamping voltage control are two independent processes. Therefore, the two processes can be improved correspondingly to achieve better output and capacitor voltage control performance. Meanwhile, the modulation strategy can also generate multilevel dc-link voltages, which is an advantage compared with traditional topologies.

V. Simulation and Experimental Verifications

In this section, both the simulation and experimental verifications are carried out with the parameters listed in Table IV. The unipolar carrier-based PWM introduced in Section IV is adopted and the carrier frequency is 2 kHz.

TABLE IV
Simulation and Experiment Parameters

Parameters	Simulation	Experiment
DC current: I_{dc}	10A	4A
DC inductance: L_{diff}	5mH	5mH
Flying capacitor: C_F	120μF	120μF
Output filter: C_{fi}	120μF	120μF
Carrier frequency: f_s	2kHz	2kHz
Load impedance: R/L	6Ω/5mH	6Ω/5mH

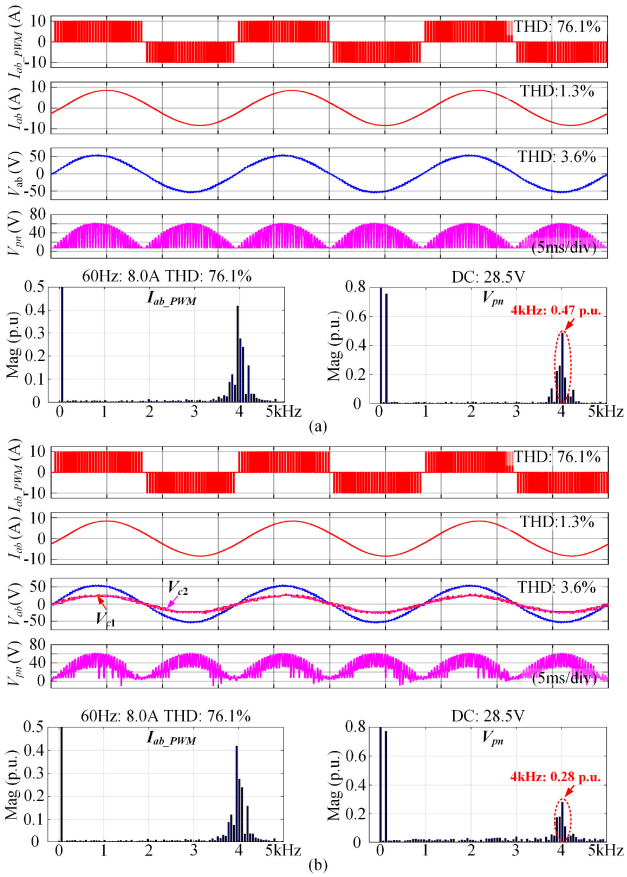

Fig. 10. Simulation results of single-phase CSC ($m_a = 0.8$). (a) Traditional DSC CSC with two series-connected devices. (b) One-stage FCC-CSC.

A. Simulation Results

Fig. 10(a) and (b) shows the simulation results of single-phase traditional DSC CSC with two series-connected devices and proposed one-stage FCC-CSC (as shown in Fig. 2) with one flying capacitor per bridge, respectively. The flying capacitor clamping voltage is regulated as half of the line voltage to make sure the device blocking voltage can be reduced to half of the line voltage as analyzed in Section III.

As it can be seen, the equivalent switching frequency is doubled to 4 kHz by adopting unipolar PWM for both traditional DSC CSC with series-connected devices and proposed FCC-CSC. The FCC-CSC can guarantee similar ac output quality as traditional DSC CSC according to the fast Fourier transform (FFT) results. The total harmonic distribution (THD) of output

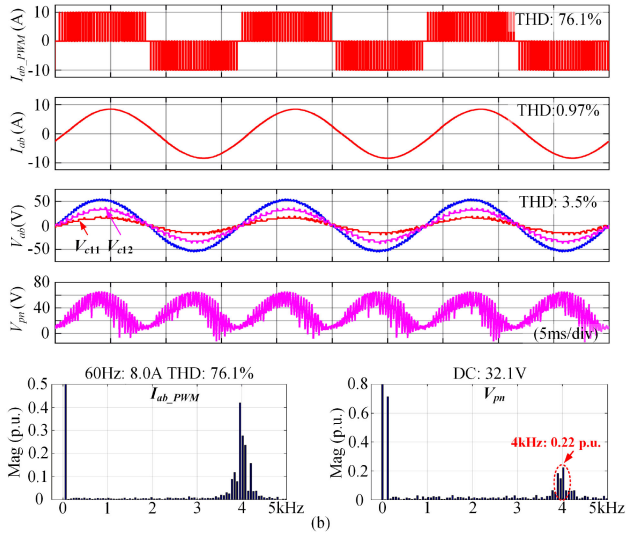

Fig. 11. Simulation results of single-phase two-stage FCC-CSC.

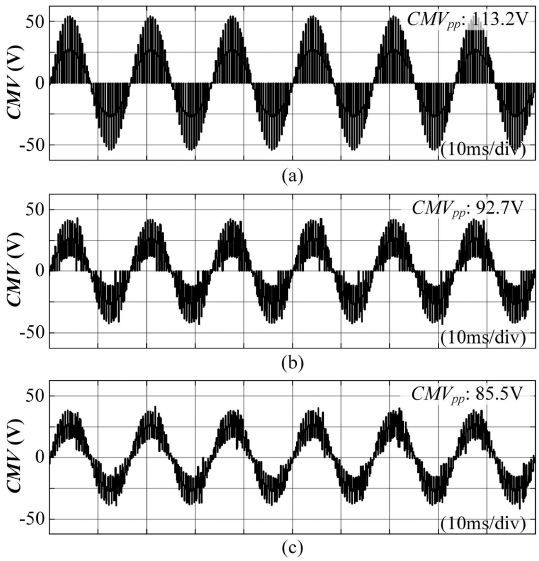

Fig. 12. Simulation results of CMV for single-phase CSC. (a) Traditional DSC CSC. (b) One-stage FCC-CSC. (c) Two-stage FCC-CSC.

current PWM for both traditional DSC CSC and FCC-CSC is 76.1%. While more voltage level of dc-link voltage and the dominant high-frequency harmonic (4 kHz) can be effectively suppressed from 0.47 to 0.28 p.u. with lower dv/dt. Meanwhile, the flying capacitor clamping voltages can be regulated to half of the output voltage with small fluctuation.

To further verify the effectiveness of the proposed FCC-CSC topology, a two-stage FCC-CSC is verified as another example of N-stage FCC-CSC as indicated in Fig. 5(b), the simulation results are shown in Fig. 11. There are two flying capacitors per bridge for two-stage FCC-CSC, and the clamping voltages are regulated to 1/3 and 2/3 of line voltage to make sure that the device blocking voltage to be 1/3 of line voltage. Similar to one-stage FCC-CSC, the ac output performance of two-stage

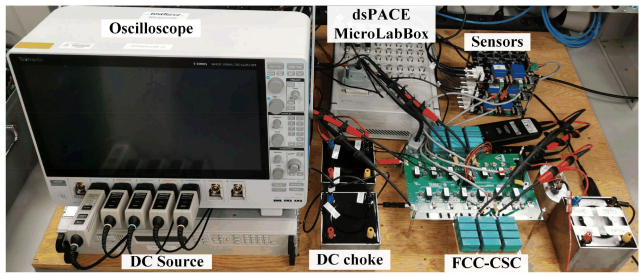

Fig. 13. Experiment setup of the single-phase FCC-CSC.

FCC-CSC can keep the same as traditional DSC CSC with better ac-link voltage quality. The clamping voltages of the two flying capacitors on the upper bridge can be regulated to 1/3 and 2/3 of the ac voltage effectively. The dominant high-frequency harmonic (4 kHz) in the dc-link voltage can be further suppressed to 0.22 p.u. This is because more voltage levels can be generated with an increased number of stages.

Besides the dc-link voltage quality improvement which is verified as above, another benefit of the proposed FCC-CSC is the increased voltage levels of CMV, which can potentionally generate smaller CMV. Fig. 12 shows the CMV comparison of traditional DSC CSC, one-stage FCC-CSC, and two-stage FCC-CSC, the peak to peak CMV values are 113.2, 92.7, and 85.5 V, respectively. It can verify that smaller CMV can be guaranteed with the proposed FCC-CSC topology.

The simulation results verify that the proposed FCC-CSC and the modulation strategy, as well as the flying capacitor voltage control method, can work effectively. Superior dc-link voltage performance and reduced CMV can be achieved simultaneously compared with the traditional DSC CSC.

B. Experimental Results

Fig. 13 shows the experiment setup of single-phase FCC-CSC, a dc source is adopted to provide constant dc-link current which is set as 4 A. The active switch is designed by series-connected MOSFET (C3M0032120K) and Diode (IDWD40G120C5). A dSPACE MicroLabBox DS1202 is adopted to generate the gating signals and achieve the flying capacitor clamping voltage control.

Fig. 14(a) and (b) shows the steady-state experiment results of traditional single-phase CSC with two series-connected switches and the proposed single-phase one-stage FCC-CSC, respectively. The modulation index is 0.8 and the output frequency is 60 Hz. For the ac output comparison, the FFT results of output voltage show that the traditional DSC CSC and proposed FCC-CSC have a similar ac output quality and the THDs are both 4.8%. This is because the gating signals of S_{an1}, S_{bn1}, S_{ap2}, and S_{bp2} adopted for the proposed FCC-CSC are exactly the same as traditional DSC CSC. The dominant high-frequency harmonic of the output voltage is doubled to 4 kHz by adopting the unipolar PWM. For the dc-link voltage comparison, the dc-link voltage of traditional DSC CSC is the envelope of output voltage and the maximum voltage step is the magnitude of line voltage. While the multilevel dc-link voltage with lower dv/dt can be achieved

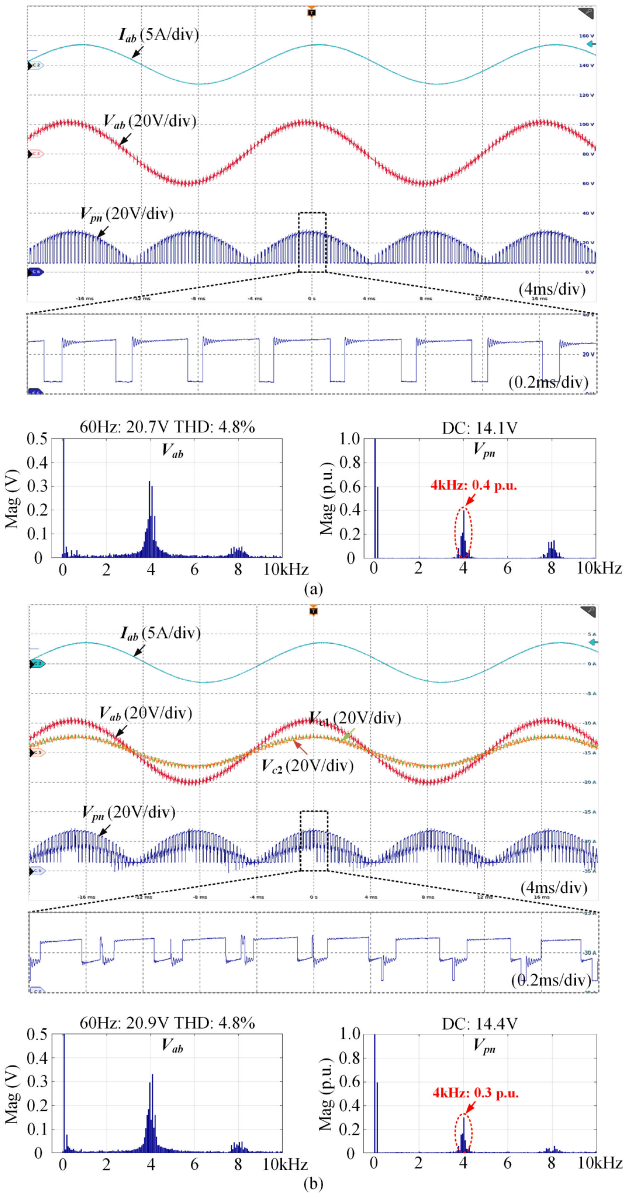

Fig. 14. Steady-state experimental results. (a) Traditional single-phase CSC with two series-connected devices. (b) Single-phase one-stage FCC-CSC.

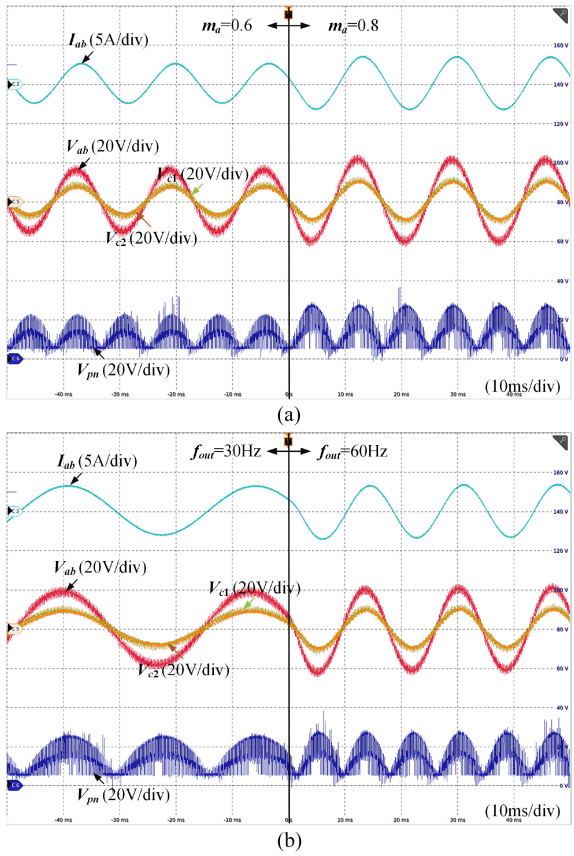

Fig. 15. Transient experimental results of single-phase FCC-CSC. (a) Modulation index change. (b) Output frequency change.

by adopting FCC-CSC and the flying capacitor clamping voltages can be controlled to half of the line voltage to reduce the device blocking voltage. The high-frequency component (e.g., 4 kHz component) in dc-link voltage can be effectively reduced from 0.4 to 0.3 p.u. As a result, the quality of the dc-link voltage can be improved.

The transient experiment results by adopting proposed methods for FCC-CSC are shown in Fig. 15. As can be seen, the proposed method can achieve good performance in terms of ac output and dc-link voltage during the modulation index and output frequency change as shown in Fig. 15 (a) and (b), respectively. The flying capacitor clamping voltages can be controlled to half of the output voltage actively during the transient. Multilevel dc-link voltage can be achieved with lower dv/dt and ripples. The improved quality of dc-link voltage guaranteed by the proposed topology can help to reduce the dc-link filter size potentially.

Besides the dc-link voltage quality improvement with low dv/dt, the possible voltage levels of CMV generated by the proposed FCC-CSC also increased. Fig. 16 shows the CMV comparison of traditional DSC CSC and proposed FCC-CSC, as can be seen, the peak to peak value can be reduced from 45.3 to 36.6 V, which is almost a 20% reduction.

Since the ac-type flying capacitors are adopted in the proposed FCC-CSC topology, the clamping voltages should be controlled with ac voltage, which is fundamentally different from the flying capacitors (with dc-type voltages) in the voltage-source counterpart. Therefore, the converter can be smoothly started up when the ac voltages cross to zero as shown in Fig. 17. For digital implementation, a trigger signal can be generated to turn ON the converter when the voltage phase angle reaches zero. As a result, the flying capacitor voltages can be regulated from zero.

To further compare the loss between traditional single-phase DSC CSC and FCC-CSC, the converter losses measured by the power analyzer (YOKOGAWA WT5000) under different dc-link current are shown in Fig. 18. The measured converter loss includes the device losses, ac filter loss, and the flying capacitor loss is also included for FCC-CSC. It shows that measured converter losses of the two converters are similar,

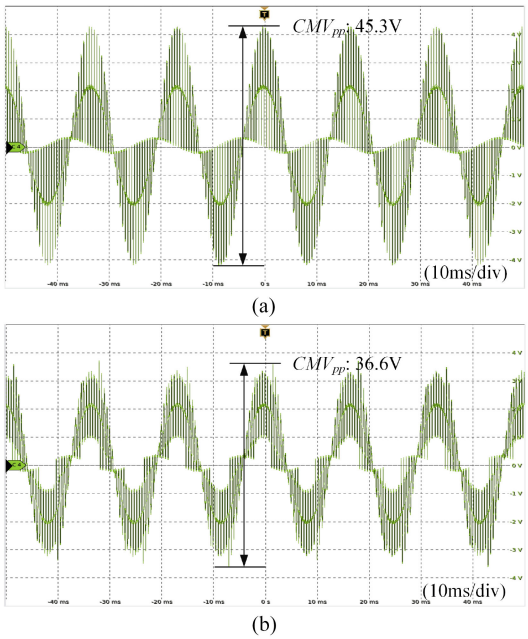

Fig. 16. Experimental results of CMV. (a) Traditional single-phase CSC with two series-connected devices. (b) Single-phase one-stage FCC-CSC.

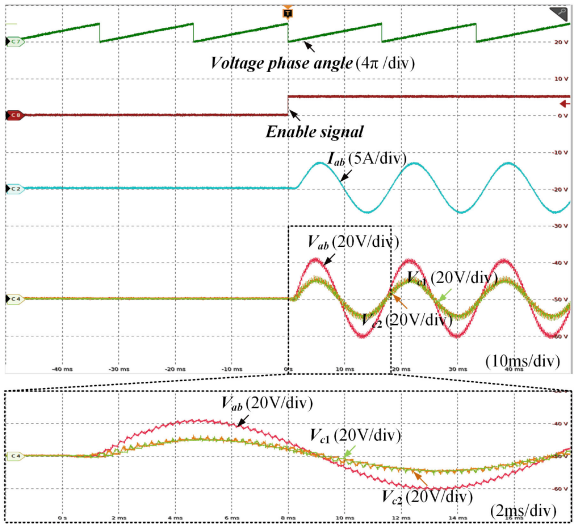

Fig. 17. Startup process of single-phase one-stage FCC-CSC.

where the converter loss of FCC-CSC is slightly higher than that of traditional DSC CSC, e.g., 0.7, 3.3, and 2.8 W difference when the dc-link currents are 10, 12, and 14 A, respectively. It shows that the added flying capacitor loss is very small. But the proposed topology does have many benefits such as multilevel dc-link voltage, lower dv/dt, and smaller CMV, etc.

In summary, the experiments verify that the proposed FCC-CSC can eliminate drawbacks of DSC CSC topology as shown in Table V. The ac output quality can be guaranteed similar to traditional DSC CSC. More importantly, the flying capacitor voltage can be controlled actively to part of the line voltage to reduce the device blocking voltages. Therefore, multilevel

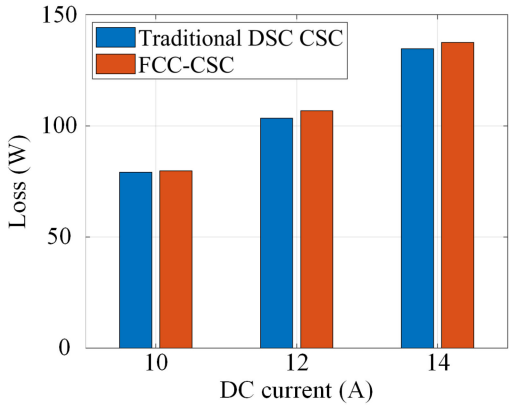

Fig. 18. Measured converter loss comparison under different dc-link current.

TABLE V
EXPERIMENTAL COMPARISONS BETWEEN THE TRADITIONAL DSC CSC AND THE PROPOSED FCC-CSC

Features of single-phase topology	Traditional DSC CSC	Proposed FCC-CSC
Switching devices (Same voltage rating)	8 MOSFET	8 MOSFET
	8 Diode	8 Diode
Passive devices (Same voltage rating)	1 AC-type capacitor	3 AC-type capacitors
AC-side power quality	THD=4.8%	
DC-link voltage quality	4kHz: 0.4 p.u.	4kHz: 0.3 p.u.
DC-side dv/dt	Full line to line	1/2 line to line
Peak CMV values	45.3V	36.6V
Voltage blocking technique	Device series connection	AC-type flying capacitor

dc-link voltage can be achieved with lower dv/dt and better quality. Simultaneously, the CMV of FCC-CSC can also be reduced effectively.

VI. CONCLUSION

In this article, FCC-CSC topology is invented through the isomorphic theory. Compared to traditional DSC CSC topology, it has the same active devices, the ac flying capacitors are used to clamp the device voltage to partial of output voltage, therefore the system voltage rating can be increased without the series device or converter connection. A unipolar carrier-based PWM and flying capacitor clamping voltage regulation methods are developed to produce sinusoidal outputs and control the clamping voltage actively. Meanwhile, multilevel dc-link voltage can be achieved with reduced ripples and dv/dt. At the same time, the CMV can be reduced due to increased switching state flexibility. The feasibility of the proposed FCC-CSC is verified by simulation and experiment results. Different from the existing CSCs, the proposed new type of converter shows great potential for applications requiring low dc-link dv/dt and low CMV and can benefit from using low-voltage devices for higher voltage.

REFERENCES

[1] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2786–2797, Jul. 2008.

[2] K. Gnanasambandam, A. K. Rathore, A. Edpuganti, D. Srinivasan, and J. Rodriguez, "Current-fed multilevel converters: An overview of circuit topologies, modulation techniques, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3382–3401, May 2017.

[3] C. Saber, D. Labrousse, B. Revol, and A. Gascher, "Challenges facing PFC of a single-phase on-board charger for electric vehicles based on a current source active rectifier input stage," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6192–6202, Sep. 2016.

[4] V. Madonna, G. Migliazza, P. Giangrande, E. Lorenzani, G. Buticchi, and M. Galea, "The rebirth of the current source inverter: Advantages for aerospace motor design," *IEEE Ind. Electron. Mag.*, vol. 13, no. 4, pp. 65–76, Dec. 2019.

[5] N. R. Zargari, S. C. Rizzo, Y. Xiao, H. Iwamoto, K. Satoh, and J. F. Donlon, "A new current-source converter using a symmetric gate-commutated thyristor (SGCT)," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 896–903, May/Jun. 2001.

[6] B. Wu, *High-Power Converters and AC Drives*. Hoboken, NJ, USA: Wiley, 2006, pp. 189–218.

[7] T. M. Jahns, and B. Sarlioglu, "The incredible shrinking motor drive: Accelerating the transition to integrated motor drives," *IEEE Power Electron. Mag.*, vol. 7, no. 3, pp. 18–27, Sep. 2020.

[8] N. R. Zargari, Z. Cheng, and R. Paes, "A guide to matching medium-voltage drive topology to petrochemical applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1912–1920, Mar./Apr. 2018.

[9] H. Kazuno, "Commutation of a three-phase thyristor bridge with commutation capacitors and series diodes," *Elec. Eng. Jpn.*, vol. 90, pp. 91–100, 1970.

[10] X. Guo, D. Xu, and B. Wu, "Four-Leg current-source inverter with a new space vector modulation for common-mode voltage suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6003–6007, Oct. 2015.

[11] J. He *et al.*, "A fault-tolerant operation approach for grid-tied five-phase current-source converters with one-phase supplying wire broken," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6200–6218, Jul. 2019.

[12] X. Guo, "A novel CH5 inverter for single-phase transformerless photovoltaic system applications," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 64, no. 10, pp. 1197–1201, Oct. 2017.

[13] X. Guo, "Three-Phase CH7 inverter with a new space vector modulation to reduce leakage current for transformerless photovoltaic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 708–712, Jun. 2017.

[14] S. Nishikata, and F. Tatsuta, "A new interconnecting method for wind turbine/generators in a wind farm and basic performances of the integrated system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 468–475, Feb. 2010.

[15] P. Liu, Z. Wang, Q. Song, Y. Xu, and M. Cheng, "Optimized SVM and remedial control strategy for cascaded current-source-converters-based dual three-phase PMSM drives system," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6153–6164, Jun. 2020.

[16] D. Xu, N. R. Zargari, B. Wu, J. Wiseman, B. Yuwen, and S. Rizzo, "A medium voltage AC drive with parallel current source inverters for high power applications," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, 2005, pp. 2277–2283.

[17] L. Ding, Z. Quan, and Y. W. Li, "Common-mode voltage reduction for parallel CSC-fed motor drives with multilevel modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6555–6566, Aug. 2018.

[18] L. Ding, and Y. Li, "Multilevel CSC system based on series-parallel connected three-phase modules with optimized carrier-shift SPWM," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3957–3966, Apr. 2021.

[19] F. Gao, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Pulse width modulated buck-boost five-level current source inverters," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Austin, TX, USA, 2008, pp. 469–475.

[20] F. Gao, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Five-Level current-source inverters with buck–boost and inductive-current balancing capabilities," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2613–2622, Aug. 2010.

[21] Suroso and T. Noguchi, "Common-emitter topology of multilevel current-source pulse width modulation inverter with chopper-based dc current sources," *IET Power Electron.*, vol. 4, no. 7, pp. 759–766, Aug. 2011.

[22] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[23] X. Guo, Y. Yang, and X. Wang, "Optimal space vector modulation of current-source converter for DC-Link current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1671–1680, Mar. 2019.

[24] X. Guo, N. Wang, J. Zhang, B. Wang, and M. Nguyen, "A novel transformerless current source inverter for leakage current reduction," *IEEE Access*, vol. 7, pp. 50681–50690, 2019.

[25] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[26] Y. Li, L. Ding, and Y. W. Li, "Isomorphic relationships between voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7131–7135, Aug. 2019.

[27] Y. Li, and Y. W. Li, "Power converters topological transformation using dual and isomorphic principles," *IEEE Open J. Power Electron.*, vol. 1, pp. 74–87, 2020.

[28] T. A. Meynard *et al.*, "Multicell converters: Derived topologies," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 978–987, Oct. 2002.

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