A Highly Reliable Single-Phase AC to Three-Phase AC Converter With a Small Link Capacitor

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***Abstract*—Single-phase ac to three-phase ac converters are needed in numerous applications, including motor drives used for residential applications. These converters, however, suffer from an inherent problem of mismatch between instantaneous input and output powers. Specifically, the instantaneous input power has a dc component along with an alternating component with double-line frequency, while the three-phase instantaneous output power is only dc. Conventional single-phase ac to three-phase ac converters use large electrolytic capacitors to handle this mismatch of power. However, these electrolytic capacitors may have high failure rates, which contribute to reduced lifetime of the converters. Moreover, these capacitors can be bulky and heavy. This article introduces a new single-phase ac to three-phase ac converter that uses a small film capacitor instead of large electrolytic capacitors. Despite using a small film capacitor, the double-line frequency harmonic does not appear at the input or output currents/voltages. The principles of the operation of the proposed topology are presented in this article, and its performance is evaluated through both simulations and experiments.**

***Index Terms*—AC−AC conversion, adjustable speed drives, double-line frequency ripple, universal converter.**

I. Introduction

THE GROWING dependency on renewable energy sources and the wide range of electrical loads in residential and industrial applications demand the next generation of power electronic circuits to be more flexible. For example, it is beneficial if they are capable of transferring electrical power from different types of input sources, including dc, single-phase ac, or multiphase ac, to different types of loads (dc, single-phase ac, or multiphase ac), without compromising reliability, cost, efficiency, or power density. This leads to difficult technical challenges, particularly when the instantaneous values of input and output power are not equal. Among these applications are dc to single-phase ac and single-phase ac to three-phase ac converters, the latter of which is common in residential motor drives. In single-phase ac to three-phase ac converters, the source power has both a dc component and an alternating component at twice the frequency of the source voltage; whereas, the instantaneous power of a three-phase ac load is a constant dc value. The mismatch of instantaneous input and output powers makes developing a reliable and compact power converter more challenging.

The simplest approach to transfer power from a single-phase ac source to a three-phase ac load is to use a first stage diode bridge to create a dc-link voltage with small ripple. Then the dc-link voltage is cascaded with a three-phase active bridge to power the load. Despite simplicity of this structure, there two major concerns associated with it. First, a large electrolytic capacitor is usually needed at the link to keep the dc-link voltage ripple as small as possible. Failure to reduce the dc bus voltage ripple may result in considerable distortion in the output waveforms and a high total harmonic distortion (THD). Second, the input power factor is low and additional power factor correction circuits are required. Nonunity power factor leads to larger values of the input current and lower utilization factor.

Replacing the diode bridge with a single-phase four-switch active bridge helps the converter to achieve a unity power factor. This strategy results in another group of single-phase ac to three-phase ac converters that are formed by cascading the single-phase pulsewidth modulation (PWM) rectifier and a three-phase inverter decoupled through a large electrolytic capacitor [1]. Several topologies with smaller number of switches have been proposed in [2] and [3] where two of the output switches are replaced by two identical capacitors. The core structure of these topologies consists of four switches and four free-wheeling diodes (B4). These topologies still require high capacitance valued electrolytic capacitors for suppressing the double frequency harmonic, and these electrolytic capacitors have shorter lifetime than film capacitors due to wear-out degradation phenomena [4], [5]. Eliminating the electrolytic capacitors in a power converter and replacing it with small film capacitors is one of the effective solutions for increasing the lifetime of a power converter. Although significant amount of research has been undertaken on improving the reliability of single-phase inverters [6], [7], only a small number of papers have concentrated on electrolytic-capacitor-less single-phase ac to three-phase ac converters [8], [9].

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Single-phase ac to three-phase ac matrix converters, in which the dc-link capacitor is eliminated, were proposed in [10] to improve the lifetime and power density. One possible drawback of these topologies is that the voltage gain is limited. Moreover, the double frequency harmonic still appears at the output currents [1]. In [11], a single-stage single-phase ac to three-phase ac converter is introduced to eliminate the electrolytic capacitor; nonetheless, large tapped coupled inductors are used at the link, which negatively affects the power density of the converter.

Eliminating or reducing the size of the dc-link electrolytic capacitor increases double-line frequency ripples across the link voltage, which leads to unwanted harmonics at the input/output and high THD. Several solutions have been reported in the literature based on additional passive or active elements attached to the converter to compensate or decouple double-line frequency ripple on the dc-link bus.

Among the passive approaches, using an inductor to manage the ripple power and helping the link capacitor to compensate the power mismatch is another technique that is proposed in [12]. Again, though, sometimes the inductor must be large, causing the drawbacks of lower power density and additional power loss due to inductor equivalent resistance. In [13], another inductor-based topology is proposed in which the link inductor is the main energy transferring component and an active capacitor-based compensator is used to suppress double-line frequency harmonic. The topology has the benefits of soft-switching operation but with the possible drawback of larger number of semiconductor switches. Connecting active circuit compensators at the link [14] is one of the main solutions that many researchers have been focusing on. These power decoupling structures can be based on bidirectional buck [15], boost [16], [17], flyback [18] converters, or any other bidirectional dc−dc topology. Of course, the tradeoff is that there is added extra circuitry and sometimes [18], for instance, high peak value of the current flowing through the transformer. In [19], a flying capacitor architecture has been added to two-stage single-phase inverter at the expense of two additional semiconductor switches to decouple double-line frequency harmonics. A small capacitor is placed in series with the traditional dc-link capacitor that is controlled using pulse currents to cancel out the dc-link voltage ripple in [20]. These capacitive methods may even have the benefit of smaller size compared to inductive methods but suffer from the typical pulsating currents found in switched capacitor circuits.

Changing the shape of the reference current/voltage to balance the dc-link voltage in single-phase ac to three-phase ac converters is one of the solutions that has been reported in a number of papers. In [21], the shape of the input reference current has been modified to a square root of a sinusoidal waveform synchronized with the single-phase input source voltage, and, in [22], a trapezoidal torque waveform is injected to the motor control scheme to compensate the dc-link voltage and the mismatch of instantaneous input and output power. Both methods address the issue at the expense of high input current THD and higher low-frequency harmonics spectrum of it. A state feedback control based on average voltage constrain is used in [23] to improve the vulnerability of the system to controller parameters that is a shortcoming of the ideas proposed in [22]. Adding third and fifth harmonics to the reference of the single-phase ac current is another method that has been reported in the literature [24]−[27]. However, this method reduces the input power factor extensively and is not a practical solution for higher power applications. The dc-link voltage reshaping or swing bus operation is another technique that has been used in two stage power converters [28]−[30]. In order to avoid overmodulation, the dc-link capacitance and voltage have to be carefully selected in this technique, which drastically increases the sensitivity of the converter control scheme to the parameters. Changing the control scheme is another approach that has been investigated recently. In [31], a modified PWM approach is proposed to allow 20% ripple swing at the dc bus. Using a dual-loop control method based on sliding mode control is reported in [32] that mitigates 2ω ripples as well. Nonetheless, the complexity of the control can be highlighted in these works.

Another limitation of most of the state-of-the-art single-phase ac to three-phase ac converters, including the topologies proposed in [2], [3], and [10], is that galvanic isolation can only be provided through low frequency transformers that are bulky, heavy, and expensive.

Recently, a family of single-stage capacitive-link universal converters has emerged, which can be used in a wide range of applications, including dc to three-phase ac inverters [33] and three-phase ac to three-phase ac converters [34], [35], [36]. In these converters, only a small film capacitor is used to absorb the energy from the source in the first portion of a switching cycle and discharge the energy to the load in the second portion of a switching cycle. Since the instantaneous power of the input and the output are both constant [35]−[37], there is no technical concern about any ac double-line frequency ripple at the link capacitor voltage.

This article broadens the operation of universal converters to single-phase ac to three-phase ac systems. The research presented in this article derives control schemes to manage the mismatch of instantaneous input and output powers, while eliminating the need for large electrolytic capacitors. The approach is to permit the voltage across the link capacitor, which is placed in series with the input and output switch bridges, to have a large voltage ripple; however, the converter is controlled such that this ripple does not affect the input/output currents or voltages. The topology is bidirectional. Given that the proposed converter belongs to the family of capacitive-link universal converters, in which the isolation is provided through single-phase high frequency transformers, it can be configured as an isolated configuration in a similar way, too. However, the leakage inductance of the transformer can cause voltage spikes and ringing in the isolated single-phase to three-phase ac converter; therefore, a Snubber may be necessary for the isolated configuration. This article only focuses on the nonisolated configuration. For applications that require unidirectional flow of power, a modified topology with a smaller number of switches is derived. This converter was first proposed by the authors in conference paper [38]. This article presents a deep dive analysis of the topology, extends the application of this converter to motor drives, and introduces extensive experimental results. Additionally, a novel

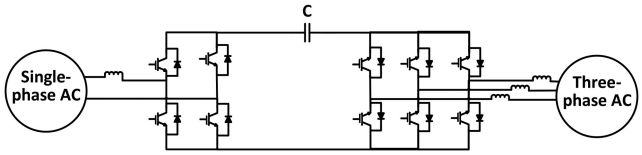

Fig. 1. Proposed bidirectional single-phase ac to three-phase ac converter.

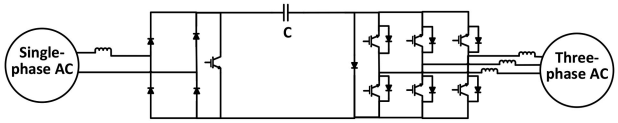

Fig. 2. Proposed unidirectional single-phase ac to three-phase ac converter.

control method is proposed in this article. This control method is able to successfully drive an electric motor as will be demonstrated in the experimental results. The proposed controller is fast enough to draw adequate current from the input source and compensate any sharp and fast load changes. Although motor drive application may not require a very fast controller (like field programmable gate array (FPGAs) or fast analog to digital converter (ADCs)), the proposed control method can be used for faster and more demanding loads like controlled current three-phase load. The proposed control method can be implemented in regular microcontrollers with not very fast ADCs as the sampling time of it can be as low as its switching frequency.

The rest of this article if organized as follows. Section II introduces the proposed topology and presents its principles of the operation. Design and analysis of the converter will be discussed in Section III. The proposed control method will be presented in Section IV. The proposed single-phase ac to three-phase ac converter will be evaluated through simulation and experiments in Sections V and VI, respectively, and its efficiency will be analyzed in Section VII. Finally, Section VIII presents the conclusion.

II. Proposed Topology and Principles of the Operation

Fig. 1 depicts the proposed bidirectional single-phase ac to three-phase ac converters. For applications with unidirectional power flow, the proposed topology can be modified as shown in Fig. 2. The proposed converter transfers power entirely through a series link capacitor, which is first charged from the source and then is discharged into the load.

The proposed single-phase ac to three-phase ac converter has four operating modes in each switching cycle. If the power flows from the single-phase ac source toward the three-phase ac load, there will be one charging mode, two discharging modes, and a mode during which no power is transferred. Fig. 3 shows the behavior of the converter in each of the modes.

For the time span considered in Fig. 3, $I_{\rm in}$, $I_{\rm Ao}$, and $I_{\rm Co}$ are positive (left to right) and $I_{\rm Bo}$ is negative (right to left). Assuming that the three line-to-line reference voltages that need to be generated at the output of the converter are

$$v_{\rm ab}\ (t) = V_{\rm mo}\sin\left(2\pi f_o t\right) \tag{1}$$

$$v_{\rm bc}\ (t) = V_{\rm mo}\sin\left(2\pi f_o t - 2\pi/3\right) \tag{2}$$

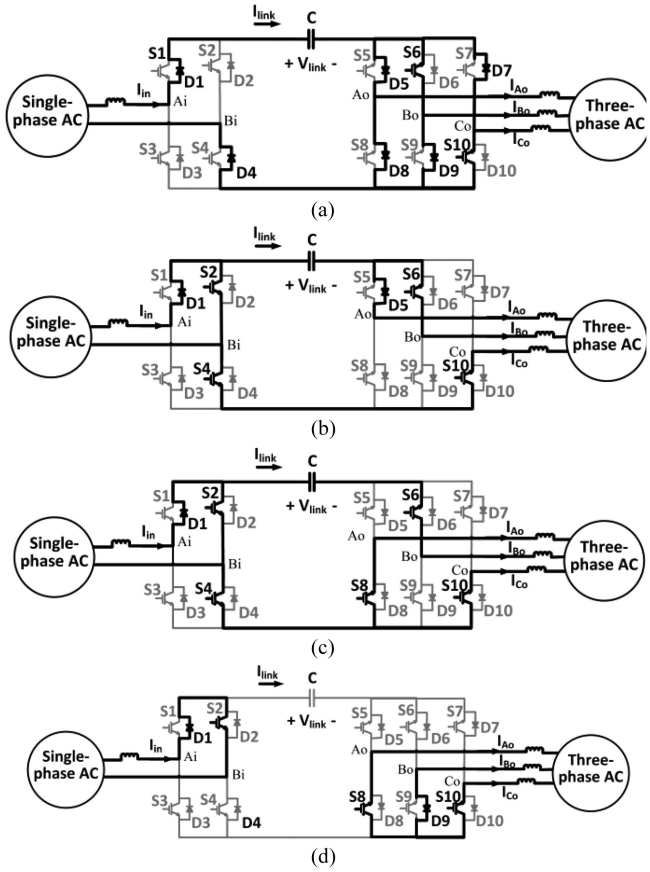

Fig. 3. Principles of the operation of the proposed bidirectional single-phase ac to three-phase ac converter. (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4 .

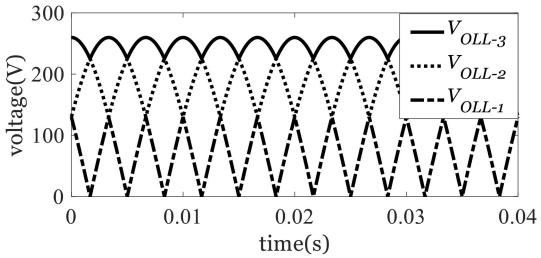

Fig. 4. Comparison of output line-to-line reference voltages.

$$v_{\rm ca}\ (t) = V_{\rm mo}\sin\left(2\pi f_o t + \frac{2\pi}{3}\right). \tag{3}$$

At any moment, the line-to-line reference voltage that has the maximum absolute value is called $V_{\rm OLL-3}$, the line-to-line reference voltage that has the second highest absolute value is called $V_{\rm OLL-2}$, and, finally, the one with the minimum absolute value is named $V_{\rm OLL-1}$. For instance, for a 50-Hz, 150-V reference system, the above waveforms are shown in Fig. 4.

For the case shown in Fig. 3, the voltage across the output phase pair BCo is assumed to have the maximum line-to-line output voltage and it is negative. Moreover, voltage reference of ABo has the second maximum absolute value, CAo holds the minimum absolute value, and both are positive. Also, assuming the input current is positive, the operation of the converter during

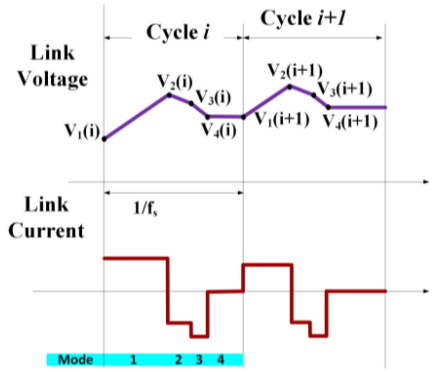

Fig. 5. Link voltage and current for a single-phase ac to three-phase ac configuration when instantaneous input power is higher than instantaneous output power ($P_{\rm in}(t) > P_o(t)$).

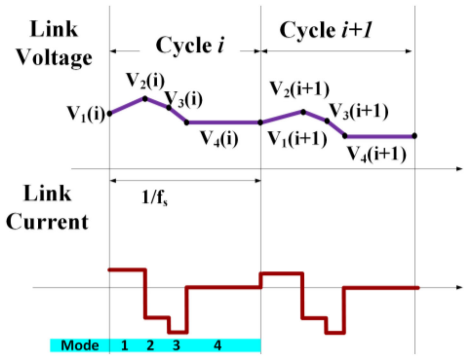

Fig. 6. Link voltage and current for a single-phase ac to three-phase ac configuration when instantaneous input power is lower than instantaneous output power ($P_{\rm in}(t) < P_o(t)$).

each mode is described below. It is clear that the phase pair carrying the maximum line-to-line voltage and its polarity continuously change over a load/source cycle. Also, the polarities of the input and output currents change over a load/source cycle.

As depicted in Fig. 3, during mode 1, diodes D1 and D4 at the input side and diodes D5, D8, D7, and D9 along with switches S6 and S10 at the output-side conduct. Depending on the instantaneous values of the input current, $I_{\rm in}$, and $I_{\rm Bo}$, which is the largest output current for the case assumed in Fig. 3, diodes D10 and D6 might also conduct; however, this does not affect the operation of the converter as the output side bridge is in shoot-through state during mode 1. The input current passes through the link capacitor and charges it during this mode. In mode 2, switches S2 and S4 are turned ON and diodes D8, D4, D7, and D9 stop conducting. During this mode, $-|I_{\rm Co}|$ passes through the link capacitor, and since this current is negative, the link capacitor starts discharging. To end this mode and initiate mode 3, switch S8 is turned ON. By turning ON switch S8, diode D5 stops conducting, and $-|I_{Bo}|$ passes through the link capacitor. The link capacitor continues discharging during mode 3. To end this mode, which is the last power transferring mode, switches S6 and S4 will be tuned OFF, and diode D9 starts to conduct. During mode 4, the link current is zero, and the link voltage remains constant.

Figs. 5 and 6 show the link voltage and link current of this converter during different modes. In Fig. 5, it is assumed that the instantaneous input power is higher than the output power, and, in Fig. 6, it is assumed that the instantaneous input power is lower than the output power. Although either the ac input current or the ac output current flows through the link capacitor during modes 1 to 3, and these currents are sinusoidal, they can be considered almost constant in the fast switching cycle. The voltage of the link capacitor at the beginning of modes $1-4$ in any arbitrary cycle (ith cycle) is expressed as $V_1(i)$, $V_2(i)$, $V_3(i)$, and $V_4(i)$, respectively. During the fourth mode, no current passes the link capacitor, and the link voltage remains equal to $V_4(i)$. During the first mode (charging mode), the input current flows into the link capacitor and charges the capacitor. This results in an increase of the link voltage from $V_1(i)$ to $V_2(i)$. During the second and third modes (discharging modes), the load currents passes the link capacitor. However, the current of the link capacitor during these modes is negative. This results in a decrease of the link voltage from $V_2(i)$ to $V_3(i)$ and from $V_3(i)$ to $V_4(i)$ in modes 2 and 3, respectively. As shown in Figs. 5 and 6, if the instantaneous value of the input power is higher than the instantaneous value of the output power, $V_4(i)$ (which is equal to $V_1(i+1)$) will be higher than $V_1(i)$; otherwise, $V_4(i)$ will be lower than $V_1(i)$.

Fig. 7 depicts the unfiltered line-to-line input and output voltages, in addition to the link voltage and link current for two successive switching cycles. As seen in this figure, the unfiltered input voltage (V_{AiBi} in Fig. 3) is equal to the link voltage during mode 1, and it is zero in all other modes. The voltage across the output phase pair with maximum line-to-line voltage, which is labeled as $V_{\rm OLL\_3\_unfiltered}$ in Fig. 7 ($V_{\rm BCo}$in Fig. 3), is equal to the link voltage in modes 2 and 3, and it is zero in modes 1 and 4. The other two line-to-line output voltages that are labeled as $V_{\rm OLL\_1\_unfiltered}$ (line-to-line voltage with minimum absolute reference value—$V_{\rm CAo}$ in Fig. 3) and $V_{\rm OLL\_2\_unfiltered}$ (second maximum line-to-line voltage—$V_{\rm ABo}$ in Fig. 3) are equal to the link voltage either in mode 2 or 3. By filtering the unfiltered line-to-line voltages, the output sinusoidal waveforms can be generated and also the input current can be controlled.

More information on selecting the proper switches at the output side can be found in [33] and [34]. Depending on the instantaneous values of the three-phase line-to-line output voltage references and the load currents, a load cycle is divided into 12 zones, and the switching pattern over in each zone can be determined.

$V_1(i)$, $V_2(i)$, $V_3(i)$, and $V_4(i)$ can be calculated based on the instantaneous values of the input and output powers. The input power that is injected to link capacitor during mode 1 can be determined by multiplying the input voltage by the input current. Moreover, input current and voltage can be formulated based on $V_1(i)$, $V_2(i)$, link capacitor, and switching frequency. Following specifies the relationship between them.

To make sure the input current and input voltage are properly regulated in each arbitrary cycle (cycle i) and the voltage changes of the link capacitor do not affect the input current/voltage, the average of the unfiltered input voltage, $V_{\rm AiBi}$, (labeled in Fig. 3), must be equal to the reference voltage $v_{\rm in}(t)$ as formulated in (4). This reference $v_{\rm in}(t)$ can be calculated using the input source

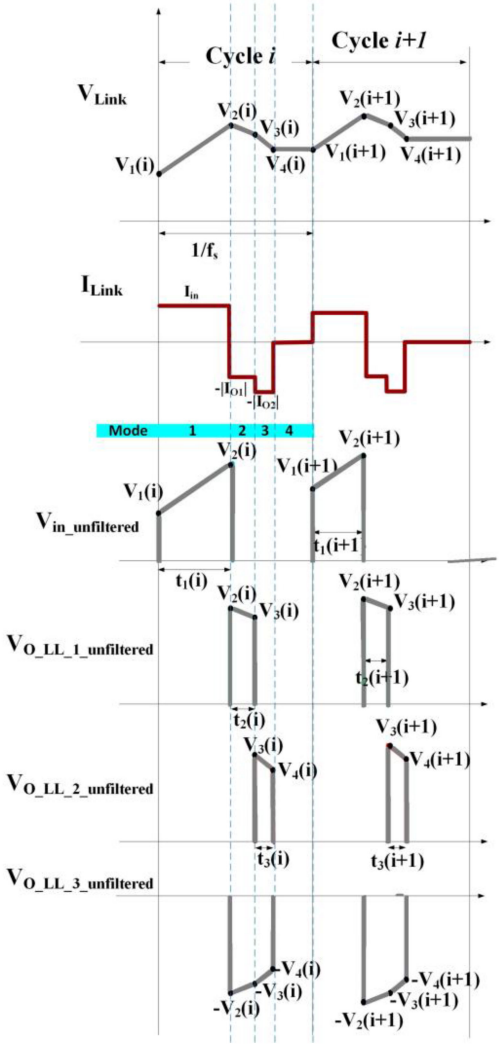

Fig. 7. Link voltage, link current, unfiltered input, and output line-to-line voltages.

voltage ($v_{\rm src}(t)$), input current reference, and the input filter inductance. In other words, $v_{\rm in}(t)$ is equal to $v_{\rm src}(t)$ minus the voltage drop across the input inductor at steady-state operation (Kirchhoffs Voltage Law (KVL) at the input side loop). During mode 1, the input current ($I_{\rm in}(t)$) flows through the link, increasing the link voltage from $V_1(i)$ to $V_2(i)$. Even though $I_{\rm in}(t)$ is an ac current with the input source frequency, it can be considered a dc current for the time duration of each switching cycle, as the switching frequency is assumed to be much higher than the input source frequency. The relationship among $V_1(i)$, $V_2(i)$, and $I_{in}(t)$ is shown in (5). According to Fig. 7, the following equations must be valid:

$$v_{\rm in}\ (t) = 0.5\left(V_1\ (i) + V_2\ (i)\right) t_1\ (i)\ f_s \tag{4}$$

$$I_{\rm in}\ (t) = C\frac{V_2\ (i) - V_1\ (i)}{t_1\ (i)} \tag{5}$$

$$P_{\rm in}\ (t) = v_{\rm in}\ (t)\, I_{\rm in}\ (t)\ = 0.5\left(V_2^2\ (i) - V_1^2\ (i)\right) C f_s \tag{6}$$

where f_s and $t_1(i)$ are the switching frequency and duration of mode 1 in *i*th cycle, respectively.

The output power is equal to the average power that is transferred from the link capacitor to the output during modes 2 and 3, which are denoted by $P_{o1}(t)$ and $P_{o2}(t)$, respectively. These values can be calculated by multiplying the current and average voltage of the link capacitor during modes 2 and 3, the same way that input power is calculated in (6). More accurately, $P_{o1}(t)$ is the average power transferred during mode 2, $P_{o2}(t)$ is the average power transferred during mode 3, and $P_o(t)$ is the average power transferred during modes 2 and 3, which is equal to the average input and output power values. It can be shown that the following equations must be valid to properly regulate the output currents/voltages and eliminate the double frequency harmonic from these current and voltages:

$$P_{o1}\ (t) = V_{\rm OLL\_1}\,(t)\, i_{o1}\ (t) = 0.5\left(V_2^2\ (i) - V_3^2\ (i)\right) C f_s \tag{7}$$

$$P_{o2}\ (t) = V_{\rm OLL\_2}\,(t)\, i_{o2}\ (t) = 0.5\left(V_3^2\ (i) - V_1^2\ (i+1)\right) C f_s \tag{8}$$

$$P_o\ (t) = P_{o1}\ (t) + P_{o2}\,(t)\ = 0.5\left(V_2^2\ (i) - V_1^2\ (i+1)\right) C f_s. \tag{9}$$

In (7), $V_{\rm OLL-1}(t)$ is the reference of $V_{\rm OLL\_1\_unfiltered}$ and $i_{o1}(t)$ is the output phase current discharging the link capacitor in mode 2, which is $I_{\rm Co}$ in the case assumed in Fig. 3. Similarly, $V_{\rm OLL-2}(t)$ is the reference of $V_{\rm OLL\_2\_unfiltered}$ and $i_{o2}(t)$ is the output phase current discharging the link capacitor in mode 3, which is $I_{\rm Ao}$ in the case assumed in Fig. 3. Using (4)−(9), the link voltage at the end of modes 1−3 ($V_2(i)$, $V_3(i)$, and $V_4(i)$) can be determined. Duration of each mode can be calculated as follows using the references of the unfiltered voltages:

$$t_1\ (i) = \frac{2|v_{\rm in}\ (t)\,|}{\left(V_1\ (i) + V_2\ (i)\right) f_s} \tag{10}$$

$$t_2\ (i) = \frac{2V_{O\_LL\_1}\,(t)}{\left(V_2\ (i) + V_3\ (i)\right) f_s} \tag{11}$$

$$t_3\ (i) = \frac{2V_{O\_LL\_2}\,(t)}{\left(V_3\ (i) + V_4\ (i)\right) f_s} \tag{12}$$

$$t_4\ (i) = \frac{1}{f_s}\ - t_1\ (i) - t_2\ (i) - t_3\ (i)\,. \tag{13}$$

Fig. 8(a) shows the duty cycles of each mode which can be simply calculated by multiplying time duration of each mode derived above by the switching frequency. For the implementation purposes, it is important to know the accumulated duty cycles of each mode, as shown in Fig. 8(b). Using the duty cycle information provided in this figure, the exact moment that each switch needs to be ON/OFF with respect to the start of a switching cycle can be determined.

Equations (10)–(13) will be used later in the article (Section IV) to control the converter and generate appropriate duty cycle references for the switches.

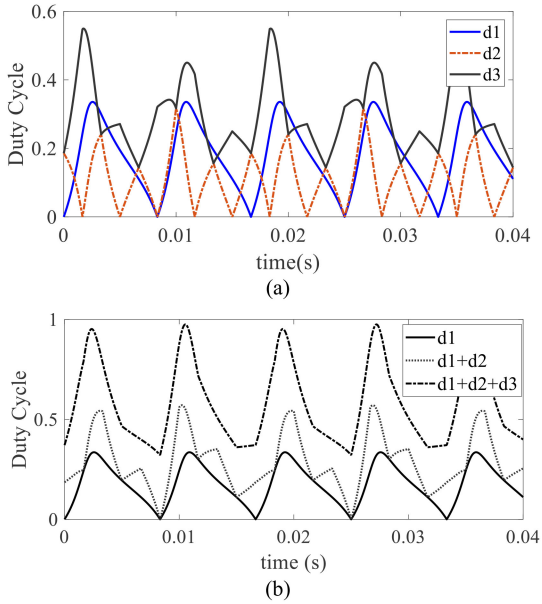

Fig. 8. Duty cycles for each mode for 60-Hz input 50-Hz output systems. (a) Individual duty cycles. (b) Accumulated duty cycle.

III. Design and Analysis

A. Design and Analysis of the Link Capacitor

The input current ($i_{\rm in}(t)$) and voltage ($v_{\rm src}(t)$) and current and voltage of phase A of the three-phase ac load are expressed by the following equations:

$$v_{\rm src}\ (t) = V_{\rm mi}\ \sin\left(2\pi f_i t + \theta_{\rm Vi}\right) \tag{14}$$

$$I_{\rm in}\ (t) = I_{\rm mi}\ \sin\left(2\pi f_i t + \theta_{Ii}\right) \tag{15}$$

$$v_{\rm Ao}\ (t) = V_{\rm mo}\ \sin\left(2\pi f_o t + \theta_{\rm Vo}\right) \tag{16}$$

$$i_{\rm Ao}\ (t) = I_{\rm mo}\ \sin\left(2\pi f_o t + \theta_{\rm Io}\right). \tag{17}$$

The instantaneous power of the input can be calculated by multiplication of $v_{\rm in}$ and $i_{\rm in}$, which results in the following equation:

$$P_{\rm in}\ (t) = \frac{I_{\rm mi}V_{\rm mi}}{2}\ \left\{\cos\left(\theta_{\rm Vi} - \theta_{Ii}\right) - \cos\left(4\pi f_i t + \theta_{\rm Vi} + \theta_{Ii}\right)\right\}. \tag{18}$$

Similarly, the instantaneous output power can be calculated as

$$\begin{aligned} P_o\ (t) &= P_{\rm Ao}\ (t) + P_{\rm Bo}\,(t) + P_{\rm Co}\ (t) \\ &= \frac{3I_{\rm mo}V_{\rm mo}}{2}\ \cos\left(\theta_{\rm Vo} - \theta_{\rm Io}\right). \end{aligned} \tag{19}$$

The dc component of the input power in (18) is equal to the output power:

$$\frac{I_{\rm mi}V_{\rm mi}}{2}\ \cos\left(\theta_{\rm Vi} - \theta_{Ii}\right) = \frac{3I_{\rm mo}V_{\rm mo}}{2}\ \cos\left(\theta_{\rm Vo} - \theta_{\rm Io}\right). \tag{20}$$

The mismatch of input and output power values needs to be managed by the link capacitor. Therefore, the instantaneous power of the link capacitor is equal to

$$P_c\ (t) = \frac{I_{\rm mi}V_{\rm mi}}{2}\ \cos\left(4\pi f_i t + \theta_{\rm Vi} + \theta_{Ii}\right). \tag{21}$$

As a result, the energy of the capacitor is

$$E_c\ (t) = \int_{t_0}^{t} P_c\,(\tau)\,d\tau = \frac{1}{2}Cv_c(t)^2 - \frac{1}{2}CV_{C0}^2 \tag{22}$$

where V_{C0} is the dc component of the link capacitor voltage when the capacitor is large ($C \to \infty$). Without loss of generality, assuming $t_0 = 0$ leads to

$$v_c\ (t) = \sqrt{\frac{I_{\rm mi}V_{\rm mi}}{4\pi f_i C}\ \sin\left(4\pi f_i t + \theta_{\rm Vi} + \theta_{Ii}\right) + V_{C0}^2}. \tag{23}$$

The voltage across the link capacitor will increase when the instantaneous input power is higher than the load power, and it will decrease when the load power is higher than the instantaneous input power. Fig. 9 shows the waveform of the link voltage ($v_c(t)$) with respect to the input voltage when C is chosen to be 20 μF and $V_{C0} =$ 600 V for a 2.5-kW system.

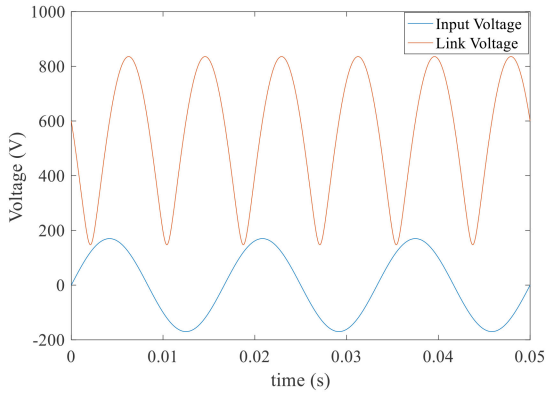

Fig. 9. Link voltage and the input voltage waveforms when $V_{C0} = 600$ V.

Although the net energy of the link capacitor in each switching cycle is not zero, its net energy over a $2f_i$ cycle is zero. The peak value of the link voltage is as follows:

$$V_{\rm link,\ max} = \sqrt{\frac{I_{\rm mi}V_{\rm mi}}{4\pi f_i C} + V_{C0}^2}. \tag{24}$$

According to (24), choosing a smaller value for C will result in having a higher link peak voltage.

The size of the link capacitor in the proposed converter can be determined similar to conventional dc-link converters:

$$C\ = \frac{I_{\rm mi}V_{\rm mi}}{4\pi f_i * V_{\rm dc} * \Delta V_{\rm dc}} \tag{25}$$

where $V_{\rm dc}$ is the average voltage of the link capacitor and $\Delta V_{\rm dc}$ is the voltage ripple across the link capacitor. In dc-link converters for proper operation of the converter, $\Delta V_{\rm dc}$ must be very small; whereas, in the proposed converter, $\Delta V_{\rm dc}$ can be very large without affecting the input or output currents/voltages, thus allowing the designer to use a small link capacitor at the link. Different values of the link capacitance result in different values for the link voltage ripple. Fig. 10 indicates the different

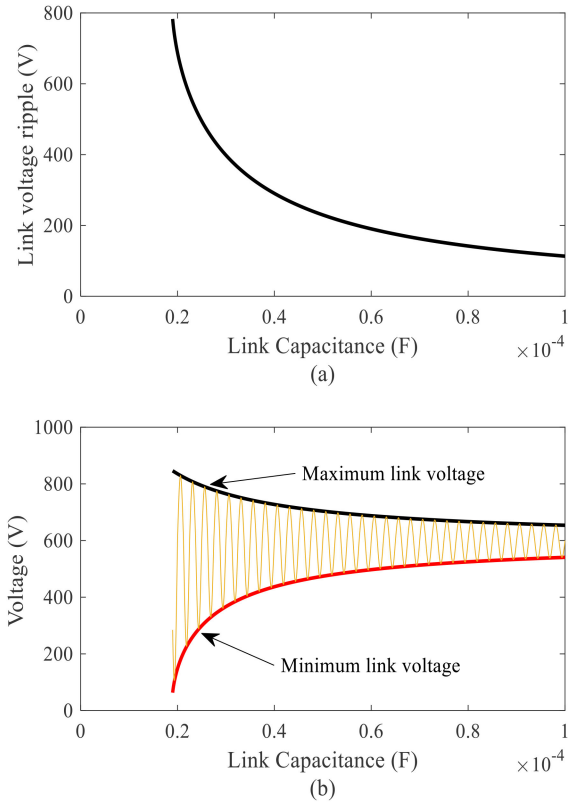

Fig. 10. (a) Link voltage ripple vs. link capacitance. (b) Maximum and minimum values of the link voltage vs. link capacitance when $V_{C0} = 600$ V.

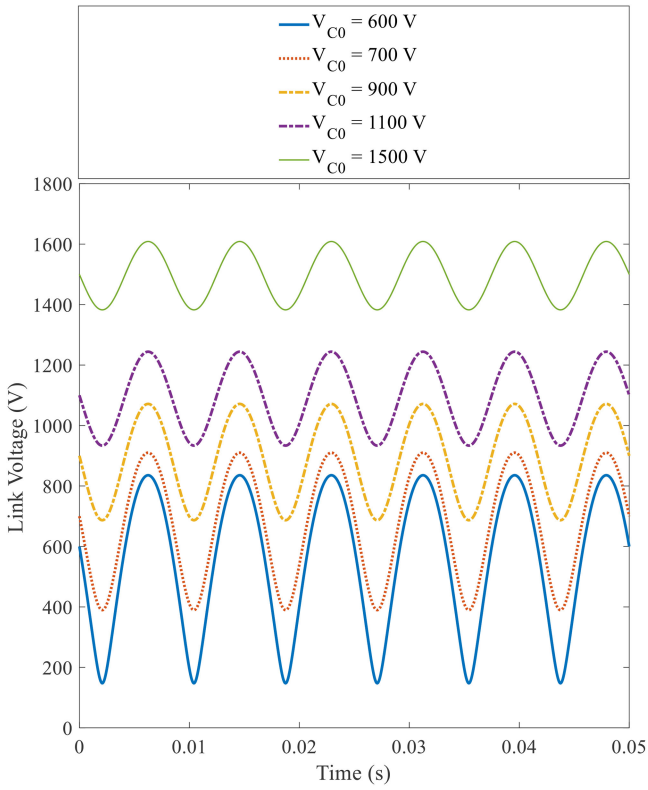

Fig. 11. Link voltage waveform for different values of V_{C0}.

values for the link voltage when different link capacitances are chosen. Fig. 10(a) shows the link voltage ripple for different values of the link capacitor. Obviously, lower values of the link capacitor results in lower dc ripple, but it should be noted that this relationship is not linear, and below a certain capacitance, a small change in the link capacitance causes a drastic change in the voltage ripple. As a result, choosing the link capacitance close to the knee point of the curve can be a good choice. Fig. 10(b) shows the maximum and minimum values of the link voltage when $V_{C0} = 600$ V. By choosing larger values for the link capacitance, obviously, the link voltage ripple and maximum value of the link voltage reduce.

The other parameter that affects the link voltage is V_{C0} is specified in (23). Selecting larger values for V_{C0} leads to smaller values for the link voltage ripple but, at the same time, increases the peak value of the link capacitor voltage, which is the voltage that needs to be blocked by the semiconductor switches. Fig. 11 shows the effect of V_{C0} on the link voltage for a 2.5-kW system with a 20-μF link capacitance. As exhibited in this figure, by choosing $V_{C0} = 600$ V, the link voltage swings between 160 and 820 V, which leads to a high dc-link voltage ripple. Opting $V_{C0} = 1500$ V reduces the ripple, while it increases the link peak voltage to 1600 V.

B. Input and Output Filter Design

In order to design the input and output inductors, the simplified model of the converter during the four modes of operation should be considered. During modes 2−4, the input source voltage charges the input inductor. Even though this voltage is a sinusoidal voltage, during each switching cycle, it can be considered as a dc source. Therefore, current ripple of this inductor can be calculated as

$$\Delta\, I_{\text{in}} = \frac{v_{\text{in}}}{L_{\text{in}}}\ (t_2 + t_3 + t_4) = \frac{v_{\text{in}}}{L_{\text{in}}}\ (T_s - t_1) \tag{26}$$

where $t_i,\ i \in \{12, 34\}$ is the time duration of mode i, v_{in} is the input source voltage, L_{in} is the input side inductor, and T_s is the switching period ($1/f_s$). Substituting t_1 from (10) in (26) yields

$$\Delta\, I_{\text{in}} = \frac{v_{\text{in}}}{L_{\text{in}}}\left(T_s - \frac{2|v_{\text{in}}\,(t)\,|}{(V_1\,(i) + V_2\,(i))}T_s\right). \tag{27}$$

By taking the derivative of (27) and making it equal to zero, the maximum value of the input current ripple can be calculated as

$$\Delta I_{\text{in}}\ (\max) = \frac{(V_1\,(i) + V_2\,(i))}{L_{\text{in}}}\ T_s. \tag{28}$$

As $V_1(i)$ and $V_2(i)$ are almost close and equal to the link capacitor voltage, (28) can be approximated by

$$\Delta I_{\text{in}}\ (\max) = \frac{2V_{\text{link-max}}}{L_{\text{in}}}\ T_s \tag{29}$$

where $V_{\text{link-max}}$ is the maximum link voltage and is derived in (24). So, the input inductor value can be calculated based on the desired maximum input current ripple.

The behavior of the converter during modes 2 and 3 should be analyzed to design the value of the output side inductors

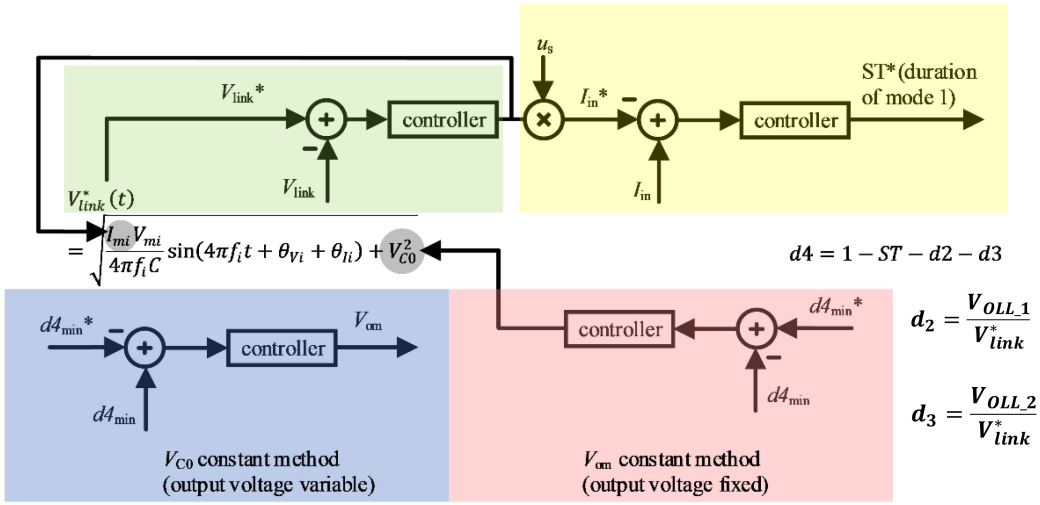

Fig. 12. Link capacitor voltage control.

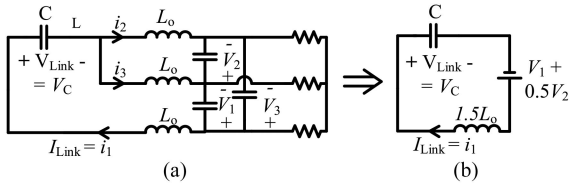

Fig. 13. Equivalent circuit of the converter during modes 2 and 3.

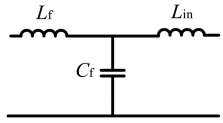

Fig. 14. *LCL* filter for the input side.

(L_o). Fig. 13(a) illustrates this equivalent circuit regardless of the operating zone. Even though the switching pattern for modes 2 and 3 are not the same, the equivalent circuit model of Fig. 13(a) can be used to derive differential equations describing the circuit in both modes. To simplify the three-phase circuit model of Fig. 13(a) into an equivalent circuit that is seen from the link perspective, the following equations can be considered:

$$V_1 - L_o\frac{di_1(t)}{dt} - V_C(t) - L_o\frac{di_3(t)}{dt} = 0 \tag{30}$$

$$V_2 + L_o\frac{di_3(t)}{dt} - L_o\frac{di_2(t)}{dt} = 0 \tag{31}$$

$$i_2(t) + i_3(t) = i_1(t). \tag{32}$$

Substituting $i_2(t)$ from (32) into (31) yields

$$V_2 + 2L_o\frac{di_3(t)}{dt} - L_o\frac{di_1(t)}{dt} = 0. \tag{33}$$

And finally, by replacing $\frac{di_3(t)}{dt}$ from (33) into (30), a simple differential equation between $i_1(t)$ and $V_C(t)$ can be derived as

$$V_1 + \frac{1}{2}V_2 - V_C(t) - \frac{3}{2}L_o\frac{di_1(t)}{dt} = 0. \tag{34}$$

Therefore, the equivalent circuit can be simplified as exhibited in Fig. 13(b). It is worth mentioning that although V_1, V_2, and V_3 are sinusoidal voltages, they are almost constant during each switching cycle and can be modeled as constant dc voltages.

The output current ripple can be calculated in the same manner as the input current ripple was calculated. To calculate the current ripple of the output inductors, the equivalent circuit of the converter during modes 1 and 4, when the output converter legs are shorted, can be considered; thus

$$2V_1 + V_2 = 3L_o\frac{di_1(t)}{dt} \tag{35}$$

$$\Delta I_o = \frac{2V_1 + V_2}{3L_o}\ (T_1) \tag{36}$$

where V_1 and V_2 are the output filtered line-to-line voltages; therefore, by substituting the maximum value of $2V_1 + V_2$ in a three-phase system, the maximum ripple, based on which L_o can be designed, is equal to

$$\Delta I_{o-\max} = \frac{\sqrt{3}V_{\mathrm{ll,peak}}}{3L_o}\ (t_1(\max) + t_4(\max)) \tag{37}$$

where $V_{\mathrm{ll,peak}}$ is the peak value of the line-to-line output voltage.

In order to further reduce the input current ripple, an additional *LC* filter stage is cascaded before the input inductor L_{in} as shown in Fig. 14.

C_f and L_f filter components are chosen based on traditional second-order low-pass filter design. The cutoff frequency of the filter can be chosen as

$$\frac{1}{\sqrt{L_f C_f}} = 0.1 * 2\pi f_s. \tag{38}$$

IV. Control Scheme and Implementation

Controlling the converter such that input and output currents/voltages meet their references, their THD values are low, and the converter response to any load demand appropriately is a critical task in the proposed converter. It will be shown that to

achieve these goals, the voltage of the link capacitor needs to be controlled precisely.

Fig. 12 shows the link capacitor voltage control block diagram that is proposed, implemented, and tested for this topology. In order to generate the link capacitor reference voltage, $V^*_{\rm link}\,(t)$ in Fig. 12, two parameters should be controlled as shown in Fig. 12 and in (23): $I_{\rm mi}$ and V_{C0}. One method is to consider a fixed valued for V_{C0}, leading to a variable output voltage amplitude $V_{\rm om}$. The other method, which is used in the experimental evaluation of the converter in Section VI, considers a constant value for $V_{\rm om}$ and changes V_{C0} such that the minimum value of mode-4 duration is as small as possible. Lowering the minimum value of mode 4 will reduce the link capacitor voltage. The utilization factor of the converter is increased, and semiconductors with lower voltage rating can be used. The red box in Fig. 12 illustrates the control blocks adjusting V_{C0}. The desired value of $d4^*_{\rm min}$ (minimum value of mode 4) can be as small as 0%. By comparing this value with the measured value of $d4_{\rm min}$ and passing the error through a controller, V^*_{C0} is achieved. The controller can be as simple as an up-counter/down-counter block based on the sign of the error. It is worth bearing in mind that $d4$ is a periodic signal with a fixed frequency that depends on the input and output frequencies. So, $d4_{\rm min}$ is detected by sampling d4.

After generating the reference value of the link capacitor voltage $V^*_{\rm link}\,(t)$, it is compared with the measured link voltage. As shown in the green box of Fig. 12, by comparing the reference value of the link capacitor voltage and its measured value, the amplitude of the reference input current is generated. The controller used for this purpose can be a PI controller. By multiplying the output of this controller by u_s, which is a unity amplitude signal synchronized with the input source voltage, the reference for the input current (I^*_{in}) is generated. This reference current is obviously in-phase with the input source voltage, providing unity power factor feature for the converter. It should be noted that the input current reference generated by the controller is also used for determining the reference link capacitor voltage ($V^*_{\rm link}$), as shown in Fig. 12.

As shown in the yellow box in Fig. 12, by comparing the input current reference ($I^*_{\rm in}$) and the measured input current and feeding their error signal into another controller, the duty cycle of mode 1 is generated. As the duration of mode 1 has a reverse impact on the amplitude of the input current (the shorter the duty cycle of mode 1, the larger the amplitude of the input current), reference current ($I^*_{\rm in}$) should be subtracted from the measured current ($I_{\rm in}$) in this case.

The bandwidth and the speed of each controller are critical factors for appropriate control of the converter. The inner current controller, for instance, should be faster than the outer loop link voltage controller. And the speed of the most outer loop controller, shown in red box in Fig. 12, should be the slowest controller.

In addition to the control block that generates the duty cycle of mode 1, the duration of the remaining modes needs to be calculated also. The time duration of each mode has been derived in (10)−(13). In (10)−(12), $V_j(i),\ j \in \{12, 34\}$, which is the link voltage at the end of modes $1-4$, can be considered almost constant and equal to $V^*_{\rm link}(t)$ during each switching cycle. Therefore, d_2, which is the duty cycle of mode 2, can be approximated as

$$d_2 = \frac{V_{\rm OLL_1}\,(t)}{V^*_{\rm link}}. \tag{39}$$

Similarly, the duty cycle of the third mode d_3 can be generated as

$$d_3 = \frac{V_{\rm OLL_2}\,(t)}{V^*_{\rm link}}. \tag{40}$$

And, finally, the last duty cycle, which is the duty cycle of the fourth mode, is equal to

$$d_4 = 1 - d_1 - d_2 - d_3. \tag{41}$$

When $V^*_{\rm link}$ has its minimum value, the controller needs to check the duty cycle of the last mode d_4 to make sure it is a positive value. The red box in the control block diagram of Fig. 12 is implemented for this purpose. This part of the control block makes sure that d_4 is positive. When $V^*_{\rm link}$ is very low, the controller increases V_{C0} to compensate for the effect of low $V^*_{\rm link}$ and avoid a modulation distortion.

TABLE I
PARAMETERS OF THE SIMULATED CONVERTER

Parameter	Value
Power	2500 W
Input Voltage (RMS)	120 V
Output Voltage Line-to-line (RMS)	208 V
Switching Frequency	36 kHz
Link Capacitance	20 μF
Input Frequency	60 Hz
Output Frequency	40 Hz

V. SIMULATION RESULTS

A 2.5-kW single-phase ac to three-phase ac converter with the parameters listed in Table I was designed and simulated in PSIM. According to (25), by choosing $V_{\rm dc} = 724$ V and $\Delta\, V_{\rm dc} =$ 450 V, the link capacitance can be as small as 20 μF, while, depending on the selected dc-link voltage ripple, in the conventional back-to-back converters, the link capacitor could be as large as 20 mF, assuming $V_{\rm dc} = 300$ V and 1% ripple allowance.

Fig. 15(a) shows the input current and voltage. As shown in this figure, the converter is controlled such that unity power factor is achieved. To show the performance of the converter in output voltage regulation, output line-to-line voltages have been exhibited in Fig. 15(b). The voltage of the link capacitor is depicted in Fig. 15(c). As expected, the link voltage has a double-line frequency ripple, which obeys (23). In spite of this high voltage ripple, the input and output voltages/currents do not contain any double frequency harmonics. The zoomed-in voltage across the link capacitor as well as the link current is depicted in Fig. 16. Different modes of operation are specified in this figure for the condition in which the instantaneous input power is higher than the output power.

In this simulation, *L* filters are used at the input and output. To improve the quality of the currents *LC* or *LCL* filters can be employed.

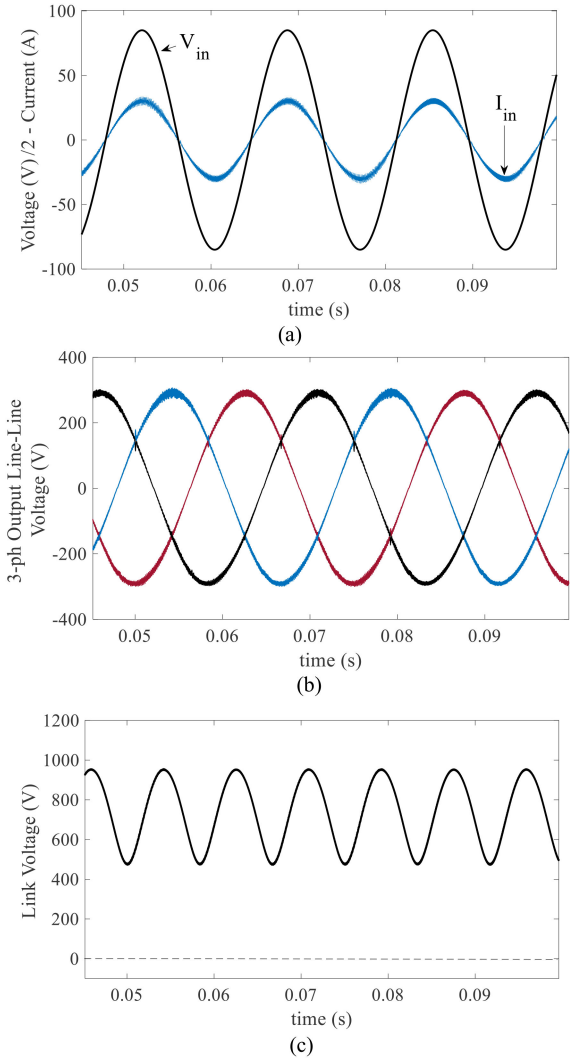

Fig. 15. Simulation of (a) input voltage and current, (b) output line−line voltage, and (c) link voltage.

TABLE II
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Power	2500 W
Input Voltage (RMS)	208 V
Output Voltage Line-to-line (RMS)	0-230 V
Switching Frequency	40 kHz
Link Capacitance	20 μF
Input Frequency	60 Hz
Output Frequency	0-60 Hz
RL load	R=17Ω, L=8mH
Induction Motor: 230V, 5 HP, 1750 rpm, 4-pole	

VI. EXPERIMENTAL RESULTS

The operation of the proposed converter is evaluated with an experimental prototype. Table II summarizes the specifications of the setup, which is a 2.5-kW SiC-based prototype operating at 40 kHz switching frequency. A photograph of the prototype is shown in Fig. 17. The prototype is tested for two types of loads: a three-phase RL load and a three-phase induction motor.

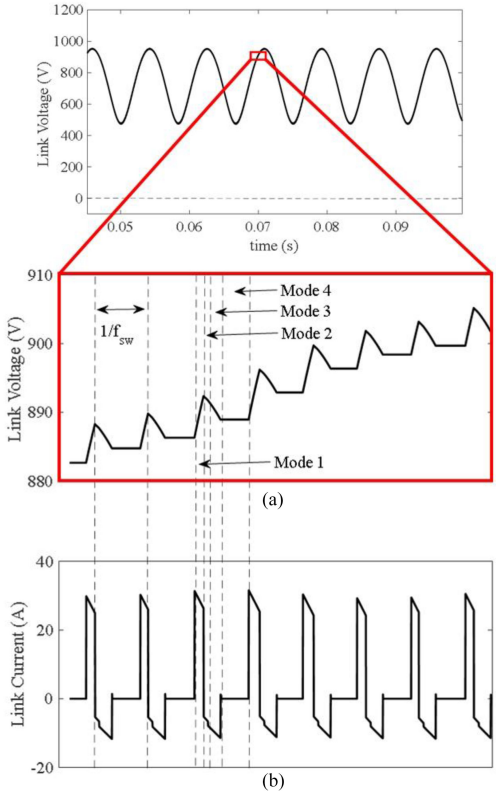

Fig. 16. Simulation of the waveforms of the link (a) voltage and (b) current.

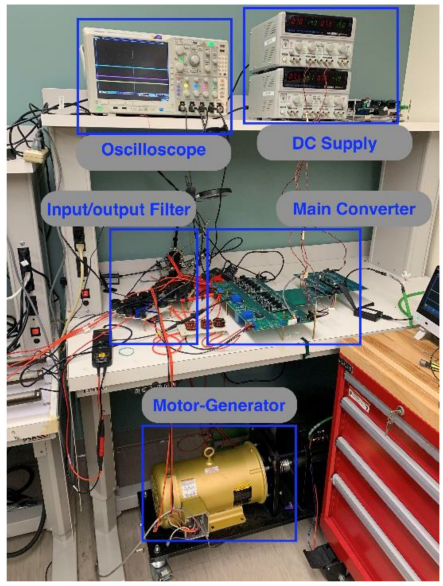

Fig. 17. Experimental prototype.

A. RL Load

The system is tested at two different operating points: full power and 50% of full power. Fig. 18(a) indicates the input current and voltage, which are in phase, as well as the link capacitor voltage. The large double-line frequency ripple of the link voltage does not affect the input or output currents/voltages. The input current THD in this case is about 2.3%. Fig. 18(b)

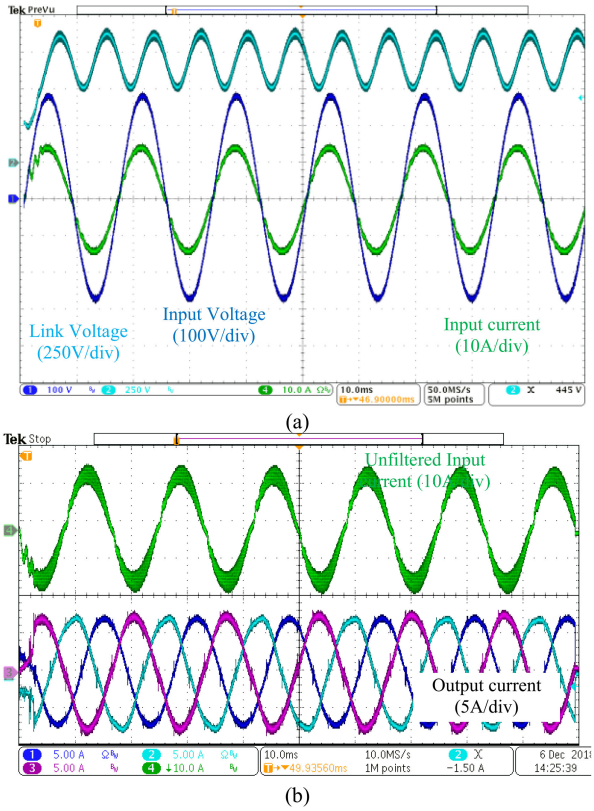

Fig. 18. Experimental result for full-power. (a) Input voltage, input current and link capacitor voltage. (b) Unfiltered input current and three-phase load currents.

shows the output load currents with THD value of about 3.5%. This validates the effectiveness of the control method in compensating the large double-line frequency of the link capacitor. An LCL filter is used at the input to reduce the total filter inductance of the converter. In order to show the effect of the LCL filter, the waveform of the input current before the filter is also shown in Fig. 16(b) that obviously has larger switching ripples than the filtered one which is shown in Fig. 18(a).

Fig. 19 depicts the test results when the load is reduced to 50% of its nominal value. Input line voltage as well as the filtered input current are illustrated in Fig. 19(a). Again, the unity power factor is achieved in spite of the power level change. The link capacitor voltage is demonstrated in Fig. 19(b). As expected, the peak-to-peak voltage ripple amplitude is lower than that of the full power level. The three-phase load currents as well as the unfiltered input current are shown in Fig. 19(c).

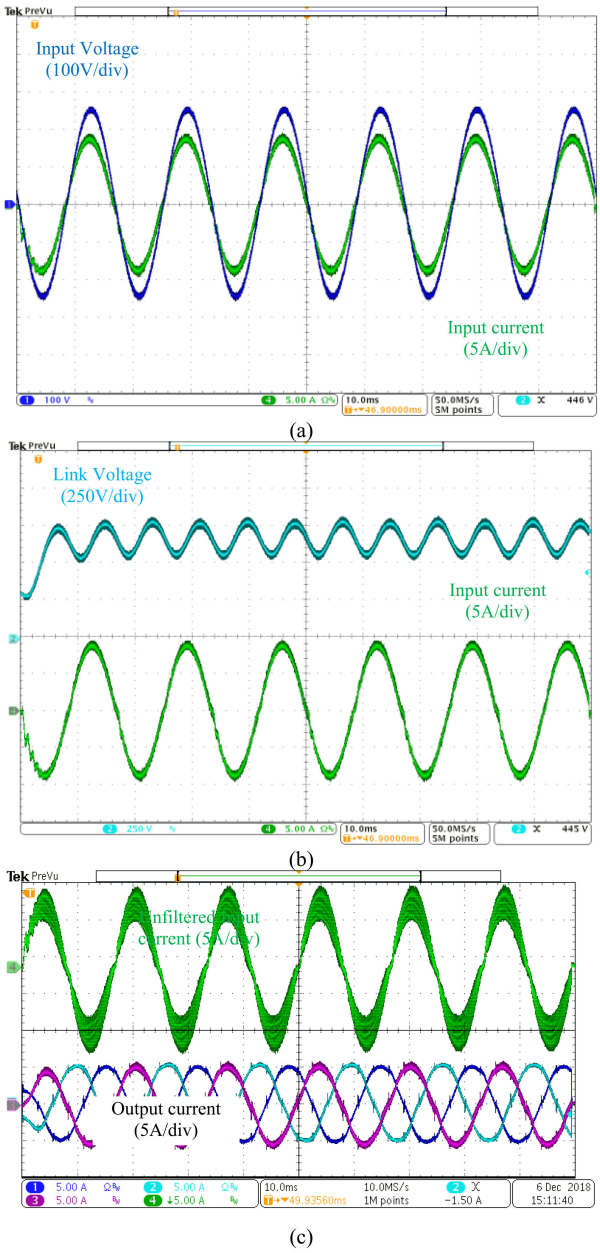

Fig. 19. Experimental result for 50% of full power. (a) Input voltage and current. (b) Link capacitor voltage. (c) Unfiltered input current and three-phase load currents.

B. Induction Motor Load

The performance of the converter and the proposed control method is further evaluated by driving a squirrel-cage induction motor using *V/f* control method. The specifications of the inductor motor can be found in Table II. Fig. 20 shows the speed of the rotor as it is built up to its nominal value using *V/f* control method [39]. The *V/f* control method controls the magnitude of frequency, voltage, or current. This control scheme maintains the air-gap flux of the induction motor constant, achieving higher run-time efficiency. In steady-state operation, the machine air-gap flux is approximately proportional to the ratio *Vs/fs*, where *Vs* is the amplitude of motor phase voltage and *fs* is the synchronous electrical frequency of the voltage applied to the motor. By increasing the voltage and the frequency with the same slope, the maximum value of the torque that the motor can handle remains almost constant. Details of this control method can be found at [39]–[41].

The stator currents, link capacitor voltage, and the single-phase input source current are shown in Fig. 21. As *V/f* control is used here for the startup, the frequency and the amplitude of the output three-phase voltages have been increased in several

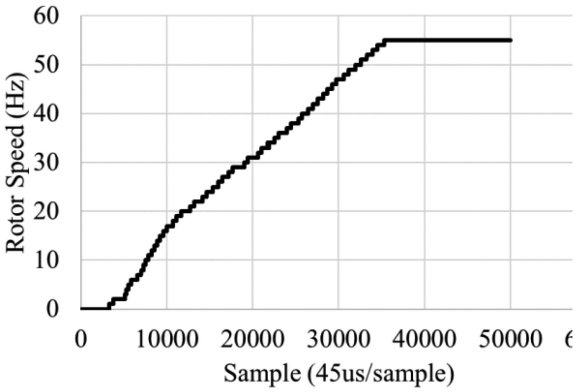

Fig. 20. Speed of the induction motor.

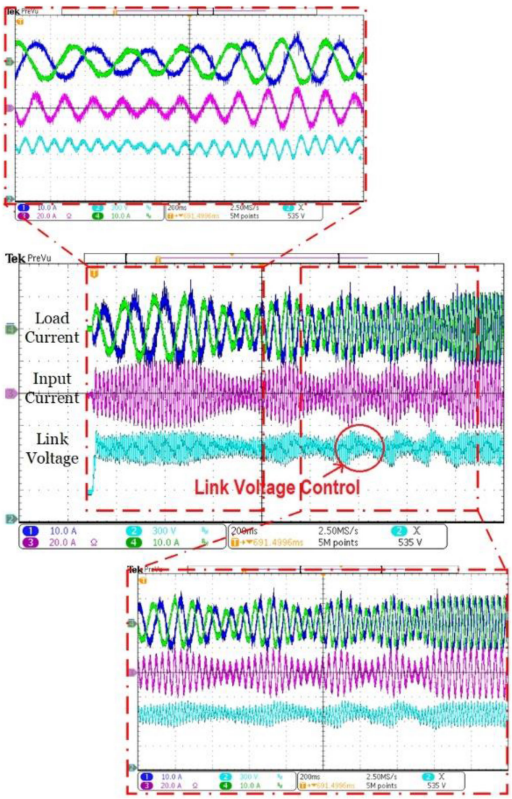

Fig. 21. Experimental results for some critical waveforms of the converter with motor load.

steps to provide a smooth startup transition as well as confining the input and output currents. The THD values of the input and output currents during the steady-state operation of the motor are 2.6% and 4.9%, respectively.

VII. Efficiency and Reliability

Owing to the use of SiC MOSFETs as main switches of the converter, a higher efficiency is expected compared to Si-based converter as the transition times are much shorter in SiC MOSFETs. This results in lower switching losses, which helps increasing the efficiency. Fig. 22 illustrates the efficiency curve

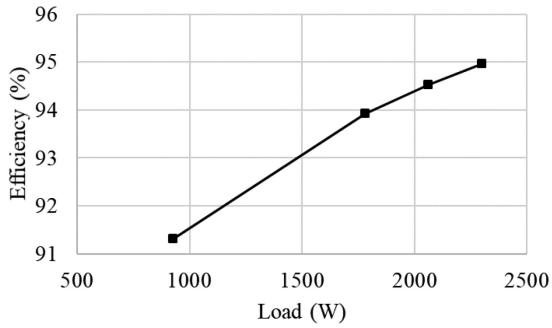

Fig. 22. Efficiency of the converter for different load power levels.

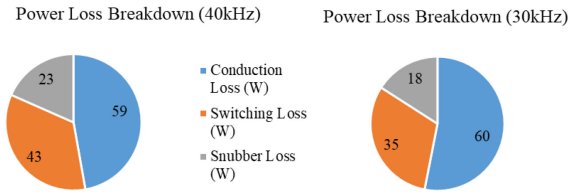

Fig. 23. Power loss breakdown charts for 30 and 40 kHz switching frequencies.

of the converter at different power levels with 40 kHz switching frequency.

To further investigate the impact of switching losses on the overall efficiency of the converter, power loss breakdown charts at two different switching frequencies are provided in Fig. 23. As shown in this figure, 47% of the total losses are due to conduction losses when operating at 40 kHz and switching losses account for about 35% of the total loss. When the switching frequency is reduced to 30 kHz, the conduction losses are slightly increased due to higher inductor current ripples, but the switching losses as well as the Snubber losses are reduced noticeably. The switching loss in this case accounts for only 30% of the total losses. Snubber losses are reduced by 22%.

The Snubber loss in the proposed converter may be slightly larger than conventional dc-link converters. Due to the parasitic inductance of the link path, a high voltage ringing is observed across the output side switches. This phenomenon is observed in conventional dc-bus converters as well; however, in the conventional dc-bus based converters, the parasitic inductance can be minimized by placing several small-sized capacitors as close as possible to the output side bridge in the experimental layout. But due to the presence of shoot-through state at the output bridge in the proposed converter, this method is not practical. Therefore, larger Snubbers are required in order to suppress the voltage ringing at the output side, which lead to a slightly lower efficiency compared to conventional approach as shown in Fig. 23. Moreover, the conduction losses of the proposed converter are slightly higher than the conventional approach since currents passing through switches/diodes in the proposed converter are slightly higher than those of the conventional converter.

As seen in Table II, the fabricated single-phase ac to three-phase ac converter requires only a 20-μF film capacitor, which is much smaller than the capacitors used in dc-link converter. This

significantly increases the reliability and reduces the volume and weight of the system. In general, the lifetime of a film capacitor is much longer than that of an electrolytic capacitor. One of the important factors affecting the reliability of capacitors is the ratio of applied voltage to voltage rating. Although the voltage applied across the link capacitor in the proposed converter is higher compared to dc-link converters, the voltage rating of the selected capacitor will also be higher, given that film capacitors are typically available at higher voltage ratings than electrolytic capacitors. Moreover, even though the current ripple of the link capacitor in the proposed converter is higher than the traditional dc-link converter, this has negligible impact on the reliability and temperature increase since the equivalent series resistor (ESR) of the film capacitors is typically very small. The higher voltage across the link capacitor in the proposed converter results in higher voltage rating of the switches, too. Nonetheless, by recent advances in high voltage wide bandgap switches, high voltage rating is not expected to be a key constrain. The cost of these switches is expected to reduce over time.

As discussed in Section III, the proposed converter needs *L* filters or *LCL* filters. The inductors typically have negligible impact on the overall lifetime of the converter. The filter capacitors are small film capacitors, and their specifications and ratings are similar to filter capacitors in conventional converters. Therefore, the impact of designed filters of the proposed converter on reliability and cost will be similar to that of conventional converters.

VIII. Conclusion

This article proposes a novel single-phase ac to three-phase ac converter that uses a small series capacitor for transferring power from input to output and handling the mismatch of instantaneous input and output power values. Despite using a small capacitor, the double-line frequency harmonic does not appear at either the input or output. In this article, the principles of the operation of the proposed converter are presented and its performance is evaluated through both simulations and experiments. The performance of the converter in driving an induction motor using *V/f* control is also verified in the experiments.

Acknowledgment

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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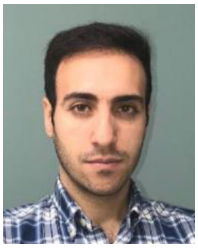

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