

A Generalized Selective Harmonic Elimination PWM Formulation With Common-Mode Voltage Reduction Ability for Multilevel Converters

Mingzhe Wu ¹, Student Member, IEEE, Cheng Xue ¹, Student Member, IEEE, Yun Wei Li ¹, Fellow, IEEE, and Kehu Yang ², Member, IEEE

Abstract—In this article, a generalized selective harmonic elimination pulsewidth modulation (SHE-PWM) formulation with common-mode voltage (CMV) reduction ability for multilevel converters (MLCs) is presented. The CMV is suppressed by regulating the low-order dominant zero-sequence harmonics (ZSHs) of the three-phase SHE-PWM waveforms. Two formulations are included in the proposed model to achieve the full range operation objective, i.e., with zero low-order ZSHs in low and medium modulation index (m_a) range and with an optimal third-harmonic injection in high m_a range. With the proposed formulation, the amplitude of CMV can be effectively reduced for all types of MLCs over the whole m_a range. Besides, two kinds of solving algorithms, i.e., off-line and real-time based, are introduced to provide efficient solution tools targeted at the proposed model. In this article, a case study with three-level neutral-point clamped inverters is discussed in detail to better illustrate the proposed formulation and the coupling effects between the CMV reduction and capacitor voltage balancing objectives of MLCs. Simulation and experimental results based on multiple MLC topologies are carried out to validate the effectiveness of this generalized SHE-PWM formulation with reduced CMV values.

Index Terms—Common-mode voltage (CMV), multilevel converters (MLCs), selective harmonic elimination (SHE).

I. INTRODUCTION

MULTILEVEL converters (MLCs) are widely implemented on various occasions of power conversion since the 1980s due to their numerous merits over the traditional two-level converters, including higher output voltage levels with low harmonic distortion, reduced electromagnetic interferences (EMI), etc. [1]–[3]. Some of the widely implemented or emerging multilevel topologies, e.g., three-level neutral-point clamped

Manuscript received December 4, 2020; revised January 22, 2021; accepted February 27, 2021. Date of publication March 3, 2021; date of current version June 1, 2021. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) and in part by the National Natural Science Foundation of China under Grants 61973307 and 61936008. Recommended for publication by Associate Editor A. Lindemann. (Corresponding author: Mingzhe Wu.)

Mingzhe Wu, Cheng Xue, and Yun Wei Li are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 1H9, Canada (e-mail: mwu2@ualberta.ca; cxue1@ualberta.ca; yunwei.li@ualberta.ca).

Kehu Yang is with the School of Mechanical Electronic and Information Engineering, China University of Mining and Technology, Beijing 100083, China (e-mail: ykh@cumt.edu.cn).

Digital Object Identifier 10.1109/TPEL.2021.3063299

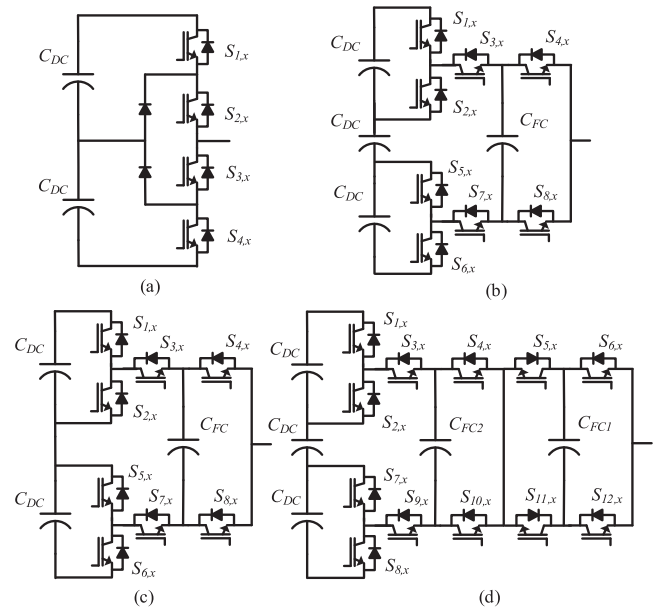


Fig. 1. Widely implemented or emerging MLCs with phase $x = a, b, \text{ or } c$. (a) 3L-NPC. (b) 4L-HC. (c) 5L-ANPC. (d) 7L-HC.

(3L-NPC) [4], four-level hybrid-clamped (4L-HC) [5], five-level active NPC (5L-ANPC) [6], and seven-level HC (7L-HC) [7] converters, are presented in Fig. 1.

In high/medium-voltage applications where MLCs are usually adopted, the magnitude of common-mode voltage (CMV) is considerable, which is harmful to converter systems, e.g., the shaft voltage and bearing current resultant from the CMV will shorten the life expectancy of the motor, the CM leakage currents generated are responsible for the EMI problem that might lead to device failure of the converters, etc.

In order to suppress the CMV in MLC system, various studies have been carried out from the perspective of hardware solutions [8]–[11] and advanced pulsewidth modulation (PWM) (software) solutions [12]–[38], where the hardware-based ones will increase the cost and size of the converter system greatly. As for the commonly adopted software solutions with reduced/zero CMV developed for specific types of MLC topology, they can be generally classified into the following.

TABLE I
COMPARISONS AMONG THE STATE-OF-THE-ART GENERALIZED PWM
METHODS WITH REDUCED/ZERO CMV

Generalized Ref.	Complexity	CMV Amplitude	THD Degradation	Switching Frequency	Application Scope
SVM [32]	Medium	Zero	Medium	Medium	Odd-Level MLCs
SVM [33]	Medium	Zero	Medium	Low	Odd-Level MLCs
SVM [34]	High	Zero/Reduced	Medium	High	Cascaded MLCs
CBM [35]	High	Zero	Medium	Medium	Odd-Level MLCs
CBM [36]	High	Zero	High	Medium	All MLCs
CBM [37]	Medium	Reduced	Low	Medium	ANPC Converters
Virtual SVM [38]	High	Reduced	High	High	All MLCs
Proposed SHE-PWM	Low	Reduced	Medium	Low	All MLCs

- 1) *Space Vector Modulation (SVM)-Based Solutions*: The SVM-based CMV regulation methods are the most widely implemented and straightforward ones, since they are directly operated by selecting the voltage vectors with reduced/zero CMV. The CMV elimination PWM which selects the voltage vectors that produce zero CMV has been adopted for 3L-NPC [12], [13], 5L-NPC [14], 5L-ANPC [15], and 5L nested NPC converters [16]. However, the problems of low dc voltage utilization, degraded output performance, as well as poor capacitor balancing effect and high power losses exist with the zero CMV approach [17]. The CMV reduction methods based on discontinuous PWM, i.e., five-segment SVM, are conducted in [18] and [19] for 3L-NPC inverters, where 19 out of the 27 vectors are used with reduced CMV. However, the NP balancing and low-frequency NP voltage fluctuation problem still exist with this approach. The studies with seven-segment SVM under the principles of two-level SVM are proposed for 3L quasi-Z-source converters in [20], 3L-NPC in [21], and 3L-NPC based drive system in [22]. The switching sequence designs behind such works are quite complicated, which makes the seven-segment SVM approach difficult to be generalized to N -level MLCs. The virtual SVM-based CMV reduction methods are presented in [23], but with huge switching losses and worse harmonic profile due to the generation process and implementations of the virtual vectors, which is also unsuitable for generalization.
- 2) *Carrier-Based (CB) Solutions*: In [24] and [25], the CMVs of back-to-back 3L-NPC and 4L-HC systems are reduced by zero-sequence voltage (ZSV) injection. The limitation of the ZSV-based methods is that the MLC system must be in back-to-back configuration. As for other CB methods [26]–[28], they are actually operated by adjusting the carriers in each switching period to generate the expected voltage vectors with reduced/eliminated CMV. For example, in [27], a double modulation wave CB modulation (CBM) is used to suppress the CMV by rearranging the switching sequence; in fact, it is still based on the principle of abandoning the utilization of certain voltage vectors with large CMVs.
- 3) *Model Predictive Control (MPC)-Based Solutions*: The MPC-based CMV reduction/elimination methods are proposed for 3L-NPC [29], 3L-TNPC [30], and 5L-ANPC [31], respectively. In essence, they are also based on

selecting specific voltage vectors with reduced/eliminated CMV, but just with a more straightforward way with MPC to facilitate the voltage vector selection process.

In addition to those CMV reduction methods discussed above that targeted on specific MLC topologies, some generalized CMV reduction/elimination methods based on SVM or CBM for N -level MLCs are proposed in [32]–[38], the characteristics of which are summarized in Table I. It should be noted that the comparisons are based on the results and discussions presented in the corresponding studies in the literature.

Although the SVM-, CBM-, and MPC-based CMV reduction/elimination methods could effectively suppress the amplitude of CMV, a relatively high switching frequency is required to ensure the satisfactory performance of these methods. When MLCs are applied to high-power cases, significant considerations are given to the device switching frequency, since high switching frequency will induce huge system power losses, reducing the system efficiency greatly. Thus, many of the above-mentioned CMV reduction methods are not suitable to be implemented in high-power cases.

Among the commonly adopted PWM strategies, selective harmonic elimination (SHE) PWM has high-quality output voltage with low ratio of switching frequency over fundamental frequency, which makes it highly suitable for MLCs operated in high-power conditions with low switching frequency [39], [40]. However, the CMV reduction method with SHE-PWM is from a totally different perspective of the CBM- and SVM-based ones, i.e., the variables with SHE-PWM are the switching angles instead of the voltage vectors or carrier distributions. To achieve the CMV regulation goal for MLCs under SHE-PWM, Zhao *et al.* proposed a modified SHE-PWM model with reduced CMV for 3L-NPC inverters by incorporating the zero-sequence harmonics (ZSHs) into the SHE equations and set their amplitudes to zero [41]. Therefore, the CMV can be reduced due to the lack of ZSHs in the harmonic spectrum of phase voltages. However, the maximum achievable modulation index (m_a) is limited to 1 due to the absence of third-order harmonic in the output voltage of each inverter leg. Besides, only the three-level model is studied, whose application scope is limited. Moreover, [41] uses additional hardware devices for capacitor voltage control, further increasing the cost and size of the system. In addition, the same idea was used in [42], but with a different off-line solving algorithm. Recently, the CMV reduction problem has also been studied in [43] with selective harmonic mitigation PWM (SHM-PWM). Although the PWM method in [43] has been changed from SHE to SHM compared with [41] and [42], the main idea behind the CMV reduction mechanism is the same, i.e., by eliminating the ZSHs; thus, it still has the problem of limited achievable m_a range. Besides, the application scope of [43] is still confined to 3L-NPC converters.

In this article, a generalized multilevel SHE-PWM formulation with CMV reduction ability for N -level MLCs is presented. In low and medium m_a range, the low-order ZSHs in the SHE model are all set to zero for the best CMV reduction effect. In high m_a range, an optimal value of third-order harmonic component is incorporated, with which the maximum achievable m_a can be extended from 1 to 1.15 compared with [41]–[43], while

the same CMV reduction effect and good output performances can still be achieved. Two kinds of high-performance solving algorithms, i.e., off-line and real-time based, are both introduced in this article to provide a comprehensive view in efficiently solving the proposed model. The case study with 3L-NPC inverters is discussed in detail to better illustrate the proposed model and the coupling effects between the CMV reduction and capacitor voltage balancing of MLCs under SHE-PWM. Simulation and experimental results are carried out on various topologies to validate the effectiveness of the proposed generalized SHE-PWM formulations with reduced CMV. Comparisons with other generalized CMV reduction methods are presented in Table I to further demonstrate the overall advantages of the proposed model, i.e., simple implementation process with low switching frequency and reduced CMV amplitude that could be applied to any type of MLCs. Moreover, the idea of injecting an optimal third-order harmonic proposed in this article can be easily extended to other programmed PWM alternatives, e.g., SHM and THD minimization PWM, in reducing the CMV for N -level MLCs over the whole m_a range.

II. GENERALIZED MULTILEVEL SHE-PWM FORMULATION WITH CMV REDUCTION ABILITY

A. Conventional Multilevel SHE-PWM and CMV Formulation

For three-phase MLC systems, the PWM waveforms of phase a , b , and c that exhibit quarter-wave (QW) symmetries can be expressed as

$$\begin{cases} V_{ao} = \sum_{n=1,3,\dots}^{\infty} b_n \sin n(\omega t + \theta) \\ V_{bo} = \sum_{n=1,3,\dots}^{\infty} b_n \sin n(\omega t - \frac{2\pi}{3} + \theta) \\ V_{co} = \sum_{n=1,3,\dots}^{\infty} b_n \sin n(\omega t + \frac{2\pi}{3} + \theta) \end{cases} \quad (1)$$

where θ is the initial phase angle, b_n is the Fourier coefficient which is shown as follows, with N switching angles α and step output voltage E :

$$b_n = \begin{cases} \frac{4E}{n\pi} \left[\pm \sum_{i=1}^N \cos(n\alpha_i) \right] & L \text{ is odd} \\ \frac{4E}{n\pi} \left[\pm \sum_{i=1}^N \cos(n\alpha_i) - \frac{1}{2} \right] & L \text{ is even.} \end{cases} \quad (2)$$

The conventional nonlinear SHE equations of odd-level MLCs can be derived as

$$\begin{cases} \pm \sum_{i=1}^N \cos \alpha_i = \frac{\pi V_{DC}}{8E} m_a \\ \pm \sum_{i=1}^N \cos(n\alpha_i) = 0, \quad n = 5, 7, \dots, 3N - 2 \end{cases} \quad (3)$$

where V_{DC} denotes the dc-link voltage of the MLCs, and m_a is defined as the quotient of the fundamental voltage magnitude and half of the dc-link voltage.

The CMV of three-phase MLC system is defined as the voltage between the central NPs of the dc-link and the three-phase

load, which is denoted as V_{cm} in the following:

$$V_{cm} = \frac{V_{ao} + V_{bo} + V_{co}}{3}. \quad (4)$$

Based on (1) and (4), the V_{cm} under SHE-PWM operated MLC system can be expressed as

$$\begin{aligned} V_{cm} &= \sum_{n=1,3,\dots}^{\infty} b_n \frac{\sin n(\omega t + \theta) + \sin n(\omega t - \frac{2\pi}{3} + \theta) + \sin n(\omega t + \frac{2\pi}{3} + \theta)}{3} \\ &= \sum_{n=1,3,\dots}^{\infty} b_n \sin 3n(\omega t + \theta). \end{aligned} \quad (5)$$

As shown in (5), the harmonic components in V_{cm} under SHE-PWM are only those ZSHs (third, ninth, ...), since the three-phase nontriple harmonics (fifth, seventh, ...) are canceled automatically in V_{cm} , while the even-order harmonics are eliminated naturally under QW SHE-PWM patterns.

B. SHE-PWM Formulation With Reduced CMV

As shown in the traditional SHE-PWM formulation (3), the triple harmonics are not included in the harmonic elimination objectives of phase voltages, since for normal operations, they will be eliminated automatically in three-phase systems, and thus have no influence on the output line-to-line voltage/current waveform qualities. However, based on (5), the dominant harmonic components in the CMV of MLCs V_{cm} under SHE-PWM are exactly the low-order triple harmonics, especially the 3rd, 9th, and 15th harmonic components. These low-frequency components contribute much to the CMV of the MLC system, which also lead to bulky CM inductors and heated CM filters. Therefore, the modified SHE-PWM model with CMV reduction ability is supposed to include those low-order ZSHs to actively control them in the three-phase SHE-PWM voltages. As a result, both the amplitude and rms values of the CMV can be suppressed accordingly with reduced volume and cost of the converter system as well, which is the main objective of the proposed formulation.

The generalized odd-level SHE-PWM formulation with reduced CMV by setting the amplitude of some specific low-order ZSHs to zero is shown as

$$\begin{cases} \pm \sum_{i=1}^N \cos \alpha_i = \frac{\pi V_{DC}}{8E} m_a \\ \pm \sum_{i=1}^N \cos(n\alpha_i) = 0, \quad n = 3, 5, \dots, 2N - 1. \end{cases} \quad (6)$$

Although the CMV can be effectively reduced over low m_a range with (6), the maximum achievable m_a is only limited to 1 due to the absence of third-order harmonic component in the output voltage of each inverter leg [41]. Therefore, if the MLC system only operates with (6), a specially designed LC filter needs to be installed in the MLC system to suppress the CMV in high m_a range, which increases the cost and volume of the system significantly.

In order to achieve the full range operation of the generalized SHE-PWM formulation with CMV reduction ability, an improved model in high m_a range is proposed in this article by injecting an optimal third-order harmonic component to each

SHE-PWM phase voltage; hence, the maximum achievable m_a can be extended from 1 to 1.15 without affecting the CMV reduction effect. This improved SHE-PWM formulation in high m_a range is presented as

$$\begin{cases} \pm \sum_{i=1}^N \cos \alpha_i = \frac{\pi V_{DC}}{8E} m_a \\ \pm \sum_{i=1}^N \cos 3\alpha_i = \frac{\pi V_{DC}}{8E} k_3 m_a \\ \pm \sum_{i=1}^N \cos(n\alpha_i) = 0, \quad n = 5, 7, \dots, 2N - 1 \end{cases} \quad (7)$$

where k_3 is a positive fraction to describe the optimal third-order harmonic magnitude in terms of the fundamental voltage, the calculation process of which is shown below.

Based on (7), the three-phase voltage expressions (1) are modified after the optimal third-harmonic injection and the elimination of other specific low-order harmonic components

$$\begin{cases} V_{ao} = b_1 \sin(\omega t + \theta) + b_3 \sin 3(\omega t + \theta) \\ \quad + \sum_{n=2N-1, \dots} b_n \sin n(\omega t + \theta) \\ V_{bo} = b_1 \sin(\omega t - \frac{2\pi}{3} + \theta) + b_3 \sin 3(\omega t - \frac{2\pi}{3} + \theta) \\ \quad + \sum_{n=2N-1, \dots} b_n \sin n(\omega t - \frac{2\pi}{3} + \theta) \\ V_{co} = b_1 \sin(\omega t + \frac{2\pi}{3} + \theta) + b_3 \sin 3(\omega t + \frac{2\pi}{3} + \theta) \\ \quad + \sum_{n=2N-1, \dots} b_n \sin n(\omega t + \frac{2\pi}{3} + \theta). \end{cases} \quad (8)$$

Since the high-order harmonics have limited influence on the output voltage compared with the low-order ones, they are temporally ignored in (8). With this simplification, the three-phase voltage expressions are rewritten as follows, which is theoretically equivalent to the reference voltage expressions of the CBM model with third harmonic injection [44], [45]:

$$\begin{cases} V_{ao} = b_1 \sin(\omega t + \theta) + b_3 \sin 3(\omega t + \theta) \\ V_{bo} = b_1 \sin(\omega t - \frac{2\pi}{3} + \theta) + b_3 \sin 3(\omega t - \frac{2\pi}{3} + \theta) \\ V_{co} = b_1 \sin(\omega t + \frac{2\pi}{3} + \theta) + b_3 \sin 3(\omega t + \frac{2\pi}{3} + \theta). \end{cases} \quad (9)$$

Based on the results in [44] and [45], the optimal value of the third-harmonic amplitude b_3 is one-sixth of b_1 in order to extend the maximum achievable m_a from 1 to 1.15 in a three-phase system. Then, together with (2) and (7), the following set of equations can be obtained:

$$\begin{cases} b_n = \frac{4E}{n\pi} \left[\pm \sum_{i=1}^N \cos(n\alpha_i) \right] \quad n = 1, 3 \\ b_3 = \frac{b_1}{6} \\ \pm \sum_{i=1}^N \cos(3\alpha_i) = k_3 \left[\pm \sum_{i=1}^N \cos(\alpha_i) \right]. \end{cases} \quad (10)$$

By solving the equation set in (10), the optimal value of k_3 is calculated as 0.5 that could extend the m_a range from 1 to 1.15 by optimal third-order harmonic injection.

In summary, the generalized CMV reduction method for MLCs under SHE-PWM can be divided into two parts—with the ZSHs eliminated model as (6) in low and medium m_a range ($m_a \leq 1$) and with the modified model based on optimal third-harmonic injection as (7) in high m_a range ($1 < m_a \leq 1.15$). In other words, the generalized model can be simply represented

using (7), but with two different values of the decision variable k_3 in accordance with the modulation index, as shown in (11). With this model, the amplitude of the CMV can be reduced greatly for MLCs compared with the conventional model. It should be noted that the injected third-harmonic component is usually quite small, which will not affect the expected CMV reduction effect in high m_a range

$$k_3 = \begin{cases} 0 & m_a \leq 1 \\ 0.5 & m_a > 1. \end{cases} \quad (11)$$

The generalized SHE-PWM formulation with reduced CMV for even-level MLCs is shown as follows, with identical k_3 cases in (11) as the odd-level model. Due to the space limitation, the examples in the following sections are all based on the odd-level model:

$$\begin{cases} \pm \sum_{i=1}^N \cos \alpha_i = \frac{\pi V_{DC}}{8E} m_a + \frac{1}{2} \\ \pm \sum_{i=1}^N \cos 3\alpha_i = \frac{\pi V_{DC}}{8E} k_3 m_a + \frac{1}{2} \\ \pm \sum_{i=1}^N \cos(n\alpha_i) = \frac{1}{2}, \quad n = 5, 7, \dots, 2N - 1. \end{cases} \quad (12)$$

Besides, in order to maintain a good balance between the CMV reduction goal and to keep the low switching frequency characteristic of SHE-PWM, it is important to find out the optimal number of switching angles that could achieve the reduced CMV amplitude over the whole m_a range with an acceptable switching frequency in high-power applications. As mentioned previously, the dominant ZSHs in V_{cm} are usually the 3rd, 9th, and 15th harmonic components, hence eight or nine switching angles in (7) and (12), i.e., $N = 8$ or $N = 9$, are good enough for most cases to ensure a satisfactory CMV reduction effect while operating at a low switching frequency.

As for the closed-loop implementation of SHE-PWM, the shifting point for changing m_a could be either placed within one fundamental period to achieve the fast response [58], or at the end of one fundamental period to ensure the waveform quality, i.e., harmonic elimination effects [59]–[61]. However, both ways have little influence on the steady-state CMV reduction effect of the proposed formulation, since the three-phase SHE waveforms with the switching angles calculated from (7) and (12) have inherent CMV reduction ability over the whole m_a range and at any time instant. Therefore, the load conditions and shifting points of m_a in the closed-loop SHE-PWM implementation will not increase the CMV amplitude under the proposed formulation.

III. SOLVING PROCEDURES AND CAPACITOR VOLTAGE CONTROL WITH THE PROPOSED SHE-PWM FORMULATION

Due to the presence of ZSH component in the generalized SHE-PWM model, some commonly adopted switching angle solving algorithms for the nonlinear SHE equations are no longer applicable. Therefore, two kinds of efficient solving algorithms targeted at (7) and (12) are investigated to provide a more comprehensive view in dealing with the proposed formulation. Besides, the coupling effects between the capacitor voltage

TABLE II
COMPARISONS OF REAL-TIME AND TABLE-DRIVEN METHODS

Real-Time Implementation	Table-Driven Implementation
Higher Solution Accuracy	Resolution Constraints
High Implementation Complexity	Low Implementation Complexity
No Demand for LUT	Require LUT
Longer Execution Time	Shorter Execution Time
Not suitable for Large Number of Switching Angles	No Constraints for the Number of Switching Angles

balancing strategy of MLCs and the CMV reduction effect with the proposed model are also discussed.

A. Off-Line Solving Procedure

Although there are numerous off-line algorithms developed in recent decades, the solving method by minimizing the objective goal as (13) is considered as one of the simplest ways in dealing with the proposed SHE-PWM model. Based on (7), the objective function $F(\alpha_i)$ for odd-level MLC can be formulated as

$$\begin{aligned}
 F(\alpha_1, \dots, \alpha_N) = & \left(\pm \sum_{i=1}^N \cos \alpha_i - \frac{\pi V_{DC}}{8E} m_a \right)^2 \\
 & + \left(\pm \sum_{i=1}^N \cos 3\alpha_i - \frac{\pi V_{DC}}{8E} k_3 m_a \right)^2 + \dots \\
 & + \left(\pm \sum_{i=1}^N \cos(2N-1)\alpha_i \right)^2
 \end{aligned} \quad (13)$$

with the following constraint and the k_3 values in (11):

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \dots < \alpha_N < \frac{\pi}{2}. \quad (14)$$

The model (13) can be solved easily by the state-of-the-art intelligent solving algorithms [46]–[48] or just with the built-in *fmincon* function in MATLAB that is based on the interior-point algorithm [49].

B. Real-Time Solving Procedure

Due to the limited number of switching angles that can be discontinuously stored in the microprocessor (MCU), their accuracy is often confined with off-line-based SHE algorithms. In order to obtain higher accuracy of switching angles, the real-time SHE algorithm using the hybrid algebraic–numerical method in [50] is well-suited in solving (7) and (12), which has higher solution accuracy and shorter calculation time compared with other real-time-based methods [51]–[53]. This method naturally includes the ZSH components in the SHE formulation, which just fit into the CMV reduction model, i.e., (7) and (12) proposed in this article. The flowchart of this real-time algorithm is shown in Fig. 2.

C. Selection Guide on SHE Solving Algorithms

According to the previous analysis, the advantages and disadvantages of the real-time and table-driven methods can be summarized as Table II, based on which some selection guides on the solving algorithms can be concluded—if the objective m_a undergoes slight adjustments constantly in the targeted

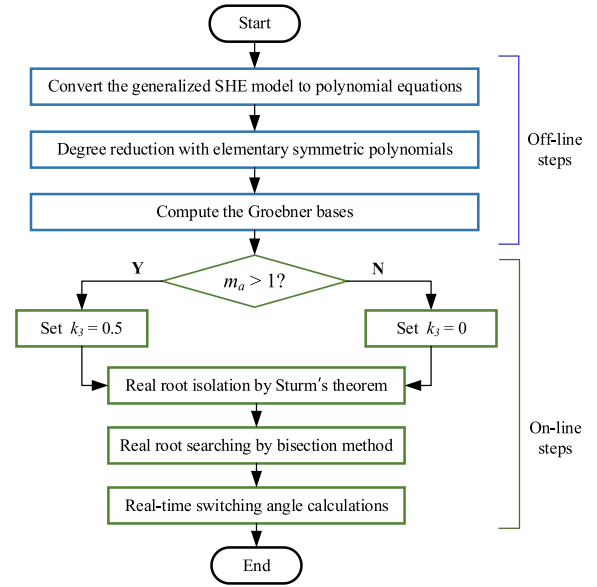


Fig. 2. Flowchart of real-time implementations of the proposed SHE-PWM formulation with CMV reduction ability.

application and/or a very high solution accuracy is required, the real-time solving algorithm is recommended to achieve the most accurate switching angles in all operating conditions. As for situations where the targeted m_a is almost constant or only adjusted between some certain values, e.g., grid-connected applications, and when the number of switching angles adopted is larger than ten, the off-line-based method is sounder than the real-time strategy.

D. Capacitor Voltage Balancing Control and the Coupling Effects With CMV

For most MLCs, their dc-link and/or flying capacitor voltages must be regulated actively to avoid voltage drift and degraded output qualities. However, when the CMV reduction objective and the capacitor voltage balancing goal are considered simultaneously, their coupling effects cannot be neglected, i.e., sometimes the CMV reduction method will cause unbalanced capacitor voltages or limit the effective voltage balancing control range to a specific margin due to the specific voltage vectors/carrier distributions adopted, while such coupling effects for SVM- and CBM-based methods have been well-studied in the existing literature.

However, the voltage balancing methods under SHE-PWM are quite different from the SVM- or CBM-based ones. With SHE-PWM, the commonly adopted voltage balancing methods include angle modifications [54], redundant states selection [55], and SHE model predictive control (SHE-PWM) [56], which have been summarized comprehensively in [40]. Among them, the redundant state selections and SHE-MPC are operated by swapping the redundant phase switching states for certain voltage levels, which will not interfere with the switching angles, hence, having no influence on the CMV reduction effect. However, for angle modification, since it will slightly adjust the

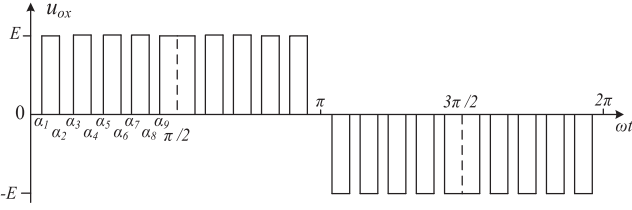


Fig. 3. Three-level SHE-PWM waveforms with nine switching angles.

switching angles based on the voltage balancing demand, which might couple with the CMV control objective, i.e., unexpected CMV spike will be generated due to the slight adjustment on the expected optimal switching angles with CMV reduction ability. Such a mechanism will be discussed thoroughly in the 3L-NPC example in Section IV.

IV. DESIGN EXAMPLE: REDUCED CMV SHE-PWM FOR 3L-NPC INVERTERS

Based on the previous analysis, the dominant ZSHs in three-level waveforms are also the 3rd, 9th, and 15th harmonics. Therefore, nine switching angles are adopted under this reduced CMV SHE-PWM, where the corresponding three-level phase voltage waveform is shown in Fig. 3.

According to the proposed odd-level generalized model (7), the SHE model for 3L-NPC inverters with $V_{DC} = 2E$ and $N = 9$ is shown as

$$\begin{cases} \cos \alpha_1 - \cos \alpha_2 + \cos \alpha_3 - \cos \alpha_4 + \cos \alpha_5 - \cos \alpha_6 \\ \quad + \cos \alpha_7 - \cos \alpha_8 + \cos \alpha_9 = \frac{\pi}{4} m_a \\ \cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) + \cos(3\alpha_5) \\ \quad - \cos(3\alpha_6) + \cos(3\alpha_7) - \cos(3\alpha_8) \\ \quad + \cos(3\alpha_9) = \frac{\pi}{4} k_3 m_a \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) + \cos(5\alpha_5) \\ \quad - \cos(5\alpha_6) + \cos(5\alpha_7) - \cos(5\alpha_8) + \cos(5\alpha_9) = 0 \\ \dots \\ \cos(17\alpha_1) - \cos(17\alpha_2) + \cos(17\alpha_3) \\ \quad - \cos(17\alpha_4) + \cos(17\alpha_5) - \cos(17\alpha_6) + \cos(17\alpha_7) \\ \quad - \cos(17\alpha_8) + \cos(17\alpha_9) = 0. \end{cases} \quad (15)$$

where the value of the decision variable k_3 is the same as (11).

By solving the three-level model (15) for 3L-NPC inverters using the SHE nonlinear equation solving algorithms discussed in Section III, the nine switching angles with CMV reduction ability for the three-level waveform in Fig. 3 is shown as Fig. 4 over the full m_a range with resolution 0.005, which is precise enough for most applications.

In order to achieve the expected CMV reduction effects and good output performances, the NP voltage of 3L-NPC converters must be well-balanced with the angle modification methods. However, it has some coupling effects with the CMV reduction objective due to the slight variations to the switching angles; thus, the angle modification degree should be well-coordinated. The implementation diagrams of the angle modification method under the proposed SHE model are shown in Fig. 5(a) and (b), where the constant K refers to the degree of angle modifications.

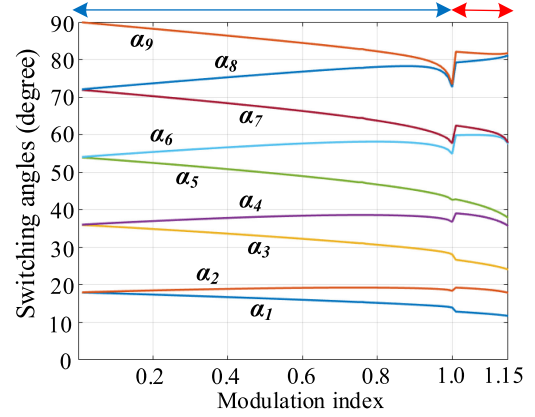


Fig. 4. Solutions for the nine switching angles with CMV reduction ability.

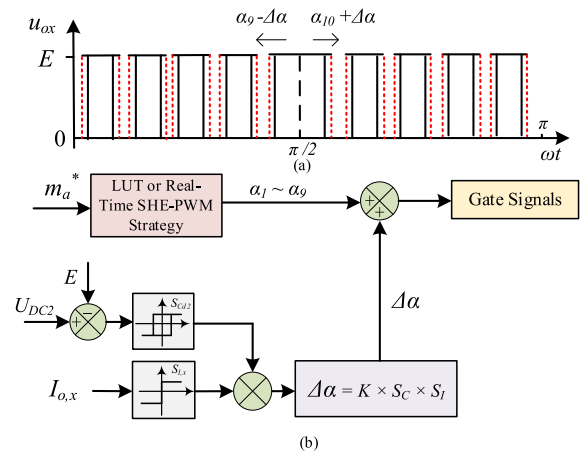


Fig. 5. Control diagrams of the angle modification method for NP balancing. (a) Angle modification diagram. (b) Overall implementation process.

According to the proposed SHE-PWM model, it is obvious that introducing the slight variation $\Delta\alpha$ to the switching angles will influence the harmonic elimination effects, then the output performance as well as the CMV reduction effect. Therefore, it is important to find out the appropriate range of the constant K to ensure that the resultant harmonic suppression and CMV reduction effects are both satisfied with the angle modification method. The specific requirements can be summarized as follows.

- 1) The nontriple harmonics (5th, 7th, 11th, 13th, and 17th) should not exceed the magnitude regulated by the grid code to ensure a good output voltage quality [57].
- 2) The CMV should always be regulated at one-sixth of the dc-link voltage.

In order to search out the optimal range limits of the constant K , the low-order harmonic elimination and CMV reduction effects with various values of K are analyzed. The results with $m_a = 0.8$ and 1.1 are presented as Fig. 6(a) and (b), while a similar process can be applied to other cases.

Take the measured values in Fig. 6(a) as an example, where the results are with $m_a = 0.8$. As shown in the case with $K = 0.6$, although the CMV is still controlled as one-sixth of the dc-link

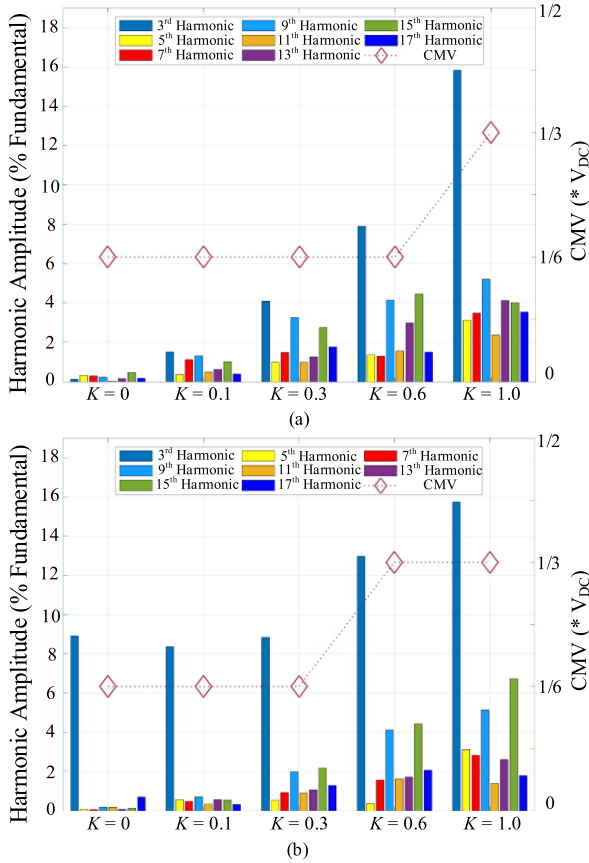


Fig. 6. Effects on harmonic elimination and CMV reduction performance with various values of K . (a) $m_a = 0.8$. (b) $m_a = 1.1$.

voltage, the magnitude of the 13th harmonic (3.02%) exceeds the grid code requirement ($< 3\%$), thus K should be restricted to less than 0.6 in this case.

Besides, it can also be observed from Fig. 6 that the ZSHs are more sensitive to switching angle variations, especially the third-harmonic component, which is the main reason for the amplified CMV in higher K situations.

V. SIMULATION AND COMPARATIVE ANALYSIS

In this section, the steady-state simulation results for 3L-NPC, 4L-HC, 5L-ANPC, and 7L-HC inverters, as shown in Fig. 1, using the MATLAB/Simulink under the conditions of $V_{DC} = 2400$ V, R - L load $28 \Omega - 30$ mH, $C_{DC} = 3300$ mF, and/or $C_{FC} = 1000$ mF are carried out. The conventional SHE-PWM formulation is used in the first half-period of all simulations, while this generalized SHE-PWM model proposed with reduced CMV is adopted in the second half-period to clearly demonstrate the effectiveness of the proposed model.

The simulation results of phase voltage, line voltage, line current, two dc-link capacitor voltages, and the CMV of 3L-NPC is presented in Fig. 7, using the conventional model in [0.1, 0.2] s and the proposed formulation in [0.2, 0.3] s, respectively. As shown in Fig. 7, both good output waveform qualities and the reduction of the amplitude of CMV are achieved with the proposed model.

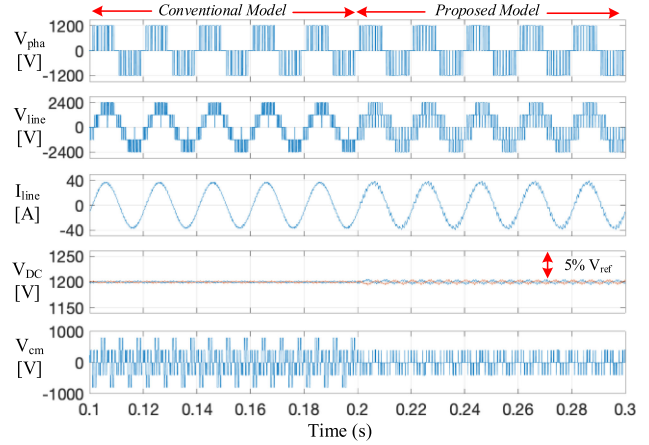


Fig. 7. Simulation results of 3L-NPC inverters with the conventional SHE model in [0.1, 0.2] s and the CMV reduction model in [0.2, 0.3] s.

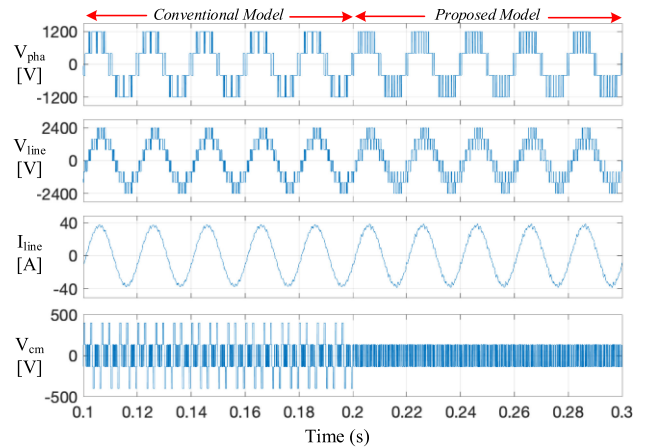


Fig. 8. Simulation results of 4L-HC inverters with the conventional SHE model in [0.1, 0.2] s and the CMV reduction model in [0.2, 0.3] s.

To further demonstrate the effectiveness of the proposed generalized model for N -level inverters, simulation results of 4L-HC in Fig. 8, 5L-ANPC in Fig. 9, and 7L-HC converters in Fig. 10 are carried out, respectively. The corresponding simulations include steady-state waveforms of phase voltage, line voltage, output current, and CMV, using the conventional SHE-PWM model and the proposed formulation. Same as the results with 3L-NPC converters in Fig. 7, the conventional model is used in [0.1, 0.2] s while the modified formulation is adopted during [0.2, 0.3] s. As shown in Figs. 8–10, both good output waveform qualities and great reduction of the CMV amplitude are achieved for these three types of MLCs.

In Tables III and IV, the numerical values of Figs. 7–10 are presented. As shown in Table II, which contains the results concerning the CMV reduction effects, the amplitude of CMV for the presented four types of MLCs are reduced by at least one-half, while the rms values of CMV are also suppressed significantly. It should be noted that, the CMV reduction degree depends on the specific type of the MLCs adopted, but the main ideas as in (7) and (12) are the same. The THD comparisons

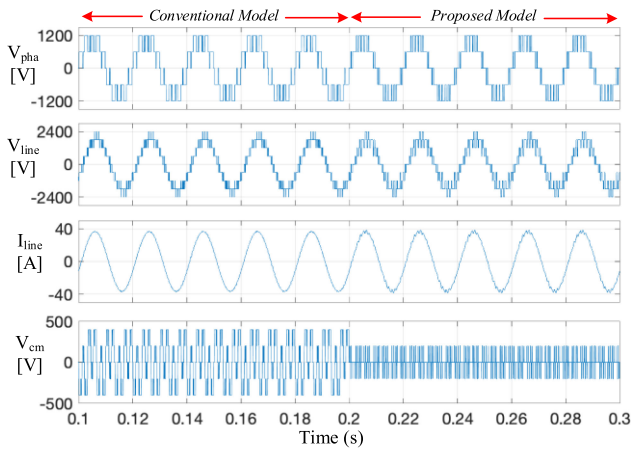


Fig. 9. Simulation results of 5L-ANPC inverters with the conventional SHE model in [0.1, 0.2] s and the CMV reduction model in [0.2, 0.3] s.

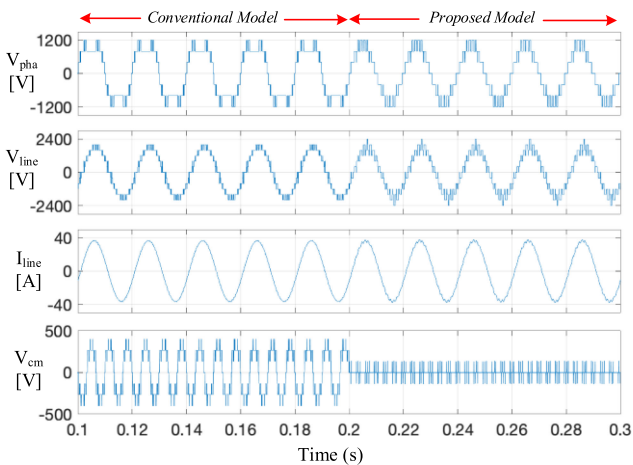


Fig. 10. Simulation results of 7L-HC inverters with the conventional SHE model in [0.1, 0.2] s and the CMV reduction model in [0.2, 0.3] s.

TABLE III
CMV COMPARISONS BETWEEN THE TWO MODELS

Converter Type	Conventional Model		Proposed Model	
	Amplitude	RMS	Amplitude	RMS
3L-NPC	800 V	417.8 V	400 V	124.1 V
4L-HC	400 V	238.2 V	133.4 V	133.4 V
5L-ANPC	400 V	296.8 V	200 V	134.9 V
7L-HC	400 V	245.5 V	133.4 V	40.44 V

between the conventional and the proposed model are carried out in Table III, where the line voltage THD of the proposed method is slightly larger than the conventional one. The reason behind such an increase is due to the three fewer nontriple harmonics being eliminated than the conventional model. This tradeoff between the output performance and the CMV reduction effect exists in almost all the CMV reduction methods in [12]–[38]. Compared with the other methods, the proposed SHE-PWM formulation has one advantage that the dominant output harmonics are usually the first two noneliminated harmonics. Therefore, a simple and low volume high-order filter can be used to suppress

TABLE IV
THD COMPARISONS BETWEEN THE TWO MODELS

Converter Type	Conventional Model		Proposed Model	
	THD _{pha}	THD _{line}	THD _{pha}	THD _{line}
3L-NPC	68.44 %	41.29 %	63.28 %	50.97 %
4L-HC	43.32 %	30.04 %	42.85 %	39.24 %
5L-ANPC	43.22 %	18.74 %	32.44 %	29.07 %
7L-HC	35.25 %	14.31 %	21.44 %	20.69 %

TABLE V
PARAMETERS OF THE 3L-NPC EXPERIMENT PLATFORM

Experiment Parameters	
DC-link voltage (V)	100
DC-link capacitor (μ F)	3300
Load resistance (Ω)	14.7
Load inductance (mH)	30
Switching angle No.	9
Base frequency (Hz)	50

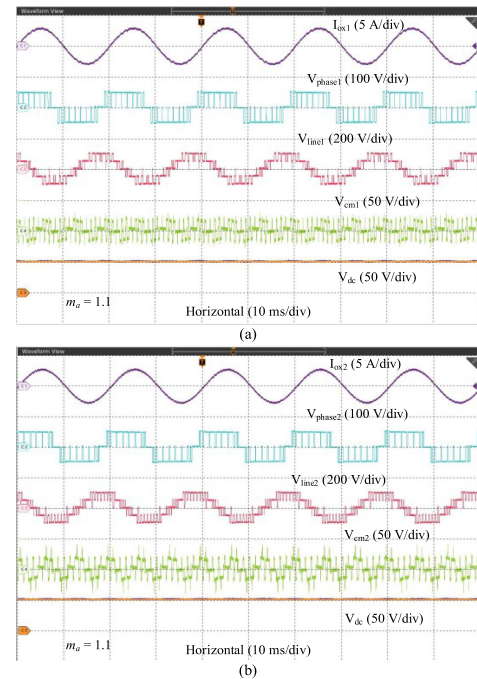


Fig. 11. Steady-state experimental results with $m_a = 1.1$. (a) With the CMV reduction model. (b) With the conventional SHE model.

the first two noneliminated high-order harmonics, after which the output performance of the proposed model will be much better.

VI. EXPERIMENTAL VALIDATIONS

To further verify the validity of the proposed SHE-PWM formulation for CMV reduction, a range of experiments for 3L-NPC inverters have been carried out by a low-power platform. The circuit parameters used for the experiment are summarized in Table V, while the switching angles and NP balancing method are based on Section IV.

In Figs. 11 and 12, the steady-state experimental results of output current, phase voltage, line voltage, CMV, and two dc-link

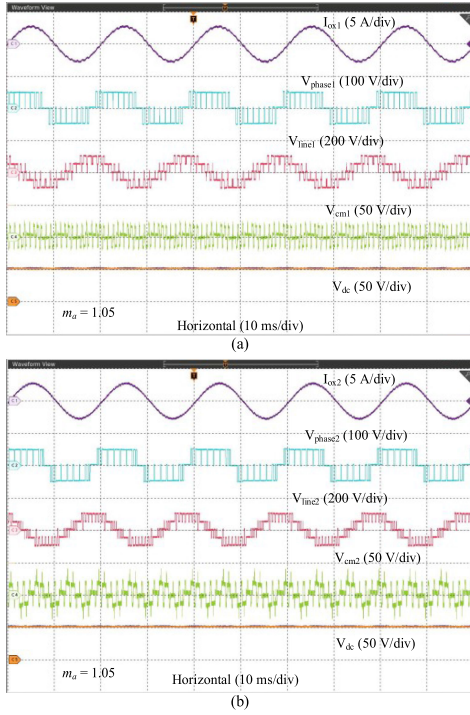


Fig. 12. Steady-state experimental results with $m_a = 1.05$. (a) With the CMV reduction model. (b) With the conventional SHE model.

capacitor voltages using the proposed CMV reduction model and the traditional model without eliminating the ZSHs with $m_a = 1.1$ and 1.05 are presented. Since the modulation index is above 1, the proposed optimal third-order harmonic injection model as (15) and $k_3 = 0.5$ is adopted in Figs. 7(a) and 8(a). Compared with the results in [41], the modulation index range has been successfully extended larger than 1, without affecting the CMV reduction effect and the output performance, i.e., one-sixth of the dc-link voltage. It could also be observed that the dc-link capacitors are well-balanced with the angle modification method.

In Fig. 13, the fast Fourier transform (FFT) analysis results of output current, phase voltage, and line voltage with $m_a = 1.1$ are presented for both models with CMV reduction ability and the traditional one, in order to bring more insights to the proposed method. As shown in Fig. 13, the 9th and 15th harmonics are all eliminated in the phase voltages with the proposed CMV reduction model, while the small amount of third-order harmonic present is due to the optimal injection process to extend m_a from 1 to 1.1; while in the FFT analysis result of the phase voltage with the traditional SHE model, large low-order ZSH components exist, which is the main reason for the increased CMV amplitude in Fig. 11. Besides, as shown in Fig. 13, although the proposed CMV reduction model does not eliminate the 19th, 23th, and 25th harmonic components with the available nine switching angles, the output line voltage performance, i.e., THD, does not turn worse compared with the one with the traditional method in high m_a range. Moreover, even if the angle modification method is adopted, the amplitudes of the harmonics eliminated

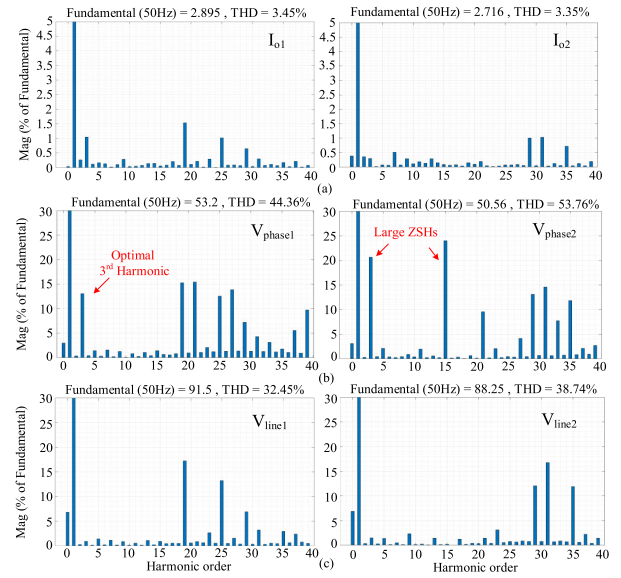


Fig. 13. FFT analysis results of (a) output current, (b) phase voltage, and (c) line voltage for 3L-NPC inverters with $m_a = 1.1$, (1) with the CMV reduction model and (2) with the traditional model.

are all well-regulated within the grid code requirements while the expected CMV reduction effect is still achieved.

In order to validate the improved SHE-PWM model with reduced CMV amplitude in medium and low m_a range, the same sets of experimental results are carried out with the proposed model and the traditional model, for $m_a = 0.9$, $m_a = 0.6$, and $m_a = 0.3$, as shown in Figs. 14–16, respectively. It can be observed that both high-quality output waveforms and good CMV reduction effects are achieved with the proposed formulation. The voltages of dc-link capacitors are also well-balanced with the angle modification method.

The theoretical power losses based on the experimental parameters in Table V are also analyzed for both models in order to provide a more comprehensive comparison between these two methods. Since the STARPOWER IGBT GD100MLT65L3SF is used in the experiments, the power losses calculation is also based on the same switch. Fig. 17 shows the comparison of the switching losses and conduction losses of the proposed and conventional SHE under different modulation indexes. The switching losses include the turn ON and turn OFF losses of the IGBTs and the reverse recovery losses of the diodes. The conduction losses include the conduction losses of the IGBTs and the diodes. From the comparison results, both the switching losses and conduction losses of the proposed model are nearly the same compared with the conventional model. Because the voltage and power rating are small, a low-power fast-speed IGBT is used and the dominant loss is the conduction loss. Whereas in medium-voltage high-power applications where the ratio of switching loss will be increased significantly, the advantages of our proposed method with comparably much lower switching frequency in the CMV reduction will be more apparent.

In Fig. 18, the magnitudes of the 3rd-, 9th-, and 15th-harmonic components in CMV are presented based on the results in Figs. 11, 12, and 14–16, to bring more principium insights into

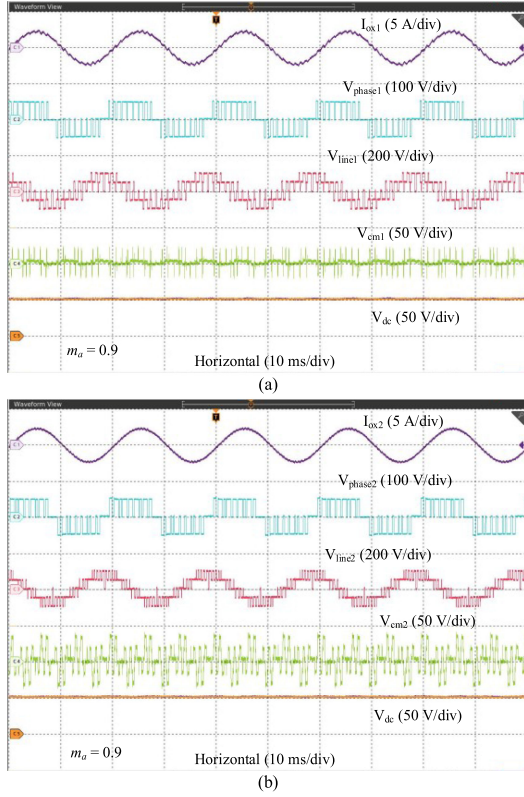


Fig. 14. Steady-state experimental results with $m_a = 0.9$. (a) With the CMV reduction model. (b) With the conventional SHE model.

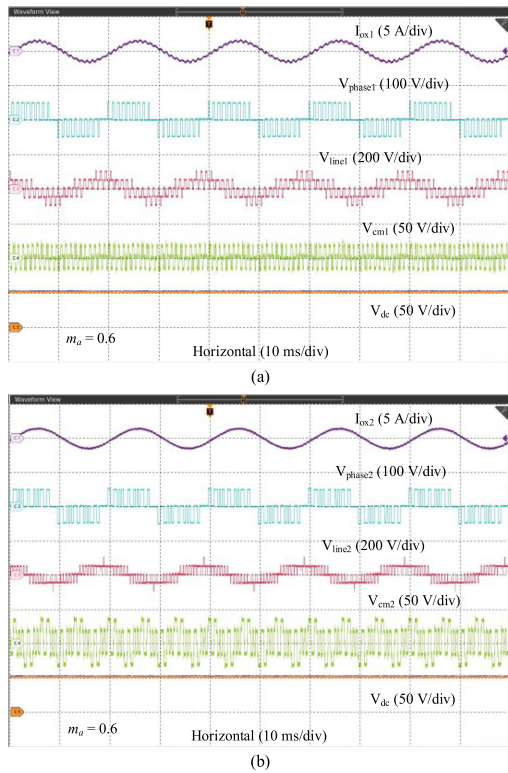


Fig. 15. Steady-state experimental results with $m_a = 0.6$. (a) With the CMV reduction model. (b) With the conventional SHE model.

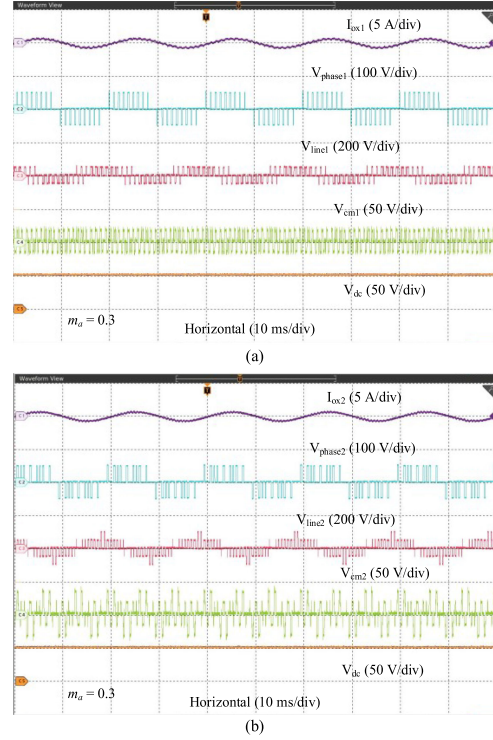


Fig. 16. Steady-state experimental results with $m_a = 0.3$. (a) With the CMV reduction model. (b) With the conventional SHE model.

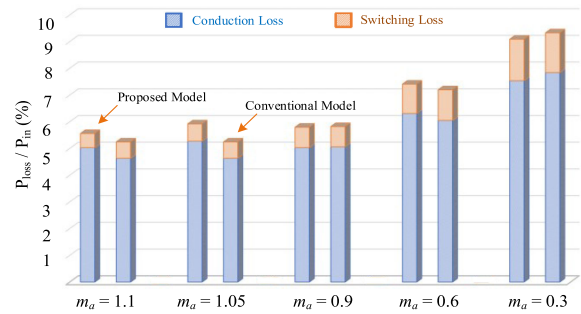


Fig. 17. Numerical comparison analysis of the switching loss and conduction loss of the proposed and conventional SHE-PWM.

the CMV reduction formulation proposed. It should be noted that the magnitude of the third harmonic with $m_a = 0.3$ is selected as the reference value and is set to 1 p.u. As shown in the results of the 9th- and 15th harmonic components, most of them are much smaller with the proposed model than the conventional model, while the same results are with the third harmonic in low and medium m_a range. This phenomenon is exactly the reason for the reduced CMV with the proposed model. As for the results with third harmonic at high m_a range, i.e., 6.1 p.u. in $m_a = 1.05$ and 8.4 p.u. in $m_a = 1.1$ with the proposed model, they are the injected optimal values to achieve the extended m_a , while the third harmonic becomes larger with higher m_a . However, such injections have little influence on the CMV reduction effects as shown in Figs. 11 and 12, and are also much smaller than the ones with the conventional model, which further demonstrate the effectiveness of the proposed formulation.

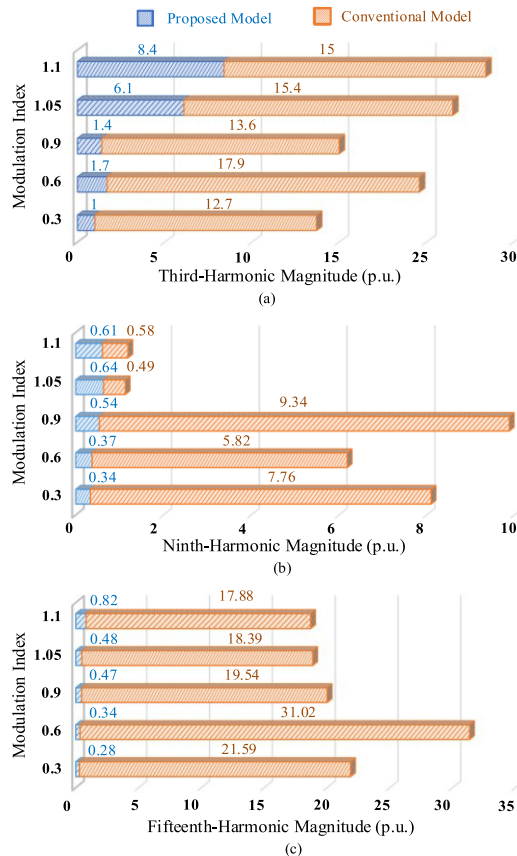


Fig. 18. Numerical comparison analysis of the low-order ZSHs in CMV. (a) Third-harmonic case. (b) Ninth-harmonic case. (c) Fifteenth-harmonic case.

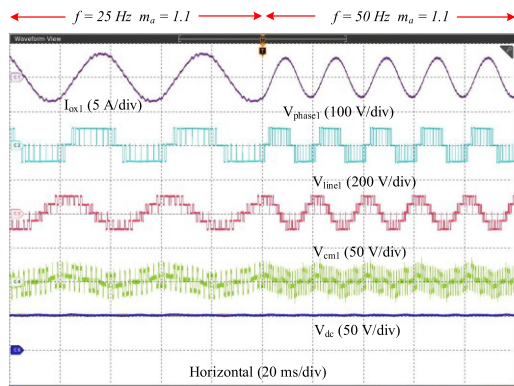


Fig. 19. Dynamic experiment results on changing the fundamental frequency from 25 to 50 Hz with $m_a = 1.1$.

To further demonstrate the dynamic performances of the proposed CMV reduction model, the experimental results on changing the fundamental frequency from 25 to 50 Hz is presented in Fig. 19. As shown in Fig. 19, both the waveform quality, CMV reduction, and dc-link capacitor balancing effects are not affected by this transition, which demonstrates the validity of the proposed method in variable fundamental frequency situation.

Since the CMV reduction models in medium and high m_a ranges are slightly different, i.e., with different values of k_g as shown in (12), the ability of smooth transition between the two

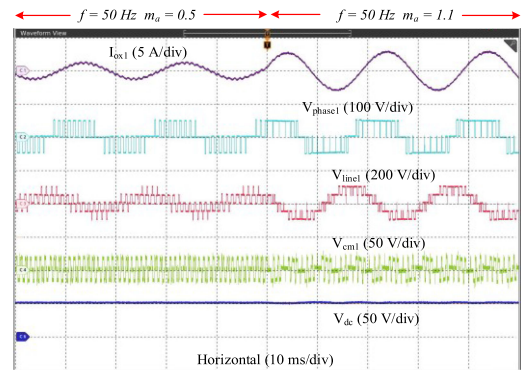


Fig. 20. Dynamic experiment results on changing the modulation index from $m_a = 0.5$ to $m_a = 1.1$ (50 Hz).

models is also very important, the result of which is presented in Fig. 20. As shown in Fig. 20, the SHE-PWM model adopted is changed from the one with $m_a = 0.5$ ($k_g = 0$) to the one with $m_a = 1.1$ ($k_g = 0.5$), where no ripple and peak current/voltage is presented in all waveforms, and the CMV reduction and dc-link capacitor voltage balancing effects are not influenced by this transition as well. Therefore, it is proved that the smooth transition between the two models can be easily achieved.

VII. CONCLUSION

This article proposes a generalized multilevel SHE-PWM formulation with CMV reduction abilities that is valid in full modulation index range. The CMV reduction in low and medium modulation index range is achieved by eliminating the low-order ZSHs in the three SHE-PWM phase voltage waveforms, while an optimal third-harmonic component is injected in high modulation index range to extend the maximum achievable modulation index from 1 to 1.15. Compared with the existing CMV reduction methods, the proposed method has the following advantages.

- 1) The proposed CMV reduction method can be generalized and is suitable for any type of MLCs with any output levels (N -level), i.e., both odd-level and even-level cases, operated over the whole modulation index range without any auxiliary hardware installed.
- 2) The implementation complexity of the proposed method is much lower compared with the SVM- and CBM-based ones with complex vector/carrier distribution design. The proposed method only needs to solve the nonlinear SHE equations as in (7) and (12), which are very easy to deal with by using the simple and efficient solving algorithms introduced in this article, i.e., with off-line optimization method by just using the *fmincon* with MATLAB or with the real-time hybrid algebraic-numerical method.
- 3) The switching frequency and switching losses with the proposed method are lower than the other methods due to the implementation of SHE-PWM.
- 4) Related capacitor voltage balancing methods for the proposed model are explained, and the coupling effects with CMV reduction are analyzed in detail.

REFERENCES

- [1] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.
- [2] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multi-level voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [4] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.
- [5] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A four-level hybrid-clamped converter with natural capacitor voltage balancing ability," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1152–1162, Mar. 2014.
- [6] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1907–1918, May 2013.
- [7] H. Tian and Y. W. Li, "An active capacitor voltage balancing method for seven-level hybrid clamped (7L-HC) converter in motor drives," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2372–2388, Mar. 2020.
- [8] M. H. Hedayat, A. B. Acharya, and V. John, "Common-mode filter design for PWM rectifier-based motor drives," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5364–5371, Nov. 2013.
- [9] D. O. Boillat, F. Krismer, and J. W. Kolar, "EMI filter volume minimization of a three-phase, three-level T-type PWM converter system," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2473–2480, Apr. 2017.
- [10] H. Akagi, H. Hasegawa, and T. Doumoto, "Design and performance of a passive EMI filter for use with a voltage-source PWM inverter having sinusoidal output voltage and zero common-mode voltage," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1069–1076, Jul. 2004.
- [11] A. Muetze and C. R. Sullivan, "Simplified design of common-mode chokes for reduction of motor ground currents in inverter drives," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2570–2577, Nov./Dec. 2011.
- [12] T. K. T. Nguyen, N. V. Nguyen, and N. R. Prasad, "Novel eliminated common-mode voltage PWM sequences and an online algorithm to reduce current ripple for a three-level inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7482–7493, Oct. 2017.
- [13] T. K. T. Nguyen and N. V. Nguyen, "An efficient four-state zero common mode voltage PWM scheme with reduced current distortion for a three level inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1021–1030, Feb. 2018.
- [14] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008.
- [15] Q. A. Le and D. Lee, "Elimination of common-mode voltages based on modified SVPWM in five-level ANPC inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 173–183, Jan. 2019.
- [16] W. Li, Y. Wang, J. Hu, H. Yang, C. Li, and X. He, "Common-mode current suppression of transformerless nested five-level converter with zero common-mode vectors," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4249–4258, May 2019.
- [17] L. Kai, J. Zhao, W. Wu, L. Ma, and G. Zhang, "Performance analysis of zero common-mode voltage pulse-width modulation techniques for three level neutral point clamped inverters," *IET Power Electron.*, vol. 9, no. 14, pp. 2654–2664, Sep. 2016.
- [18] X. Yuan, J. Yon, and P. Mellor, "Common-mode voltage reduction in three level neutral-point-clamped converters with neutral point voltage balance," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2013, pp. 1–6.
- [19] J. Wang *et al.*, "A novel discontinuous modulation strategy with reduced common-mode voltage and removed DC offset on neutral-point voltage for neutral-point-clamped three-level converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7637–7649, Aug. 2019.
- [20] C. Qin, C. Zhang, X. Xing, X. Li, A. Chen, and G. Zhang, "Simultaneous common-mode voltage reduction and neutral-point voltage balance scheme for the quasi-Z-source three-level T-type inverter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1956–1967, Mar. 2020.
- [21] X. Zhang, X. Wu, C. Geng, X. Ping, S. Chen, and H. Zhang, "An improved simplified PWM for three-level neutral point clamped inverter based on two-level common-mode voltage reduction PWM," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 11143–11154, Oct. 2020.
- [22] A. Choudhury, P. Pillay, and S. S. Williamson, "Modified DC-bus voltage balancing algorithm for a three-level neutral-point-clamped PMSM inverter drive with reduced common-mode voltage," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 278–292, Jan./Feb. 2016.
- [23] W. Jiang *et al.*, "A novel virtual space vector modulation with reduced common-mode voltage and eliminated neutral point voltage oscillation for neutral point clamped three level inverter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 884–894, Feb. 2020.
- [24] X. Xu, Z. Zheng, K. Wang, B. Yang, and Y. Li, "A comprehensive study of common mode voltage reduction and neutral point potential balance for a back-to-back three-level NPC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7910–7920, Aug. 2020.
- [25] K. Wang, Y. Li, Z. Zheng, L. Xu, and B. Fan, "A common-mode voltage reduction method for a back-to-back four-level hybrid-clamped converter," *Proc. 18th Int. Conf. Elect. Mach. Syst.*, Pattaya, Thailand, 2015, pp. 1558–1563.
- [26] K. D. Pham and N. V. Nguyen, "A reduced common-mode-voltage pulse width modulation method with output harmonic distortion minimization for three-level neutral-point-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6944–6962, Jul. 2020.
- [27] P. Liu, S. Duan, C. Yao, and C. Chen, "A double modulation wave CBPWM strategy providing neutral-point voltage oscillation elimination and CMV reduction for three-level NPC inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 16–26, Jan. 2018.
- [28] M. Tsai, H. Chen, M. Tsai, Y. Wang, and P. Cheng, "Evaluation of carrier-based modulation techniques with common-mode voltage reduction for neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3268–3275, Apr. 2018.
- [29] F. Wang, Z. Li, and X. Tong, "Modified predictive control method of three-level simplified neutral point clamped inverter for common-mode voltage reduction and neutral-point voltage balance," *IEEE Access*, vol. 7, pp. 119476–119485, 2019.
- [30] Y. Yang *et al.*, "Computation-efficient model predictive control with common-mode voltage elimination for five-level ANPC converters," *IEEE Trans. Transp. Electric.*, vol. 6, no. 3, pp. 970–984, Sep. 2020.
- [31] X. Xing, A. Chen, Z. Zhang, J. Chen, and C. Zhang, "Model predictive control method to reduce common-mode voltage and balance the neutral-point voltage in three-level T-type inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2016, pp. 3453–3458.
- [32] H. Zhang, A. V. Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.
- [33] J. Rodriguez, J. Pontt, P. Correa, P. Cortes, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 834–839, Aug. 2004.
- [34] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sep. 2007.
- [35] T. T. Nguyen, N. Nguyen, and N. R. Prasad, "Eliminated common-mode voltage pulsewidth modulation to reduce output current ripple for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5952–5966, Aug. 2016.
- [36] N. Nguyen, T. T. Nguyen, and H. Lee, "A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5425–5438, Oct. 2015.
- [37] Z. Lim, A. I. Maswood, and G. H. P. Ooi, "Common-mode reduction for ANPC with enhanced harmonic profile using interleaved sawtooth carrier phase-disposition PWM," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7887–7897, Dec. 2016.
- [38] K. D. Pham and N. V. Nguyen, "A reduced common-mode-voltage pulsewidth modulation method with output harmonic distortion minimization for three-level neutral-point-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6944–6962, Jul. 2020.
- [39] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.
- [40] M. Wu, Y. W. Li, and G. Konstantinou, "A comprehensive review of capacitor voltage balancing strategies for multilevel converters under selective harmonic elimination PWM," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2748–2767, Mar. 2021.
- [41] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1152–1158, Mar. 2012.

- [42] J. Dai, G. Li, and C. Hu, "Study on a new method to eliminate the common-mode voltage based on improved SHEPWM," in *Proc. IEEE 10th Conf. Ind. Electron. Appl.*, Auckland, New Zealand, 2015, pp. 1633–1636.
- [43] M. Sharifzadeh *et al.*, "Hybrid SHM-PWM for common mode voltage reduction in three-phase three-level NPC inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Nov. 11, 2020, doi: [10.1109/JESTPE.2020.3037283](https://doi.org/10.1109/JESTPE.2020.3037283).
- [44] S. Bowes and B. Bird, "Novel approach to the analysis and synthesis of modulation processes in power converters," *Proc. Inst. Elect. Eng.*, vol. 122, no. 5, pp. 507–513, May 1975.
- [45] B. Tan, Z. Gu, K. Shen, and X. Ding, "Third harmonic injection SPWM method based on alternating carrier polarity to suppress the common mode voltage," *IEEE Access*, vol. 7, pp. 9805–9816, 2019.
- [46] M. H. Etesami, D. M. Vilathgamuwa, N. Ghasemi, and D. P. Jovanovic, "Enhanced metaheuristic methods for selective harmonic elimination technique," *IEEE Trans. Ind. Inform.*, vol. 14, no. 12, pp. 5210–5220, Dec. 2018.
- [47] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, Apr. 2012.
- [48] K. Haghdar, "Optimal DC source influence on selective harmonic elimination in multilevel inverters using teaching–learning-based optimization," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 942–949, Feb. 2020.
- [49] R. H. Byrd, J. C. Gilbert, and J. Nocedal, "A trust region method based on interior point techniques for nonlinear programming," *Math. Program.*, vol. 89, no. 1, pp. 149–185, Nov. 2000.
- [50] K. Yang *et al.*, "Real-time switching angle computation for selective harmonic control," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8201–8212, Aug. 2019.
- [51] H. Zhao, T. Jin, S. Wang, and L. Sun, "A real-time selective harmonic elimination based on a transient-free inner closed-loop control for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1000–1014, Feb. 2016.
- [52] D. Ahmadi and J. Wang, "Online selective harmonic compensation and power generation with distributed energy resources," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3738–3747, Jul. 2014.
- [53] Y. Zhang, Y. W. Li, N. R. Zargari, and Z. Cheng, "Improved selective harmonics elimination scheme with online harmonic compensation for high-power PWM converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3508–3517, Jul. 2015.
- [54] S. R. Pulikanti, M. S. A. Dahidah, and V. G. Agelidis, "Voltage balancing control of three-level active NPC converter using SHE-PWM," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 258–267, Jan. 2011.
- [55] M. Wu, K. Wang, K. Yang, G. Konstantinou, Y. W. Li, and Y. Li, "Unified selective harmonic elimination control for four-level hybrid-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11488–11501, Nov. 2020.
- [56] M. Wu, H. Tian, Y. W. Li, G. Konstantinou, and K. Yang, "A composite selective harmonic elimination model predictive control for seven-level hybrid-clamped inverters with optimal switching patterns," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 274–284, Jan. 2021.
- [57] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std 519-2014 (Revision of IEEE Std 519-1992), Jun. 2014.
- [58] J. R. Tibola, H. Pinheiro, and R. F. de Camargo, "Closed loop selective harmonic elimination applied to a grid connected PWM converter with LCL filter," in *Proc. XI Brazilian Power Electron. Conf.*, Natal, Brazil, 2011, pp. 746–752.
- [59] N. Su, W. Huang, and S. Zheng, "Closed-loop dynamic control for dual-stator winding induction generator at low carrier ratio with selective harmonic elimination pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4737–4747, Jun. 2021.
- [60] I. Abdel-Qawee, N. Abdel-Rahim, H. A. Mansour, and T. Dakrory, "Closed-loop control of single phase selective harmonic elimination PWM inverter using proportional-resonant controller," in *Proc. 5th Int. Conf. Model., Identification Control*, Cairo, Egypt, 2013, pp. 169–174.
- [61] T. M. Parreiras and B. J. C. Filho, "Current control of three level neutral point clamped voltage source rectifiers using selective harmonic elimination," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Dallas, TX, USA, 2014, pp. 4608–4614.



Mingzhe Wu (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the China University of Mining and Technology, Beijing, China, in 2019. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada.

From 2017 to 2019, he was a Research Assistant with the Department of Electrical Engineering, Tsinghua University, Beijing, China, working on power system resilience and multilevel converters. His current research interests include harmonic control technologies and multilevel converters.



Cheng Xue (Student Member, IEEE) received the B.Eng. degree (Yisheng Mao honors.) and M.Sc. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada.

His research interests include advanced control of power electronic converters for microgrid applications and electrical machine drives.



Yun Wei (Ryan) Li (Fellow, IEEE) received the B.Eng. degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2006.

In 2005, he was a Visiting Scholar with Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow with Ryerson University, Toronto, ON, Canada. In 2007, he was also with Rockwell Automation Canada, Calgary, AB, Canada. He then joined the University of Alberta,

Edmonton, AB, Canada, where he is currently a Professor. His research interests include distributed generation, microgrid, renewable energy, high-power converters, and electric motor drives.

Dr. Li is an Editor-in-Chief for the IEEE TRANSACTIONS ON POWER ELECTRONICS LETTERS. Prior to that, he was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON SMART GRID, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the recipient of the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2013 and the Second Prize Paper Award of the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014. He is listed as a Highly Cited Researcher by the Web of Science Group.



Kehu Yang (Member, IEEE) received the B.S. degree in electrical engineering from Northwestern Polytechnical University, Xi'an, China, in 2003, and the Ph.D. degree in control theory and control engineering from the Institute of Automation, Chinese Academy of Sciences, Beijing, China, in 2009.

From 2013 to 2014, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH, USA, working on selective harmonic elimination technology and its applications in high-

power converter and electric drives. He is currently a Professor with the China University of Mining and Technology, Beijing, China. His research interests include harmonic control technologies, modeling and control methods for high-power converters, and the applications of computer algebra in power electronics.