Letters

A Double-Sided Bidirectional Power Module With Low Heat Concentration and Low Thermomechanical Stress

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***Abstract*—Double-sided structure leads to severe thermal mismatch, making attachments easy to fail. For the double-sided bidirectional switch (BDS) module, the heat concentration in the buffering spacers further increases the risk of thermal fatigue failure of the attachment, which is the key difficulty that limits the reliability and the application of the double-sided BDS module. This letter proposed a reliable double-sided BDS module with the bridge buffering spacers for both improving the heat dissipation and reducing the thermomechanical stresses. Simulation results showed that the bridge buffering spacer can decrease T_{jmax} and the maximum thermomechanical stress of the attachment between the IGBT-1 and the spacer by ∼9% and ∼35%, respectively. Furthermore, it was proved by the power cycling tests that the lifetime of the double-side BDS module using the bridge buffering spacer can be at least two times longer, i.e., more than 200 k cycles, than the one using the traditional brick buffering spacer under the same load and ∼21% longer under the same T_{jmax} and ΔT_{j}.**

***Index Terms*—Double-sided cooling, power cycling test (PCT), thermal concentration, thermomechanical stress.**

I. Introduction

An ARRAY of controlled bidirectional switches (BDSs) is a key component of the matrix converter (MC), which is a direct ac–ac power converter topology. As we know, MC can realize high performance transformation of many parameters of input/output ac without dc-link capacitors and internal energy storage components [1]. However, the operation of BDSs for the higher frequency, higher power density, and higher temperature [2] may pose great challenges on its packaging since the packaging can significantly influence the thermal, electrical, mechanical performances, and reliability of the BDSs as well as the MC.

For the conventional commercial power modules, wire bonding was widely used for power packaging. However, wire-bonded modules had relatively poor heat dissipation due to one-sided cooling capability. The bonding wires were also susceptible to thermomechanical fatigue as well as introducing significant parasitic inductance [3]. Castellazzi *et al*. [4] proposed a double-sided concept for the BDS modules, which reduced the maximum junction temperature by 25° and achieved very low stray inductance. Furthermore, the footprint could be reduced by ∼50%.

However, such double-sided packing leads to excessive heat concentration and causes tremendous thermomechanical stress [5], leading to the degradation of the soldered die attachment. Therefore, it is significant to come up with a highly integrated BDS with both low maximum junction temperature (T_{jmax}) and thermomechanical stress to benefit the reliability of the BDS. However, there is always a tradeoff between heat dissipation and thermomechanical stress. For example, Wang *et al.* [6] used molybdenum instead of copper as spacers for buffering the thermomechanical stress. Thanks to its low coefficient of thermal expansion (CTE), which matches well with silicon chips, the thermomechanical stress of the chips could be reduced by 9.8%; however, the maximum junction temperature in this case increased by 5.2% due to the poor thermal conductivity of the molybdenum. Similar conclusions could be reached by optimizing the spacer shape [7], using the trenched copper plate [8], etc.

In this letter, we propose a reliable double-sided BDS module with specially designed bridge buffering spacers instead of conventional brick buffering spacers, as shown in Fig. 1. The bridge buffering spacer can provide more heat conduction paths and stiffness rather than the conventional brick buffer spacer due to more bonding area. As a result, the heat concentration and the thermomechanical stress of the sintered attachment, especially the one between the chip and the spacer, can be reduced. It is also worth noting that the bridge buffering spacer is capable

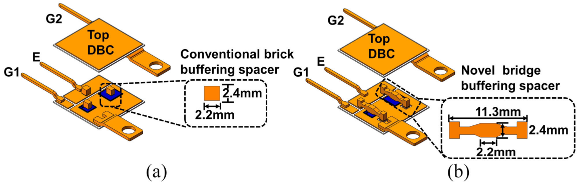

Fig. 1. Schematic diagram of the double-sided BDS module with (a) conventional brick buffering spacer and (b) novel bridge buffering spacer.

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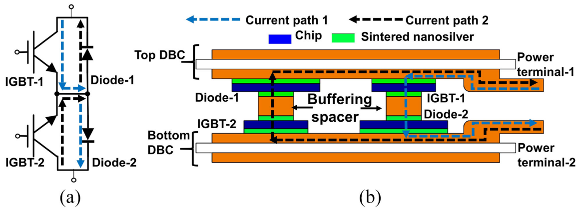

Fig. 2. (a) Circuit diagram of a double-sided BDS module. (b) Cross-sectional view of PCoP structure.

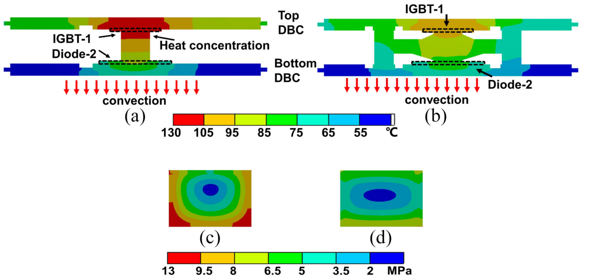

Fig. 3. Temperature comparison of double-sided BDS modules with (a) traditional brick buffer spacer. (b) Bridge buffer spacer; von Mises stresses comparison of sintered attachment between the IGBT-1 and (c) traditional brick buffer spacer. (d) Bridge buffering spacer.

of bonding the emitter and the Kelvin emitter sense terminal instead of extra unreliable bonding wires. Numerical simulation and power cycling tests (PCTs) were employed to validate the feasibility of the bridge buffering spacer.

II. Module Design

The topology of the demonstrated BDS module is defined as the common emitter BDS [9], as shown in Fig. 2(a). By controlling the insulated gate bipolar transistor (IGBT), the current could flow either through IGBT-1 and Diode-2 or IGBT-2 and Diode-1. Power Chip on Chip (PCoP) structure [4] was proposed to achieve double-sided cooling for the BDS module, as shown in Fig. 2(b).

The double-sided integration is typically composed of many materials with great mismatch of the CTEs, which causes tremendous thermomechanical stress, as well as die attachment failure usually between the chip and the spacer [5]. For the double-sided BDS module, Fig. 3(a) shows both the IGBT-1 and the Diode-2 should generate power losses, which lead to excessive heat concentration in the buffering spacers potentially, when the current flows from the power terminal-1 to the power terminal-2 as the path-1. Such excessive heat concentration in the buffering spacer further increases the risk of thermal fatigue failure of the attachment between the chip and the spacer, which is the key limitation of the reliability and promising application of double-sided BDS module.

In order to relieve such heat concentration and thermomechanical stress, we proposed the bridge buffering spacer. Fig. 3(b) shows that T_{jmax} decreases by 9.1%, i.e., 11.5 °C, compared with 126 °C of the one using the conventional brick buffering spacer, as shown in Fig. 3(a). Moreover, the maximum thermomechanical stress of the attachment between the IGBT-1 and the spacer decreases by 35%, as shown in Fig. 3(c) and (d).

TABLE I
Materials and Dimensions

Components	Description
IGBT	650-V/30-A, silicon, INFINEON IGC15T65QE 3.92mm×3.88mm×0.07mm
Diode	1200-V/50-A, silicon, INFINEON SIDC08D65C8 5.5mm×5.5mm×0.12mm
Substrate	20mm×20mm, Al_2O_3 Direct Bond Copper with 0.32mm thick Al_2O_3, 0.3mm thick copper
Attachment	Nanosilver paste, 80-µm thick
Encapsulant	Henkel Epoxy resin
Terminals	Copper plating with nickel
Bonding wires	8 mils Aluminum wire for gate pads
Buffering spacer	Copper plate plating with silver

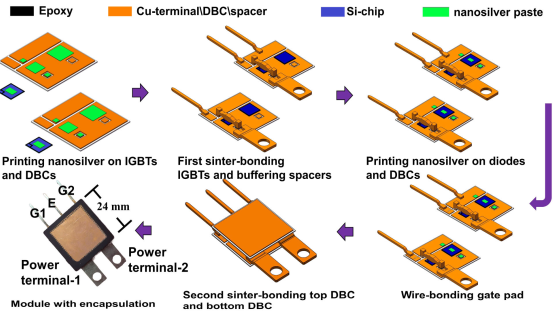

Fig. 4. Schematic fabrication process of a designed BDS module.

Furthermore, nanosilver paste has a porous microstructure and exhibits a relatively low elastic modulus, i.e., (~9 GPa) [6], which can relieve the thermomechanical stress [10], thus, we used nanosilver paste as the die-attach material instead of conventional solder alloys. The specifications of the proposed BDS module are listed in Table I.

III. Module Fabrication and Characterizations

A. Module Fabrication

In order to further confirm the benefit brought by the bridge buffering spacer, double-sided cooling BDS modules with the brick buffering spacers and the bridge buffering spacers were fabricated separately. Fig. 4 shows an example of taking the module with bridge buffering spacer to describe the fabrication process. First, 80-μm nanosilver paste was printed separately on the sides of the DBCs and the emitters of the IGBTs with the layout patterns. Then, the IGBTs, the diodes, the spacers, and the terminals were attached by pressureless sintering at 280 °C for 30 min in the formic acid reduction atmosphere according to Wang *et al.* [6]. After the first sinter-bonding, another 80-μm nanosilver paste was printed on the sides of the DBCs and the positive electrodes of the diodes for assembling the as-sintered top directed bonded copper (DBC) and the as-sintered bottom one. The gate pad was connected with the DBC substrate still using an aluminum wire. It is worth noting that an 8-mil aluminum wire was also used to bond the emitter with the Kelvin emitter terminal for the module with brick buffering spacer to monitor V_{CE} and V_{F}, whereas there is no need for the module with bridge buffering spacer thanks to the bridge shape. Then, the two DBCs were assembled by sintering at 280 °C for 30 min in the formic acid reduction atmosphere. The double-sided

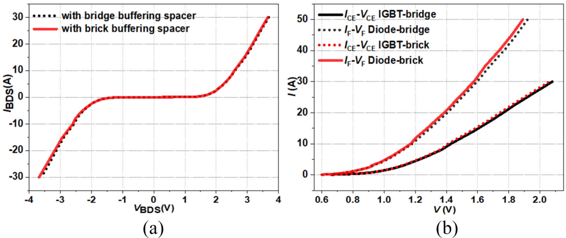

Fig. 5. *I–V* curves of (a) a BDS module and (b) IGBT and diode chips.

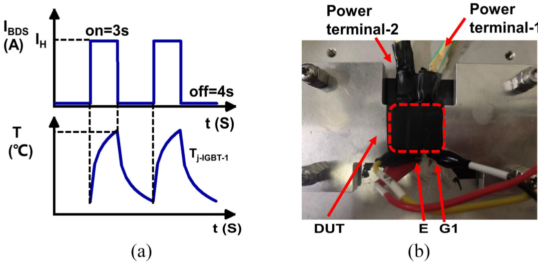

Fig. 6. (a) Schematic profile and (b) configuration of a PCT.

assembly was encapsulated by filling the gap between the two assembled DBCs with the epoxy resin at last.

B. Static Electrical Performance

The static electrical characteristics of these two types of the module were measured by a curve tracer, i.e., Tektronix 371A at 25 °C. Fig. 5 shows the *I–V* characteristics of the proposed BDS module, the IGBT, and diode bare die, respectively. In this letter, V_{BDS} was defined as the voltage between the power terminal-1 and the power terminal-2 and I_{BDS} as the current from the power terminal-1 to the power terminal-2. V_{BDS} is equal to the sum of V_{CE} and V_F. $V_{\mathrm{CE\ (sat)}}$ of the two IGBTs tested at $I_{\mathrm{C}} = 30$ A is 2.08 and 2.06 V, and V_F of the two diodes tested at $I_{\mathrm{F}} = 50$ A is 1.92 and 1.89 V, which are consistent with the values on their datasheets. It was believed that there was no device failure during the double-sided packaging, whatever using bridge or brick buffering spacer.

IV. Power Cycling Tests

A. Test Conditions

To validate the feasibility of the proposed bridge buffer, four cases were used to find out how much the service lifetime could be improved in the PCTs. The Cases A and C are the double-sided BDS modules with the conventional brick buffering spacers, whereas the Cases B and D are the ones with the bridge buffering spacers. The period of each power cycles is 7 s, i.e., 3 s for power-ON and 4 s for power-OFF, as shown in Fig. 6(a). The Cases A and B are in constant current mode to verify the reduction of the heat concentration, T_{j} of the IGBT-1 of the Case A swung between 45 to 130 °C initially. However, the Cases C and D are in the mode of constant ΔT_{j}, i.e., the same variation of T_{j} of the IGBT-1, i.e., 45 to 130 °C, to verify the improvement of the reliability even at the same T_{jmax} and ΔT_{j} when using the bridge buffering spacers. Heat convection was only applied to the bottom DBC for all the four cases and

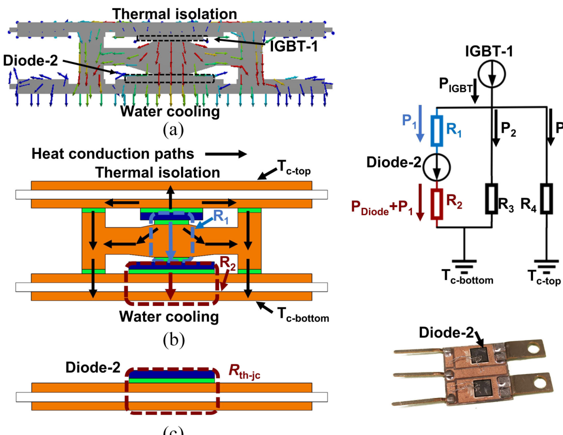

Fig. 7. (a) Heat flux simulation. (b) Equivalent thermal resistance network. (c) Sample for measuring $R_{\mathrm{th\text{-}j}}$.

the top DBC is heat-insulated using the poor conductive Kapton tape, as shown in Fig. 6(b).

B. Thermal Resistance Estimation

The failure of the bond wires increases V_{CE} significantly, but does not lead to increased *R*th, which was caused by the attachment degradation [11]. It is believed that the failure mode in the double-sided BDS module was the attachment degradation because there were no bonding wires for force current in the double-sided power modules. It was critical to monitor the change of *R*th, especially of the attachment between the chip and the spacer. We proposed a simplified method to characterize the change of *R*th for monitoring the degradation of the attachment between the chip and the spacer.

Fig. 7(a) shows the simulated heat flux of the module with the bridge buffering spacer when reaching thermal equilibrium. The heat due to the power loss of the IGBT-1, i.e., P_{IGBT}, can flow out along three paths, i.e., passing to the bottom DBC through the Diode-2, i.e., P_1; passing to the bottom DBC through the spacers instead of the Diode-2, i.e., P_2; passing to the top DBC through IGBT-1, i.e., P_3. The equivalent thermal resistance network is shown in Fig. 7(b). Considering that the top DBC could be assumed as heat-insulated, P_3 could be ignored. R_1 and R_2 could be obtained as follows:

$$R_2 = \frac{T_{\mathrm{j-Diode-2}} - \mathrm{T}_{\mathrm{c-bottom}}}{P_1 + P_{\mathrm{diode}}} \tag{1}$$

$$R_1 = \frac{T_{\mathrm{j-IGBT-1}} - T_{\mathrm{j-Diode-2}}}{P_1} \tag{2}$$

where P_{IGBT} and P_{Diode} can be detected directly, whereas $T_{\text{j-IGBT-1}}$ and $T_{\text{j-Diode-2}}$ can be detected indirectly with V_{CE} as the temperature-sensitive parameter [12]. R_2 is *R*th from the Diode-2 to bottom DBC, which is equal to $R_{\mathrm{th\text{-}jc}}$ of the sample without the spacer and the top DBC, as shown in Fig. 7(c), which is easy to be measured. Moreover, it is believed that R_2 should be a constant during the PCTs due to which the power loss of the Diode-2 is much lower than that of the IGBT-1 and is close to the water cooling. R_3 is the equivalent thermal resistance from the IGBT-1 to the bottom DBC through the top DBC and the buffering spacers.

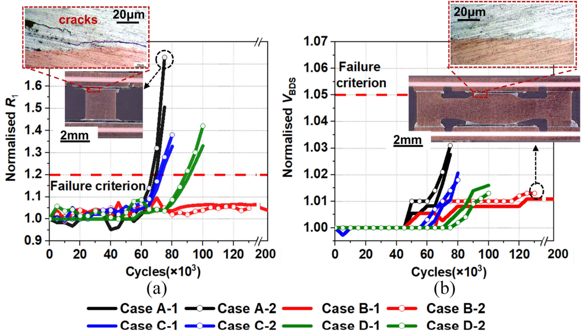

Fig. 8. (a) R_1 and (b) $V_{\rm BDS}$ of double-sided BDS modules versus number of power cycles.

R_1 is Rth between the IGBT-1 and the Diode-2, thus, the change of R_1 can indicate the degradation of the attachment between the chip and the spacer directly. Therefore, combining (1) and (2), $R_1(N)$ after N cycles of the PCTs can be calculated as the following:

$$R_1(N) = \frac{T_{\rm j-IGBT-1}(N) - T_{\rm j-Diode-2}(N)}{\frac{T_{\rm j-Diode-2}(N) - T_{\rm c-bottom}(N)}{R_2} - P_{\rm Diode-2}(N)}. \quad (3)$$

For the double-sided BDS module with the brick buffering spacer, the heat generated by the IGBT-1 can also flow out along two paths, i.e., passing to the bottom DBC through the Diode-2 and passing to the bottom DBC through the spacers between the IGBT-2 and the Diode-1 instead of the Diode-2. Thereby, the aforementioned method is also applicable.

Based on the aforementioned method, R_2 of the double-sided BDS module is 0.24 °C/W and R_1 of the double-sided BDS modules with the bridge and the brick buffering spacer is 2.00 and 2.11 °C/W, respectively.

C. Results and Discussion

The PCTs were shortly paused every 5000 cycles for recording R_1 and the failure criterion was defined as a 20% increase of R_1. The Cases A-1 and A-2 are two samples under the same PCTs conditions. After 70000 cycles, R_1 of the Cases A-1 and A-2 rose to ~21% and ~32%, respectively, as shown in Fig. 8(a). The increase of R_1 indicates the degradation in the attachment, which was also proved by the presence of the cracks in the sintered nanosilver between the IGBT-1 and the spacer, as shown in Fig. 8(a). However, there is still no failure of the Cases B-1 and B-2 even after more than 200000 cycles as expected. Thanks to the more heat conduction paths of the bridge buffering spacer, $T_{\rm jmax}$ of the Case B could be ~12 °C lower than that of the Case A, i.e., 45 to 118 °C, under the same heating current. In addition, comparing the Cases C and D, it can be proved that the service lifetime can be increased by ~21% even in the constant junction temperature mode of the same $T_{\rm jmax}$ and $\Delta T_{\rm j}$, i.e., 45 to 130 °C when using the bridge buffering spacers due to the decrease of the thermomechanical stresses.

Although the attachment degradation does not increase $V_{\rm BDS}$ significantly, $V_{\rm BDS}$ was also recorded during the short pause of the PCTs at 25 °C and $I_{\rm BDS} = 30$ A statically. Fig. 8(b) shows that $V_{\rm BDS}$ of all four cases changed no more than 3%, i.e., 0.1 V.

It is worth noting that the bonding wire with the emitter sense terminal in the Cases A and C lifted-off after 75000 cycles and 85000 cycles, respectively, due to the heat concentration as well as great junction temperature swings. Then, the Kelvin emitter terminals could not be used to monitor $V_{\rm CE}$ of the IGBT-1 and $V_{\rm BDS}$ had to be monitored by the power terminal instead. Thanks to the bridge buffering spacer, the Kelvin emitter of the Case D was always applicable without degradation. It should be risky to use any bonding wires, even when only used as sense, for a double-sided BDS module. The bridge buffering spacer could provide a guidance for the reliable design of a double-sided BDS module.

V. Conclusion

In this letter, a reliable double-sided BDS module with the bridge buffering spacers was designed and fabricated. Thanks to the relief of heat concentration, $T_{\rm jmax}$ and the lifetime of the double-side BDS module using the bridge buffering spacer can be ~9% lower and at least two times longer than the one using the traditional brick buffering spacer. Moreover, thanks to enhancement of the spacer stiffness, the bridge buffering spacer can also prolong the lifetime of the BDS module by ~21% even under the same $T_{\rm jmax}$ and $\Delta T_{\rm j}$.

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