A 2.4-GHz CMOS Differential Class-DE Rectifier With Coupled Inductors

Tingxu Hu, Mo Huang, *Senior Member, IEEE*, Yan Lu, *Senior Member, IEEE*, Xiu Yin Zhang, *Senior Member, IEEE*, Franco Maloberti, *Life Fellow, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—In this article, we present a 2.4-GHz differential class-DE synchronous rectifier. First, we investigate zero-voltage switching (ZVS), zero-current switching (ZCS), and impedance matching requirements for the single-ended class-DE rectifier. Then, we propose a differential topology that achieves near-optimum ZVS, ZCS, and impedance matching with a reduced number of *LC* networks. We use a coupled inductor structure to reduce the cost overhead of the differential topology and discuss its design considerations. To maintain the ZVS/ZCS operation within a wide input power range, we employ an adaptive bias circuit to adjust the gate bias voltages with the input power. Additionally, we discuss the imperfections caused by load variation. The chip, fabricated in a 65-nm CMOS process, measures the peak power conversion efficiency (PCE) of 68.5% at a 9-dBm input power with a 250-Ω load resistance. The measured input power range when PCE $>$ 40% is 16 dB.**

***Index Terms*—Class-DE rectifier, CMOS differential rectifier, coupled inductors, radio frequency (RF), wireless power transfer (WPT).**

I. Introduction

With the rapid development of the Internet-of-Things (IoT), there is an increasing demand to extend battery lifetime or even design a batteryless wireless sensor node. Hence, energy harvesting and wireless power transfer (WPT) techniques are highly favorable. Among these techniques, radio frequency (RF) WPT is one of the reliable solutions due to its insensitivity to environmental variations [1]. Furthermore, the industrial, scientific, and medical (ISM) bands, especially the 2.4 GHz band, attract the most attention among the RF bands, because of the compactness and infrastructural reusability to the matured standards such as Wi-Fi and Bluetooth low-energy (BLE) [2]–[10].

The power level available in many environments is as small as several μW [1], but there are IoT applications whose load circuits may consume more than 1 mW [11], [12]. Therefore, the IoT nodes may have to work with an ultralow duty-cycle mode. A dedicated power transmitter is a solution to charge the IoT nodes intensively [6]. Consequently, many rectifiers [3]–[5], [13]–[16] target a higher input power of 0.1–10 mW, which is also our design target.

In the RF WPT system, the rectifier is the critical building block to transform the received RF power to dc. One of the most critical rectifier metrics is power conversion efficiency (PCE), which affects the wireless power transmission distance. To achieve a high PCE, discrete components, e.g., Schottky diode [2], [17] with a low voltage drop, were necessary for many previous RF rectifiers. However, the Schottky diodes are incompatible with a standard CMOS process. The off-chip implementation increases the volume and cost of the system.

There are two major categories for CMOS RF rectifiers. The first one uses a diode-connected MOSFET as the rectifying device [18], with gate–source connected for unidirectional current conduction. However, it suffers from a low PCE because of the relatively high drain–source voltage drop. To mitigate this, the work in [19]–[21] proposed threshold compensation techniques, by adding a compensation voltage between the gate and source. Large reverse leakage currents can thereby result from the high compensation voltage [19]. As advanced solutions, the work in [20] clamped the compensation voltage, whereas the work in [21] made the voltage programmable.

The second category utilizes MOSFET as a turn-ON/-OFF switch, which significantly reduces the drain–source voltage drop. In [13] and [22], the cross-connected (CC) rectifying MOSFETs provide positive feedback to minimize the turn-ON resistance. However, a significant reverse leakage current occurs under a high input power (P_{IN}) because of the switches' early turn-ON and late turn-OFF. To reduce the reverse leakage current, the work in [23]–[25] proposed ac-coupled driving signals with a lower bias voltage, and the work in [26] tuned the gate bias

Manuscript received November 25, 2020; revised January 19, 2021; accepted February 19, 2021. Date of publication February 24, 2021; date of current version June 1, 2021. This work was supported in part by the Natural Science Foundation of China under Grant 61974046, in part by the Science and Technology Development Fund, Macau SAR, under Grants 145/2019/A3 and SKL-AMSV(UM)-2020-2022, and in part by the Research Committee of the University of Macau under Grant MYRG2020-00117-IME. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Mo Huang.)*

Tingxu Hu, Mo Huang, and Yan Lu are with the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, Department of Electrical and Computer Engineering, Institute of Microelectronics, University of Macau, Macao 999078, China (e-mail: yc07463@um.edu.mo; mohuang@um.edu.mo; yanlu@um.edu.mo).

Xiu Yin Zhang is with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510641, China (e-mail: zhangxiuyin@hotmail.com).

Franco Maloberti is with the Department of Electrical, Computer, and Biomedical Engineering, University of Pavia, 27100 Pavia, Italy (e-mail: franco.maloberti@unipv.it).

Rui P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, Department of Electrical and Computer Engineering, Institute of Microelectronics, University of Macau, Macao 999078, China. He is on leave from Instituto Superior Tcnico, Universidade de Lisboa, 1049-001 Lisbon, Portugal (e-mail: rmartins@um.edu.mo).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3061703.

Digital Object Identifier 10.1109/TPEL.2021.3061703

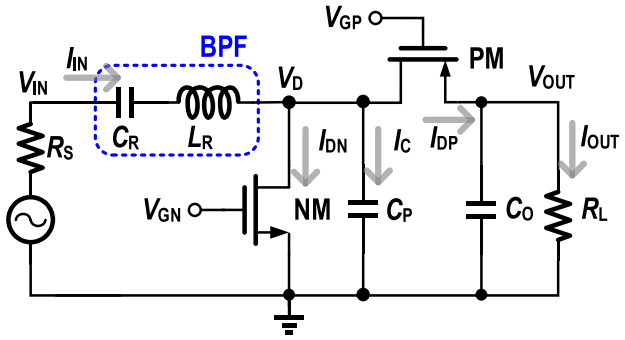


Fig. 1. Schematic of a conventional single-ended class-DE rectifier.

in the CC rectifier to an optimal point that compromises the turn-ON resistance.

Another solution against the reverse leakage current is the synchronous rectifier, which can obtain zero voltage switching (ZVS) and zero current switching (ZCS). Several publications discuss topologies of synchronous rectifier, e.g., class-E [5], [27], class-DE [14], and class-F [28]. Among these topologies, the class-DE rectifier, presented in Fig. 1, manages to achieve ZVS and ZCS with reduced voltage stress on the rectifying devices [29]. Nevertheless, a conventional single-ended class-DE rectifier needs multiple inductor–capacitor (*LC*) networks, to simultaneously achieve a matched input impedance and synchronous driving signals with a predetermined phase shift. This solution increases the device cost.

This article proposes a differential class-DE synchronous rectifier, aiming at near-optimum ZVS and ZCS operations, with a simultaneous cost reduction and high-PCE input power range extension. This article's organization is as follows. Section II presents the working principles of the differential class-DE rectifier. Section III shows the implementation of the proposed rectifier. Section IV analyzes the effects on load variation. Section V presents the measurement results and comparison with the state-of-the-art works. Finally, Section VI draws the conclusion.

II. Working Principles of the Differential Class-DE Rectifier

This section first analyzes the ZVS, ZCS, and impedance matching conditions for a conventional single-ended class-DE rectifier. Then, we derive multiple solutions based on the conditions. The circuit using a differential topology with coupled inductors minimizes the cost overhead.

A. ZVS and ZCS Conditions of a Conventional Class-DE Rectifier

Fig. 1 shows the schematic of a conventional class-DE rectifier, where R_S is the source impedance, NM and PM are the rectifying MOSFETs, C_P is the parasitic capacitance on node V_D, C_O is the output capacitor, and R_L is the load resistance. L_R and C_R make a bandpass filter (BPF) to filter the harmonics of I_{IN} out. For conciseness, we analyze its working principle based on the following assumptions, similar to [29].

1) All the passive components are ideal.

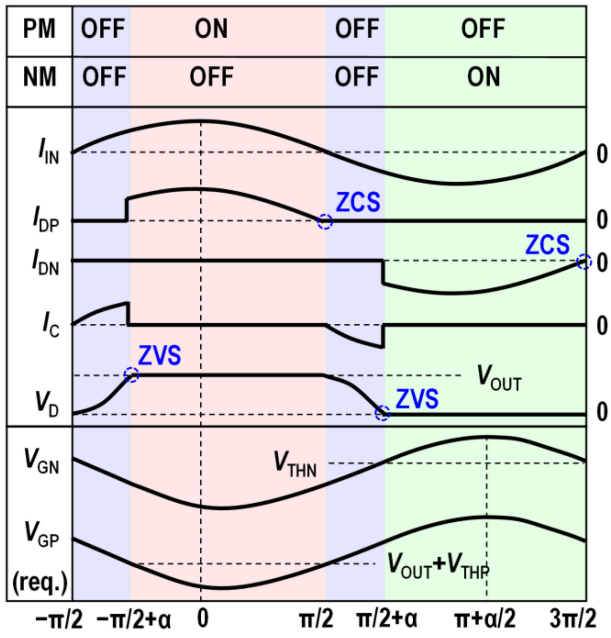


Fig. 2. Conceptual waveforms of a conventional class-DE rectifier within one operating cycle, and the required (shown as req.) driving signals for ZVS and ZCS.

2) The BPF blocks all the harmonics of I_{IN}. Thus, I_{IN} becomes an ideal sinusoidal signal $I_{IN}(\theta) = I_m \cos\theta$, where I_m is the magnitude, and $\theta = \omega t$ is the angular position.
3) The input voltage V_{IN} and the gate-drive signals of NM and PM (V_{GN} and V_{GP}) are also sinusoidal. V_{GN} and V_{GP} include both the ac and dc components.
4) The switches can fully turn-ON when $|V_{GS}| > |V_{TH}|$, with a negligible turn-ON resistance, and there is no leakage current with turned-OFF switches.

Fig. 2 displays this conventional class-DE rectifier's conceptual waveforms and the required (shown as req.) driving signals for ZVS and ZCS. We divide the analysis into four parts.

1) Within the interval of $[-\pi/2, -\pi/2 + \alpha]$, NM and PM are both turned OFF. I_{IN} charges C_P, and V_D starts to increase. V_D within this interval is

$$V_D(\theta) = \frac{1}{\omega C_P}\int_{-\pi/2}^{\theta} I_{IN}(\theta)\, d\theta = \frac{I_m}{\omega C_P}(1+\sin\theta). \tag{1}$$

For a PMOS ZVS turn-ON, V_{GP} should be equal to $V_{OUT} + V_{THP}$ when $V_D = V_{OUT}$ at an instant angular position $-\pi/2 + \alpha$. Then, V_{OUT} is

$$V_{OUT} = V_D(-\pi/2+\alpha) = \frac{I_m}{\omega C_P}(1-\cos\alpha). \tag{2}$$

2) Within $[-\pi/2 + \alpha, \pi/2]$, PM is ON, while V_D is shorted to V_{OUT} as

$$V_D(\theta) = V_{OUT}. \tag{3}$$

Regarding a PMOS ZCS turn-OFF, V_{GP} should be equal to $V_{OUT} + V_{THP}$ when $I_{IN} = 0$ at $\pi/2$. Combining the V_{GP} conditions of the ZVS turn-ON, V_{GP} is $\pi + \alpha/2$ lagging behind I_{IN}.

We solve the output current I_{OUT} by averaging the PMOS current I_{DP} within a cycle

$$I_{\mathrm{OUT}} = \frac{1}{2\pi}\int_{-\pi/2}^{3\pi/2} I_{\mathrm{IN}}(\theta)\,d\theta = \frac{I_{\mathrm{m}}}{2\pi}(1+\cos\alpha). \quad (4)$$

With (2), (4), and $V_{\mathrm{OUT}}/I_{\mathrm{OUT}} = R_{\mathrm{L}}$, α becomes

$$\alpha = \cos^{-1}\left(\frac{2\pi - \omega R_{\mathrm{L}} C_{\mathrm{P}}}{2\pi + \omega R_{\mathrm{L}} C_{\mathrm{P}}}\right). \quad (5)$$

3) Similarly, within $[\pi/2, \pi/2+\alpha]$, NM and PM are both turned OFF. I_{IN} discharges C_{P}, and V_{D} starts to decrease as

$$V_{\mathrm{D}}(\theta) = V_{\mathrm{OUT}} + \frac{1}{\omega C_{\mathrm{P}}}\int_{\pi/2}^{\theta} I_{\mathrm{IN}}(\theta)\,d\theta = V_{\mathrm{OUT}} + \frac{I_{\mathrm{m}}}{\omega C_{\mathrm{P}}}(\sin\theta - 1). \quad (6)$$

To achieve an NMOS ZVS, V_{GN} should be equal to V_{THN} when $V_{\mathrm{D}} = 0$ at $\pi/2+\alpha$.

4) Within $[\pi/2+\alpha, 3\pi/2]$, NM is turned ON. Then, V_{D} goes to ground

$$V_{\mathrm{D}}(\theta) = 0.. \quad (7)$$

To achieve an NMOS ZCS, V_{GN} should reach V_{THN} when $I_{\mathrm{IN}} = 0$ at $3\pi/2$. Similar to V_{GP}, V_{GN} should be $\pi + \alpha/2$ lagging behind I_{IN}.

B. Conditions of Simultaneous ZVS/ZCS and Impedance Matching

A conventional class-DE rectifier with ZVS and ZCS can be designed based on the analysis mentioned above. Another factor that we need to consider is the input impedance matching. It is necessary to include a phase shifter (PS) and matching networks (MN) to fulfill both aspects, as shown in Fig. 3(a).

As observed, two parallel paths are connected to the input—one is the power path to V_{D}, the other is the gate drive path to V_{G}. In [5], an *LC* matching network (MN_1), reused from BPF, transforms the V_{D} impedance to $Z_1 = R_{\mathrm{S}}$. In addition, another *LC* matching network (MN_2) transforms the V_{G} impedance to a high resistance Z_2, by canceling the imaginary part. Then, the PS network fulfills both $Z_3 = Z_2$ and the required $\pi + \alpha/2$ phase shift between V_{G} and V_{IN}. Hence, the combined input impedance becomes R_{S}, matching the source impedance.

However, as derived in detail in Appendix A, the design in Fig. 3(a) can only achieve impedance matching and ZVS/ZCS simultaneously when $R_{\mathrm{L}} = R_{\mathrm{L,OPT}}$, where

$$R_{\mathrm{L,OPT}} = \frac{2\pi\left(1-\sqrt{1-\pi\omega C_{\mathrm{P}} R_{\mathrm{S}}}\right)}{\omega C_{\mathrm{P}}\left(1+\sqrt{1-\pi\omega C_{\mathrm{P}} R_{\mathrm{S}}}\right)}. \quad (8)$$

Fig. 4 plots the calculated $R_{\mathrm{L,OPT}}$ versus C_{P} under $R_{\mathrm{S}} = 50\,\Omega$ and the 2.4-GHz frequency, where $R_{\mathrm{L,OPT}}$ increases with C_{P}. As a general design consideration, the size of the rectification devices (or C_{P}) should increase with the targeted P_{IN} level to reduce the conduction loss, indicating an increase in $R_{\mathrm{L,OPT}}$ as well. However, R_{L} should decrease with an increasing P_{IN} level to prevent a high V_{OUT} to overstress the transistors. To address this contradiction, another *LC* matching network [grey block MN, as shown in Fig. 3(a)] may be added, facilitating another design freedom for simultaneous impedance matching and ZVS/ZCS.

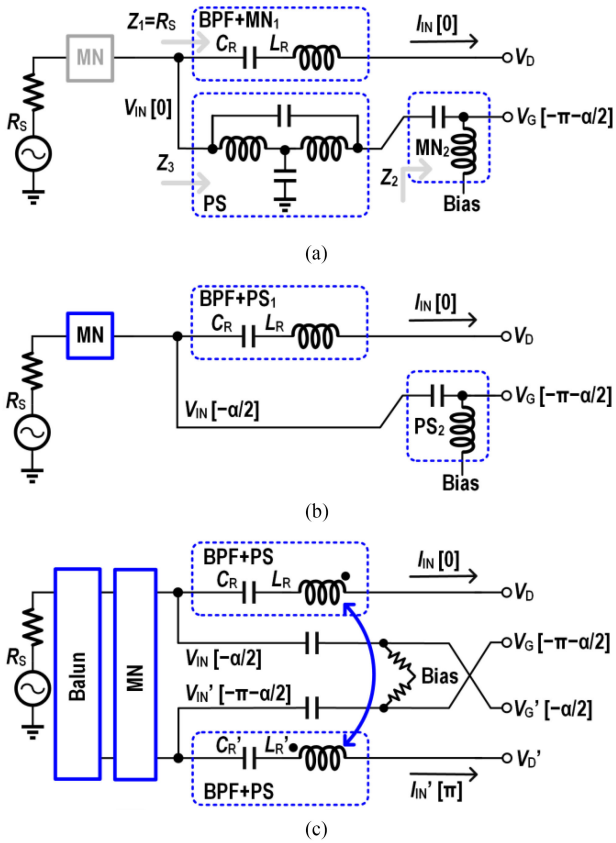


Fig. 3. BPF, PS, and MN of (a) conventional single-ended rectifier, (b) possible simplified single-ended rectifier with an extended $R_{\mathrm{L,OPT}}$ range, and (c) differential rectifier with coupled inductors and an extended $R_{\mathrm{L,OPT}}$ range. The phase value is included in the brackets.

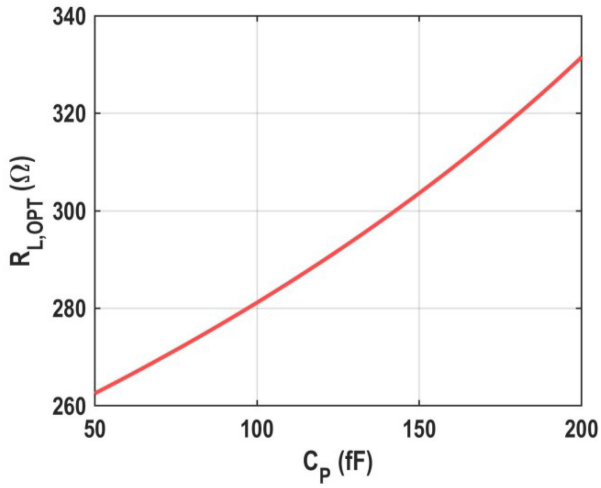


Fig. 4. $R_{\mathrm{L,OPT}}$ versus C_{P} with a matched impedance, under $R_{\mathrm{S}} = 50\,\Omega$ and 2.4-GHz frequency.

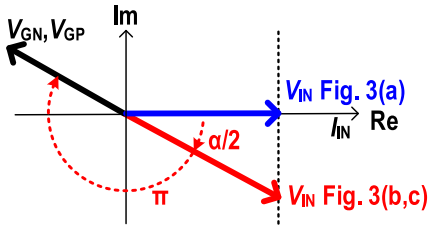


Fig. 5. Phase relationships among $I_{\rm IN}$, $V_{\rm IN}$, and $V_{\rm G}$ of the topologies in Fig. 3.

Subsequently, the synchronous driving signals $V_{\rm GN}$ and $V_{\rm GP}$ should be carefully designed to meet ZVS/ZCS, as in Fig. 5. Complying with $I_{\rm IN}$ having a zero phase (on the real axis of the complex plane), as well as the matched input impedance, $V_{\rm IN}$ should also be on the real axis of the already matched input impedance. Then, $V_{\rm GN}$, $V_{\rm GP}$ should lag $I_{\rm IN}$ by $\pi + \alpha/2$ as previously derived, which is generated by PS.

In summary, to achieve ZVS, ZCS, and impedance matching simultaneously, the conventional class-DE single-ended rectifier can be designed as follows.

1) Select the sizes of NM, PM, the value of $L_{\rm R}$, and $R_{\rm L}$ and estimate the parasitic capacitance $C_{\rm P}$ from simulation.
2) Calculated α and $C_{\rm R}$ from (5) and (18), respectively.
3) Cancel the imaginary part of Z_2 with $\rm MN_2$.
4) Design PS to obtain a $\pi + \alpha/2$ phase delay.
5) Design the bias circuit to obtain the $V_{\rm GN}$, $V_{\rm GP}$ duty cycle of $(\pi - \alpha)$ / (2π) according to Fig. 2, as discussed next.
6) Design MN in case $R_{\rm L} \neq R_{\rm L,OPT}$.

C. Single-Ended Rectifier With an Extended $\rm R_L$ Range

Fig. 3(b) shows an improved solution to reduce the number of *LC* networks, where ZVS/ZCS condition is maintained with two PS networks: $\rm PS_1$ (reused as BPF) shifts $V_{\rm IN}$ a $-\alpha/2$ radians from $I_{\rm IN}$, while $\rm PS_2$ shifts $V_{\rm G}$ a $-\pi$ radians from $V_{\rm IN}$. Based on the $V_{\rm IN}$ expression from Appendix A, the $-\alpha/2$ phase shift (or $\rm Im[\mathit{V}_{IN}]/Re[\mathit{V}_{IN}] = \tan(-\alpha/2)$) in $\rm PS_1$ [see Fig. 3(b)] requires

$$C_{\rm R,3b} = \frac{\pi C_{\rm P}}{\pi\omega^2 C_{\rm P} L_{\rm R} + \sin\alpha - \alpha}. \tag{9}$$

On the other hand, $\rm PS_2$ easily achieves the π phase shift by designing its cutoff frequency higher than the working frequency.

To match the input impedance, we add a matching network MN before $V_{\rm IN}$. Then, it allows an arbitrary $R_{\rm L}$, but the number of *LC* networks is reduced to three.

D. Differential Class-DE Rectifier

$\rm PS_2$ in Fig. 3(b) provides a π phase shift, while a natural and more solid alternative to provide this phase shift is to use a differential topology, as shown in Fig. 3(c). Similar to Fig. 3(b), the PS determines the $\alpha/2$ phase shift between $I_{\rm IN}$ and $V_{\rm IN}$, while the other differential input node $V_{\rm IN}$' defines the π phase shift between $V_{\rm G}$ and $V_{\rm IN}$. In this case, $\rm PS_2$ in Fig. 3(b) for π phase shift is eliminated. Although two BPF (PS) networks are needed, the differential currents flow through these two networks ($I_{\rm IN}$ and $I_{\rm IN}$'), making it possible to design the two inductors with a coupled structure. The solution significantly reduces the cost overhead of the differential topology. The design procedure of the conventional single-ended rectifier (in Section II-B) is still valid, by replacing $R_{\rm L}$ with $R_{\rm L,EFF}$, which equals $V_{\rm OUT}/(I_{\rm OUT}/2) = 2R_{\rm L}$, with half-output current flowing through each branch as follows.

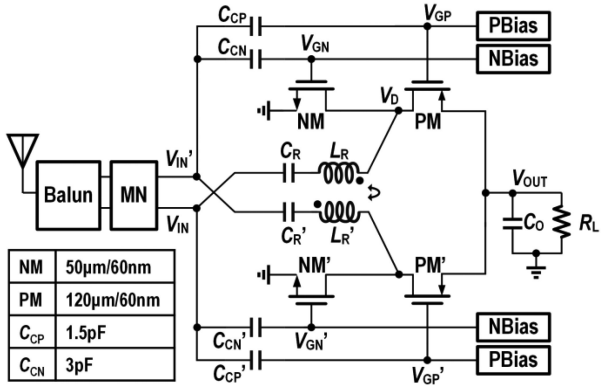


Fig. 6. Schematic of the proposed differential class-DE rectifier.

1) Select the sizes of NM, PM, the value of $L_{\rm R}$, and $R_{\rm L}$ to estimate the parasitic capacitance $C_{\rm P}$ from simulation.
2) Calculate α and $C_{\rm R}$ by (5) and (9).
3) Design the bias circuit to obtain a $V_{\rm GN}$, $V_{\rm GP}$ duty cycle of $(\pi - \alpha)/(2\pi)$.
4) Design the MN.

The advantages of the proposed differential topology are as follows.

1) Reduces the number of *LC* networks to two, comparing to four and three in Fig. 3(a) and (b). The use of coupled inductors increases almost no silicon area overhead.
2) Lowers the power loss. Under the same silicon area, the coupled inductors in a differential topology should route with approximately half-metal width of the single inductor. Hence, each inductor in the differential topology should have about twice serial resistance ($R_{\rm IND}$). Then, the overall power loss in the coupled inductors is about $2 \times (I_{\rm IN}/2)^2 \times (2R_{\rm IND}) = {I_{\rm IN}}^2 \times R_{\rm IND}$, which is comparable to that from the single-ended rectifier. And the loss of $V_{\rm G}$ path phase shifter is eliminated in the differential structure. Hence, the total power loss should be lower than the single-ended design.
3) Reduces the output ripple, which is an inherent benefit of the differential topology.

The disadvantage of the proposed scheme is that the differential input requires a Balun to fulfill the single-differential transformation, as shown in Fig. 3(c). However, a differential fed antenna may incorporate the Balun [7], [30], which is widely used in a high-efficiency rectenna.

III. Implementation

Fig. 6 presents the full schematic of the proposed rectifier, with the NM and PM ac-coupled through $C_{\rm CN}$, $C_{\rm CP}$, and biased with NBias and PBias, respectively. The design parameters of NM, PM, $C_{\rm CN}$, and $C_{\rm CP}$ are also shown in Fig. 6. In this design, $C_{\rm O} = 60$ pF and $R_{\rm L} = 250\,\Omega$ are chosen for the targeted $P_{\rm IN}$ level (-10 to 10 dBm). This section presents the design considerations of $L_{\rm R}$, bias circuit, matching network, and Balun. The circuit is simulated with a TSMC 65-nm GP model, using Cadence.

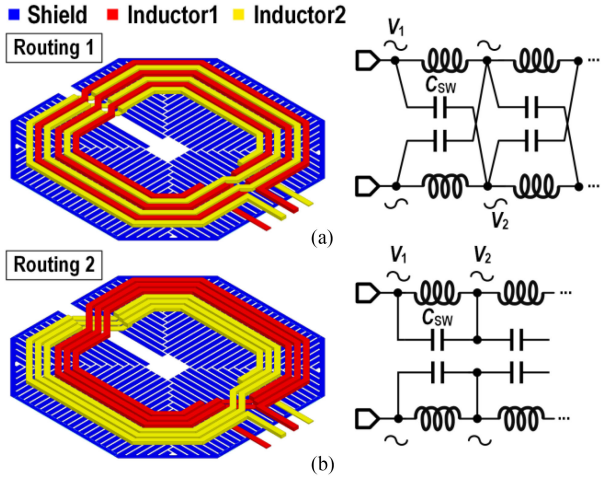


Fig. 7. Two ways of the differential coupled inductors routing, with C_{SW}s distributed between the (a) differential-mode signals and the (b) common-mode signals.

A. Design of the Coupled Inductors

To avoid the substrate loss of the coupled inductors, we used a patterned ground shield. Fig. 7 shows the two possible routings of the coupled inductors. The sidewall capacitance (C_{SW}) distributions, determining the self-resonant frequency (SRF), are different between the two routings.

For Routing-1, as in Fig. 7(a), the two inductors are intertwined, and their C_{SW}s locate between the differential-mode signals. By contrast, the C_{SW}s of Routing-2 [31] are between common-mode signals, as sketched in Fig. 7(b). The Miller effect predicts that the equivalent capacitance to ground at the input node V_1 is $(1 - A)C_{SW}$, where $A = V_2/V_1$, and V_2 is the voltage of the other plate of C_{SW}. We observe that $A \approx -1$ for the differential mode while $A \approx 1$ for the common mode. Therefore, Routing-1 has a larger equivalent input capacitance, degrading the SRF and quality factor Q. A low SRF indicates a weak blocking on high-frequency harmonics, whereas a low Q denotes a large series resistance. Both aspects are detrimental for a good PCE. Consequently, this work chooses Routing-2.

The electronic-magnetic (EM) simulation of L_R and Q from Ansys HFSS verifies the advantages of Routing-2, as plotted in Fig. 8. The two routings have the same dimension. Hence, they achieve a similar L_R at 2.4 GHz. Nevertheless, Routing-2 enjoys a higher Q and SRF as predicted. Concerning the coupled inductors mismatch, the inductance mismatch is small, while the Q mismatch is slightly larger, resulting from one inductor having additional windings with low-layer thin metal.

B. Inductance Selection

The use of 10 nH or larger L_R blocks the I_{IN} harmonics well [5], [8], making the I_{IN} waveform ideally sinusoidal, as shown in Fig. 2. Additionally, a large L_R may beneficially reduce the MOSFET conduction loss [or the root mean square (rms) value of I_{DN}]. However, a large L_R not only consumes a significant silicon area but also induces a higher loss because of the larger series resistance.

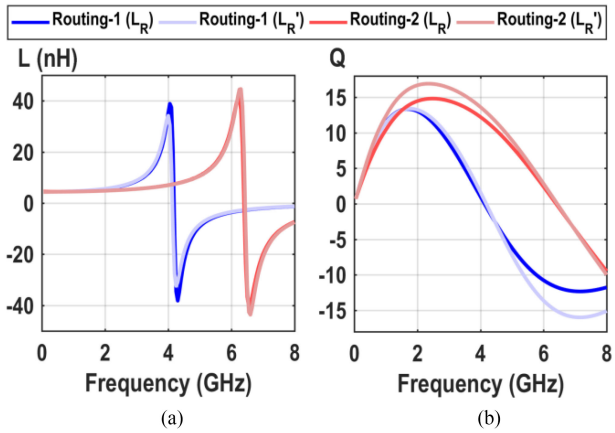


Fig. 8. Comparison on EM simulated L_R and Q, between Routing-1 and -2.

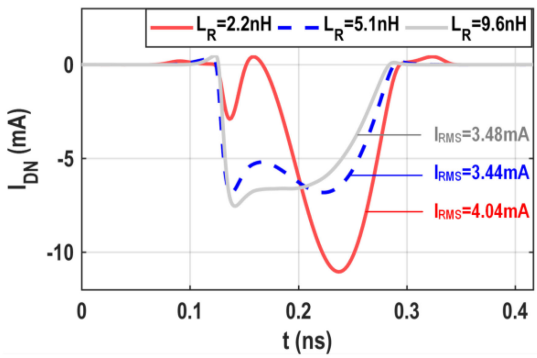


Fig. 9. Simulated I_{DN} waveforms with 2.2, 5.1, and 9.6 nH L_R that are EM simulated.

TABLE I
LOSSES COMPARISON WITH DIFFERENT L_R

L@2.4GHz	MOSFETs	Inductors	Total
2.2 nH	19.9%	3.3%	23.2%
5.1 nH	12.6%	4.6%	17.2%
9.6 nH	12.9%	5.7%	18.6%

Fig. 9 plots the simulated I_{DN} with three EM-modeled L_R (2.2, 5.1, and 9.6 nH). As observed, 2.2 nH L_R results in the highest rms I_{DN}, while that of 5.1 and 9.6 nH L_R are comparable. Table I summarizes the losses of the MOSFETs and coupled inductors, with the three L_R values. As predicted, a medium L_R value is a proper choice, being a tradeoff between the rms value of I_{DN} and inductor series resistance. Hence, in this work, we select $L_R = 5.1$ nH, and then, design C_R to be 1.04 pF.

C. Adaptive Bias Circuits

To achieve ZVS and ZCS, according to Fig. 2, V_{GN} should be a sinusoidal wave

$$V_{GN}(\theta) = V_{DCN} + V_m \cos\left(\theta - \pi - \frac{\alpha}{2}\right) \tag{10}$$

where V_{DCN} is the dc bias of V_{GN} and V_m is the magnitude of the input voltage. To achieve ZVS, as shown in Fig. 2, V_{GN}

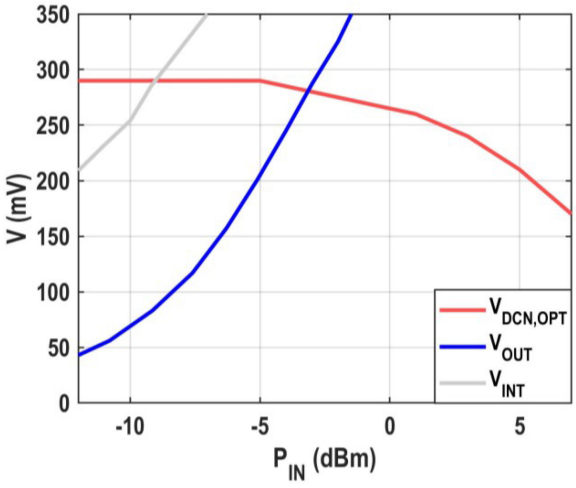


Fig. 10. V_{DCN} of the optimal bias, V_{OUT} and V_{INT}.

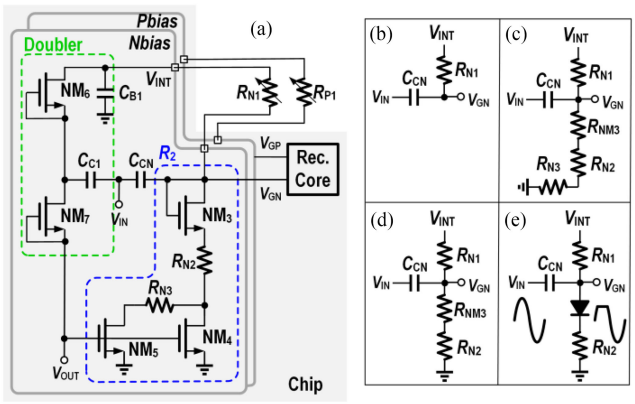


Fig. 11. (a) Overall adaptive bias circuits of NM. Adaptive bias for NMOS at (b) low, (c) medium, (d) high, and (e) very high P_{IN}.

should be equal to V_{THN} at $\theta = \pi/2 + \alpha$, then the optimum V_{DCN} ($V_{\mathrm{DCN,\,OPT}}$) becomes

$$V_{\mathrm{DCN,OPT}} = V_{\mathrm{THN}} - V_{\mathrm{m}} \sin \frac{\alpha}{2} \tag{11}$$

indicating that $V_{\mathrm{DCN,OPT}}$ should adaptively follow the V_{IN} (or P_{IN}) variation. Fig. 10 plots the $V_{\mathrm{DCN,OPT}}$ from circuit-level simulation. By sweeping the PCE versus V_{DCN} under a certain P_{IN}, the V_{DCN} corresponding to the peak PCE is regarded as $V_{\mathrm{DCN,OPT}}$. The simulated $V_{\mathrm{DCN,OPT}}$ does not strictly follow (11), because the MOSFETs in the rectifier do not turn ON/OFF ideally at V_{TH}. The resultant V_{OUT} is also plotted in Fig. 10. The design target of the bias circuits is to generate a V_{DCN} that adaptively emulates $V_{\mathrm{DCN,OPT}}$. Since $V_{\mathrm{DCN,OPT}}$ far exceeds the generated V_{OUT} at a low P_{IN}, it is necessary to boost V_{OUT} to a higher internal voltage V_{INT} to generate V_{DCN}.

The proposed adaptive bias circuits are given in Fig. 11(a), generating V_{DCN} by dividing V_{INT} with a variable resistive divider: $V_{\mathrm{DCN}} = V_{\mathrm{INT}} \times R_{\mathrm{N1}}/(R_{\mathrm{N1}}+R_2)$. V_{INT} is generated by a voltage doubler with NM_6 and NM_7, and filtered by a bypass capacitor C_{B1}. The low threshold devices NM_6 and NM_7 allow a reduced voltage drop. Fig. 10 also shows the simulated V_{INT}.

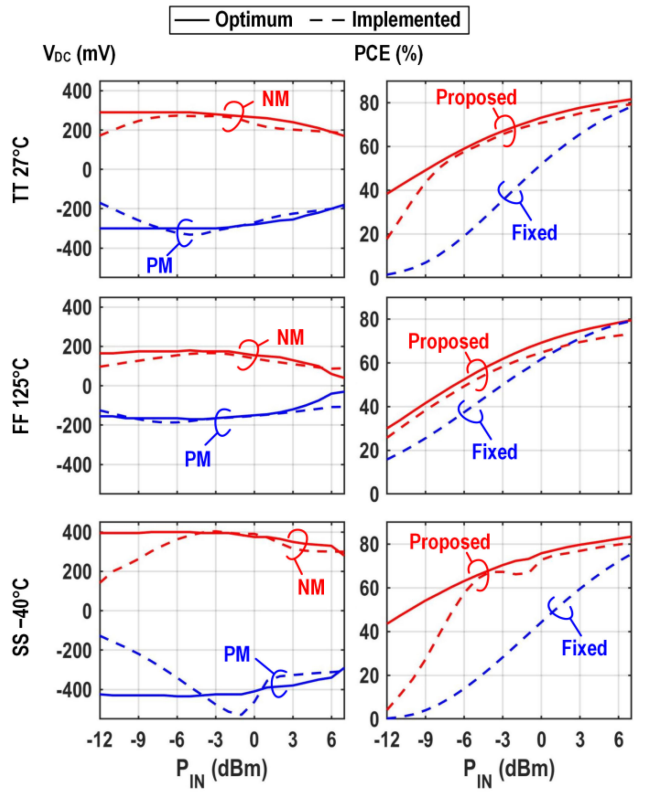


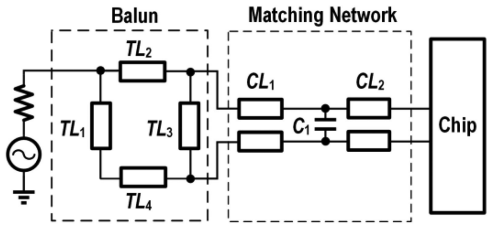
Fig. 12. $V_{\mathrm{DCN}}/V_{\mathrm{DCP}}$ and PCE comparison, between the optimum, proposed bias schemes, and fixed bias scheme with PVT variations.

The variable resistive divider in Fig. 11(a) consists of resistors R_{N1}, R_{N2}, R_{N3} and diode-connected NM_3, whereas NM_4 and NM_5 are the switches controlled by V_{OUT} (as a P_{IN} indicator). The operation of the bias circuits under different P_{IN} is based on the following.

1) Low P_{IN}: V_{OUT} is not sufficiently high to turn ON NM_4 and NM_5, and V_{INT} directly biases V_{GN}, as shown in Fig. 11(b).
2) Medium P_{IN}: V_{OUT} is high enough to turn ON NM_5 with a low threshold voltage, but not for NM_4 with a standard threshold voltage. In this case, from Fig. 11(c), $R_2 = R_{\mathrm{NM3}} + R_{\mathrm{N2}} + R_{\mathrm{N3}}$, where R_{NM3} is the equivalent resistance of the diode-connected NM_3.
3) High P_{IN}: Both NM_4 and NM_5 turn ON, shorting R_{N3}. As illustrated in Fig. 11(d), $R_2 = R_{\mathrm{NM3}} + R_{\mathrm{N2}}$.
4) Very high P_{IN}: The diode-connected NM_3 will clamp the peak voltage of V_{GN}, as depicted in Fig. 11(e), and the equivalent resistance R_{NM3} will decrease, as explained in [23].

A similar bias circuit obtains the PMOS bias voltage V_{DCP}, which is the dc component of the PMOS V_{GS}. An off-chip variable resistor makes R_{N1} (R_{P1}), which can be tuned when V_{DCN} (V_{DCP}) deviates too much from the optimum value.

Fig. 12 compares the simulated $V_{\mathrm{DCN}}/V_{\mathrm{DCP}}$ and PCE with the proposed bias circuits, the optimum biases, and fixed biases ($V_{\mathrm{DCN}} = V_{\mathrm{DCP}} = 0$) under different process, voltage, and temperature (PVT) conditions. We choose R_{N1} (R_{P1}) to obtain



	TL_1/TL_3	TL_2/TL_4	CL_1	CL_2	C_1 (pF)
W (mm)	1	1	1.8	1.8	1.3
L (mm)	37.5	18.7	2	16	
S (mm)	N.A.	N.A.	0.4	0.4	

Fig. 13. Schematic and parameters of the Balun and the matching network.

a maximum PCE at 27 °C and the typical (TT) corner, and maintain the values under different conditions in this simulation. At 27 °C and the TT corner, the proposed scheme extends the dynamic range (defined as $P_{\rm IN}$ range when PCE $>$ 40%) by 7 dB compared with the fixed bias scheme. Moreover, there is only a 3% PCE degradation from the optimum bias when $P_{\rm IN}$ is higher than -8 dBm. The adaptive bias circuits can partially compensate for the PVT variations, since the resistances of the NM_3, NM_4, and NM_5 also change with the PVT variations. Then, $V_{\rm DCN}$ and $V_{\rm DCP}$ should roughly track the optimum biases, as shown in Fig. 12. The worst case occurs at the low $P_{\rm IN}$, -40 °C slow (SS) corner, where the NM's and PM's $V_{\rm TH}$s become higher, whereas the achievable bias voltages generated from the doubler are lower. An automatic bias calibration [26] can further improve the performances with the PVT variation.

D. Matching Network and Balun

The matching of the proposed rectifier to a 100-Ω source impedance requires a matching network. This circuit uses microstrip lines for a low insertion loss. Fig. 13 exhibits the schematic and parameters of the microstrip lines. For the convenience of measurement, we replace the open-circuit lines of the microstrip lines with an external capacitor C_1. Consequently, it is possible to adjust the input impedance with the value of C_1 and the geometry (lengths of the coupled lines CL_1/CL_2). The modeling of the parasitic, bonding wires, etc., in the matching network design follows the procedure proposed in [6]. Meanwhile, a 50–100 Ω Balun is designed with a rat-race coupler.

IV. Effects on $R_{\rm L}$ Variation

Generally, with active control circuits, a perfect ZVS/ZCS can be achieved at a low frequency. Nevertheless, the control becomes difficult for a high-frequency rectifier. As discussed in this section, the variation of $R_{\rm L}$ will degrade the accuracy of ZCS and change the input impedance.

The ZVS/ZCS accuracy under $R_{\rm L}$ variation is reinvestigated here, based on the assumptions made in Section II-A. Without changing the design parameters, NM and PM are turned ON within $[\pi/2 + \alpha_0, 3\pi/2]$ and $[-\pi/2 + \alpha_0, \pi/2]$, where α_0 stands for the implemented phase shift α with specific LC and bias values, under a predefined $R_{\rm L}$. The $R_{\rm L}$ variation from the predefined value introduces a phase shift $\varphi_{\rm RL}$ as $I_{\rm IN} = I_{\rm m}\cos(\theta+\varphi_{\rm RL})$. Then, $I_{\rm IN}$ at $\pi/2$ and $3\pi/2$ are not equal to 0 for $\varphi_{\rm RL} \neq 0$, indicating the violation of ZCS. As derived in Appendix B

$$\varphi_{\rm RL} = \tan^{-1}\left(\frac{\omega C_{\rm P} R_{\rm L}}{\pi \tan\frac{\alpha_0}{2}}\right) - \frac{\alpha_0}{2}. \tag{12}$$

Besides, Appendix B shows that the $V_{\rm D}$ at turn-ON instant ($-\pi/2 + \alpha_0$ and $\pi/2 + \alpha_0$) is

$$\begin{cases} V_{\rm D}\left(-\pi/2 + \alpha_0\right) = V_{\rm OUT} \\ V_{\rm D}\left(\pi/2 + \alpha_0\right) = 0 \end{cases} \tag{13}$$

indicating that the ZVS is maintained under $R_{\rm L}$ variation.

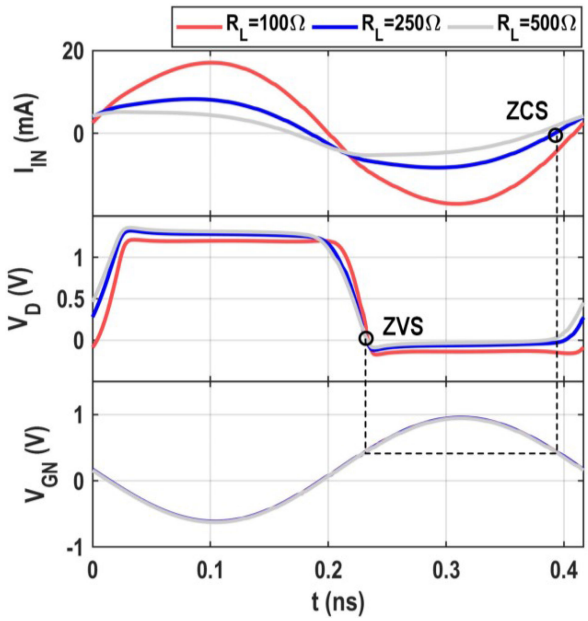


Fig. 14. Simulated $I_{\rm IN}$, $V_{\rm D}$, and $V_{\rm GN}$ versus $R_{\rm L}$. A near ZVS is achieved as predicted, but ZCS condition is violated.

Fig. 14 plots the simulated $I_{\rm IN}$, $V_{\rm D}$, and $V_{\rm GN}$ versus $R_{\rm L}$. As predicted, different values of $R_{\rm L}$ achieve near ZVS, but the ZCS conditions are violated. To regain ZCS for other value of $R_{\rm L}$, α_0 should be redesigned from (5) to make $\varphi_{\rm RL} = 0$.

The input impedance of the rectifier is $Z_{\rm IN} = V_{\rm IN}/I_{\rm IN}$, where the expression of $V_{\rm IN}$ results from (23) and (24) of Appendix B, and $I_{\rm IN} = I_{\rm m}\cos\varphi_{\rm RL} + jI_{\rm m}\sin\varphi_{\rm RL}$. Fig. 15 shows the calculated and simulated $Z_{\rm IN}$ and S_{11} versus $R_{\rm L}$, when the rectifier is purposely designed for 250 Ω $R_{\rm L}$. As observed, $R_{\rm L}$ variations cause an input impedance mismatch, but the reflected power is acceptable (< -10 dB) with $R_{\rm L}$ ranging from 100 to 450 Ω.

V. Measurement Results

Fig. 16 presents the prototype PCB and the photographs of the proposed differential class-DE rectifier chip, fabricated in a 65-nm CMOS process. The chip occupies a core area of 420 × 300 μm^2, excluding pads and ESDs. We implemented both the matching network and Balun on a Rogers RO4003 substrate with a thickness of 0.813 mm.

Fig. 17 shows the measurement setup. A vector network analyzer (Keysight E5071C) measures the S_{11} of the rectifier. For

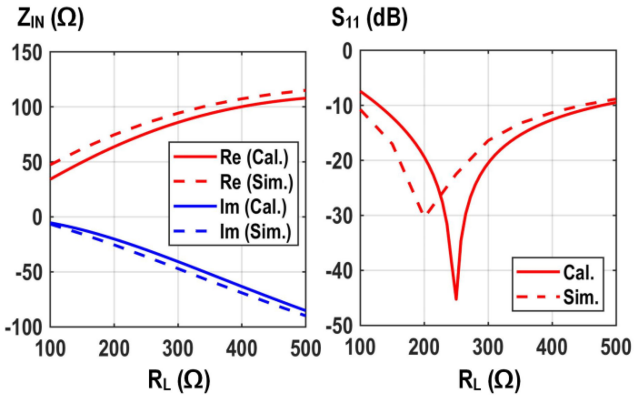


Fig. 15. Calculated and simulated (a) input impedance versus R_L and (b) S_{11} versus R_L, when the rectifier is designed for 250 Ω R_L.

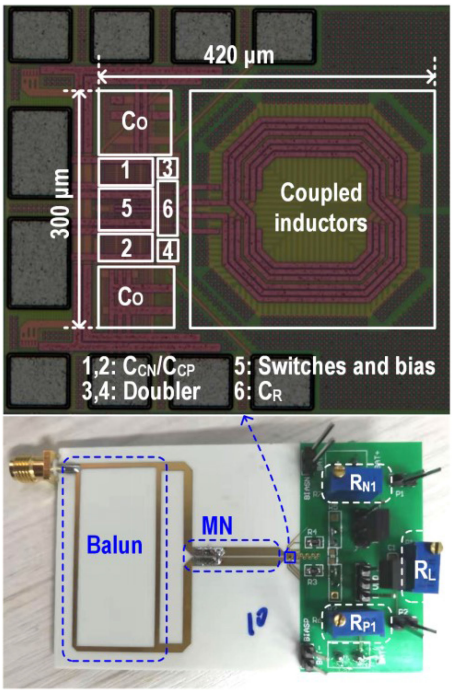


Fig. 16. Photographs of the proposed rectifier chip and the prototype PCB.

the PCE measurement, a signal generator (Keysight N5172B) provides the 2.4-GHz RF input signal, and a multimeter measures the output dc voltage V_{OUT}.

Fig. 18 shows the measured S_{11} versus P_{IN}, under 100, 250, and 500 Ω R_{L}. As observed, a good S_{11} is achieved at a high P_{IN}, but it degrades when P_{IN} becomes low. The reason is that the fully turn-ON assumption in Section II-A no longer stands at a low P_{IN}, and Z_{IN} will deviate from the calculated value.

Figs. 19 and 20 show the measured V_{OUT} and PCE under 100, 250, and 500 Ω R_{L}, where PCE is calculated as

$$\mathrm{PCE} = \frac{V_{\mathrm{OUT}}^2}{R_{\mathrm{L}} P_{\mathrm{IN}}}. \tag{14}$$

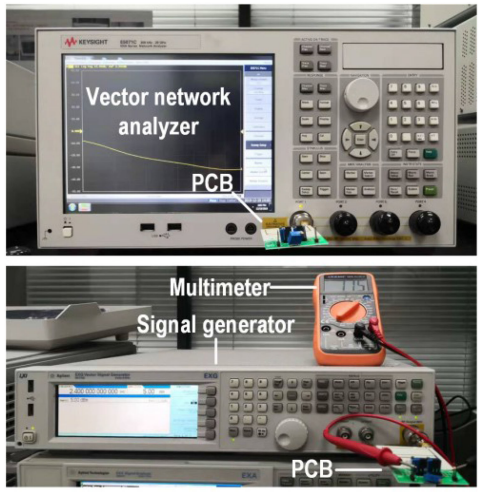


Fig. 17. Photograph of the measurement setup.

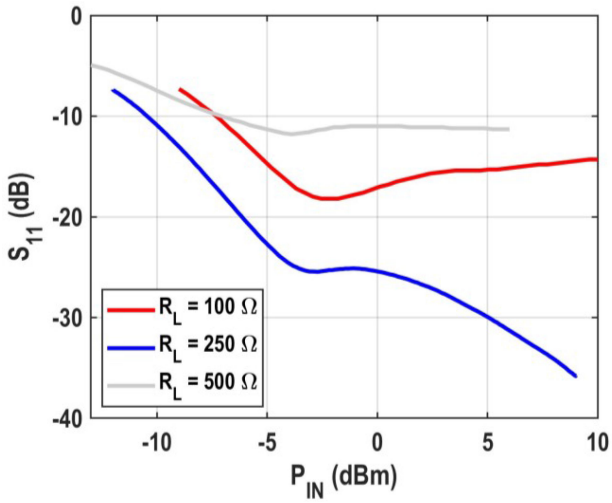


Fig. 18. Measured S_{11} versus P_{IN} with 100, 250, and 500 Ω R_{L}.

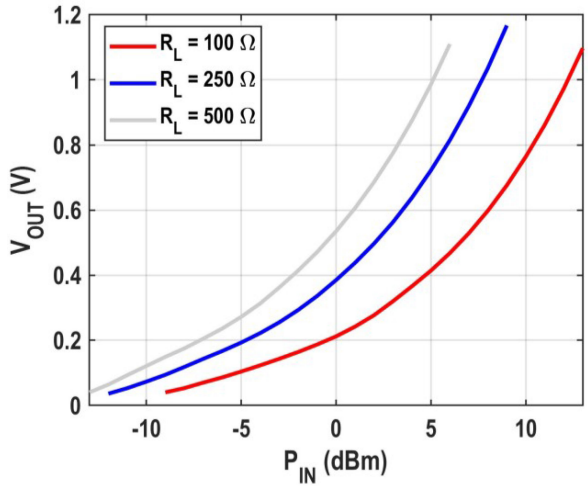


Fig. 19. Measured V_{OUT} versus P_{IN} with 100, 250, and 500 Ω R_{L}.

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE ART WORKS

	This work	[10] 2019	[13] 2017	[23] 2018	[14] 2018	[5] 2016
Technology	65 nm	65 nm	130 nm	180 nm	65 nm	130 nm
Matching Network	Included	Included	Not included	Not included	Not required*	Not required*
Active Area	0.126 mm^2	125 μm^2	0.029 mm^2	8800 μm^2	0.205 mm^2**	0.371 mm^2**
Frequency	2.4 GHz	2.45 GHz	2 GHz	900 MHz	5.8 GHz	2.4 GHz
Load	250 Ω	MPPT Module	2 kΩ	100 kΩ	400 Ω	250 Ω
Topology	Differential class-DE with adaptive gate bias	Cross-coupled	Cross-coupled with substrate bias	Cross-coupled with clamped gate bias	Single-ended class-DE with adaptive gate bias	Single-ended class-E with fixed gate bias
Peak PCE @ P_{IN}	68.5% @ 9 dBm	48.3% @ −3 dBm	73.9% @ 4.34 dBm	66% @ −19 dBm	52% @ 5 dBm	30% @ 12 dBm
Dynamic Range	[−7, 9] dBm	[−7, 0] dBm	[0, 11] dBm	[−24, −13] dBm	[0, 17] dBm	N.A.

*R_L is limited as explained in Section II. **Estimate from the micrograph.

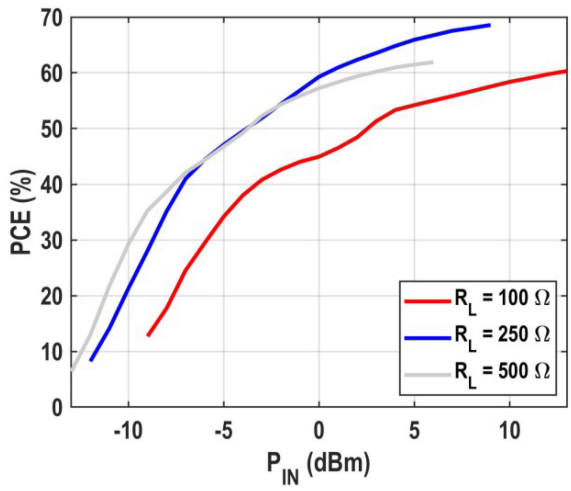


Fig. 20. Measured PCE versus $P_{\rm IN}$ with 100, 250, and 500 Ω $R_{\rm L}$.

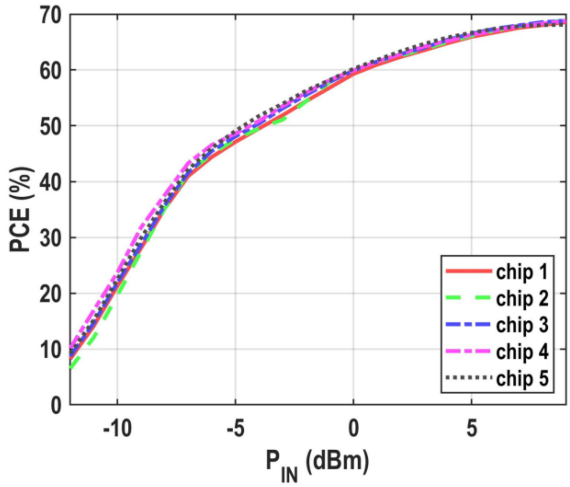


Fig. 21. Measured PCE versus $P_{\rm IN}$ with five chips, with the same $R_{\rm N1}$, and $R_{\rm P1}$ values under $R_{\rm L} = 250\ \Omega$.

The measured value of $V_{\rm OUT}$ is from 50 mV. It could be the minimum start-up voltage for the loading circuits, e.g., the cascaded dc–dc converter [32]–[34]. Under $R_{\rm L} = 250\ \Omega$, a 1.17-V $V_{\rm OUT}$ and 68.5% peak PCE are achieved at 9 dBm $P_{\rm IN}$. A protection circuit can be added in a future design to extend $P_{\rm IN}$ to a higher level. Thanks to the adaptive bias scheme, the dynamic range is from −7 to 9 dBm. With an $R_{\rm L}$ of 100 and 500 Ω, the peak PCE is 60.3% and 61.9%, respectively, comparable to the targeted $R_{\rm L}$.

Fig. 21 shows the measured PCE versus $P_{\rm IN}$ with five different chips, indicating good consistency. They use $R_{\rm L} = 250\ \Omega$ and the same off-chip bias resistors.

Table II compares the proposed differential class-DE rectifier with both the previous CC and class-E/DE rectifiers. When compared with the class-E/DE rectifiers with a similar or larger $R_{\rm L}$ [5], [14], the proposed design consumes a smaller silicon area due to the implementation of the coupled inductors and the reduced *LC* networks. Meanwhile, this work achieves a better peak PCE since the reduced *LC* networks will further enhance the PCE.

In general, the class-DE rectifiers occupy a larger silicon area than the CC ones, but trade with a smaller reverse leakage current, and thus, higher efficiency. As in Table II, the peak PCE of this article is higher than the CC rectifier with matching network [10], and comparable to those CC rectifiers without considering the loss from the matching network [13], [23]. With the adaptive bias scheme, the proposed rectifier can achieve near ZVS and ZCS, and maintain a reasonably good PCE within a wide $P_{\rm IN}$ range, better than previous works [10], [13], [23]. Future work may focus on reducing the cost overhead by codesigning the phase shifter and matching network and the automatic bias tuning.

VI. CONCLUSION

This article investigated a differential class-DE rectifier. Compared with the CC rectifier, the class-DE rectifier trades the silicon area with PCE. To minimize the design complexity and cost overhead, we proposed a differential topology with coupled inductors, reducing the number of *LC* networks. After that, we investigated the design considerations of the coupled inductors and the inductance selection. Moreover, we proposed the adaptive gate bias circuit to fulfill the near ZVS and ZCS requirements and extend the dynamic range. Then, we discussed the imperfection caused by the load variation, which degrades

the accuracy of ZCS and changes the input impedance. The measured peak PCE of the prototype rectifier is 68.5%, and the PCE is higher than 40% over 16 dB input power range.

APPENDIX A

This appendix derives the design parameters to meet the impedance matching requirement of the single-ended class-DE rectifier in Fig. 3(a)

$V_{\rm IN}$ can be written as

$$V_{\rm IN} = I_{\rm IN}\left(j\omega L_{\rm R} + \frac{1}{j\omega C_{\rm R}}\right) + V_{\rm D,1} \tag{15}$$

where $V_{\rm D,1}$ is the fundamental component of $V_{\rm D}$, with high-order harmonics filtered out by BPF. $V_{\rm D,1}$ derives from the Fourier series of the time-domain waveforms of $V_{\rm D}(\theta)$ combining (1), (3), (6), and (7)

$$\begin{aligned} V_{\rm D,1} &= \frac{1}{\pi}\left(\int_{-\pi/2}^{3\pi/2} V_{\rm D}(\theta)\cos\theta d\theta - j\int_{-\pi/2}^{3\pi/2} V_{\rm D}(\theta)\sin\theta d\theta\right) \\ &= \frac{I_{\rm m}}{\pi\omega C_{\rm P}}\left[\sin^2\alpha + j(\sin\alpha\cos\alpha - \alpha)\right]. \end{aligned} \tag{16}$$

Combining (15) and (16), $V_{\rm IN}$ is rewritten as

$$V_{\rm IN} = I_{\rm m}\left[\frac{\sin^2\alpha}{\pi\omega C_{\rm P}} + j\left(\omega L_{\rm R} - \frac{1}{\omega C_{\rm R}} + \frac{\sin\alpha\cos\alpha - \alpha}{\pi\omega C_{\rm P}}\right)\right]. \tag{17}$$

To achieve impedance matching, the imaginary part of (17) should be nullified by designing $C_{\rm R}$ in Fig. 3(a) to be

$$C_{\rm R,3a} = \frac{\pi C_{\rm P}}{\pi\omega^2 C_{\rm P} L_{\rm R} + \sin\alpha\cos\alpha - \alpha}. \tag{18}$$

The real part of (17) should meet $\sin^2\alpha/(\pi\omega C_{\rm P}) = R_{\rm S}$. Then, α becomes

$$\alpha = \cos^{-1}\sqrt{1 - \pi\omega C_{\rm P} R_{\rm S}} \tag{19}$$

which defines α from the perspective of impedance matching, and (5) from the perspective of ZVS/ZCS. Consequently, to meet (5) and (19) simultaneously, the value of $R_{\rm L}$ should be (8).

APPENDIX B

This appendix derives the waveforms of the class-DE rectifier considering the variation of $R_{\rm L}$. By keeping $V_{\rm IN}$ unchanged and assuming that the input current becomes $I_{\rm IN} = I_{\rm m}\cos(\theta+\varphi_{\rm RL})$, the previously derived (1), (4), and (6) should change to (20)–(22) as follows:

$$\begin{aligned} V_{\rm D}(\theta) &= \frac{1}{\omega C_{\rm P}}\int_{-\frac{\pi}{2}}^{\theta} I_{\rm IN}(\theta)\, d\theta \\ &= \frac{I_{\rm m}}{\omega C_{\rm P}}\left[\sin(\theta+\varphi_{\rm RL}) + \cos\varphi_{\rm RL}\right] \end{aligned} \tag{20}$$

$$I_{\rm OUT} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{3\pi}{2}} I_{\rm IN}(\theta)\, d\theta = \frac{I_{\rm m}}{2\pi}\left[\cos\varphi_{\rm RL} + \cos(\alpha_0 + \varphi_{\rm RL})\right] \tag{21}$$

$$\begin{aligned} V_{\rm D}(\theta) &= V_{\rm OUT} + \frac{1}{\omega C_{\rm P}}\int_{\frac{\pi}{2}}^{\theta} I_{\rm IN}(\theta)\, d\theta \\ &= V_{\rm OUT} + \frac{I_{\rm m}}{\omega C_{\rm P}}\left[\sin(\theta+\varphi_{\rm RL}) - \cos\varphi_{\rm RL}\right]. \end{aligned} \tag{22}$$

$$\begin{aligned} \mathrm{Re}\left[V_{\rm IN}\right] &= \frac{I_{\rm m}R_{\rm L}}{\pi^2}\left[\cos\varphi_{\rm RL} + \cos(\alpha_0+\varphi_{\rm RL})\right]\cos\alpha_0 \\ &\quad + \frac{I_{\rm m}}{\pi\omega C_{\rm P}}\left[\frac{1}{2}\cos(2\alpha_0+\varphi_{\rm RL}) - 2\cos\alpha_0\cos\varphi_{\rm RL}\right. \\ &\quad \left. + \frac{3}{2}\cos\varphi_{\rm RL} + \sin\alpha_0\sin\varphi_{\rm RL}\right] \end{aligned} \tag{23}$$

$$\begin{aligned} \mathrm{Im}\left[V_{\rm IN}\right] &= -\frac{I_{\rm m}R_{\rm L}}{\pi^2}\left[\cos\varphi_{\rm RL} + \cos(\alpha_0+\varphi_{\rm RL})\right]\sin\alpha_0 \\ &\quad - \frac{I_{\rm m}}{\pi\omega C_{\rm P}}\left[\frac{1}{2}\sin(2\alpha_0+\varphi_{\rm RL}) - \cos\varphi_{\rm RL}\sin\alpha_0 - \frac{1}{2}\sin\varphi_{\rm RL}\right] \end{aligned} \tag{24}$$

The real part and imaginary part of $V_{\rm IN}$ can be written as in (23) and (24) from (15) and (16). Substituting (23) and (24) into $\mathrm{Im}[V_{\rm IN}]/\mathrm{Re}[V_{\rm IN}] = \tan(-\alpha_0/2)$, $\varphi_{\rm RL}$ is written as (12).

By (12), (21), and $R_{\rm L} = V_{\rm OUT}/I_{\rm OUT}$, the relationship between $I_{\rm m}$ and $V_{\rm OUT}$ can be written as

$$I_{\rm m} = \frac{\omega C_{\rm P} V_{\rm OUT}}{\cos\varphi_{\rm RL} - \cos(\alpha_0 + \varphi_{\rm RL})}. \tag{25}$$

By substituting (25) into (20) and (22), $V_{\rm D}$ at turn-ON instant ($-\pi/2 + \alpha_0$ and $\pi/2 + \alpha_0$) is written as (13), indicating that ZVS is maintained.

ACKNOWLEDGMENT

The authors would like to thank Prof. H. Jia for his suggestions on the coupled inductors design.

REFERENCES

[1] H. J. Visser and R. J. M. Vullers, "RF energy harvesting and transport for wireless sensor network applications: Principles and requirements," in *Proc. IEEE*, vol. 101, no. 6, pp. 1410–1423, Jun. 2013.

[2] M. Huang *et al.*, "Single- and dual-band RF rectifiers with extended input power range using automatic impedance transforming," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 5, pp. 1974–1984, May 2019.

[3] S. Fan *et al.*, "A 2.45-GHz rectifier-booster regulator with impedance matching converters for wireless energy harvesting," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3833–3843, Sep. 2019.

[4] Z. Zeng, X. Li, A. Bermak, C. Tsui, and W. Ki, "A WLAN 2.4-GHz RF energy harvesting system with reconfigurable rectifier for wireless sensor network," in *Proc. IEEE Int. Symp. Circuits Syst.*, Montreal, QC, Canada, May 2016, pp. 2362–2365.

[5] S. Dehghani and T. Johnson, "A 2.4-GHz CMOS Class-E synchronous rectifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 5, pp. 1655–1666, May 2016.

[6] X. Li, Y. Lu, M. Huang, and R. P. Martins, "A 2.4-GHz mid-field CMOS wireless power receiver achieving 46% maximum PCE and 163-mW output power," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 67, no. 2, pp. 360–364, Feb. 2020.

[7] J. Kang, P. Chiang, and A. Natarajan, "Bootstrapped rectifier–antenna co-integration for increased sensitivity in wirelessly-powered sensors," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 5031–5041, Nov. 2018.

[8] S. Dehghani and T. Johnson, "2.4 GHz CMOS class D synchronous rectifier," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Phoenix, AZ, USA, May 2015, pp. 1–3.

[9] K. R. Sadagopan, J. Kang, Y. Ramadass, and A. Natarajan, "A cm-scale 2.4-GHz wireless energy harvester with nanowatt boost converter and antenna-rectifier resonance for WiFi powering of sensor nodes," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3396–3406, Dec. 2018.
[10] P. Xu, D. Flandre, and D. Bol, "Analysis, modeling, and design of a 2.45-GHz RF energy harvester for SWIPT IoT smart sensors," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2717–2729, Oct. 2019.
[11] K. Lei, P. Mak, M. Law, and R. P. Martins, "A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-μW steady-state power," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2624–2635, Sep. 2018.
[12] S. Movassaghi, M. Abolhasan, J. Lipman, D. Smith, and A. Jamalipour, "Wireless body area networks: A survey," *IEEE Commun. Surv. Tut.*, vol. 16, no. 3, pp. 1658–1686, Jul.–Sep. 2014.
[13] A. K. Moghaddam *et al.*, "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy harvesting systems," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 64, no. 4, pp. 992–1002, Apr. 2017.
[14] S. Dehghani, S. Mirabbasi, and T. Johnson, "A 5.8-GHz bidirectional and reconfigurable RF energy harvesting circuit with rectifier and oscillator modes," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 66–69, Mar. 2018.
[15] *Powercast. P2110B. 915 MHz RF Powerharvester Receiver*. Accessed: Jul. 2020. [Online]. Available: https://www.powercastco.com/documentation/p2110b-module-datasheet/
[16] V. Marian, B. Allard, C. Vollaire, and J. Verdier, "Strategy for microwave energy harvesting from ambient field or a feeding source," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4481–4491, Nov. 2012.
[17] Q. Lin and X. Zhang, "Differential rectifier using resistance compression network for improving efficiency over extended input power range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 9, pp. 2943–2954, Sep. 2016.
[18] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.
[19] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011.
[20] H. Nakamoto *et al.*, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101–110, Jan. 2007.
[21] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, May 2008.
[22] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.
[23] A. S. Almansouri, M. H. Ouda, and K. N. Salama, "A CMOS RF-to-DC power converter with 86% efficiency and -19.2-dBm sensitivity," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 5, pp. 2409–2415, May 2018.
[24] W. W. Y. Lau, H. W. Ho, and L. Siek, "Deep neural network (DNN) optimized design of 2.45 GHz CMOS rectifier with 73.6% peak efficiency for RF energy harvesting," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 67, no. 12, pp. 4322–4333, Dec. 2020.
[25] M. H. Ouda, W. Khalil, and K. N. Salama, "Self-biased differential rectifier with enhanced dynamic range for wireless powering," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 64, no. 5, pp. 515–519, May 2017.
[26] X. Li, F. Mao, Y. Lu, and R. P. Martins, "A VHF wide-input range CMOS passive rectifier with active bias tuning," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2629–2638, Oct. 2020.
[27] F. You, S. Dong, Y. Wang, X. Yu, and C. Li, "Design method of self-driving RF-DC rectifier based on waveform-guided solutions to passive matching network," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6498–6509, Jul. 2019.
[28] S. Abbasian and T. Johnson, "Power-efficiency characteristics of Class-F and inverse Class-F synchronous rectifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4740–4751, Dec. 2016.
[29] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Iked, "Class DE high-efficiency tuned power amplifier," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 43, no. 1, pp. 51–60, Jan. 1996.
[30] Y. Ushijima, T. Sakamoto, E. Nishiyama, M. Aikawa, and I. Toyoda, "5.8-GHz integrated differential rectenna unit using both-sided MIC technology with design flexibility," *IEEE Trans. Antennas Propag.*, vol. 61, no. 6, pp. 3357–3360, Jun. 2013.
[31] P. Findley, G. A. Rezvani, and J. Tao, "Novel differential inductor design for high self-resonance frequency," in *Proc. IEDM Tech. Dig. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, 2004, pp. 467–470.
[32] J. Im, S. Wang, S. Ryu, and G. Cho, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3055–3067, Dec. 2012.
[33] B. Lim, J. Seo, and S. Lee, "A Colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3293–3302, Nov. 2018.
[34] Y. Teh and P. K. T. Mok, "Design of transformer-based boost converter for high internal resistance energy harvesting sources with 21 mV self-startup voltage and 74% power efficiency," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2694–2704, Nov. 2014.

Tingxu Hu received the B.E. degree from the South China University of Technology, Guangzhou, China, in 2019. He is currently working toward the Ph.D. degree with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China.

His research interests include RF energy harvesting and power management.

Mo Huang (Senior Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in microelectronics and solid-state electronics from Sun Yat-sen University, Guangzhou, China, in 2005, 2008, and 2014, respectively.

From 2008 to 2014, he was an IC Design Engineer and a Project Manager with Rising Microelectronic Ltd., Guangzhou, China. From 2015 to 2016, he was a Postdoctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, where he is currently an Assistant Professor with the Institute of Microelectronics. From 2017 to 2019, he was with the School of Electronic and Information Engineering, South China University of Technology (SCUT), Guangzhou, China, as an Associate Professor. His current research interests include analog and mixed-signal IC designs, power management IC design, and wireless power transfer.

Dr. Huang was a technical program committee member of many conferences and a reviewer for many journals. He was a recipient of the IEEE ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper.

Yan Lu (Senior Member, IEEE) received the B.Eng. and M.Sc. degrees from the South China University of Technology, Guangzhou, China, in 2006 and 2009, respectively, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2013.

In 2014, he joined the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, where he is currently an Associate Professor. He has authored or coauthored more than 80 peer-reviewed technical articles and one book entitled *CMOS Integrated Circuit Design for Wireless Power Transfer* (Springer), and edited one book entitled *Selected Topics in Power, RF, and Mixed-Signal ICs* (River Publishers). His research interests include wireless power transfer circuits and systems, highly integrated power management solutions, and low-power analog circuits.

Dr. Lu is a TPC Member for the International Solid-State Circuits Conference (ISSCC) and Custom Integrated Circuits Conference (CICC). He was a recipient/co-recipient of the 2018 Macao Science and Technology Award (Second Prize, with the First Prize Vacancy), the IEEE Solid-State Circuits Society Predoctoral Achievement Award for the period of 2013–2014, the IEEE CAS Society Outstanding Young Author Award in 2017, and the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper. He was a Guest Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS in 2019 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 2018 to 2019.

Xiu Yin Zhang (Senior Member, IEEE) received the B.S. degree in communication engineering from the Chongqing University of Posts and Telecommunications, Chongqing, China, in 2001, the M.S. degree in electronic engineering from the South China University of Technology, Guangzhou, China, in 2006, and the Ph.D. degree in electronic engineering from the City University of Hong Kong, Kowloon, Hong Kong, China, in 2009.

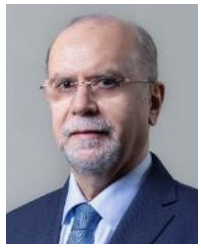
From 2001 to 2003, he was with ZTE Corporation, Shenzhen, China. He was a Research Assistant from July 2006 to June 2007 and a Research Fellow from September 2009 to February 2010 with the City University of Hong Kong. He is currently a Full Professor and Vice Dean with the School of Electronic and Information Engineering, South China University of Technology. He is also the Vice Director of the Guangdong Key Laboratory of Millimeter-Wave and Terahertz and the Vice Director of the Engineering Research Center for Short-Distance Wireless Communications and Network, Ministry of Education. He has authored or coauthored more than 150 internationally referred journal papers (including more than 90 IEEE Transactions) and 80 conference papers. His research interests include antennas and arrays, MMIC, RF components and subsystems, and wireless sensing and communications.

Dr. Zhang is a fellow of the Institution of Engineering and Technology. He has served as general chair/technical program committee (TPC) chair/member and session organizer/chair for a number of conferences. He was a recipient of the National Science Foundation for Distinguished Young Scholars of China, the Leading Talent of Technological Innovation of Ten-Thousand Talents program, the Young Scholar of the Changjiang Scholars Program of the Chinese Ministry of Education, the First Prize of 2015 Guangdong Provincial Natural Science Award, and the First Prize of 2020 Guangdong Provincial Technological Invention Award. He was the supervisor of several conference best paper award winners. He is an Associate Editor for the *IEEE Antennas and Wireless Propagation Letters*, *IEEE Antennas and Propagation Magazine*, IEEE OPEN JOURNAL OF ANTENNAS AND PROPAGATION, and IEEE ACCESS.

Franco Maloberti (Life Fellow, IEEE) received the Laurea degree in physics *(summa cum laude)* from the University of Parma, Parma, Italy, and the Honoris Causa degree in electronics from the Inaoe, Puebla, Mexico, in 1996.

He was a Visiting Professor with ETH-PEL, Zurich, Switzerland, and with EPFL-LEG, Lausanne, Switzerland. He was the TI/J.Kilby Analog Engineering Chair Professor with the Texas A&M University, College Station, TX, USA, and the Distinguished Microelectronic Chair Professor with the University of Texas at Dallas, Dallas, TX, USA. He is an Emeritus Professor with the University of Pavia, Pavia, Italy. He is Honorary Professor, University of Macau, Macau, China. He has authored or coauthored more than 600 published papers, ten books, and holds 39 patents. His professional expertise is in the design, analysis, and characterization of integrated circuits and analogue digital applications, mainly in the areas of switched capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analogue and mixed A-D design.

Prof. Maloberti is the Chairman of the Academic Committee of the AMSV State Key Lab., Macau, China, and the Director-Elect Division I IEEE. He was the Past President of the IEEE CAS Society (2017–2018) and President (2015–2016), VP Region 8 of IEEE CAS (1995–1997), President of the IEEE Sensor Council (2002–2003), IEEE CAS BoG Member (2003–2005), and VP Publications IEEE CAS (2007–2008). He was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II. He was DL IEEE SSC Society (2009–2010) and DL IEEE CAS Society (2006–2007 and 2012–2013). He was the recipient of the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, the IEEE Millenium Meda, the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award, the IEEJ Workshop 2007 and 2010 Best Paper Award, and the IEEE CAS Society 2013 Mac Van Valkenburg Award.



Rui P. Martins (Fellow, IEEE) born on April 30, 1957. He received the B.Eng., M.Eng., and Ph.D. degrees, as well as the Habilitation degree for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering (DECE), Instituto Suerior Técnico (IST), University of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since October 1980, he has been with the DECE/IST, University of Lisbon. Since October 1992, he has been on leave from the University of Lisbon and with the DECE, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair Professor since August 2013. In FST, he was the Dean (1994–1997), and has been UM's Vice-Rector since September 1997, Vice-Rector (Research) from September 2008 to August 2018, and Vice-Rector (Global Affairs) from September 2018 to August 2023. Within the scope of his teaching and research activities he has taught 21 bachelor's and master's courses and, in UM, has supervised (or cosupervised) 47 theses, Ph.D. (26) and master's (21). He has authored or coauthored seven books and 12 book chapters, 36 patents—USA (32), Taiwan (3), and China (1), 567 papers, in scientific journals (220), and in conference proceedings (347), as well as 66 other academic works, in a total of 688 publications. In 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory at UM, elevated in January 2011 to State Key Laboratory (SKLAB) of China (the first in engineering in Macao), being its Founding Director. From January 2009 to March 2019, he was the Founding Chair of UMTEC (UM company), supporting the incubation and creation in 2018 of *Digifluidic,* the first UM spin-off. He was also a Co-Founder of Chipidea Microelectronics (Macao) (now Synopsys-Macao) in 2001–2002.

Prof. Martins was a Founding Chair of the IEEE Macau Section (2003–2005) and IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) (2005–2008) [2009 World Chapter of the Year of IEEE CAS Society (CASS)], General Chair IEEE Asia-Pacific Conference on CAS – *APCCAS'2008*, Vice-President (VP) Region 10 (Asia, Australia, and Pacific) (2009–2011), and VP-World Regional Activities and Membership of IEEE CASS (2012–2013). He was an Associate Editor for the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS (2010–2013) and nominated *Best Associate Editor* (2012–2013). He was also member of the IEEE CASS Fellow Evaluation Committee (2013, 2014, 2018—Chair, 2019 and 2021—Vice-Chair), IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) (2014), IEEE CASS Nominations Committee (2016–2017), the General Chair of ACM/IEEE Asia South Pacific Design Automation Conference – *ASP-DAC'2016*, the General Chair of the IEEE Asian Solid-State Circuits Conference – *ASSCC 2019*, and the Vice-President (2005–2014) and President (2014–2017) of the Association of Portuguese Speaking Universities (AULP). He was the recipient of the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016, two Macao Government decorations—the Medal of Professional Merit (Portuguese-1999) and the Honorary Title of Value (Chinese-2001). In July 2010, he was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences.