Reduction of MMC Capacitances Through Parallelization of Symmetrical Half-Bridge Submodules

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***Abstract*—Modular multilevel converters (MMCs) enjoy the benefits of modularity and scalability. In particular, MMCs with symmetrical half-bridge submodules enable bipolar operation yet with a simple structure and low conduction losses. However, bulky dc capacitors in MMC submodules act as one major obstacle that retards the further improvement of system size, weight, and cost performance. Additionally, tight regulation and balance of dc capacitor voltages necessitate expensive voltage sensors paired with dedicated voltage controllers. This article proposes an effective hardware-based strategy that achieves MMC capacitance reduction through parallelization of symmetrical half-bridge submodules. On top of capacitance saving, the proposed strategy balances capacitor voltages in a sensorless fashion, which translates into the removal of voltage sensors and great simplification of control efforts. In addition, the proposed strategy allows fault-tolerant operation of MMCs. Finally, simulation and experimental results validate the effectiveness of the proposed strategy in capacitance reduction and capacitor voltage balancing of MMCs as static compensators.**

***Index Terms*—Capacitance saving, fault operation, modular multilevel converter (MMC), static compensator (STATCOM), submodule parallelization, voltage balance.**

I. Introduction

MULTILEVEL converters find widespread applications in high-voltage dc/ac transmissions [1], medium-voltage motor drive [2], renewable generation [3], grid-scale energy storage systems [4], power quality enhancement equipment [5], medical applications [6], and electric vehicles [7]. As compared to two-level counterparts, multilevel converters benefit from the use of low-voltage semiconductors for high-voltage treatments, high power quality, small passive filters, low electromagnetic interference noise, and high redundancy. Among multilevel converters, cascaded-bridge, diode-clamped, and flying capacitor converters are proven options [8]–[10]. In particular, cascaded-bridge converters stand out among the three mostly because of their simplicity (i.e., without additional diodes or balancing capacitors), modularity, and scalability [2]. One can readily derive modular multilevel converters (MMCs) when replacing the active switches of standard two-level converters by cascaded-bridge converters [11]. As such, MMCs inherit all the advantages from cascaded-bridge converters. The past decade witnessed a huge progress in the commercialization and development of MMCs [12].

Despite indisputable advantages, MMCs are criticized for their complexity in terms of both circuit hardware and control software due to the large quantities of active switches and passive components involved. Since MMCs, particularly in high-voltage applications, consist of numerous submodules, the simplification of submodules or proper use of redundancy will greatly reduce system complexity and failure rate [13], [44]. Fig. 1(a) shows the schematics of two commonly used MMC submodules—H-bridge and asymmetrical half-bridge submodules. In comparison, asymmetrical half-bridge submodules outweigh H-bridge submodules in terms of simplicity, which further translates into lower cost and conduction losses as well as smaller system size and weight, whereas the opposite is true in respect of module functionality. Specifically, H-bridge submodules allow bipolar outputs, while asymmetrical half-bridge submodules can only output either a positive or zero voltage,

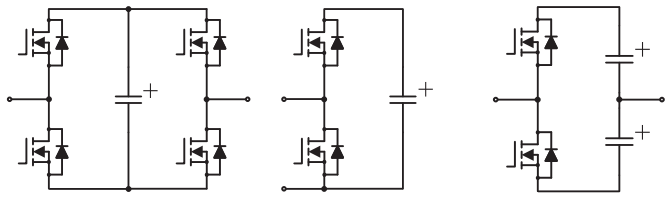

Fig. 1. Schematic diagrams of MMC submodules. (a) H-bridge and asymmetrical half-bridge. (b) Symmetrical half-bridge.

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thereby excluded from certain applications, such as cascaded-bridge converters and four-quadrant MMCs [14]. Other emerging submodules, such as multilevel submodules (exemplified by flying capacitor and neutral-point-clamped submodules [13]), clamp-double [15], double-zero [12], mixed half-bridge and H-bridge [13], and double H-bridge submodules [16], improve system performances in several aspects, e.g., voltage levels, short-circuit protection, and parallel connectivity. However, they suffer from increased complexity.

As a promising alternative, the symmetrical half-bridge submodule depicted in Fig. 1(b) possesses the merits of both simplicity and bipolar outputs [17]. With the upper switch ON and lower switch OFF, the symmetrical half-bridge submodule yields a positive upper capacitor voltage. Alternatively, a negative voltage contributed by the lower capacitor will be expected. Similar to asymmetrical half-bridge submodules, each symmetrical half-bridge submodule uses only one switch at a time to conduct load/grid currents, thus reducing conduction losses compared to H-bridge submodules, as detailed in [17]. Symmetrical half-bridge modules themselves as converters are used in active rectifiers [18], active power filters [19], power decoupling circuits [20], unified power quality conditioners [21], and linear compressors [22]. By series connection, symmetrical half-bridge submodules can form cascaded-bridge converters or MMCs.

As for MMCs with symmetrical half-bridge submodules, also applicable to other MMCs, module capacitors are bulky and expensive components that play a dominant role on system size, weight, and cost. In this sense, there is a strong motivation for MMC capacitance reduction. From the implementation point of view, capacitance reduction can be achieved through either software- or hardware-based strategies.

As a software-based example, modulation signals are intentionally distorted with calculated harmonics to reduce capacitor voltage ripples, thereby saving capacitances of H-bridge submodules [23]. However, complicated calculation inevitably increases computation efforts, and its effectiveness depends greatly on system operating conditions and accuracy of sensors and sampling circuits. Additionally, MMCs with symmetrical half-bridge submodules suffer from another problem—the imbalance of upper and lower capacitor voltages [17]. This problem occurs in the case of capacitance mismatches, voltage sensor offsets, and/or improper modulation [21]. As a result, the imbalance problem further challenges those software-based capacitance reduction approaches. Another problem related to MMCs with symmetrical half-bridge submodules is that submodules cannot be bypassed under fault conditions.

As hardware-based solutions, additional buffer circuits are proven to be effective in submodule capacitance reduction [24]−[32]. For selection of energy buffers, typical options are the inductor with one-pair of switches [24], [25], the conventional buck converter [26], [27], the buck converter formed by split dc submodule capacitors [28], [29], and the inverter acting as a dynamic voltage restorer [30], [31]. In combination with additional hardware, dedicated controllers further complicate the operation of submodules and MMCs with buffer circuits [32]. In addition, isolated transformers, together with rectifiers, enable the removal of submodule voltage regulators and capacitance reduction [33]. However, isolated transformers are often bulky and expensive with complicated structures.

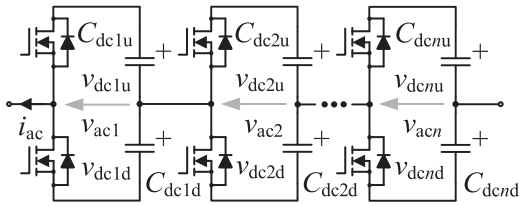

Fig. 2. Schematic of MMC arms with symmetrical half-bridge submodules.

This article proposes a novel hardware-based strategy that achieves significant MMC capacitance saving through parallelization of symmetrical half-bridge submodules. In parallel to capacitance reduction, the proposed strategy balances dc voltages among upper and lower capacitors as well as individual submodules with only one voltage controller and the associated voltage sensors. Moreover, the proposed strategy allows fault-tolerant operation of MMCs via bypassing submodules. The rest of this article is organized as follows. Section II presents the fundamental operating principles of MMCs with symmetrical half-bridge submodules. On top of that, we introduce the control architecture in static compensator (STATCOM) applications. Section III begins with the introduction of the proposed strategy through submodule parallelization, which is followed by a simple and effective control scheme that achieves submodule voltage balancing. Moreover, we include fault tolerant operation of MMCs. Section IV focuses on the analysis of capacitance reduction through the proposed strategy. Once again, we carry out the analysis in STATCOM applications. Section V provides simulation and experimental results for verification purposes. Finally, Section VI concludes this article.

II. Fundamental Operating Principles of MMCs With Symmetrical Half-Bridge Submodules

This section introduces fundamental operating principles of MMCs with symmetrical half-bridge submodules. It begins with the system schematic diagram. Subsequently, we show the relevant control architecture.

A. System Schematic Diagram

Fig. 2 illustrates the schematic diagram of cascaded-bridge converters or MMC arms based on symmetrical half-bridge submodules, where $v_{\mathrm{dc}i\mathrm{u}}$ and $v_{\mathrm{dc}i\mathrm{d}}$ ($i \in \{1, 2, \ldots, n\}$) represent the voltages of upper and lower dc capacitors, respectively. Correspondingly, $v_{\mathrm{ac}i}$ stands for the output voltage of each submodule. n denominates the number of submodules. Although submodules may output dc voltages, their output voltages are denoted with the subscript ac for clarity. The total output voltage amounts to v_{ac}, i.e., $v_{\mathrm{ac}} = v_{\mathrm{ac1}} + v_{\mathrm{ac2}} + \cdots + v_{\mathrm{ac}n}$, while i_{ac} designates the grid/load current. In each submodule, the upper switch and lower one (including both active switches and diodes) operate complimentarily. With the upper switch ON and lower switch OFF, the symmetrical half-bridge submodule yields a

positive voltage $v_{\mathrm{dc}iu}$, otherwise a negative output $-v_{\mathrm{dc}id}$ given by the lower capacitor is expected.

By adjusting the time durations of the two operating modes in every switching period, the submodule controls its output voltage $v_{\mathrm{ac}i}$, mathematically described by

$$v_{\mathrm{ac}i}(t) = \frac{1}{T_{\mathrm{s}}}\left\{d_i(t)T_{\mathrm{s}}v_{\mathrm{dc}iu}(t) - \left[1-d_i(t)\right]T_{\mathrm{s}}v_{\mathrm{dc}id}(t)\right\} \quad (1)$$

where T_{s} stands for the switching period, and $d_i(t) \in (0, 1)$ denotes the duty ratio of each submodule. Normally, we regulate all the dc capacitor voltages to be identical, namely, $v_{\mathrm{dc}iu} = v_{\mathrm{dc}id} = v_{\mathrm{dc}i}$. However, we may also control capacitor voltages with different values so as to generate more voltage levels [33]. Assuming that the upper and lower capacitor voltages are equal to $v_{\mathrm{dc}i}$, (1) reduces to

$$v_{\mathrm{ac}i}(t) = \left[2d_i(t) - 1\right]v_{\mathrm{dc}i}(t) \quad (2)$$

from which it is clear that a d_{i} less than 0.5 indicates a negative output voltage, as $v_{\mathrm{dc}i}$ should always be positive.

B. Control Architecture

The control architecture of MMCs depends greatly on applications. In this article, we apply MMCs to STATCOMs or reactive power compensation applications. Conventionally, switched capacitor banks are used for reactive power compensation in bulk power systems [34]. Despite their simplicity, they are very inflexible (only providing capacitive power at several discrete power levels) and may introduce extra resonances when interacting with existing inductive components. In contrast, power electronic equipment (e.g., STATCOMs) allows flexible and smooth reactive power compensation with the possibility of delivering other grid-supportive services (say inertia) [35]. MMCs are one of the most ideal enabling technologies for STATCOMs [2], [3], [5], [23], [36].

Overall, the control of MMCs is briefly classified into two categories—high-frequency pulsewidth modulated (PWM) control and fundamental-frequency scheduler-based control [37]−[39]. Since the STATCOM application requires high power quality, PWM control is employed here. Fig. 3 illustrates the control architecture of MMCs with symmetrical half-bridge submodules operating as STATCOMs, where the input reference signals $v_{\mathrm{dc\_ref}}$ and $i_{\mathrm{q\_ref}}$ target at dc capacitor voltages and reactive current, respectively. The grid voltage v_{grid} is sensed, which goes through a phase-locked loop, yielding the phase angle information $\sin\theta$ and $\cos\theta$. Moreover, $G_{\mathrm{PI}}(s)$, $G_{\mathrm{PR}}(s)$, and $G_{\mathrm{Fil\_2}}(s)$ stand for the complex frequency domain transfer functions of proportional-integral controllers, proportional-resonant controllers, and notch filters tuned at second harmonic, respectively, expressed as

$$G_{\mathrm{PI}}(s) = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s} \quad (3)$$

$$G_{\mathrm{PR}}(s) = K_{\mathrm{p}} + \frac{2K_{\mathrm{r}}\omega_{\mathrm{i}}s}{s^2 + 2\omega_{\mathrm{i}}s + {\omega_{\mathrm{o}}}^2} \quad (4)$$

$$G_{\mathrm{Fil\_2}}(s) = \frac{s^2 + (2\omega_{\mathrm{o}})^2}{s^2 + 2\omega_{\mathrm{i}}s + (2\omega_{\mathrm{o}})^2} \quad (5)$$

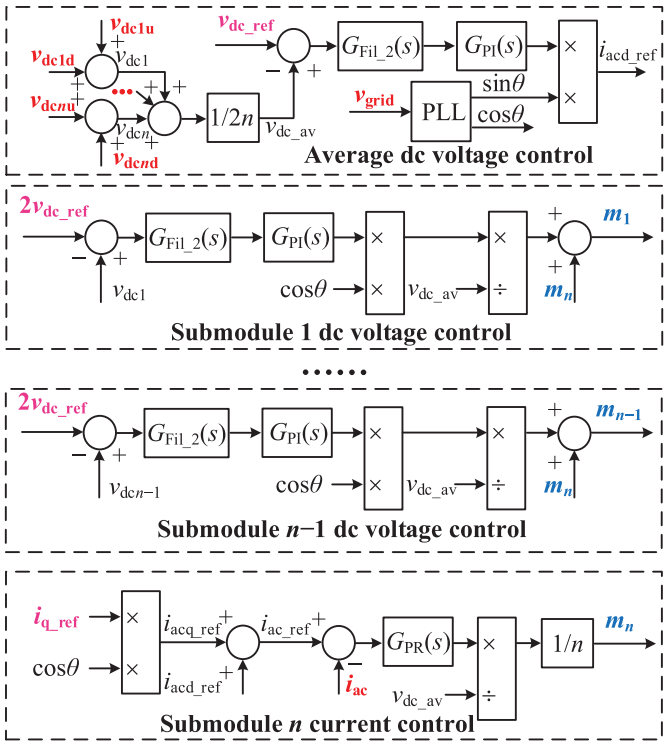

Fig. 3. Control architecture of MMCs with symmetrical half-bridge submodules operating as STATCOMs.

where K_{p}, K_{i}, and K_{r} represent the proportional, integral, and resonant gains, respectively. $\omega_{\mathrm{o}} = 2\pi f_{\mathrm{o}}$ denotes the fundamental angular frequency, while ω_{i} determines the width of rejected bands of notch filters. In Fig. 3, the modulation signals m_i serve as the outputs that feed PWM drivers. During normal operation, $m_i \in (-1, +1)$. Considering the duty ratio in (1), we have $d_i(t) = 0.5m_i(t) + 0.5$.

As shown in Fig. 3, the control architecture comprises n voltage controllers (including one average dc voltage controller and $n-1$ submodule dc voltage controllers) as well as one ac current controller, which is implemented by the submodule n current control. Notably, the dc voltage controllers can regulate the voltage sums of upper and lower dc capacitors of individual submodules. However, they fail to clear the voltage difference between upper and lower capacitors in each submodule, as will be demonstrated in the following sections.

III. Proposed Submodule Parallelization Strategy

This section introduces the proposed hardware-based strategy via parallelization of symmetrical half-bridge submodules in MMCs. Through a simple control approach, we can balance the voltages of all dc capacitors in a sensorless fashion. Moreover, we introduce fault tolerant operation of MMCs.

A. Description of the Proposed Strategy

Recapping Fig. 2, we notice that a special problem related to MMCs with symmetrical half-bridge submodules lies in the mismatch of upper and lower capacitor voltages, i.e.,

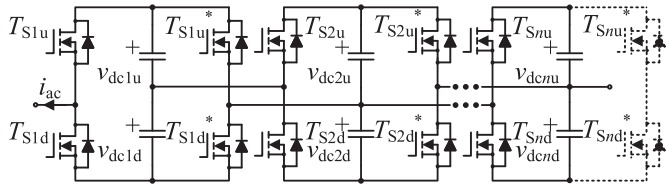

Fig. 4. Schematic of the proposed strategy through parallelization of half-bridge MMC submodules.

$v_{\mathrm{dc}iu} \neq v_{\mathrm{dc}id}$. This problem is caused by capacitance mismatches, voltage sensor offsets, and/or improper modulation [21]. Negative results of the problem include over-modulation, current distortion, and/or even malfunction of MMC systems.

By injection of a dc component into the ac grid-injected current through control software, half-bridge-based power converters achieve capacitor voltage balancing in a straightforward manner [19], [21], [22]. This solution will increase the dc output current as long as the upper capacitor voltage exceeds the lower one. Consequently, the upper capacitor charges the lower capacitor, leading to the balance of capacitor voltages. Unfortunately, a direct transplant of this solution from half-bridge converters to MMCs with symmetrical half-bridge submodules fails due to submodule control conflicts. To be more specific, the dc component of the grid current gives only one degree of extra control freedom, which is insufficient to balance all upper and lower capacitor voltages [17].

In contrast, hardware-based strategies can enable capacitor voltage balancing through parallelization of submodules. For example, MMCs with paralleled double H-bridge and double asymmetrical half-bridge submodules have been investigated in [7], [16], [40], [41]. Further, we propose the parallelization strategy of MMCs (or cascaded-bridge converters) with identical symmetrical half-bridge submodules, as shown in Fig. 4, where $T_{\mathrm{s}iu}{}^*$ and $T_{\mathrm{s}id}{}^*$ ($i \in \{1, 2, \ldots, n\}$) are newly added switches, which allow parallel connection of submodule capacitors. Notably, we may remove $T_{\mathrm{s}nu}{}^*$ and $T_{\mathrm{s}nd}{}^*$ for simplification.

Fig. 5 demonstrates the proposed modulation and control scheme for MMC submodules, where the modulation signals m_i come from the voltage and current controllers in Fig. 3. After modulated, the gate signal $g_{\mathrm{TS}i}$ (i.e., $g_{\mathrm{TS}iu}$) drives the corresponding upper switch $T_{\mathrm{S}iu}$, while its complimentary signal $g_{\mathrm{TS}id}$ drives the lower switch $T_{\mathrm{S}id}$.

Special attention should be paid to the gate signals $g_{\mathrm{TS}iu}{}^*$ and $g_{\mathrm{TS}id}{}^*$, which control the additional switches (with asterisk notations) of each submodule in Fig. 4. Noticeably, the proposed control or modulation scheme derives $g_{\mathrm{TS}iu}{}^*$ and $g_{\mathrm{TS}id}{}^*$ directly from the gate signal $g_{\mathrm{TS}(i+1)}$ of an adjacent submodule, indicating that no extra controller is required for the additional circuits or switches, which in turn greatly saves control efforts. Although not shown in Fig. 5, dead zones are inserted between upper and lower switch pairs in practice.

B. Voltage Balancing Analysis

We proceed to analyze the mechanism of voltage balancing through the proposed parallelization strategy. Returning back to

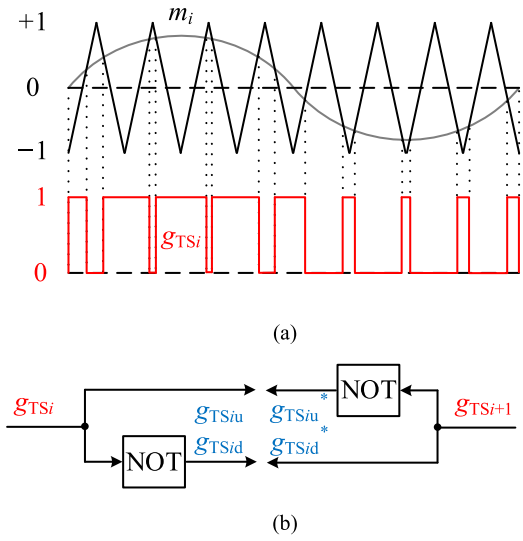

Fig. 5. Modulation and control scheme for MMC submodules. (a) PWM generation. (b) Gate signals.

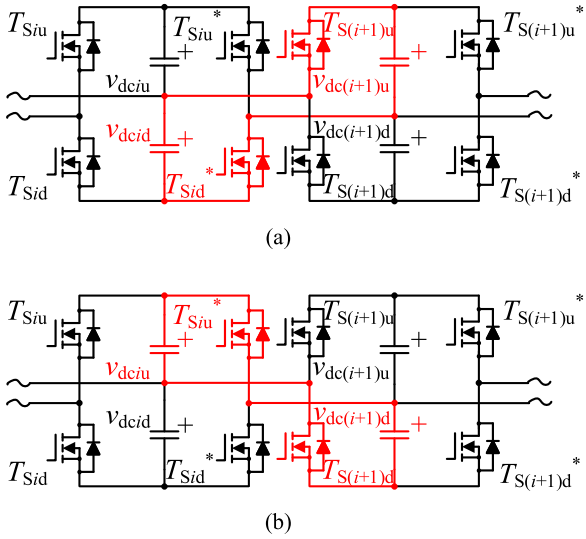

Fig. 6. Voltage balancing mechanism of the proposed strategy through parallelization of half-bridge MMC submodules. (a) Mode I. (b) Mode II.

Figs. 4 and 5, we know that $T_{\mathrm{S}iu}{}^*$ and $T_{\mathrm{S}(i+1)\mathrm{d}}$ switch ON and OFF simultaneously, as complimentary to $T_{\mathrm{S}id}{}^*$ and $T_{\mathrm{S}(i+1)u}$.

Fig. 6 details the operation of these switches, where two adjacent submodules are incorporated. For simplification of analysis, let us first ignore the ON-state voltage drops of semiconductor switches and equivalent series resistors (ESRs) of capacitors. As shown in Fig. 6(a), when $T_{\mathrm{S}(i+1)\mathrm{u}}$ and $T_{\mathrm{S}id}{}^*$ turn ON (with $T_{\mathrm{S}iu}{}^*$ and $T_{\mathrm{S}(i+1)\mathrm{d}}$ OFF), the upper capacitor of submodule $(i+1)$ and the lower capacitor of submodule (i) connect in parallel. This parallel connection clears the voltage difference between $v_{\mathrm{dc}(i+1)\mathrm{u}}$ and $v_{\mathrm{dc}id}$, thereby making $v_{\mathrm{dc}id} = v_{\mathrm{dc}(i+1)\mathrm{u}}$. Alternatively, $v_{\mathrm{dc}iu} = v_{\mathrm{dc}(i+1)\mathrm{d}}$ satisfies when $T_{\mathrm{S}(i+1)\mathrm{d}}$ and $T_{\mathrm{S}iu}{}^*$ turn ON (with $T_{\mathrm{S}id}{}^*$ and $T_{\mathrm{S}(i+1)\mathrm{u}}$ OFF), as illustrated in Fig. 6(b). It should be commented that the sudden parallelization of two voltage sources (like capacitors) with different voltages is

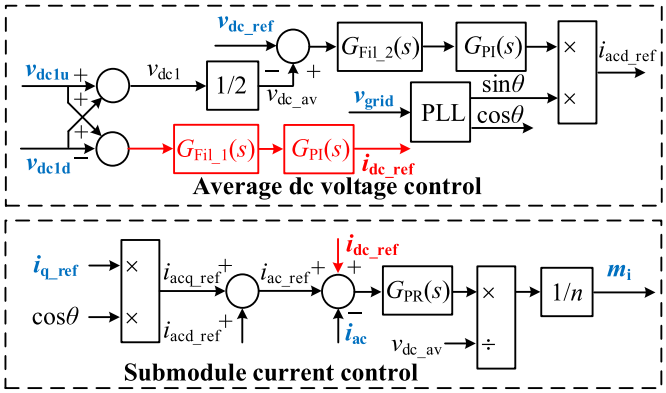

Fig. 7. Simplified control architecture of MMCs with symmetrical half-bridge submodules and the proposed strategy.

not allowed according to the circuit theory. However, capacitor ESRs, line inductances, and forward voltage drops of switches attenuate current spikes in practice. Detailed feasibility analysis of module parallelization can be found in [7], [16], [40], [41].

In every switching period, $T_{\mathrm{S}iu}$ and $T_{\mathrm{S}id}$ switch ON and OFF once. By mathematical induction, we can derive the following equations without considering switching ripples:

$$\begin{aligned} v_{\mathrm{dc1u}} &= v_{\mathrm{dc2d}} = v_{\mathrm{dc3u}} = \cdots = v_{\mathrm{dc}(2k+1)\mathrm{u}} = v_{\mathrm{dc}(2k+2)\mathrm{d}} \\ v_{\mathrm{dc1d}} &= v_{\mathrm{dc2u}} = v_{\mathrm{dc3d}} = \cdots = v_{\mathrm{dc}(2k+1)\mathrm{d}} = v_{\mathrm{dc}(2k+2)\mathrm{u}} \end{aligned} \tag{6}$$

where $2k+2 \leq n$(k is a natural number). Equation (6) indicates that diagonal dc capacitor voltages are equalized through the proposed submodule parallelization strategy.

To completely equalize all capacitor voltages, we can follow the dc current injection method detailed in [19], [21], [22]. In addition, we still need one voltage controller that regulates all the dc capacitor voltages to their reference values, namely

$$v_{\mathrm{dc}iu} = v_{\mathrm{dc}id} = v_{\mathrm{dc\_ref}} (i \in \{1, 2, \ldots, n\}). \tag{7}$$

With the proposed strategy, the control architecture of MMCs is greatly simplified. Most of the voltage controllers in Fig. 3 is removed, except for one voltage controller that ensures dc voltage tracking. Fig. 7 demonstrates the simplified control architecture of MMCs with symmetrical half-bridge submodules and the proposed parallelization strategy, where the dc current injection part is highlighted. $G_{\mathrm{Fil\_1}}(s)$ models a notch filter tuned at the fundamental frequency, i.e.,

$$G_{\mathrm{Fil\_1}}(s) = \frac{s^2 + {\omega_{\mathrm{o}}}^2}{s^2 + 2\omega_{\mathrm{i}} s + {\omega_{\mathrm{o}}}^2} \tag{8}$$

which aims to get rid of dominant ripples in $(v_{\mathrm{dc1u}} - v_{\mathrm{dc1d}})$. The simplified control architecture in Fig. 7 is almost identical to that of symmetrical half-bridge converters [19], [21], [22].

C. Fault Tolerant Operation

Referring to Fig. 2, we observe that symmetrical half-bridge submodules in conventional MMCs cannot be bypassed in case of submodule faults, e.g., open-circuit faults. Fortunately, the proposed strategy allows fault tolerant operation of MMCs with symmetrical half-bridge submodules.

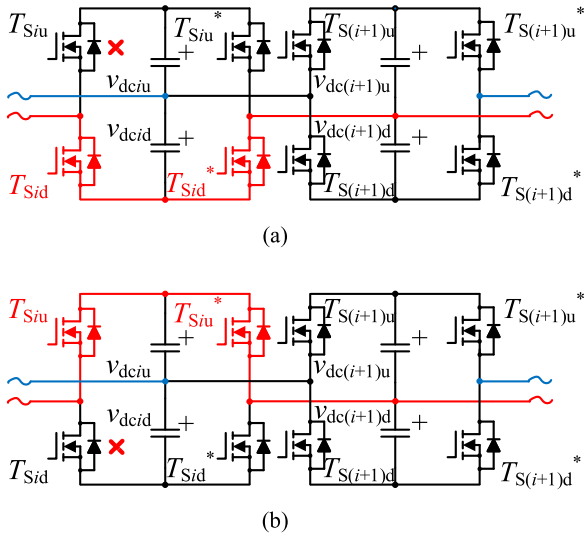

Fig. 8. Fault tolerant operation of MMCs with symmetrical half-bridge submodules and the proposed strategy. (a) Fault mode I. (b) Fault mode II.

Fig. 8 presents the proposed bypass strategy of symmetrical half-bridge submodules, where adjacent submodules work together for bypass purposes. In the case of $T_{\mathrm{s}iu}$ fault, we keep $T_{\mathrm{s}id}$ and $T_{\mathrm{s}id}{}^*$ turned ON, as depicted in Fig. 8(a). In this way, it is evident that the submodule (i) is bypassed. However, note that the submodule ($i+1$) cannot turn ON its switches $T_{\mathrm{s}(i+1)\mathrm{u}}$ and $T_{\mathrm{s}(i+1)\mathrm{d}}$ freely, and hence also bypassed equivalently. Similarly, under the fault condition of $T_{\mathrm{s}id}$, we maintain the switches $T_{\mathrm{s}iu}$ and $T_{\mathrm{s}iu}{}^*$ ON, leading again to the bypass of the submodules (i) and ($i+1$). It is worth mentioning that MMCs can still operate normally without the parallel connectivity of faulty submodules when only additional switches (e.g., $T_{\mathrm{s}iu}{}^*$) collapse.

In summary, the proposed submodule parallelization strategy greatly simplifies MMC control into symmetrical half-bridge converter control. It addresses the voltage balance problem in a sensorless fashion with the removal of almost all dc voltage sensors and voltage controllers. Moreover, the proposed strategy allows fault tolerant operation of MMCs.

IV. Analysis of Capacitance Reduction Through the Proposed Strategy

This section focuses on the analysis of dc capacitor voltage ripples, which further determines the design of dc capacitances. First, we analyze the capacitance requirement of conventional MMCs with symmetrical half-bridge submodules. Next, we compare the result with that of the proposed parallelization strategy, indicating the effectiveness of capacitance saving.

A. Capacitance Requirement of Conventional MMCs

In MMCs, dc capacitors are bulky and expensive components that play a decisive role on system size, weight, and cost [17]. As such, the reduction of dc capacitances will greatly benefit MMC systems. In this subsection, we intend to analyze the capacitance requirement of MMCs shown in Fig. 2, i.e., those with

symmetrical half-bridge submodules yet without the proposed submodule parallelization scheme, in STATCOM applications.

Generally, STATCOMs inject inductive (absorb capacitive) reactive power into (from) power grids. Under this condition, the ac voltage and grid-injected current can be represented by

$$v_{\rm ac}(t) = \sqrt{2}V_{\rm ac}\sin(\omega_0 t),$$
$$i_{\rm ac}(t) = -\sqrt{2}I_{\rm ac}\cos(\omega_0 t) \tag{9}$$

where $V_{\rm ac}$ and $I_{\rm ac}$ refer to the root-mean-square values of $v_{\rm ac}$ and $i_{\rm ac}$, respectively. Note that $V_{\rm ac}$ can be derived from $v_{\rm grid}$ by subtraction of the voltage drop across the output filter.

Recapping Fig. 2, we imply that the upper capacitor $C_{\rm dciu}$ will be charged during the period that $i_{\rm ac}$ is negative. Besides, the charge happens when the upper switch $T_{s\,iu}$ turns ON. Taking these two points into consideration, we can derive the peak to peak value of capacitor voltage ripples as

$$\Delta v_{{\rm dc}i\_{\rm wo}} = -\frac{1}{C_{\rm dc}}\int_{-0.25/f_{\rm o}}^{0.25/f_{\rm o}} d_i(t)i_{\rm ac}(t){\rm d}t \tag{10}$$

where $C_{\rm dc}$ refers to the capacitance of all dc capacitors. Next, using the symmetrical feature of ac output voltages, we obtain

$$\int_{-0.25/f_{\rm o}}^{0} d_i(t)i_{\rm ac}(t){\rm d}t = \int_{0}^{0.25/f_{\rm o}} [1-d_i(t)]\,i_{\rm ac}(t){\rm d}t. \tag{11}$$

Substitution of (11) into (10), the latter reduces to

$$\Delta v_{\rm dci\_wo} = \frac{1}{\omega_0 C_{\rm dc}}\int_0^{\pi/2}\sqrt{2}I_{\rm ac}\cos(\omega_0 t){\rm d}(\omega_0 t) = \frac{\sqrt{2}I_{\rm ac}}{\omega_0 C_{\rm dc}}. \tag{12}$$

Clearly, the resultant capacitor voltage ripple depends on the grid current $I_{\rm ac}$, dc capacitance $C_{\rm dc}$, and fundamental angular frequency ω_0. However, it has no relationship with the number of submodules, indicating the independence of each submodule capacitor. Given a system operating condition (including $I_{\rm ac}$ and ω_0 among others), the dc capacitance should be designed to limit capacitor voltage ripples, that is,

$$C_{\rm dc} \geq C_{\rm dc\_wo} = \frac{\sqrt{2}I_{\rm ac}}{\omega_0 \Delta v_{{\rm dc}i\_{\rm wo}}}. \tag{13}$$

Considering that the rated value of all capacitor voltages equals $v_{\rm dc\_ref}$, we derive the minimum total stored energy as

$$E_{\rm wo} = \frac{2n}{2}C_{\rm dc\_wo}{v_{\rm dc\_ref}}^2 = \frac{\sqrt{2}I_{\rm ac}{v_{\rm dc\_ref}}^2 n}{\omega_0 \Delta v_{{\rm dc}i\_{\rm wo}}} \tag{14}$$

which also reflects the total cost of all dc capacitors [42].

B. Capacitance Requirement of MMCs With the Proposed Submodule Parallelization Strategy

In this subsection, we will derive the expressions of submodule voltage ripples as well as capacitance and energy storage requirements with the proposed submodule parallelization strategy. Due to parallel connectivity, symmetrical half-bridge submodules equalize diagonal capacitor voltages in each switching period, i.e., $v_{{\rm dc}iu} = v_{{\rm dc}(i+1){\rm d}}$ and $v_{{\rm dc}i{\rm d}} = v_{{\rm dc}(i+1){\rm u}}$ ($i = 1, 2, n-1$). Accordingly, we divide all submodule capacitors into two groups for simplification of analysis. Specifically, with an even number of submodules (i.e., $n = 2k+2$), the two groups are $\rm C_{dc1u}$, $\rm C_{dc2d}$, $\rm C_{dc3u}$, …, $\rm C_{dc(n-1)u}$, $\rm C_{dcnd}$ and $\rm C_{dc1d}$, $\rm C_{dc2u}$, $\rm C_{dc3d}$, …, $\rm C_{dc(n-1)d}$, $\rm C_{dcnu}$. When the number of submodules n is odd ($n = 2k+1$), the two groups become $\rm C_{dc1u}$, $\rm C_{dc2d}$, $\rm C_{dc3u}$, …, $\rm C_{dc(n-1)d}$, $\rm C_{dcnu}$ and $\rm C_{dc1d}$, $\rm C_{dc2u}$, $\rm C_{dc3d}$, …, $\rm C_{dc\,(n-1)u}$, $\rm C_{dcnd}$.

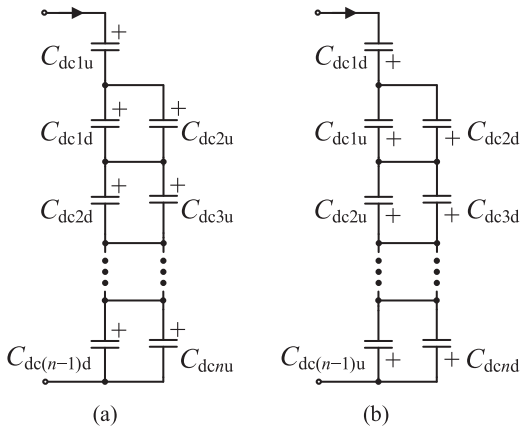

Fig. 9. Charging and discharging conditions of all dc capacitors in MMCs with the proposed strategy. (a) Charging. (b) Discharging.

Referring to the control architecture in Fig. 7, we observe that all the modulation signals m_i (or d_i) are identical. This fact, together with Fig. 6, leads to the charging and discharging conditions in Fig. 9. Notably, the parity of the number of submodules n greatly affects capacitor ripples.

In the case of an even n (i.e., $n = 2k+2$), we charge the first group capacitors $C_{\rm dc1u}$, $C_{\rm dc2d}$, $C_{\rm dc3u}$, … $C_{{\rm dc}(n-2){\rm d}}$, and $C_{{\rm dc}(n-1){\rm u}}$ according to Fig. 9(a). Alternatively, $C_{\rm dc1u}$, $C_{\rm dc2d}$, … $C_{{\rm dc}(n-1){\rm u}}$, and $C_{{\rm dc}n{\rm d}}$ are discharged in Fig. 9(b), leading to the average charge of each capacitor in the first group as

$${\rm d}Q_{\rm even}(t) = \frac{-i_{\rm ac}(t)}{n}\left\{\frac{n}{2}d_i(t) - \frac{n}{2}[1-d_i(t)]\right\}{\rm d}t \tag{15}$$

where the negative sign is caused by the definition of the direction of $i_{\rm ac}(t)$ (see Fig. 4). Note that the average charge remains unchanged as for the other group of capacitors.

The average capacitor voltage ripple is further derived by integration of the average charge in (15) during a half fundamental period and divided by the capacitance $C_{\rm dc}$ as

$$\Delta v_{{\rm dc}i\_{\rm even0}} = \frac{-1}{2C_{\rm dc}}\int_{-0.25/f_{\rm o}}^{0.25/f_{\rm o}} i_{\rm ac}(t)\,[2d_i(t)-1]\,{\rm d}t. \tag{16}$$

By use of (2), we rearrange (16) as

$$\Delta v_{{\rm dc}i\_{\rm even0}} = \frac{-1}{2C_{\rm dc}}\int_{-0.25/f_{\rm o}}^{0.25/f_{\rm o}}\frac{v_{{\rm ac}i}(t)}{v_{{\rm dc}i}(t)}i_{\rm ac}(t){\rm d}t$$
$$\xrightarrow{v_{{\rm ac}i}=v_{\rm ac}/n,\,v_{{\rm dc}i}\approx v_{\rm dc\_ref}} \frac{-1}{2C_{\rm dc}n}\int_{-0.25/f_{\rm o}}^{0.25/f_{\rm o}}\frac{v_{\rm ac}(t)}{v_{\rm dc\_ref}}i_{\rm ac}(t){\rm d}t = 0 \tag{17}$$

where the assumption of small dc voltage ripples ensures $v_{{\rm dc}i} \approx v_{\rm dc\_ref}$. Due to the symmetry of $v_{\rm ac}$ and $i_{\rm ac}$ in (17), the resultant voltage ripple equals zero in a half of the line cycle, i.e., during

the negative period of $i_{\rm ac}$. Instead, the voltage ripple maximizes in a quarter of the line cycle at

$$\Delta v_{{\rm dc}i\_{\rm wi\_even}} = -\frac{1}{2C_{\rm dc}n}\int_0^{0.25/f_{\rm o}} \frac{v_{\rm ac}(t)}{v_{\rm dci\_ref}} i_{\rm ac}(t){\rm d}t = \frac{V_{\rm ac}I_{\rm ac}}{2\omega_0 C_{\rm dc} v_{\rm dc\_ref} n}. \tag{18}$$

To limit the voltage ripple, we derive the capacitance requirement as

$$C_{\rm dc} \geq C_{\rm dc\_wi\_even} = \frac{V_{\rm ac}I_{\rm ac}}{2\omega_0 v_{\rm dc\_ref}\Delta v_{{\rm dc}i\_{\rm even}} n}. \tag{19}$$

To directly compare the degree of capacitance saving, we fix the capacitor voltage ripples in (13) and (19), which give the ratio of capacitances

$$\frac{C_{\rm dc\_wi\_even}}{C_{\rm dc\_wo}} = \frac{\sqrt{2}V_{\rm ac}}{4v_{\rm dc\_ref}n} < \frac{1}{4} \tag{20}$$

where the voltage ripple is maintained and fixed. Notably, the inequality in (20) must be satisfied according to $nv_{\rm dc\_ref} > |v_{\rm ac}|$ so as to avoid over-modulation problems [43]. As a result, at least four times capacitance saving can be expected with the even number of paralleled submodules.

Next, we derive the minimum total stored energy based on (19) as

$$E_{\rm wi\_even} = \frac{2n}{2}C_{\rm dc\_wi\_even}{v_{\rm dc\_ref}}^2 = \frac{V_{\rm ac}I_{\rm ac}v_{\rm dc\_ref}}{2\omega_0\Delta v_{{\rm dc}i\_{\rm wi\_even}}}. \tag{21}$$

Similarly, we divide (19) by (14), yielding the ratio of stored energies:

$$\frac{E_{\rm wi\_even}}{E_{\rm wo}} = \frac{\sqrt{2}V_{\rm ac}}{4v_{\rm dc\_ref}n} < \frac{1}{4}. \tag{22}$$

Once again, we expect at least four times reductions of the stored energy and related capacitor cost [42].

Next, we analyze the case of an odd n (i.e., $n = 2k + 1$). Under this condition, the average charge of diagonal capacitors is derived from Fig. 9 as

$${\rm d}Q_{\rm odd}(t) = \frac{-i_{\rm ac}(t)}{n}\left\{\frac{n+1}{2}d_i(t) - \frac{n-1}{2}\left[1-d_i(t)\right]\right\}{\rm d}t \tag{23}$$

By integration of ${\rm d}Q_{\rm odd}(t)$ in a half fundamental line period, the average capacitor voltage peak to peak ripple takes the form of

$$\Delta v_{{\rm dc}i\_{\rm wi\_odd}} = \frac{-1}{2C_{\rm dc}n}\int_{-0.25/f_{\rm o}}^{0.25/f_{\rm o}} \{ni_{\rm ac}(t)\left[2d_i(t)-1\right] + i_{\rm ac}(t)\}{\rm d}t. \tag{24}$$

With the help of (16) and (17), we simplify (24) as

$$\Delta v_{{\rm dc}i\_{\rm wi\_odd}} = \frac{1}{2\omega_0 C_{\rm dc}n}\int_{-\pi/2}^{\pi/2}\sqrt{2}I_{\rm ac}\cos(\omega_0 t){\rm d}(\omega_0 t) = \frac{\sqrt{2}I_{\rm ac}}{\omega_0 C_{\rm dc}n}. \tag{25}$$

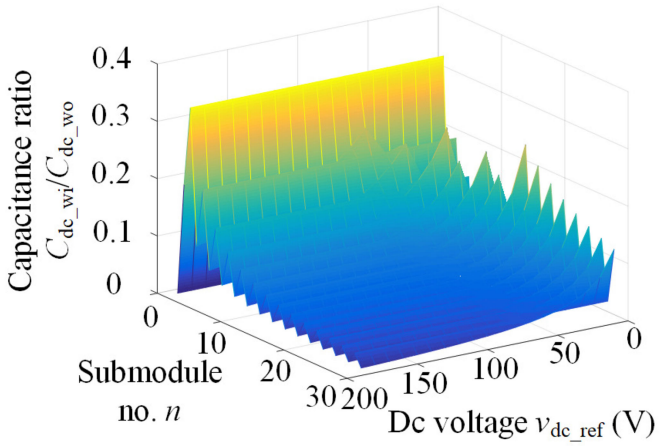

Fig. 10. Capacitance reduction ratio $C_{\rm dc\_wi}/C_{\rm dc\_wo}$ as functions of the number of submodules n and dc voltage reference $v_{\rm dc\_ref}$ with a constant ac voltage 220 Vrms.

Accordingly, the dc capacitance requirement becomes

$$C_{\rm dc} \geq C_{\rm dc\_wi\_odd} = \frac{\sqrt{2}I_{\rm ac}}{\omega_0\Delta v_{{\rm dc}i\_{\rm wi\_odd}} n}. \tag{26}$$

In comparison, the capacitance saving becomes

$$\frac{C_{\rm dc\_wi\_odd}}{C_{\rm dc\_wo}} = \frac{1}{n} \tag{27}$$

which clearly indicates that the saving grows linearly with the number of submodules. Also, we can obtain the minimum total stored energy on the basis of (26) as

$$E_{\rm wi\_odd} = \frac{2n}{2}C_{\rm dc\_wi\_odd}{v_{\rm dc\_ref}}^2 = \frac{\sqrt{2}I_{\rm ac}{v_{\rm dc\_ref}}^2}{\omega_0\Delta v_{{\rm dci\_wi\_odd}}}. \tag{28}$$

Similarly, the ratio of stored energies is calculated as

$$\frac{E_{\rm wi\_odd}}{E_{\rm wo}} = \frac{1}{n}. \tag{29}$$

Fig. 10 plots the capacitance saving ratio $C_{\rm dc\_wi}/C_{\rm dc\_wo}$ (or the energy saving ratio $E_{\rm wi}/E_{\rm wo}$) as functions of the number of submodules n and the dc voltage reference $v_{\rm dc\_ref}$, where the ac voltage is fixed as $V_{\rm ac} = 220$ V. Depending on the parity of n, we plot the curved surface according to (20) and (27), respectively. Obviously, the capacitance or energy reduction is always greater than three times. In favorable cases, more than 10-time saving of capacitance and stored energy is possible. In comparison, an odd n yields more pronounced saving than an even n with large n and small $v_{\rm dc\_ref}$. To sum up, the analysis in this section fully discloses the benefits of the proposed strategy in capacitance reduction or saving.

V. Simulation and Experimental Results

This section provides simulation and experimental results of conventional MMCs with symmetrical half-bridge submodules as well as MMCs with symmetrical half-bridge submodules and the proposed submodule parallelization strategy for verification purposes. Tables I and II summarize the relevant system and control parameters, respectively.

TABLE I
MMC SYSTEM PARAMETERS

Descriptions	Symbols	Values
Fundamental frequency	f_o	50 Hz
Grid voltage (rms)	v_{grid_ref}	220 Vrms/110 Vrms
Filter inductance	L_c	10 mH
Nominal dc capacitance	C_{dc}	4.7 mF and 470 μF
Nominal dc voltage	v_{dc_ref}	200 V/100 V
Submodule number	n	3 and 4/2

TABLE II
MMC CONTROL PARAMETERS

Descriptions	Symbols	Values
Voltage control P gain	K_{vp}	0.5
Voltage control I gain	K_{vi}	5
Current control P gain	K_{cp}	10
Current control R gain	K_{cr}	300
Reactive current reference	i_{q_ref}	30 A/15 Arms
Filter damping factor	ω_i	$1\%\omega_o$
Switching/ sampling frequency	f_s	10 kHz

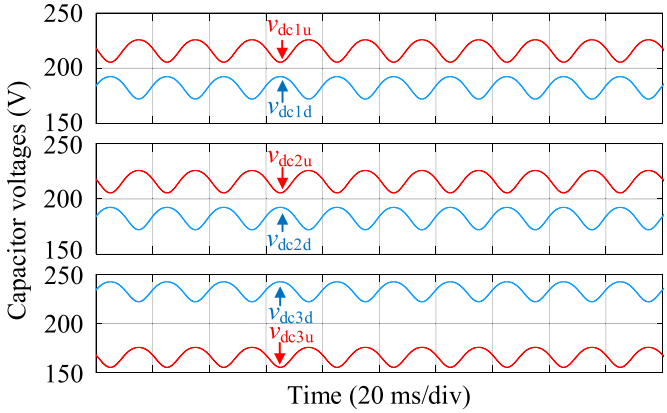

Fig. 11. Simulation results of conventional MMCs with three symmetrical half-bridge submodules.

A. Simulation Results

Fig. 11 illustrates the Matlab simulation results of conventional MMCs with three symmetrical half-bridge submodules, where the initial voltage of one submodule capacitor is intentionally designed to be 50 V greater than the nominal dc voltage $v_{dc\_ref} = 200$ V, leading to the imbalance of upper and lower capacitor voltages, as analyzed in Section III-A. In Fig. 11, the voltage controllers regulate the sums of upper and lower capacitor voltages in each submodule to their references, i.e., $v_{dciu} + v_{dcid} = 2v_{dc\_ref}$ $(i = 1, 2, 3)$. Additionally, the peak to peak voltage ripple reaches 20.3 V, which agrees with (12).

Fig. 12 shows the simulation results of MMCs with three symmetrical half-bridge submodules and the proposed strategy, where the initial voltage of one submodule capacitor is 50 V

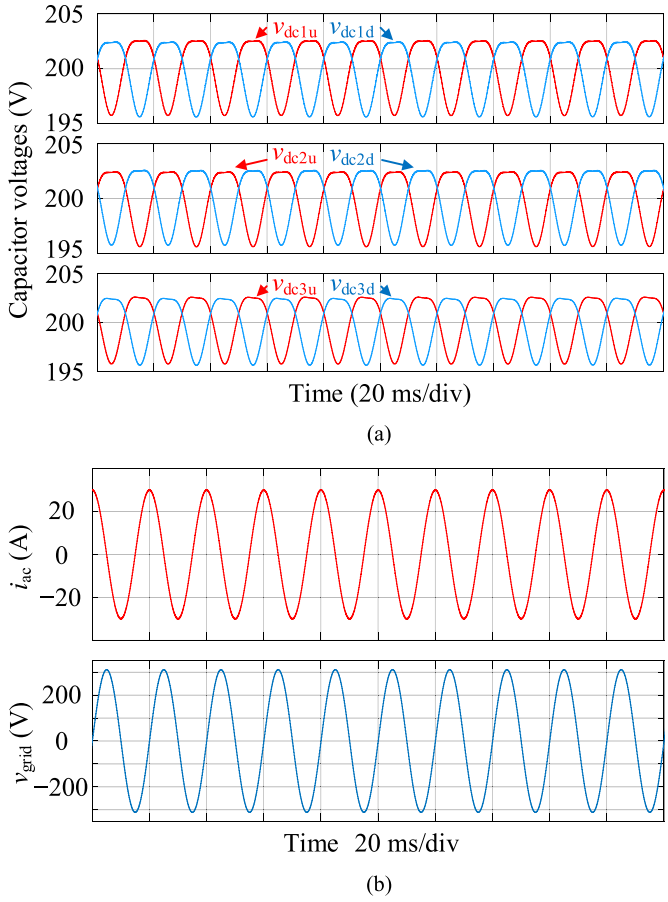

Fig. 12. Simulation results of MMCs with three symmetrical half-bridge submodules and the proposed submodule parallelization strategy. (a) Individual capacitor voltages. (b) Grid current i_{ac} and voltage v_{grid}.

greater again. Obviously, the proposed strategy clears voltage differences and achieves voltage balancing in Fig. 12(a). Moreover, the strategy achieves a three-time reduction of voltage ripples to 6.8 V, as (27) indicates. With balanced dc capacitor voltages, MMCs work properly as STATCOMs for reactive power compensation, as shown in Fig. 12(b).

Fig. 13 compares capacitor voltage ripples in the case of an even number of submodules, i.e., four submodules. In this case, the proposed strategy allows ripple reduction even with 10-time smaller capacitances. According to (20), almost 15-times capacitance saving is expected. As shown in Fig. 13(b), the period of voltage ripples becomes one half line period, which proves the analysis in Section IV-B.

Fig. 14 provides the simulation results of MMC fault operation, where two submodules are bypassed according to Fig. 8. This bypass activity poses no threat to the normal operation of MMCs as STATCOMs [see Fig. 14(b)]. However, it is clear from Fig. 14(a) that the voltage ripple increases due to fewer working submodules.

B. Experimental Results

We conducted experiments for further validation purposes based on the schematic shown in Fig. 4. The major experimental

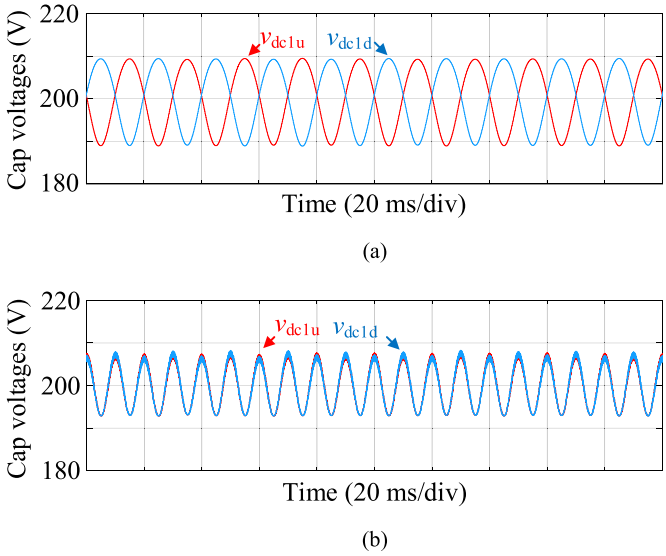

Fig. 13. Simulation results of MMCs with four symmetrical half-bridge submodules. (a) Conventional MMCs with $C_{\rm dc} = 4.7$ mF. (b) MMCs with the proposed strategy and $C_{\rm dc} = 470\ \mu$F.

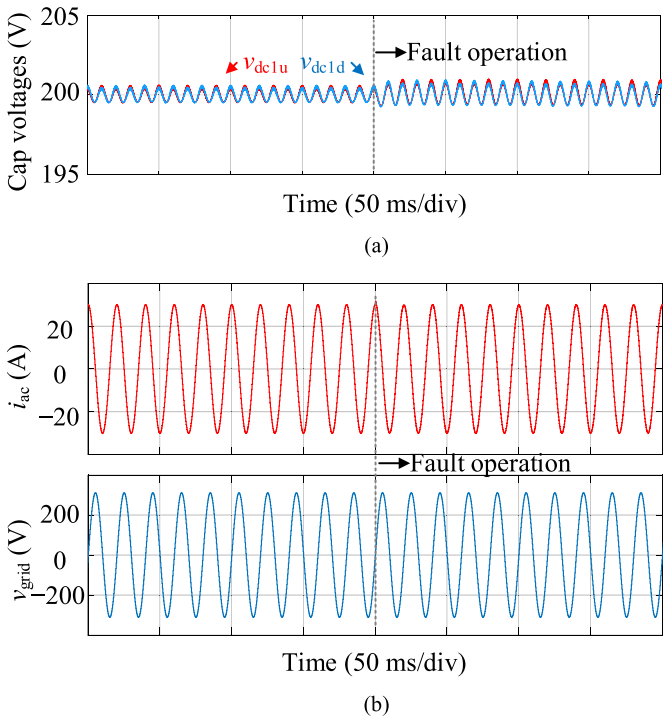

Fig. 14. Simulation results of MMCs' fault tolerant operation. (a) Capacitor voltages. (b) Grid current $i_{\rm ac}$ and voltage $v_{\rm grid}$.

equipment and devices include two oscilloscopes (Agilent DSO-X 3024A: 200 MHz, four channels), a grid emulator (ITECH IT7625: 4.5 kVA, 300 V), a digital controller (Plexim RT Box 1: 32 DACs + 32 ADCs), and three submodules with IGBTs (INFINEON IHW50N65R5XKSA1: 650 V, 80 A). For illustration, Fig. 15 presents a photo of the experimental prototype. Due to limited experimental conditions, we scaled down the grid voltage (i.e., $v_{\rm grid\_ref} = 110$ Vrms), nominal dc voltage (i.e., $v_{\rm dc\_ref} =$

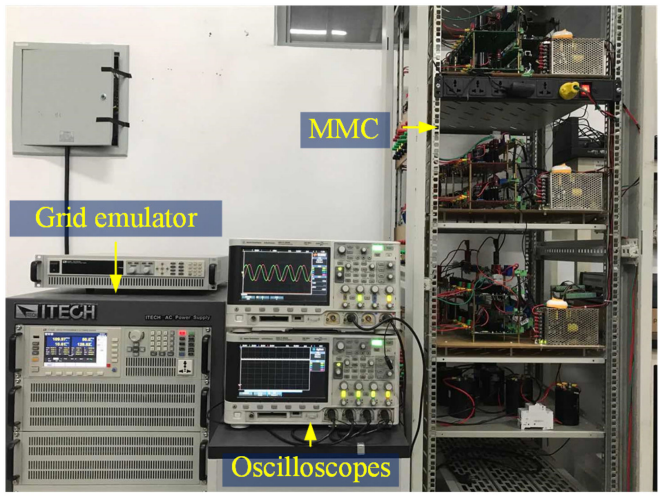

Fig. 15. Photo of the experimental prototype.

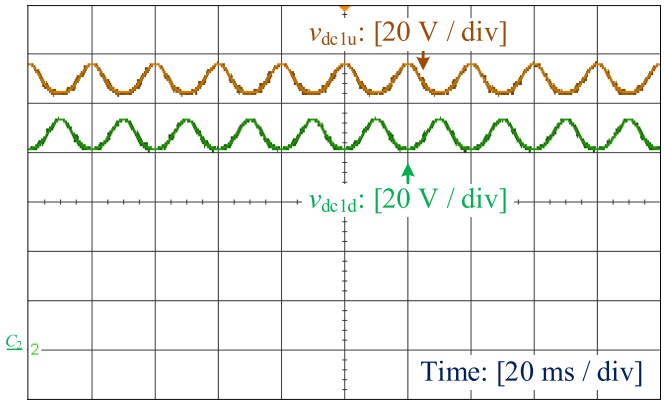

Fig. 16. Experimental results of conventional MMCs with three symmetrical half-bridge submodules.

100 V), and reactive current reference (i.e., $i_{\rm q\_ref} = 15$ Arms), as documented in Table II.

Fig. 16 shows the experimental waveforms of conventional MMCs with three symmetrical half-bridge submodules, where the first submodule has a 130 V initial voltage (which is 30 V greater than the nominal dc voltage 100 V). For clarity, only the voltages of the first submodule are shown. Noticeably, the voltage imbalance occurs with 14.4 V dc voltage ripples, as predicted by (12).

Fig. 17 illustrates the experimental results of MMCs with three symmetrical half-bridge submodules and the proposed strategy, where the initial voltages of all submodules remain unchanged as in those of Fig. 16. As shown, the proposed parallelization strategy addresses the voltage imbalance problem. Ideally, the voltage ripple should be reduced to 14.4/3 = 4.8 V according to (27). In practice, ON-state voltage drops as well as switch and capacitor ESRs slightly increase the voltage ripple. Nevertheless, the ripple reduction exceeds two times, thus demonstrating the capacitance saving effect.

Further, Fig. 18 demonstrates the experimental results of MMCs with two submodules, showing a case of an even number of submodules. Here, the number of submodules is reduced from

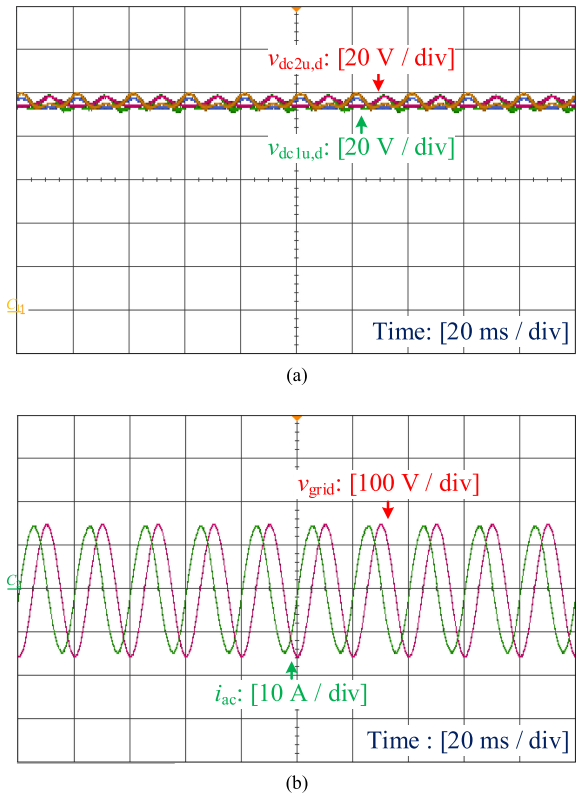

Fig. 17. Experimental results of MMCs with three symmetrical half-bridge submodules and the proposed submodule parallelization strategy. (a) Capacitor voltages. (b) Grid current and voltage.

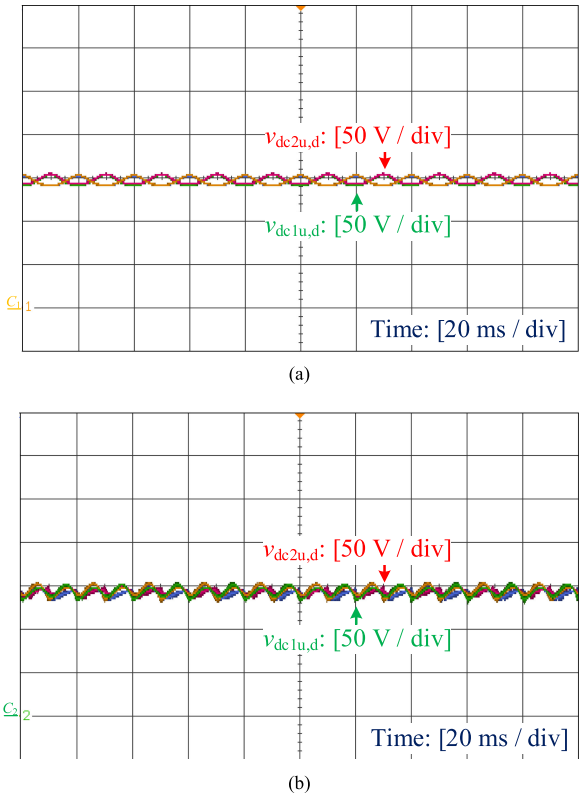

Fig. 18. Experimental results of MMCs with two symmetrical half-bridge submodules. (a) Conventional MMCs with $C_{dc} = 4.7$ mF. (b) MMCs with the proposed strategy and $C_{dc} = 940$ μF.

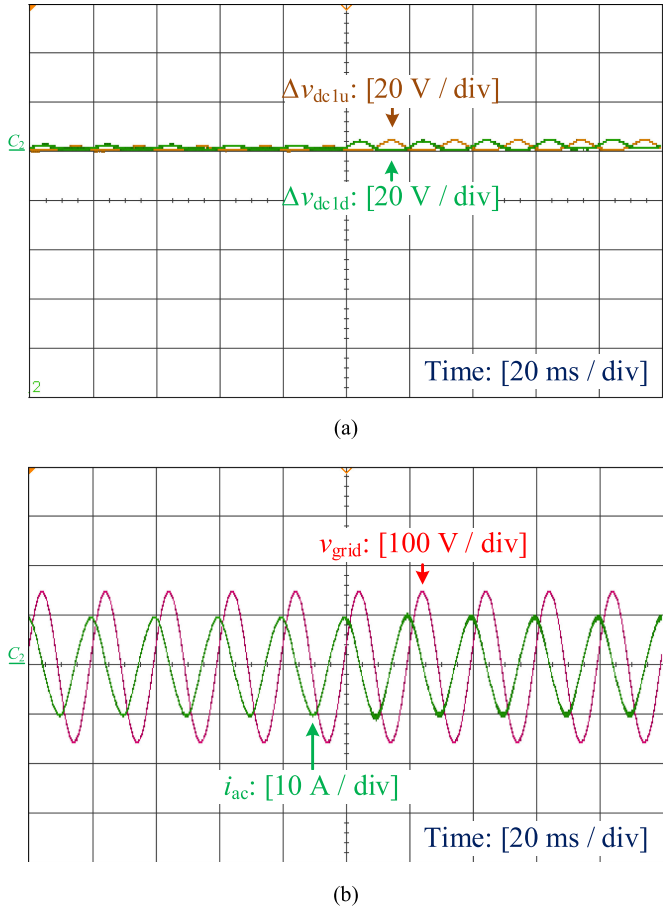

Fig. 19. Experimental results of MMCs' fault tolerant operation. (a) Capacitor voltages. (b) Grid voltage and current.

TABLE III
COMPARISONS BETWEEN THE CONVENTIONAL AND PROPOSED MMCS WITH SYMMETRICAL HALF-BRIDGE SUBMODULES

Descriptions	Conventional	Proposed
Submodule count	n	n
Capacitor count	$2n$	$2n$
Switch count	$2n$	$4n$
Voltage sensor count	$2n$	2
Voltage controller count	n	1
Fault tolerant operation	NA	Yes
Submodule capacitance	C_{dc}	n is odd: $= C_{dc}/n$
		n is even: $< C_{dc}/4$

4 (in simulations) to 2 due to available submodules. In this case, the proposed strategy achieves around five-time capacitance reduction.

Finally, Fig. 19 shows the fault-tolerant operation of MMC, where two abnormal submodules are bypassed again. Clearly, MMCs with the proposed strategy exhibit satisfactory dynamics during system faults.

In summary, Table III compares the proposed MMC with parallel connectivity (see Fig. 4) and the conventional MMC with symmetrical half-bridge submodules (see Fig. 2). Through comparison, it is easy to notice the benefits of the proposed MMC, including the removal of almost all voltage sensors, great simplification of control, fault tolerant operation, and significant reduction of capacitances.

VI. Conclusion

This article proposes a hardware-based submodule voltage balancing strategy for MMCs with symmetrical half-bridge submodules. The proposed strategy allows significant saving and reduction of dc capacitances, thereby allowing the reduction of system size, volume, and cost. Moreover, the proposed strategy balances dc capacitor voltages of individual submodules in a simple and reliable way, leading to the removal of voltage sensors and dedicated controllers. Control of the proposed circuits is easy and straight forward, where the relevant driving signals are readily available from existing ones. Additionally, the proposed strategy allows fault tolerant operation of MMCs. Finally, simulation and experimental results validate the proposed strategy applied to MMCs as STATCOMs.

References

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[2] J. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[3] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[4] L. Zhang, Y. Tang, S. Yang, and F. Gao, "Decoupled power control for a modular-multilevel-converter-based hybrid AC–DC grid integrated with hybrid energy storage," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2926–2934, Apr. 2019.

[5] F. Z. Peng and J. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509−517, May/Jun. 1996.

[6] S. M. Goetz, M. Pfaeffl, J. Huber, M. Singer, R. Marquardt, and T. Weyh, "Circuit topology and control principle for a first magnetic stimulator with fully controllable waveform," in *Proc. IEEE Annu. Int. Conf. Eng. Med. Biol. Soc.*, 2012, pp. 4700–4703.

[7] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel submodule connectivity: Topology and control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

[8] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, 1975.

[9] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.

[10] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE Power Electron. Specialists Conf.*, 1992, pp. 397–403.

[11] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *Proc. Conf. Rec. Eur. Conf. Power Electron. Appl.*, 2003, pp. 1–10.

[12] R. Marquardt, "Modular multilevel converters: State of the art and future progress," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 24–31, Dec. 2018.

[13] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[14] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[15] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. IEEE Int. Power Electron. Conf.*, 2010, pp. 502–507.

[16] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity—Application to battery systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017.

[17] J. Fang, Z. Li, and S. M. Goetz, "Multilevel converters with symmetrical half-bridge submodules and sensorless voltage balance," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 447–458, Jan. 2021.

[18] Y. Lo, C. Ho, and J. Wang, "Elimination of the output voltage imbalance in a half-bridge boost rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1352–1360, Jul. 2007.

[19] J. Fang, G. Xiao, X. Yang, and Y. Tang, "Parameter design of a novel series-parallel-resonant *LCL* filter for single-phase half-bridge active power filters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 200–217, Jan. 2017.

[20] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.

[21] V. S. Cheung, R. S. Yeung, H. S. Chung, A. W. Lo, and W. Wu, "A transformer-less unified power quality conditioner with fast dynamic control," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3926–3937, May 2018.

[22] J. Park, J. Kim, S. Park, and K. Kang, "DC voltage balancing control of half-bridge PWM inverter for linear compressor," in *Proc. IEEE Power Electron. Distrib. Gener. Syst.*, 2012, pp. 598–602.

[23] G. Farivar, B. Hredzak, and V. G. Agelidis, "Reduced-capacitance thin-film H-bridge multilevel STATCOM control utilizing an analytic filtering scheme," *IEEE Trans. Power Electron.*, vol. 62, no. 10, pp. 6457–6468, Oct. 2015.

[24] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 4, pp. 1419–1429, Sep./Oct. 2000.

[25] M. Su, X. Long, Y. Sun, and J. Yang, "An active power decoupling method for single-phase AC/DC converters," *IEEE Trans. Ind. Inform.*, vol. 10, no. 1, pp. 461–468, Jan. 2014.

[26] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[27] R. Wang, F. Wang, D. Boroyevich, and P. Ning, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1378–1383, May 2011.

[28] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855–1865, Apr. 2015.

[29] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.

[30] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[31] H. Wang, H. S. H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-Link capacitance in a capacitor supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.

[32] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A dual voltage control strategy for single-phase PWM converters with power decoupling function," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7060–7071, Dec. 2015.

[33] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.

[34] R. C. Dugan, M. F. McGranaghan, S. Santoso, and H. W. Beaty, *Electrical Power Systems Quality*. New York, NY, USA: McGraw-Hill, 2004, pp. 295–325.

[35] J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "On the inertia of future more-electronics power systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2130–2146, Dec. 2019.

[36] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[37] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[38] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.
[39] N. Tashakor, Z. Li, and S. Goetz, "A generic scheduling algorithm for low-frequency switching in modular multilevel converters with parallel functionality," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2852–2863, Mar. 2021.
[40] K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H. Nee, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3518–3527, Jul. 2015.
[41] N. Tashakor, M. Kilictas, J. Fang, and S. M. Goetz, "Switch-clamped modular multilevel converters with sensorless voltage balancing control," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2020.3028814.
[42] Aluminum Electrolytic Capacitors, [Online]. Available: https://www.digikey.com/, Accessed on: May 22, 2020.
[43] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.
[44] S. M. Goetz, C. Wang, Z. Li, D. L. K. Murphy, and A. V. Peterchev, "Concept of a distributed photovoltaic multilevel inverter with cascaded double H-bridge topology," *Int. J. Elect. Power Energy Syst.*, vol. 110, pp. 667–678, Sep. 2019.

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