Modelling and Compensation Design of Class-E Rectifier for Near-Resistive Impedance in High-Frequency Power Conversion

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***Abstract*—This article presents the investigation of circuit modelling, design, and optimization of the class-E rectifier to achieve a near-resistive impedance during a large load-range. Based on circuit modelling and impedance depiction, a circuit design concept of impedance compensation to achieve near-resistive impedance is proposed, and we selected the series inductor as the compensation network for class-E rectifiers. After an optimized design, a 6.78-MHz wireless power transfer prototype was built with applying the proposed concept and tested. The experimental results match well with the circuit modelling and validate the impedance shift can be optimized by the proposed circuit design concept. The experimental prototype achieves 87.2% dc–dc efficiency at the rated 220-W output and the phase angle shift is lower than 10° during the load decreasing from 220-W rated output to the 40-W light-load output. We also discuss the circuit design considerations and the hardware implementation of the prototype for the proposed design concept.**

***Index Terms*—Class-E rectifier, high-frequency power converters, resonant power converters, wireless power transfer (WPT) system.**

I. Introduction

RESONANT converters have been widely used in dc–dc power conversion with high-frequency (HF) operation [1]–[3]. A typical resonant dc–dc converter comprises an inverter, a resonant tank, and a rectifier, as illustrated in Fig. 1. With the operation frequency in MHz range, the benefits of a lower volume of magnetic components and the reduced voltage stress on capacitors can be achieved on resonant converters along with the rapid development of semiconductors. For instance, an inductive power transfer system as a typical resonant converter naturally benefits from the higher operation frequency, where the size and weight of the transmitter and receiver coils can be reduced simultaneously [4]–[7]. However, the converters' operation in MHz range brings more design challenges in topology selection, circuit design, hardware implementation, and output regulation [8]–[10].

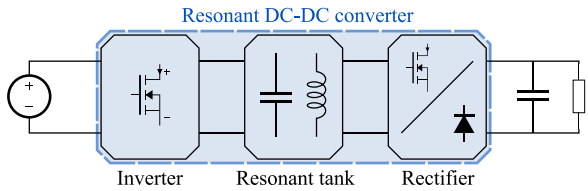

Fig. 1. General structure of a resonant dc–dc converter with a voltage source and a load.

Near-resistive impedance is a desirable feature for rectifiers in resonant converters, especially for higher power applications. Above all, the rectifier as a resistive impedance can minimize the reactive power delivered from the resonant tank and the inverter, thus the power loss due to the harmonic current can be minimized. In wireless power transfer (WPT) systems, the similar feature is usually called zero-phase angle (ZPA). Besides, achieving resistive impedance of rectifiers simplifies the design of the impedance matching for the inverters, where an inductive load is normally designed for an inverter to achieve the soft switching. In general, half-bridge and full-bridge rectifiers can perform as near-resistive impedance even with a variable resistive load. However, with the operation frequency further increased, the parasitic capacitors of semiconductors will shift the rectifiers' impedance to more capacitive, and this impedance shift varies with different resistive load. Consequently, the efficiency of the entire converter reduces and the soft switching of the inverter loses, which may lead to system failure from unpredictable hot spots and regulation invalidation. Though the past decade has seen the implementation of various topologies, including full-bridge [11], class-E [12], class-DE [13], [14], and class-EF [15] rectifiers into high-frequency/very high-frequency (HF/VHF) applications, the rectifier with a near-resistive impedance especially during a large load-range is still regarded as a design challenge for resonant converters. Especially, adding resonant matching network has been recognitzed an effective method to adjust the impedance for the resonant tanks and the rectifiers and several various topologies of the

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matching network can be found in [16]–[20] for resonant converters as well as in WPT systems. However, the solution also faces the challenges of the increasing number of components and complex design process, which significantly induce less power density, less efficiency, and more product delivery delay.

The class-E rectifier is an alternative in resonant converters and has been implemented in several HF/ VHF applications. One major advantage of this topology is that it can achieve low-voltage-derivation switching, which helps to reduce the switching loss and suppress the high-frequency ringing on the switches [21], [22]. Besides, the parasitic capacitance of the switch can work as part of the resonant capacitor and it further reduces the impedance shift from the parasitic parameters. Therefore, these superiority produces more reliability if the converter shifts from its rated operation from load shifting and also makes the system robust with components aging.

In general, in a class-E rectifier if the load shifts, its equivalent impedance will also shift correspondingly not only for the impedance's magnitude but also for its phase angle, which induces more power loss in the converter with a shifted load. In order to overcome the challenge, few investigations were reported to design a near-resistive class-E rectifier by parameter design or regulating the switches. In 2015, a design method to achieve near-resistive impedance of class-E rectifiers was reported in [13], where the phase-angle of input impedance of the rectifier is optimized by circuit design. In 2018, a load-independent class-E rectifier was reported by implementing an active switch (a MOSFET in this case) in the class-E rectifier as well as auxiliary phase-detection, controlling, and gate-driving circuit [23] and in [24] the detailed matchmatical model and a WPT demonstration can also be referred to with similar solution. Though these researches have been carried out on modifying the class-E rectifier for a near-resistive impedance, it is still complicated to model the impedance shifting during a large load range for the class-E rectifier. Moreover, a simplified and low-cost solution is still in demand, especially for its increasing applications in industry.

In this article, the study to design the passive near-resistive class-E rectifier during a large load-range is presented, including detailed circuit modelling, proposed circuit design concept of impedance compensation, a circuit optimization process, the hardware implementation, and the experimental validation. Verified by the experimental results, the near-resistive class-E rectifier is designed and built for HF power conversion with simplified circuit modification. Consequently, the proposed class-E rectifier is able to maintain a near-resistive impedance during a large load-range (below 10° phase-shift when the load power is changed from 220-W rated power to a very light load 40 W). Besides, the overall efficiency of the total system as well as the rectifier performs quite stable under the 6.78-MHz operation. In Section II, the circuit modelling of the class-E rectifier is introduced, by which the operation of class-E rectifier can be fully derived with given circuit parameters. Section III, first, gives a visualized depiction for the impedance shift of class-E rectifier during a large load-range. Then based on the impedance depiction, the circuit design concept of impedance compensation is proposed with modified circuit model. In Section IV, the case study to implement the proposed circuit design concept on a 220-W/ 6.78-MHz WPT system is presented along with a general parameter optimization algorithm and hardware implementation. In Section V, we provide the experimental validation and discuss several observation of our measurement results. Finally, Section VI concludes the article.

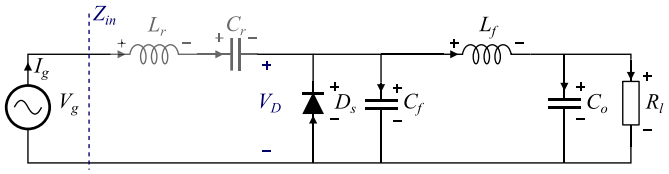

Fig. 2. Class-E rectifier with a driving source and a *LC* resonant tank (L_r and C_r operate in series resonance).

II. Time-Domain Modelling for the Class-E Rectifier

In this section, the numerical model of the class-E rectifier is derived with a driving source, as illustrated in Fig. 2. In the first place, the input impedance of the rectifier is defined as

$$Z_{\text{in}} = \frac{V_g}{I_g} \tag{1}$$

whose impedance angle is the major optimization target in this article and the V_g and I_g are the input voltage and the current of the rectifier, correspondingly.

In the modelling process, three assumptions are made for feasible simplification as follows.

1) The diode is regarded as an ideal unidirectional switch, which has zero forward voltage during the conduction and infinite impedance during the reversed bias.

2) All the inductors and capacitors have high enough quality factor thus their ESRs are neglected.

3) The resonant quality factor of the series resonant tank (including the L_r and C_r) is also high enough thus the driving current (I_g) of the rectifier is a purely sinusoidal waveform and it is defined as

$$I_g = i_g \sin(\omega t + \varphi) \tag{2}$$

where ω is the frequency of the driving current (given by $\omega = 2\pi f_s$ and f_s is the switching frequency) and φ is the phase shift of the current.

Correspondingly, the voltage of the rectifier is derived as same as the voltage of the switch (V_D), since the inductor L_r and the capacitor C_r operates in series resonance, as given in

$$V_g = V_{L_r} + V_{C_r} + V_D = V_D \tag{3}$$

where V_{L_r} is the voltage of the inductor L_r and the V_{C_r} is the voltage of the capacitor C_r.

The equivalent circuit during the operation as well as the key waveforms of the rectifier are given in Fig. 3. During the steady-state operation, one operation period consists of two subintervals: In the subinterval I (e.g., $2D\pi < \omega t < 2\pi$), the diode D_s turns ON thus its voltage and the current can be

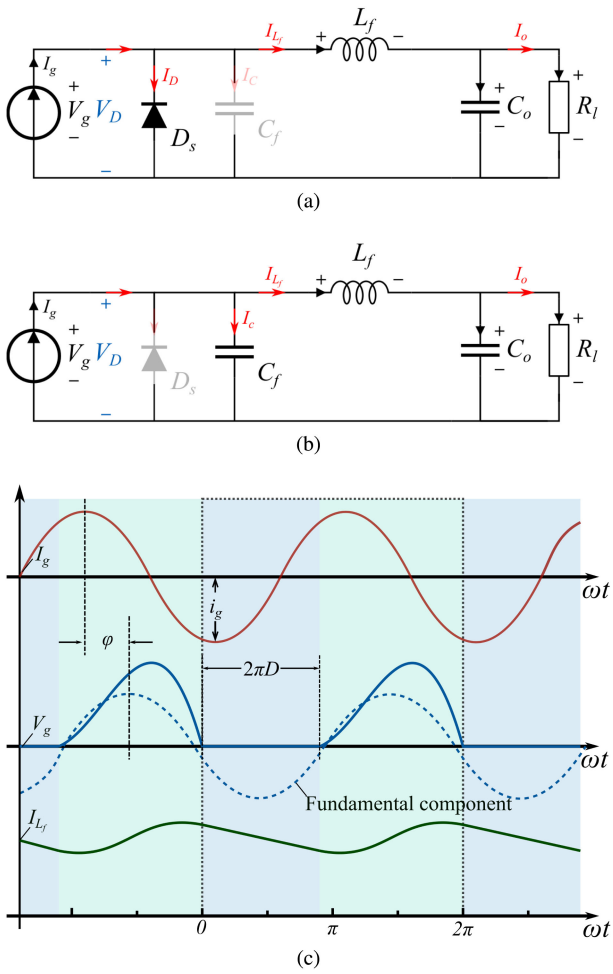

Fig. 3. Equivalent circuit model and key-waveforms of the current-driving class-E rectifier. (a) Circuit model in subinterval I, where diode D_s turns ON. (b) Circuit model in subinterval II, where diode D_s is in reverse bias. (c) Key-waveforms of the rectifier (not scaled; φ is the phase-shift between the fundamental component of the voltage V_D and the driven-current I_g).

described as

$$\begin{cases} V_D = 0 \\ I_D = I_{L,t=2D\pi} + \frac{V_o}{\omega L_f} \cdot (\omega t - 2D\pi) + i_g \sin(\omega t + \varphi) \end{cases} \tag{4}$$

where$D$ is the duty-cycle of the diode, and $I_{L,t=2D\pi}$ is the current of the inductor L_f, when $t = 2D\pi$.

In the subinterval II (e.g., $0 < \omega t < 2D\pi$), the diode D_s is in reversed bias while the capacitor C_f is resonant with L_f. And in this subinterval, the voltage and current of diode D_s is described as

$$\begin{cases} V_D = v_D(\omega t) \\ I_D = 0 \end{cases} \tag{5}$$

where the $v_D(\omega t)$ can be solved by

$$\omega C_f \cdot \frac{v_D}{\omega t} = \frac{1}{\omega L} \int_{D\pi}^{\omega t} (V_o - v_D) d\omega t + I_{L,t=2D\pi} + i_g \sin(\omega t + \varphi) \tag{6}$$

where V_o is the dc output voltage of the rectifier. It can be found that though the voltage of the switch V_D has been described, a numerical solution of V_D during the subinterval II is required to solve the input impedance of the rectifier. This derivation of the V_D will be give as follows.

Differentiating both sides of (6) gives

$$\frac{1}{q^2} \frac{d^2 v_{Dn}}{d\omega t^2} - p \cdot \cos(\omega t + \varphi) + v_{Dn} - 1 = 0 \tag{7}$$

where v_{Dn} is the normalized voltage of the switch, defined as

$$v_{Dn} = \frac{v_D}{V_o} \tag{8}$$

where the V_o is the output dc voltage on the load R_l and two key factors q and p are defined as

$$q = \frac{1}{\omega \sqrt{L_f C_f}} \tag{9}$$

$$p = \frac{i_g \omega L_f}{V_o}. \tag{10}$$

Then, the general solution for (6) can be derived as

$$v_{Dn}(\omega t) = 1 + \xi_1 \cos(q\omega t) + \xi_2 \sin(q\omega t) - \xi_3 \cos(\omega t + \varphi) \tag{11}$$

where ξ_1, ξ_2, and ξ_3 are the coefficients related to the parameters of the rectifier. Particularly, ξ_3 is given by

$$\xi_3 = \frac{q^2 p}{1 - q^2}. \tag{12}$$

In order to solve the other two coefficients ξ_1 and ξ_2 in (11), two boundary conditions, where the switch must achieve zero-voltage switching (ZVS) and zero-current switching (ZCS) turn-OFF as a diode, are given as

$$v_{Dn}(2\pi D) = 0 \tag{13}$$

$$\left. \frac{dv_{Dn}(\omega t)}{d\omega t} \right|_{\omega t = 2\pi D} = 0. \tag{14}$$

Then, the ξ_1 and ξ_2 can be derived as

$$\begin{aligned} \xi_1 = \xi_3 [&\cos(2\pi D \cdot q) \cos(\varphi + 2\pi D) + \\ &\frac{1}{q} \sin(2\pi D \cdot q) \sin(\varphi + 2\pi D \cdot q)] - \cos(2\pi D \cdot q) \end{aligned} \tag{15}$$

$$\begin{aligned} \xi_2 = \xi_3 [&\cos(2\pi D \cdot q) \cos(\varphi + 2\pi D) - \\ &\frac{1}{q} \sin(2\pi D \cdot q) \sin(\varphi + 2\pi D \cdot q)] - \sin(2\pi D \cdot q). \end{aligned} \tag{16}$$

Until (16), three coefficients p, φ, and D are still needed to solve to get a solution of V_D, while the other three constraint equations can be used as follows.

a) The volt-second balance of L_f given by

$$\int_{2\pi D}^{2\pi} v_{Dn} d\omega t = 2\pi. \tag{17}$$

b) The energy conservation condition given by

$$p_r \cdot p \cdot \int_{2\pi D}^{2\pi} v_{Dn} \cdot \sin(\omega t + \varphi) d\omega t = 2\pi \tag{18}$$

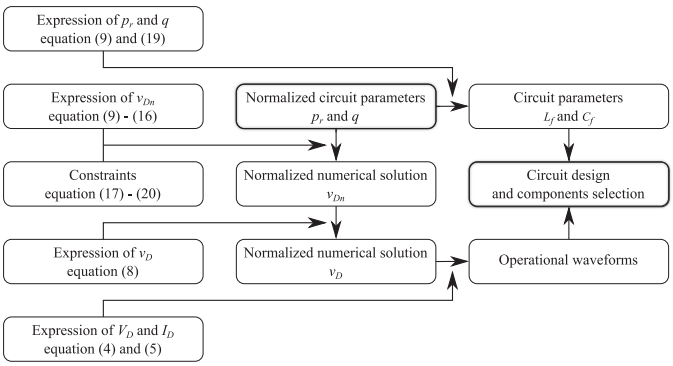

Fig. 4. Numerical model structure for the class-E rectifier.

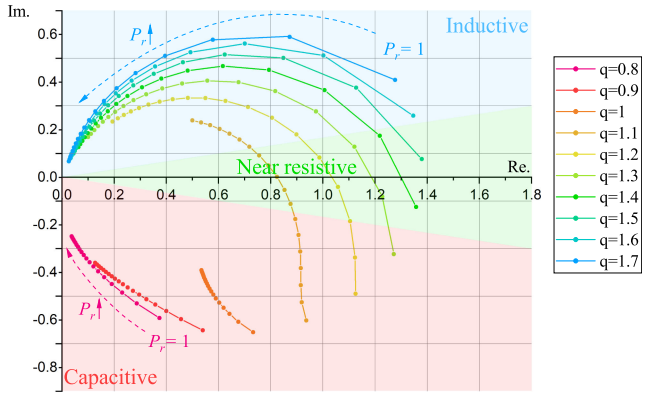

Fig. 5. Normalized impedance plot of the class-E rectifier during a large-load range. The complex plane is generally divided in to three regions (near-resistive region, inductive region, and capacitive region) and a line in same color represents a specific design with normalized L_f and C_f.

where p_r is the load factor defined as

$$p_r = \frac{R_l}{\omega L_f} \tag{19}$$

which is related to the output power and the R_l is the load resistance.

c) The diode turns ON with ZVS condition at $\omega t = 2\pi$ gives

$$v_{Dn}(2\pi) = 0. \tag{20}$$

As a result, the three state variables ξ_1, ξ_2, and ξ_3 can be solved numerically by combining the three constraint equations (17)–(20) and presetting the circuit parameters q and p_r. The normalized input current is defined as

$$i_{\text{inn}} = p \cdot p_r \cdot \sin(\omega t + \varphi). \tag{21}$$

Then, the input impedance of the rectifier

$$Z_{\text{in}} = Z_{\text{inn}} \cdot R_l \tag{22}$$

can be obtained by dividing the fundamental harmonic of input voltage and current as

$$Z_{\text{inn}} = \frac{\int_{2\pi D}^{2\pi} v_{Dn}\left[\sin(\omega t + \varphi) + j \cdot \cos(\omega t + \varphi)\right] d\omega t}{\int_0^{2\pi} i_{\text{inn}} \cdot \sin(\omega t + \varphi) d\omega t} \tag{23}$$

where the Z_{inn} is the normalized input impedance of the rectifier.

At this point, the numerical model of the operation for a class-E rectifier is derived: With a specific circuit design (a pair of design parameters q and p_r), both the voltage and current waveforms of the diode D_s, as presented in (4)–(20), and the impedance of the rectifier, as presented in (23), can be found with normalized parameters. In Fig. 4, a structure for the numerical model of the class-E rectifier is given to connect the design parameters (q and p_r) to the operation waveform of the rectifier and this illustration indicates that the selection of q and p_r actually determines the performance of the rectifier.

III. Impedance Shifting Depiction During a Large Load-Range and the Impedance Compensation Concept

Based on the numerical model of the class-E rectifier in Section II, the impedance of the class-E rectifier is found as nonlinear dependence with the load, which makes it difficult to qualify impedance shifting with the changing of the load. In this section, first the normalized impedance shifting was illustrated with the shifted load, which visually indicates that a near-resistive class-E rectifier cannot be designed only with parameters optimization. Afterwards, the concept by using series impedance network to compensate the class-E rectifier is proposed to build the near-resistive class-E rectifier. In this article, the compensation is achieved by a series inductor and the numerical analysis is given as well.

A. Impedance Shift of Class-E Rectifier During a Large-Load Range

In Section II, two factors, q and p_r, are defined in the normalized numerical model of the class-E rectifier. It is important to highlight that with a pair of specific q and p_r value, a stated circuit has already been defined with corresponding components values, including L_f, C_f, and dc load R_l. In particular, the factor q being a constant while the factor p_r shifting means that the dc load changes because the value of L_f and C_f normally is fixed during converters' operation. In this section, the load range is swept from the p_r =1 to the $p_r = 10$ on the class-E rectifier to depict the operation from the rated load to the light load as a general observation.[1]

In Fig. 5, the normalized impedance of class-E rectifier is plotted on the complex plane and based on the plot, several observations can be concluded as follows.

a) With a series of specific circuit parameters, the impedance shifting performs nonlinearly with the change of the dc load: Both the norm and the angle of the impedance would shift nonlinearly when the load shifts from $p_r = 1$ to $p_r = 10$.

b) The factor q directly determines the impedance location on the complex plane.

[1]As described in (19), the p_r only represents a ratio between R_l and ωL_f, thus the rated dc load may be defined arbitrarily. E.g., the $p_r = 10$ can also be set as rated dc load and, correspondingly, $p_r = 50$ will indicate the load is one-fifth of the rated load. The similar impedance shift can be observed with different p_r range.

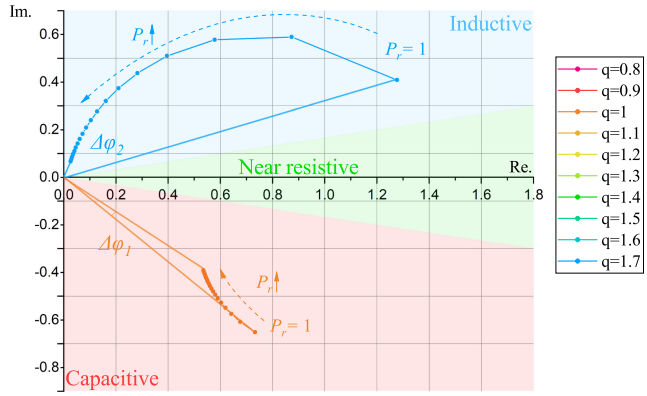

Fig. 6. Normalized impedance plot of the class-E rectifier when factor $q = 1$, and $q = 1.7$: $\Delta\varphi_1$ is the phase angle difference between rated load ($p_r = 1$) and the light load ($p_r = 10$) when $q = 1$ while $\Delta\varphi_2$ is the phase angle difference between rated load ($p_r = 1$) and the light load ($p_r = 10$) when $q = 1.7$.

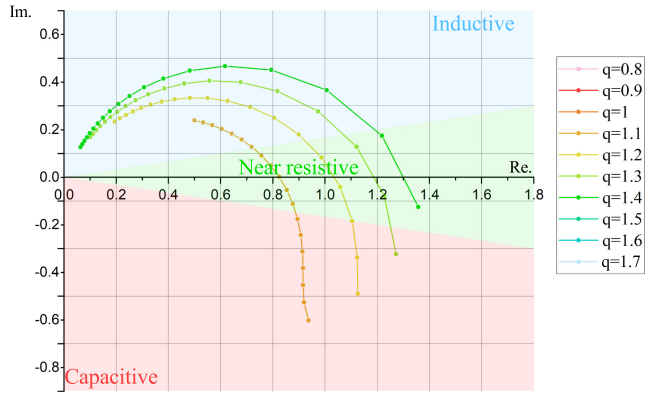

Fig. 7. Normalized impedance plot of the class-E rectifier when factor $q = 1.1$ to 1.4.

c) Only by circuit design (selecting the proper q), it is hard to build a near-resistive class-E rectifier, which further confirms the in-adaptability of class-E rectifier for the application with a large load range.

Fig. 6 depicts the impedance plot when factor the q is 1 and when the factor q is 1.7. These two curves indicates that with specific factor q, the rectifier's impedance can be designed as either capacitive or inductive. When factor $q = 1$, all the impedance performs capacitive and the corresponding phase shift $\Delta\varphi_1$ from full load to the light load is quite small. On the contrary, when factor $q = 1.7$, the all impedance performs inductive while the the corresponding phase shift $\Delta\varphi_2$ from full load to the light load is relatively large. Even though the inductive impedance may be preferable when topology of the inverters are bridge-type, the large phase shift will bring a large harmonic current as well as induced power loss for the converters.

In Fig. 7, the impedance plots when factor $q = 1.1$ to 1.4 are presented, where some of the impedance performs near-even pure-resistive. Nevertheless, the near-resistive impedance cannot be achieved by the class-E rectifier during the whole load range. In [12], similar design guideline can be found and

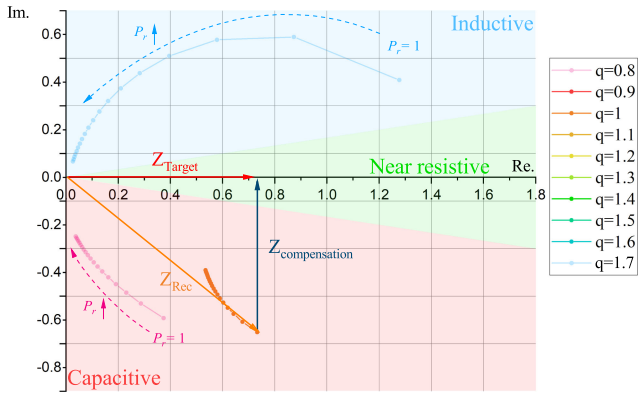

Fig. 8. Illustration of the impedance compensation concept: the rectifier's impedance in orange is compensated by an inductive impedance in dark blue. Thus, a pure-resistive impedance is finally achieved by the rectifier.

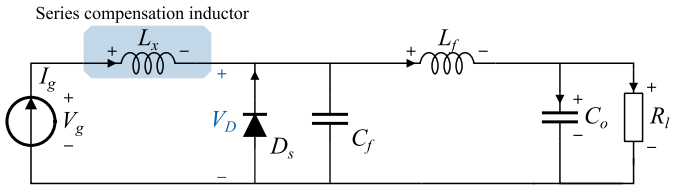

Fig. 9. Topology of class-E rectifier with proposed series inductor's compensation.

the factor $q = 1.32$ is recommended as an optimized design reference.

B. Compensation Concept of Building a Near-Resistive Class-E Rectifier

With the observation that the impedance performs nonlinear and a near-resistive impedance is hard to achieve during the load range, it is naturally proposed that the resistive/ inductive impedance can be compensated by another series impedance network to achieve a resistive input impedance of the rectifier. In Fig. 8, an illustration of the impedance compensation concept is provided. In the illustration, the original design is selected with the factor $q = 1$; thus, the compensation can be achieved by a series inductive impedance. Correspondingly, in the impedance plot, a pure-resistive impedance (in red) is depicted by the original capacitive impedance (in orange) added to an inductive impedance (in dark blue), where the impedance compensation concept is illustrated.

In this article, we select a series inductor (as shown in Fig. 9) as the compensation network for it intrinsically matches the capacitive impedance of class-E rectifiers with a small phase shift during the load range. In order to build the normalized impedance model for the compensated class-E rectifier, an inductance factor p_x is defined as

$$p_x = \frac{L_x}{L_f}. \tag{24}$$

where L_x is the inductance of the series compensation inductor, and the normalized impedance of the rectifier after compensation

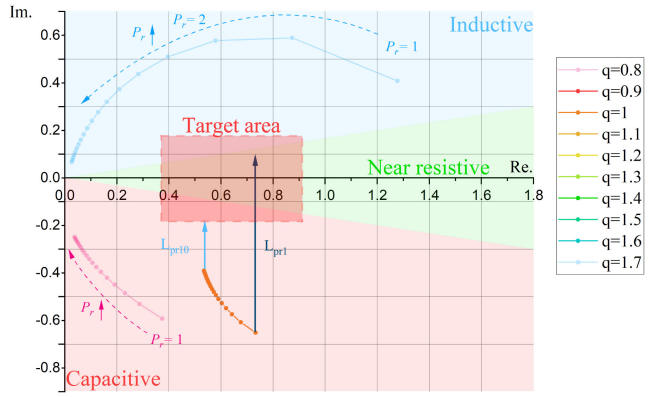

Fig. 10. Illustration of the impedance compensation concept with a series inductor: L_{pr10} is the normalized impedance of the series inductor at the light load ($p_r = 10$); L_{pr1} is the normalized impedance of the series inductor at the light load ($p_r = 1$). Though the practical inductance of the series inductor is constant, the corresponding normalized inductance should be scaled by following the p_r value.

TABLE I
PHASE SHIFT COMPARISON WITH/ WITHOUT THE IMPEDANCE COMPENSATION

	With compensation			Without compensation		
p_r	q	p_x	$\Delta\varphi(^\circ)$	q	p_x	$\delta\varphi(^\circ)$
0.1 - 1.0	1.459	0.076	7.6	1.634	0	17.4
0.2 - 2.0	1.257	0.160	9.0	1.372	0	21.6
0.3 - 3.0	1.177	0.238	9.7	1.266	0	24.0
0.4 - 4.0	1.133	0.313	10.0	1.208	0	25.5
0.5 - 5.0	1.104	0.383	10.1	1.171	0	26.6
0.6 - 6.0	1.086	0.449	10.1	1.145	0	27.4
0.7 - 7.0	1.073	0.508	10.1	1.126	0	28.3
0.8 - 8.0	1.063	0.566	10.0	1.111	0	28.5
0.9 - 9.0	1.055	0.625	9.9	1.098	0	28.9
1.0 - 10.0	1.049	0.680	9.9	1.089	0	29.2

can be calculated as

$$Z_{\text{inn}} = \frac{\int_{2\pi D}^{2\pi} v_{Dn}\left[\sin(\omega t+\varphi)+j\cdot\cos(\omega t+\varphi)\right]d\omega t}{\int_{0}^{2\pi} i_{\text{inn}}\cdot\sin(\omega t+\varphi)d\omega t} + j\frac{p_x}{p_r} \tag{25}$$

It is noticed that with the a constant compensation inductance (p_x is a constant), in the impedance illustration Fig. 10, the normalized impedance shifts from the inductance have different scales (on the complex plane means different length) under different p_r value. For example, the impedance shift of a specific p_x at light load ($p_r = 10$) is ten times of the impedance shift at the rated power ($p_r = 1$). Correspondingly, as illustrated, in the complex plane, the length of the vector (L_{pr1}) is longer than the vector L_{pr10} if a fixed inductor is used as compensation in the practical circuit. Consequently the impedance of a series inductor after scaling in the complex plane matches well with the original impedance curve of the class-E rectifier during a large load-range, especially when the factor q is in the range from 0.9 to 1.1. In addition, another advantage of the design concept for class-E rectifiers is that the rectifier is usually connected in series with the resonant tank, where the inductor may be integrated into the resonant tank, rather than implemented by extra magnetic components.

In Table I, a comparison between applying the impedance compensation and without the compensation during a large load-range for the class-E rectifier is given, which validates the proposed concept is able to reduce the phase-angle difference of the rectifier. All the parameters in this comparison is after an optimization process by parameters sweeping and the optimized value are selected to present. Though the parameters sweeping may provide a optimized circuit design, it is still very time-consuming and cannot adapt to all the design specifications.

IV. CASE STUDY OF OPTIMAL CIRCUIT DESIGN AND HARDWARE IMPLEMENTATION

In Section III, the circuit design concept, the impedance of class-E rectifier can be compensated by an impedance network as a near-resistive one, is proposed. Particularly, an series inductor is selected as the compensation network and validated for its impedance modification capability. Nevertheless, the selection of circuit parameters (including L_f, C_f, and L_x) is still the design challenge for different specifications. In this section, a circuit design process and the design considerations of the compensated class-E rectifier with near-resistive impedance are discussed along with the hardware implementation.

A. Circuit Design Process for the Class-E Rectifier

In the beginning, the design targets in the case study are defined as follows.

1) At the rated load, the impedance of the rectifier should be pure-resistive to achieve the minimal reactive power in the entire converter.
2) The phase shift from the rated load to the light load should be minimized with the compensated series inductor.

And, the design specifications of the rectifier are set as follows.

1) The load range is from rated load to the ten times of the rated power (which defined by a factor N_L= 1–10).
2) The rated power of the rectifier is 110 W and the output voltage is 48 V. The switching frequency is set as 6.78 MHz.

The general illustration of the design process is presented in Fig. 11. The detailed design will be introduced step by step.

1) *Select Rated Load Factor p_{r0}:* As mentioned when defining the factor p_r by (19), the p_r only means the ratio between the impedance of the L_f and load resistance R_l. Thus the p_r factor with different sweeping range (e.g., p_r is shifted from 0.1 to 1, or is shifted from 1 to 10) may represent the same load range (from rated load to ten times that of the rated load). On this condition, a factor p_{r0} is defined as

$$p_{r0} = \frac{L_f}{R_l,\text{rated}} \tag{26}$$

which gives a specific value of L_f.
In this design, the selection of p_{r0} is based on the voltage stress on diode D_S and the current stress of inductor L_f. In Fig. 12, the voltage stress and the current stress are depicted with the sweeping of the factor p_{r0} and the factor q. It is noticed that with the increase of the factor p_{r0},

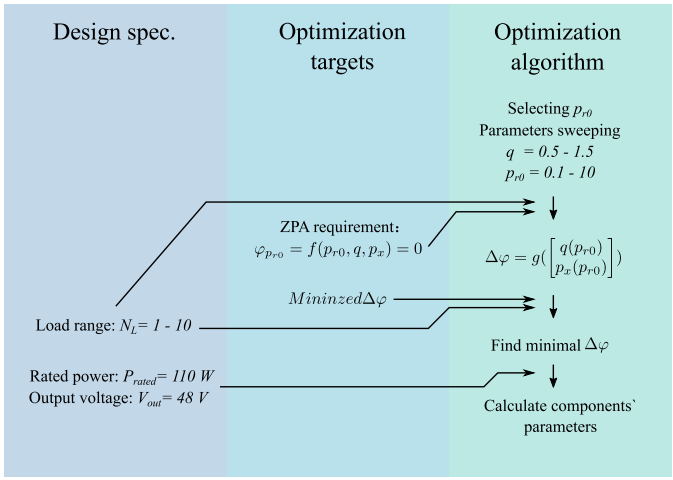

Fig. 11. Circuit design process with applying the proposed circuit design concept.

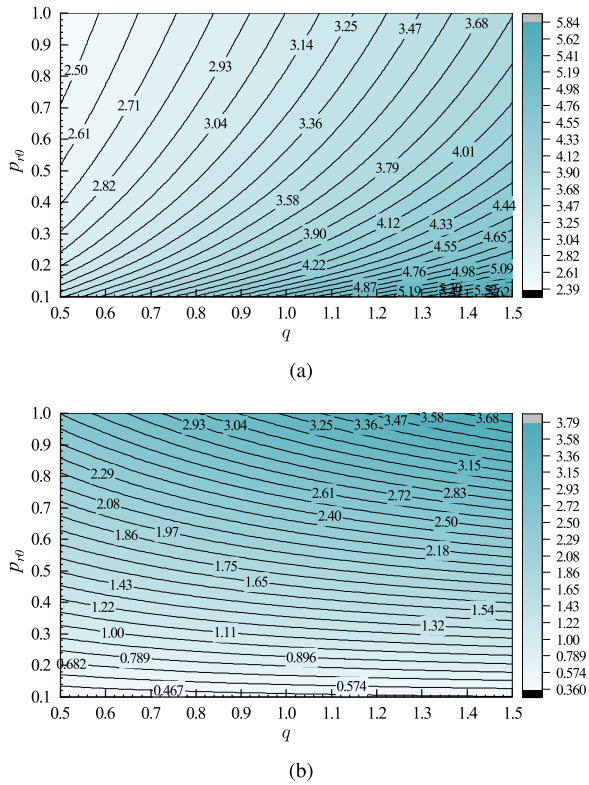

Fig. 12. Illustration of the normalized voltage stress of diode D_s and current stress on inductor L_f as functions of p_{r0} and q when $N_L = 1$–10. (a) Voltage stress depiction. (b) Current stress depiction (the factors are normalized by output voltage V_o or output current I_o).

the voltage stress will decrease, which mainly determines the diode selection; while the current stress will increase, which mainly determines the conduction loss on the inductor. In addition, the voltage stress of the diode D_s is also the voltage stress of the paralleled capacitor C_f, which may be another limitation during the hardware implementation.

In this design, the p_{r0} is selected as 0.5 by the tradeoff between the voltage and the current stress on the rectifier.

2) *Applying the ZPA Constraint*: After selecting p_{r0}, the optimization equation can be defined as

$$\Delta\varphi_{N_L=1-10,p_r=0.5-5} = f(q, p_x) \tag{27}$$

where the range of factor p_r has been defined. In the next step, the dimension of the optimization equation should be further reduced by the constraint as

$$\varphi_{p_r=0.5} = C(q, p_x) = 0. \tag{28}$$

Then, the optimization equation can be further simplified as

$$\Delta\varphi_{N_L=1-10,p_r=0.5-5} = g(\begin{bmatrix} q \\ p_x \end{bmatrix}). \tag{29}$$

3) *Find the Combination of q and p_x to Minimize the Phase Shift During the Load Range*: As shown in (29), now the phase shift during the load range is a one-variable function and the normalized optimization results (the combination of p_r, q, and p_x) corresponding to the load range from rated load to light load in ten times of the rated load impedance can be found by searching the solution with the minimal function value. In this design, the normalized solution was found as

$$\begin{bmatrix} p_{r0} \\ q \\ p_x \end{bmatrix} = \begin{bmatrix} 0.5 \\ 1.115 \\ 0.292 \end{bmatrix}. \tag{30}$$

4) *Calculate the Circuit Parameters Based on Design Specifications*: Finally, the circuit design parameters after optimization is given as

$$\begin{bmatrix} L_f \\ C_f \\ L_x \end{bmatrix} = \begin{bmatrix} 983nH \\ 451nF \\ 287nH \end{bmatrix}. \tag{31}$$

B. Hardware Implementation

The proposed design was implemented on a WPT system, which is a typical resonant converter, to experimentally validate the proposed circuit design concept. The entire WPT system consists of a differential class-E inverter, the inductive coupler with *LCC*-S compensation and a differential class-E rectifier, as illustrated in Fig. 13. The differential structure, where two identical inverters or rectifiers are connected in parallel at the dc port and they operate normally with 180° phase-shift, is able to distribute the transferred power equally into two phases. The detailed configuration and operational principle of the differential class-E inverter/rectifier (also known as push–pull structure) can refer to [25]–[27]. With the differential strucuture as shown in Fig. 13, the rated power of the prototype is set as 220 W and the output voltage is 48 V for a virtual battery charging application while the 110-W design of class-E rectifier can be directly implemented.

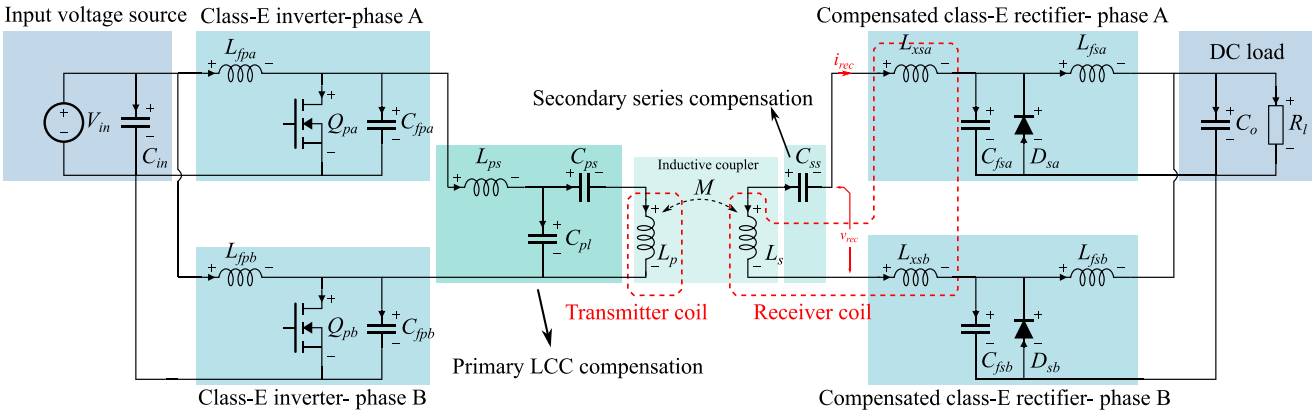

Fig. 13. Topology of WPT systems based on the proposed near-resistive class-E inverter and rectifier.

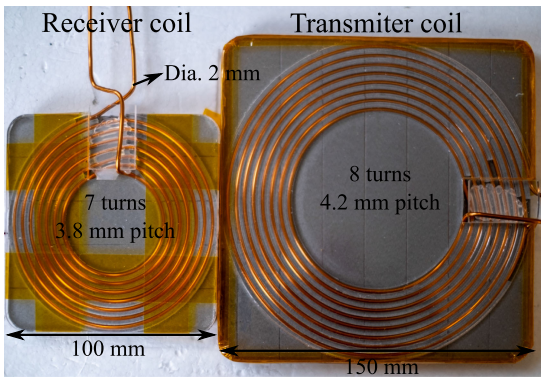

Fig. 14. Size and winding configuration of the coupled coils for the prototype.

TABLE II
CIRCUIT PARAMETER OF THE INVERTER AND THE INDUCTIVE COUPLER

	Parameter	Value *
Inverter	L_{fpa}/L_{fpb}	644nH
	C_{fpa}/C_{fpb}	513nF
	Q_{pa}/Q_{pb}	TP65H070LDG
Inductive coupler	L_{ps}	2.01μH
	C_{pl}	322.7pF
	C_{ps}	63.3pF
	L_p	9.81μH
	$L_s + L_{xsa} + L_{xsb}$	4.13μH
	M	1.70μH
	C_{ss}	145pF

*Measured by impedance analyzer 4294 A; L_p is the self-inductance of the transmitter coil; $L_s + L_{xsa} + L_{xsb}$ is the self-inductance of the receiver coil; M is the mutual-inductance between the transmitter and the receiver coil with distance of 30 mm.

1) Differential Class-E Inverter and the Inductive Coupler: In this design the differential class-E inverter is selected to convert the power from the dc input of the system to an ac power. Generally, two identical class-E inverters are connected in parallel and the gate driving signals are given with 180° phase shift to drive the class-E inverter. In terms of the inductive coupler, we chose the *LCC*-S compensation for the coupled coils to maintain a constant voltage gain from the input to the output of the inductive coupler [28], [29]. In order to achieve the constant voltage gain feature, the inductive coupler's parameters are selected based on

$$\omega = \frac{1}{\sqrt{L_{\text{ps}} C_{\text{pl}}}} = \frac{1}{\sqrt{L_p \frac{C_{\text{ps}} C_{\text{pl}}}{C_{\text{ps}} + C_{\text{pl}}}}} = \frac{1}{\sqrt{L_s C_{\text{ss}}}} \tag{32}$$

where $L_{\text{ps}}, C_{\text{pl}}, C_{\text{ps}}$, and C_{ss} are the inductor and capacitors as compensation and L_p is the self-inductance of the transmitter coil, as shown in Fig. 13. In particular, the value L_s is calculated by the self-inductance of the receiver coil minus L_{xsa} and L_{xsb} due to a integration structure used in the prototype, which will be introduced in the hardware implementation of the rectifier. In Fig. 14, the size and the winding configuration of the coupled coils are given as the reference. Besides, the detailed circuit parameters of the inverter and the inductive coupler are presented in Table II.

2) Differential Compensated Class-E Rectifier: Similar to the inverter, a differential structure was also used for the rectifier on the prototype. By following the previous optimized circuit parameters, the prototype of the rectifier are also built with two major design considerations.

a) Merge output capacitors of the diodes: It is known that the output capacitors of the diodes intrinsically exist and perform nonlinear with different voltage stress. Normally for a class-E inverter/rectifier, the designers prefer to selected a large C_f value (typically as more than ten times of the output capacitance) to merge the output capacitance. However, on a rectifier working at MHz range frequency, the C_f value may be as a similar amount of the output capacitance of the diodes, which makes it impossible to merge the output capacitance by circuit design. In this design, the C_{fsa} and C_{fsb} is physically implemented by the output capacitors of the diodes and several separate ceramic capacitors, whose value is selected by

$$C_{ex} = C_f - C_{D,E,\text{eq.}}(V_{D,\text{stress}}) \tag{33}$$

where the C_f is the previous optimized value (451 pF) and $C_{D,E,\text{eq.}}(V_{D,\text{stress}})$ is the energy-equivalent capacitance when $V_{D,\text{stress}}$ is the maximum reverse-bias voltage of the diode at the

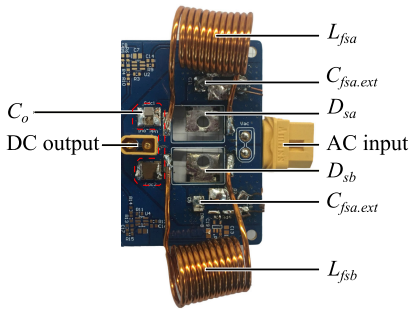

Fig. 15. Photo of the prototype: the differential near-resistive class-E rectifier.

rated load, which can be calculated by

$$C_{D,E,\text{eq.}}(V_{D,\text{stress}}) = \frac{2 \cdot \int_0^{V_{D,\text{stress}}} v \cdot C_{\text{oss}}(v)\mathrm{d}v}{V_{D,\text{stress}}^2} \tag{34}$$

In this design, the C_{oss} as a function of the reverse-bias voltage of the diode is gotten by the curve fitting from the data sheet.

b) Integrate L_x into the inductive coupler: In Fig. 13, it is noticed that on the receiver side, the compensation inductors L_{xsa} and L_{xsb} are connected in series with the receiver coil, which indicates that compensation inductors can be integrated, rather than adding extra components during the implementation. In this design, the integration is implemented by selecting the secondary series compensation capacitor C_{ss}, as indicated in (32), which naturally benefits with the size and cost reduction.

Finally, the detailed circuit parameters of the compensated class-E rectifier is given in Table II and the rectifier's prototype is shown in Fig. 15.

V. Experimental Results and Discussion

The prototype of the 6.78-MHz WPT system with proposed near-resistive class-E rectifier was tested, during which the dc load was shifted from rated load (220 W at 48 V output) to a very light load (20 W at 48 V output).

In Fig. 16, the measured waveforms of the prototype are presented. Fig. 16(a) provides the waveforms of voltage on two diodes and the driving current of the rectifier operating under rated load (220-W output power). It is noticed that the voltage waveforms of the diodes between two phases are almost identical only with a 180° phase shift and the driving current performs as a sinusoidal waveform. Nevertheless, as shown in Fig. 16 (b) when the output power was adjusted to 100 W, the driving current is slightly distorted away from a pure sinusoidal waveform. Furthermore, under a very light load condition shown in Fig. 16(c), the two phases of the rectifier are observed to be significantly unbalanced, and the driving current was much distorted, which may not fit the assumptions of the circuit model in Section II. In addition, at each load condition, the voltage stress on the diode is observed to be higher than the expectation, e.g., at rated 220-W output, the expected voltage stress is 178 V while its measured value is 205 V. These voltage stress shifting is mainly related to the nonlinearity of the output capacitor for

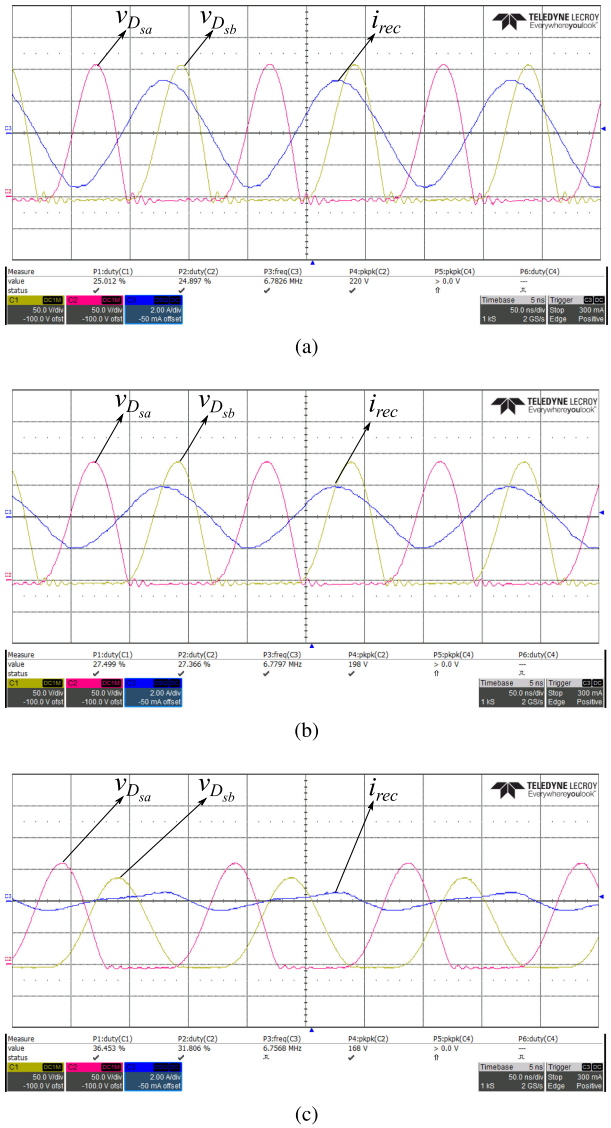

Fig. 16. Measured waveforms of the rectifier under different loads. (a) $P_{\text{o}} = 220$ W (b) $P_{\text{out}} = 100$ W. (c) $P_{\text{out}} = 20$ W (Scales: 50 V/ div. and 2 A/div.).

diodes, which indicates that a design margin of the voltage stress must be considered during the components' selection.

The comparison of the impedance and phase angle of the rectifier between the measurement and the calculated results based on the model from Section II, is given in Table IV. On account of the compensated inductors were integrated into the receiver coil, the voltage of the rectifier cannot be directly measured. Thus, in order to acquire the impedance of the rectifier, first the driving current (i_{rec}) of the rectifier was obtained by calculating the fundamental component of measured current on the secondary coil; subsequently, the voltage of the rectifier can be calculated by

$$v_{\text{rec}} = [v_{D_{sa}} - v_{D_{sb}}]_{\text{Fund. component}} + 2 \cdot i_{\text{rec}} \omega L_x. \tag{35}$$

Then, the equivalent impedance of the rectifier can be calculated by using the v_{rec} divided by i_{rec} at different load conditions.

TABLE III
PARAMETERS OF THE DIFFERENTIAL CLASS-E RECTIFIER OF THE PROTOTYPE

Parameter	Value	Description
L_{fsa}	996nH *	ESR = 253mΩ* Wire-wound air-core 12 turns with outer dia. = 17mm
L_{fsb}	1004nH*	ESR = 262mΩ* Wire-wound air-core 12 turns with outer dia. = 17mm
D_{sa}/D_{sb}	C3D10060A	600 V SiC Schottky Diode
C_{fsa}/C_{fsb}	441pF	2· 100pF separate ceramic cap. from ATC 800R series plus $C_{D,E,eq.}$ = 241pF
L_{xsa}/L_{xsb}	322.7pF	Integrated in the receiver coil
C_o	2.022μF	Ceramic capacitors
R_l	Electric load	/

*Measured by impedance analyzer 4294 A;

TABLE IV
MEASUREMENT/ CALCULATION RESULTS OF IMPEDANCE AND PHASE ANGLE FOR THE RECTIFIER

$P_{out}(W)$	Z_{in} cal.(Ω)	Z_{in} meas. (Ω)	φ cal.(°)	φ meas. (°)
220	43.01	48.12	0	-1.13
200	46.85	53.04	-2.41	-3.33
180	51.62	57.69	-4.75	-4.61
160	57.65	64.29	-6.98	-6.29
140	65.47	72.93	-9.13	-7.86
120	75.96	84.03	-10.80	-9.06
100	90.68	103.94	-12.09	-9.25
80	112.74	124.21	-12.53	-0.08
60	149.20	158.18	-11.23	-6.07
40	219.71	221.54	-5.49	2.71
20	385.53	288.34	16.42	29.56

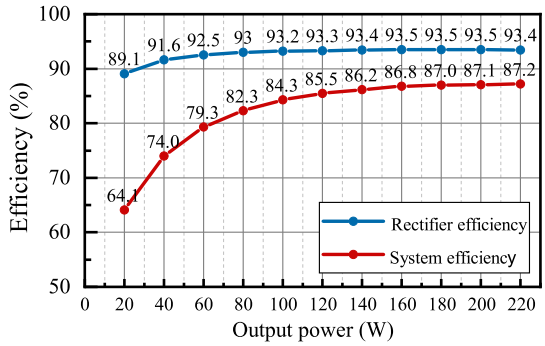

Fig. 17. Rectifier and system efficiency of the 6.78-MHz WPT prototype.

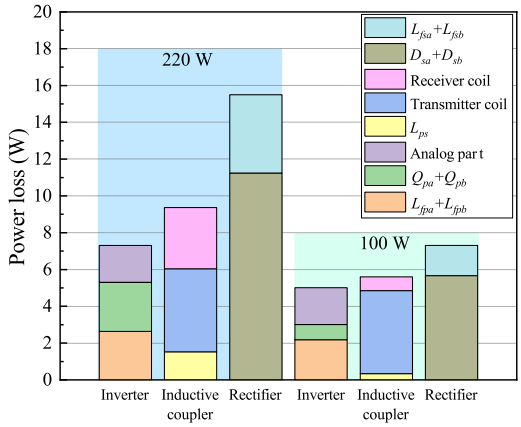

Fig. 18. Power loss breakdown of the 6.78-MHz WPT prototype.

From this table, it is apparent that the measurement results of the rectifier matches well with the calculation results from the model, and the phase shift during the range is optimized as near-resistive impedance, which validates the proposed concept and the circuit design. Particularly, as the load range varies from 220 to 40 W, the measured impedance and phase shift can be evaluated by the calculation: On the rated load, the measurement phase angle of the impedance is only $-1.13°$, where a resistive impedance of the rectifier is achieved; besides, until the output power was reduced to 40 W, the maximum phase angle of the rectifier maintains below 10°, during which the rectifier performs as near-resistive. Nevertheless, when the output power was further reduced to 20 W, the impedance's and the phase angle's error became evident.

From Fig. 16 (c), a manifest waveform distortion can be observed, where the output power is 20 W. This waveform distortion away from pure sinusoidal shape account for the mismatching between calculation result and the measurement since the modelling is derived with assumption that the rectifier is driven by a pure sinusoidal ac current source. In addition, when the converter operates with a very light load, the impedance shift from the diode's forward voltage, which is obviously nonlinear, may be the other explanation of the mismatching. Nonetheless, the measurement results can still not only validate the circuit model in Section II but also confirm the proposed concept to build a near-resistive class-E rectifier with a series compensation impedance.

In addition, the measured impedance was observed to be higher than the calculated impedance, because during the modelling the ESRs of the components and the forward voltage of the diodes are neglected for reasonable simplification. Generally the ESRs and the forward voltage can be modeled as an extra resistance in series with the rectifier, thus the error of the impedance can be interpreted.

Finally, the measured efficiency of the prototype and the calculated rectifier's efficiency are given in Fig. 17. It is noticed that the prototype achieved the peak efficiency of 87.2% at its rated load (48 V/220 W output) and the efficiency of the prototype can still maintain as higher than 80% when the power is reduced to 35% of the rated power. At a very light load (lower than 10% of the rated power) operation, the prototype can still achieve an efficiency of 64.1%. Besides, the calculated rectifier's efficiency result also indicates the high-efficiency operation capability for the proposed class-E rectifier. In Fig. 18, the calculated loss

breakdown at cases where the output power is 220 W and 100 W is presented. For both of the cases, the power loss of the rectifier contributes the largest part of the total power loss of the system and the conduction loss of the diodes dominates the loss of the rectifier on the prototype. It needs to be mentioned that the analog loss on the inverter includes the power consumption of the gate drivers and the analog circuit to generate trigger signals to the drivers, which is measured as 2 W at 6.78-MHz operation.

VI. Conclusion

In this investigation, a circuit design concept to improve the class-E rectifier for a large load-range is proposed and experimentally validated. By adding the compensation series inductor, we successfully designed and implemented a differential class-E rectifier with near-resistive impedance for a 6.78-MHz WPT system and the prototype measurement results match well with the circuit modelling. The proposed circuit design concept can be further implemented on other resonant power conversion applications to adapt the requirement of the load shifting during the operation. Based on the investigation, several conclusions can be made as follows.

1) The conventional class-E rectifier naturally performs as a nonlinear impedance during a large load range, whose impedance is highly depended on the circuit parameters. Besides, a near-resistive impedance with shifted load is hard to achieve only by circuit design.
2) The nonlinear impedance of the rectifier can be compensated by a series impedance to be near-resistive during a large load range and a series inductor is an alternative. By a circuit optimization method, a near-resistive impedance of the modified class-E rectifier can be achieved and the detailed design considerations are discussed.
3) The proposed circuit design concept and the corresponding circuit optimization method were experimentally validated by a 6.78-MHz/220-W WPT system. The system achieves 87.2% peak efficiency, and the measurement results match well with the previous circuit analysis and modelling.

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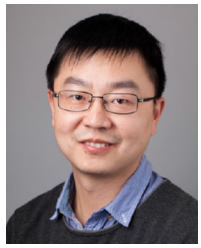

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