Identification of ZVS Points and Bounded Low-Loss Operating Regions in a Class-D Resonant Converter

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***Abstract*—This article presents an analysis of the different loss modes of the switching devices in a class-D series resonant converter operating with either fixed dead time or fixed duty cycle. A feasible operating region where the FETs in the inverter stage only exhibit reverse conduction losses, with no hard-switching, is identified. Furthermore, the impact of using a fixed dead time versus a fixed duty cycle is investigated. We find that using a fixed dead time is superior to using a fixed duty cycle, as a broader operating range can be achieved for the same losses, or the same operating range can be achieved with lower losses. A reduction in the reverse conduction losses of up to 59% or an expansion of the operational frequency range by 33% when using a fixed dead time is found. The modeling approach is validated on a 1-MHz prototype employing GaN switching devices. Lastly, a design example shows how the presented analysis can be used to determine the optimal fixed dead time/duty cycle for use with frequency modulation control such that the losses are minimized.**

***Index Terms*—DC–DC power converters, first harmonic approximation, modeling, resonant converters, wide-bandgap devices.**

I. Introduction

TODAY, most electronic devices are powered with a switch mode power supply (SMPS) thanks to their small form factor and high efficiency. The majority of SMPS are different types of hard-switching PWM topologies. These supplies have high switching losses, which limit the switching frequency that the supplies can handle. Nonetheless, higher switching frequencies allow for smaller passive components, and hence an overall smaller power supply and higher bandwidth to better react to various load and line disturbances. To improve the switching frequencies, soft-switching topologies have received much attention in recent years [1]–[7]. One family of soft-switching converters is the resonant converters [8]. Resonant converters work by having a resonant tank responsible for providing ac gain, in addition to charging and discharging the switching node during the dead time before the switching event and thus obtain zero-voltage switching (ZVS). This vastly reduces the switching losses, allowing for a higher operating frequency.

A popular family of resonant converter is the class-D series resonant converter [9]–[12] and its derivatives like the LLC [13]–[17]. These converters benefit from low device stress compared to other typologies like the class-E [4], [18], [19] and have a broad range of applicable controllers available. Some of the most common control techniques are: Tunable resonant tank capacitor control [20]–[23], bang-bang control [24]–[27], frequency modulation (FM) control [28]–[31], and lastly, phase-shift control [32], [33]. Unlike any of the other control methods, the phase-shift control uses double the number of switches in the inverter to achieve phase-control, thereby making it less compelling if cost or power density is of concern. In many cases, it is of interest to control the output voltage of the resonant converter, usually to compensate for changes or disturbances in the load or the supply voltage. Besides controlling the output voltage, it is paramount that the resonant converter upholds ZVS, which complicates the control design. These two simultaneous objectives can often be met using phase-shift control or combining FM-control with either a tunable resonant tank capacitor or adaptive duty cycle/dead time scheme [34]. However, using phase-shift control or some combined control methods vastly increase the complexity of the control circuit. As a simple control strategy is normally preferred, frequency control is often applied. Hence it is of interest to know the exact range of operation before ZVS is lost.

The investigation and analysis of ZVS operation for resonant converter has been widely covered in the prior art. However, the coverage usually focuses on the converter design process to obtain ZVS and is not concerned with postdesign considerations like the operational range and whether using a fixed duty cycle or fixed dead time is superior over the operational frequency range. In [9], the class-D series resonant converter is analyzed. The analysis only considers the use of fixed duty cycle for the dead time generation, leaving out the fixed dead time option. This is also the case for [10], [11], [13], [18], [19], [33].

This article presents an analysis of the different switching loss modes in the GaNFETs for a class-D series resonant converter (SRC) when the duty cycle/dead time is assumed fixed and FM-control is utilized. A complete mapping of the converter behavior is presented. Here, multiple ZVS points for the same dead time and limitations of the operating range are identified.

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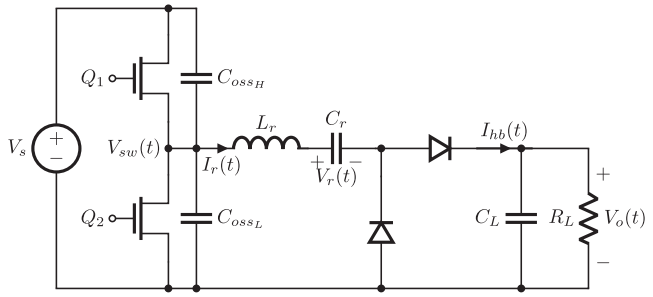

Fig. 1. Class-D series resonant converter with the parasitic capacitance for the FETs.

Further, we define a feasible soft-switching operation region that expands the operating space previously determined in [9]. In the feasible region, we determine the evolution of the losses and define an upper loss bound for the GaNFETs. The analysis considers the case where a fixed dead time is used and the case where a fixed duty cycle is used and determines the best of the two options. The findings in this article can be used for determining the optimal fixed dead time/duty cycle for use with FM-control while also providing valuable information for both the design of the converter and the selection of switching devices. The analysis is validated on a 1-MHz class-D SRC, where the feasible region and the location of the worst-case losses within the region are measured. Finally, a design example is provided on how to use the analysis for control design.

Although the presented analysis and results are carried out for a class-D SRC, the analysis and findings are applicable for any resonant converter that uses a sinusoidal current to charge and discharge the switching node. Such converters are other class-D based converters using either parallel and/or series resonance tanks like the LLC and LCC converters.

II. Losses in Inverter Switching Devices

Fig. 1 shows a Class-D SRC with the parasitic capacitances for the GaNFETs C_{oss_H} and C_{oss_L}. It is assumed that the converter operates above the resonance frequency in the inductive mode, where the resonant current lags the switching node voltage, and that the parasitic capacitances are static. When driving the converter outside the point of ZVS, losses occur in the FETs either due to insufficient charging/discharging of the combined output capacitance $C_{\text{oss}_{(t)}}$, reverse conduction losses of the FETs, or both. This section presents the loss mechanisms with the magnitude and conditions for each type of switching loss.

For resonant converters, ZVS is achieved by having the resonant tank current I_r charge/discharge the switching node V_{sw} to V_s/ground before turning on the corresponding FET. Doing this results in zero volts across the FET at the switching moment, thus achieving ZVS, and no power is dissipated. Due to the symmetry of the resonant current and the power stage, achieving ZVS in the charge direction implies that ZVS is likewise achieved in the discharge direction. Hence the presented math in this and the following sections will focus on the charging case only when determining ZVS and losses. Also, the time dependency is omitted from the equations.

The time that I_r has to charge $C_{\text{oss}_{(t)}}$ to V_s is given by the dead time t_d, which is related to the duty cycle by

$$t_d = \frac{0.5 - D}{f_{\text{sw}}} \tag{1}$$

where D is the duty cycle for each FET and f_{sw} is the switching frequency of the converter. In some cases, the dead time is implemented as a constant time and independent of the switching frequency. If the dead time is too short or the resonant current too small, $C_{\text{oss}_{(t)}}$ is insufficiently charged, leading to a voltage across the FET at the switching moment that will result in switching loss. The following equation shows the loss, where V_{DS} is the voltage across the FET at the switching moment

$$P_{\text{sw}} = \frac{1}{2} C_{\text{oss}_{(t)}} V_{DS}^2 f_{\text{sw}}. \tag{2}$$

If the dead time is too long, the GaNFET will enter reverse conduction, which prevents overcharging of C_{oss} but leads to reverse conduction losses. The voltage drop across GaNFETs in reverse conduction, V_f, tend to be higher than that for MOSFETs. However, since GaN switches have zero reverse-recovery charge ($Q_{rr} = 0$), unlike MOSFETs, the reverse recovery losses become zero, leaving the reverse conduction loss to be the only loss of interest. For applications where the dead time is short, the GaN device is more efficient than a MOSFET from a reverse conduction point of view. The following equation shows the reverse conduction loss, where V_f is the voltage drop across the FET in reverse conduction, and t_{cond} is the reverse conduction time

$$P_{rev} = V_f t_{\text{cond}} I_r f_{\text{sw}}. \tag{3}$$

Lastly, there are the two cases where the dead time is so long that the resonant tank current changes direction at time $t_r < t_d$ causing an undesired discharge of the switching node V_{sw}. In the first case, V_{sw} is completely charged hence both reverse conduction losses and switching losses occur. In the second case, V_{sw} is insufficiently charged, resulting in switching losses. Fig. 2 shows the five types of switching with the corresponding resonant tank current. From a loss modeling perspective, the first and fifth cases are equivalent.

Through a rewriting of (2) and (3), the losses of the four lossy switching modes in Fig. 2 can be determined. In the first and fifth case where partial hard-switching losses occur, V_{DS} can be determined as the voltage over $C_{\text{oss}_{(t)}}$ due to the accumulated charge from I_r during the dead time subtracted from the supply voltage. Hence, (2) can be rewritten as follows:

$$P_{\text{sw}} = \frac{1}{2} C_{\text{oss}_{(t)}} f_{\text{sw}} \left(\frac{1}{C_{\text{oss}_{(t)}}} \int_{t_d} I_r \, dt - V_s \right)^2. \tag{4}$$

In the third case where reverse conduction losses occur, the term $t_{\text{cond}} I_r$ provides the number of charges passing through the GaNFET during the conduction time. This can be written as the total number of charges accumulated during the dead time subtracted with the number of charges needed to charge $C_{\text{oss}_{(t)}}$ to V_s. The following equation shows the rewritten version of (3)

$$P_{rev} = V_f f_{\text{sw}} \left(\int_{t_d} I_r \, dt - V_s C_{\text{oss}_{(t)}} \right). \tag{5}$$

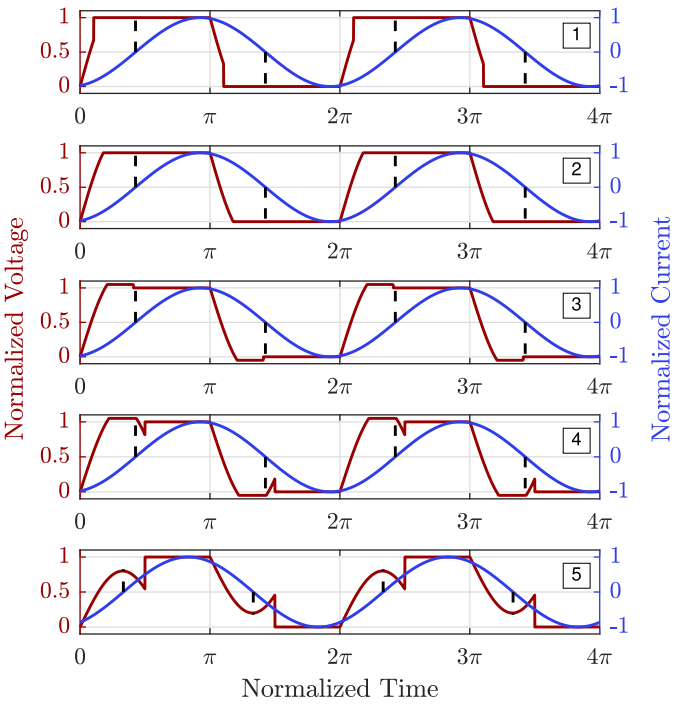

Fig. 2. Typical switching waveforms for $V_{\text{sw}}(t)$ and resonant tank currents $I_r(t)$. The dashed lines indicate the zero-crossing of the current. From top to bottom: partial hard-switching, where the dead time is too short resulting in a jump in the voltage at turn ON/OFF; *ZVS*, where $V_{\text{sw}}(t)$ is fully charged/discharged during the dead time; reverse conduction, where reverse conduction occurs due to long dead time; current reversal, where $V_{\text{sw}}(t)$ starts to discharge again before the end of the dead time; partial hard switched current reversal, where the dead time is too long and the current too small resulting in an increased jump in the voltage at turn ON/OFF compared to case 1.

Finally, in the fourth case, where both reverse conduction losses and switching losses occur due to a long dead time causing the reversal of the current flow, the losses can be written as in (6). Here the charges for P_{rev} are only accumulated up to the point where the current flow changes direction (t_r), and the switching loss is evaluated from t_r to the end of the dead time t_d

$$P_{rev} = V_f f_{\text{sw}} \left(\int_{t_r} I_r \, dt - V_s C_{\text{oss}_{(t)}} \right) \tag{6a}$$

$$P_{\text{sw}} = \frac{1}{2} C_{\text{oss}_{(t)}} f_{\text{sw}} \left(\frac{1}{C_{\text{oss}_{(t)}}} \int_{t_d - t_r} I_r \, dt \right)^2. \tag{6b}$$

III. Switching Loss Analysis

In this section, we determine a feasible operation region with regard to power losses. The region is encircled by the ZVS points and the boundary where the resonant current changes direction. Thus, both of these behaviors will be described analytically. Furthermore, the losses induced in the FET's related to switching are determined for the feasible region. The analysis is carried out using the first harmonic approximation (FHA) approach [8] combined with the methods presented by Hamill in [35] to include the effects of the parasitic capacitance in the rectifier diodes. In the analysis, the frequency is normalized by the resonance frequency to generalize the findings.

Using the FHA, we assume that the resonance current, I_r, can be adequately described as a pure sine waveform. Equation (7) shows the approximated resonance current $\hat{I}_r$

$$I_r \approx \hat{I}_r = I_m \sin(\omega_n t + \phi) \tag{7}$$

where I_m is the magnitude of the current given by (8a), and ϕ is the phase-shift between the resonant current and V_{sw} given by (8b)

$$I_m = \frac{|\mathcal{F}_1\langle V_{\text{sw}}\rangle|}{R_{eq}\sqrt{1 + Q^2\left(\omega_n - \omega_n^{-1}\right)^2}} \tag{8a}$$

$$\phi = -\arctan\left(Q\left(\omega_n - \omega_n^{-1}\right)\right) \tag{8b}$$

where $\mathcal{F}_n\langle\cdot\rangle$ denotes the function for the nth harmonic Fourier series, and ω_n is the normalized angular switching frequency given by

$$\omega_n = \omega/\omega_c \tag{9}$$

where ω is the switching frequency and ω_c is the resonance frequency of the converter in rad/s. Lastly, Q is the resonant tank quality factor, and R_{eq} is the ideal equivalent resistive load of the rectifier as seen from the output of the inverter and is given by the following:

$$R_{eq} = \frac{2R_L}{(\pi + C_d\omega R_L)^2} + R_{esr} \tag{10}$$

where R_L is the load resistance, C_d is the parasitic capacitance of the rectifier diode, and R_{esr} is the combined parasitic series resistance in the resonant tank. In Hamill's work, the rectifier diodes' parasitic capacitance is modeled as a capacitor, C_h in series with R_{eq}. The capacitor C_h being in series with the resonant capacitor C_r effectively reduces the total resonant tank capacitance and makes it dependent on the switching frequency. This impacts the resonance frequency, ω_c, and the quality factor Q such that both increase slightly with the switching frequency. Thus, Q is found as

$$Q = \frac{C_r + C_h}{C_r C_h R_{eq}\omega_c}. \tag{11}$$

Modeling the small increase in both the resonance frequency and quality factor results in a better prediction of the resonant current when the switching frequency is far away from the resonance frequency of the converter, hence improving the fidelity of the model.

A. Zero-Voltage Switching Points

Zero-voltage switching can be achieved whenever the accumulated charge from the resonant current is equal to that needed to charge the parasitic capacitance, $C_{\text{oss}_{(t)}}$, to the supply voltage, V_s. The resonance current is only able to deliver charge during the dead time, which is assumed fixed. Hence, to obtain ZVS, the equality in the following equation needs to be true

$$\int_{\bar{t}_{zvs}} -\hat{I}_r dt - V_s \bar{C}_{\text{oss}_{(t)}} = 0. \tag{12}$$

where $\bar{t}_{zvs}$ is the normalized dead time needed for ZVS when the frequency is ω_n and $\bar{C}_{\text{oss}_{(t)}}$ is the normalized parasitic

capacitance defined as

$$\bar{C}_{\mathrm{oss}_{(t)}} = C_{\mathrm{oss}_{(t)}}\omega_c. \tag{13}$$

Inserting (7) in the integral of (12) and evaluating the integral we get:

$$\frac{I_m\left(\cos(\omega_n \bar{t}_{zvs} + \phi + \theta) - \cos(\phi + \theta)\right)}{\omega_n} - V_s \bar{C}_{\mathrm{oss}_{(t)}} = 0 \tag{14}$$

where $\theta = \angle \mathcal{F}_1\langle V_{\mathrm{sw}}\rangle$. The switching node V_{sw} is described by a piecewise function such that the charge and discharge of the output capacitance is included [28]. A result of this is that the phase of the Fourier approximation becomes nonzero. Thus θ accounts for any phase-shift present in V_{sw} such that it aligns properly with I_r. By solving for $\bar{t}_{zvs}$ in (14), an expression for the dead time needed to obtain ZVS is found

$$\bar{t}_{zvs} = -\frac{\phi + \theta + \arccos\left(\cos(\phi + \theta) + \frac{V_s \omega_n \bar{C}_{\mathrm{oss}_{(t)}}}{I_m}\right)}{\omega_n}. \tag{15}$$

To obtain a condition for ZVS similar to (15) but for a fixed duty cycle, the relation in (1) is used in its normalized form as follows:

$$\bar{t}_{zvs} = 2\pi\omega_n^{-1}(0.5 - D_{zvs}). \tag{16}$$

Substituting $\bar{t}_{zvs}$ with (15) and solving for the duty cycle results in (17)

$$D_{zvs} = \frac{1}{2} + \frac{\phi + \theta + \arccos\left(\cos(\phi + \theta) + \frac{V_s \omega_n \bar{C}_{\mathrm{oss}_{(t)}}}{I_m}\right)}{2\pi}. \tag{17}$$

The results (15) and (17) are both, in theory, independent of V_s, meaning that ZVS will be achieved for any given supply voltage. However, in practice, $C_{\mathrm{oss}_{(t)}}$ changes with V_s in a nonlinear manner, thereby moving the ZVS points slightly. The effect scales with ω_n and R_L such that the ZVS points close to resonance move less than those far from resonance, and the movement is increased for smaller loads. Hence, the determined ZVS points from (15) and (17) are only valid when the supply voltage is within a local neighborhood of V_s.

By sweeping ω_n in (15) and (17) it is possible to trace out the ZVS curve. Fig. 3 shows the obtained ZVS curve for a fixed duty cycle [Fig. 3(a)] and a fixed dead time [Fig. 3(b)] when the resonant tank has a $Q = 4$. As seen, the computed solution indicates that two simultaneous ZVS points exist for each value of the fixed dead time in the normalized range from 0.44 to 0.68 and fixed duty cycle values between 42.2% and 38.5%. The phenomenon occurs because the resonant tank current I_r changes in both amplitude and phase with frequency. For the close to resonance part of the ZVS curve, i.e., the ZVS curve below the "Max Loss" curve, the resonant current is large and almost in phase with the switching node. This results in ZVS being obtained primarily due to the large amplitude of the current. For the far from resonance part of the ZVS curve, i.e., the ZVS curve above the "Max Loss" curve, the current is smaller, and ZVS is achieved due to the increased phase-shift. At the very top and bottom of the feasible operating region where the ZVS curve intersects with the "Rev. Limit" curve, class-DE operation

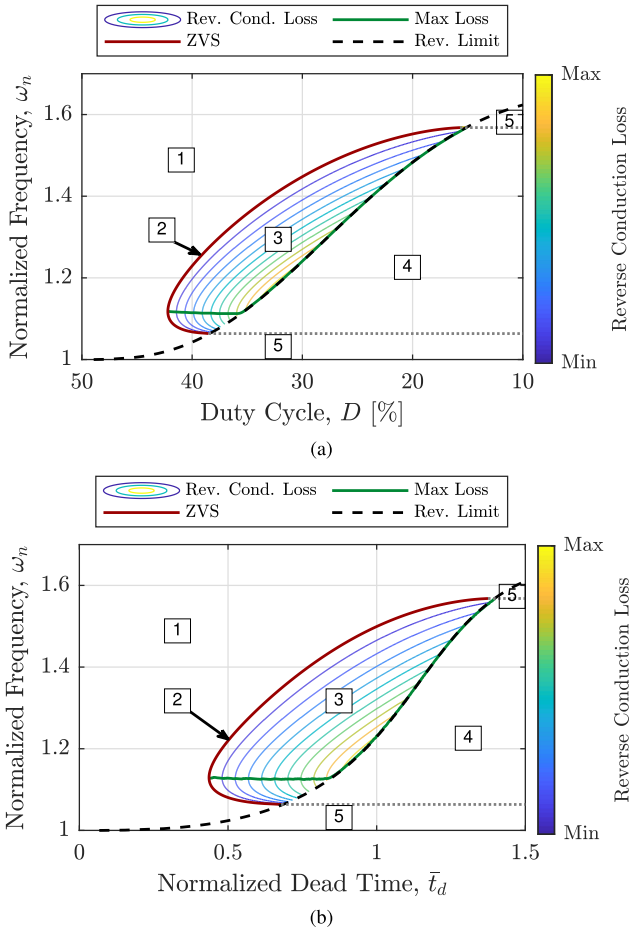

Fig. 3. Feasible operation region of the resonant converter encircled by the ZVS curve and the current reversal boundary. (a) Region when duty cycle is used. (b) Region for a normalized dead time. The max loss curve indicates the point of the worst-case loss for every duty cycle/dead time inside the feasible region. The numbers indicate the different operating regions and match the numbering in Fig. 2.

is achieved, as zero-voltage-derivative switching (ZVdS) and thereby also zero-current switching (ZCS) occur. The ZVdS results in a decreased sensitivity to changes in the dead time, which is seen in Fig. 3 by the small slope of both the low and high frequency ZVS. At large dead times or small duty cycles, the low frequency section of the ZVS curve disappears due to the reversal of the current flow marked by the dashed line.

B. Current Flow Reversal Limit

During the desired operation of a resonant converter, the resonance current will monotonically charge the switching node during the dead time period. However, if the dead time becomes too extensive, the resonant current's direction will change during the dead time, resulting in an unwanted discharge of the switching node near the end. This behavior inhibits ZVS. Thus it is of interest to work out when this phenomenon occurs.

Whenever the current flow changes direction, a zero-crossing occurs. This means that the time needed to reach the zero-crossing is equivalent to finding the point of the current flow reversal. Hence we have:

$$-I_m(\omega_s)\sin(\omega_n \bar{t}_r + \phi + \theta) = 0 \tag{18}$$

where $\bar{t}_r$ is the normalized time needed to reach the zero-crossing given by: $\bar{t}_r = t_r\omega_c$. The only practical solution to (18) is when the trigonometric term is zero. Due to the nature of the sine function, it follows:

$$\Rightarrow -\omega_n\bar{t}_r - \phi - \theta = 0 \tag{19}$$

$$\Leftrightarrow \bar{t}_r = (\phi + \theta)/\omega_n. \tag{20}$$

From where the zero-crossing time is found. Using the relationship between the normalized time and duty cycle from (16), the corresponding duty cycle limit, D_r, can be determined

$$2\pi\omega_n^{-1}(0.5 - D_r) = (\phi + \theta)/\omega_n \tag{21}$$

$$\Leftrightarrow D_r = \frac{1}{2} - \frac{\phi + \theta}{2\pi}. \tag{22}$$

The dashed lines in Fig. 3 show the boundaries for where the current flow reversal occurs. Fig. 3(a) shows it when operating with a fixed duty cycle (22), and Fig. 3(b) for when operating with a fixed dead time (20). Due to the nature of the current flow reversal limit, ZCS will always happen when operating on the limit.

C. Maximum Reverse Conduction Loss

The area encircled by the ZVS curve and the reverse current boundary in Fig. 3 is the region of reverse conduction losses. It is usually preferable to stay in this region compared to staying in the region with quadratic switching losses since lower losses are achievable. This is especially the case with GaN devices thanks to their zero reverse recovery charge. Thus, the encircled region with its encirclement constitutes the feasible operating region for the resonant converter. As only reverse conduction losses occur in the feasible region, an upper bound of the losses in the FETs can be determined to assess the worst-case operation mode and location.

To find the worst-case reverse conduction losses in the feasible operating region, we first evaluate the losses in every point in the region using the normalized reverse conduction loss given by (24). Finally, the maximum loss for each dead time/duty cycle is logged

$$\bar{P}_{rev} = V_f\frac{\omega_n}{2\pi}\left(\int_{\bar{t}_d} -I_r dt - \bar{C}_{\mathrm{oss}_{(t)}}V_s\right) \tag{23}$$

$$= V_f\frac{\omega_n}{2\pi}\int_{\bar{t}_{zvs}}^{\bar{t}_d} -I_r dt. \tag{24}$$

In Fig. 3, the contour lines indicate the magnitude of the reverse conduction losses in the feasible region. The curve "Max Loss" represents the point of the worst-case loss for every duty cycle/dead time inside the feasible region. The max loss curve follows the contour lines by intersecting the contours' peaks, which indicate the highest loss point for the given dead time/duty cycle. Once the max loss curve reaches the current flow reversal limit, the worst-case loss will follow the limit until it reaches the upper bound of the feasible region. Lastly, the curve for the current flow reversal boundary indicates the endpoints of where ZVS is achievable. However, increasing the dead time slightly beyond this boundary does not significantly impact the losses. This is because the reverse current flow reduces the voltage difference due to the forward voltage drop that would otherwise create an additional small switching loss.

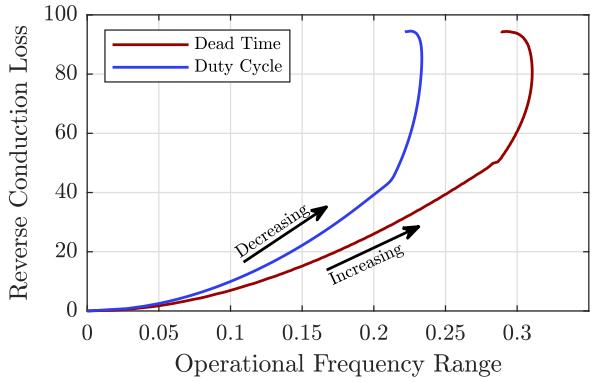

Fig. 4. Operational frequency range against the normalized worst-case reverse conduction loss in the feasible region for the given range. The arrows are indicating the direction of increased dead time and decreased duty cycle, equivalent of moving to the right on Fig. 3. The dead time and duty cycle each moves up to the point of the highest reverse conduction loss.

D. Converter Design Considerations

Based on the found feasible region, some remarks can be added regarding how to design the converter to enhance the feasible region. A usable design metric is to look at the rotation of the feasible region. If the feasible region is rotated counter-clockwise, more switching frequencies will be available for the same dead time. This means that an FM-controller will achieve a larger span of output voltages at the same amount of losses or the same output span for fewer losses. The counter-clockwise rotation can be achieved by adjusting the quality factor Q and by adjusting the output capacitance of the FETs C_{oss}. By increasing Q, a larger phase-shift in the resonant tank will occur for the same frequency step, corresponding to a counter-clockwise rotation of the feasible region. Likewise, by decreasing C_{oss}, less charge is needed to obtain ZVS. As a result, a rotation of the feasible region occurs, and the region shifts slightly to the left because less dead time is needed.

A high Q-factor is often used to ensure a high gain sensitivity, which guarantees the FHA, while a low C_{oss} is usually picked to reduce the needed dead time and/or limit the losses during partial hard-switching. Thus the design recommendations for rotating the feasible region coincide with the typical design recommendations for class-D resonant converters.

IV. Comparison of Dead Time and Duty Cycle

For a selected dead time/duty cycle, the feasible operating region will have a certain range of switching frequencies where the converter will operate within the region. For a normalized dead time of 0.5, the range of feasible operating frequencies is approximately 0.15. However, as the dead time increases, the range expands until the effect of the current reversal becomes severe and begins limiting the range once again. Fig. 4 shows this effect for both the fixed dead time and the fixed duty cycle cases.

As the dead time is increased, the feasible operating frequency range expands until it reaches 0.31 from where it rapidly

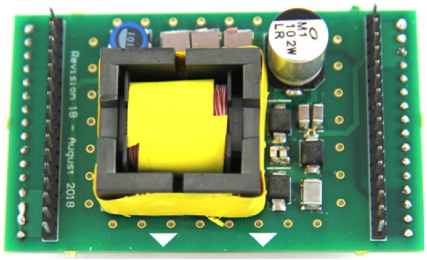

Fig. 5. Prototype Class-D SRC.

TABLE I
SPECIFICATIONS OF THE CONVERTER. THE CAPACITANCES, V_f, AND R_f ARE BASED ON DEVICE CHARACTERIZATION USING A KEYSIGHT B1505 A POWER DEVICE ANALYZER

	Value	Unit	Acquired
V_s	350	V	Measured
R_L	1000	Ω	Measured
R_{esr}	2	Ω	Measured
$C_{oss_{(tr)}}$	40	pF	Measured
C_d	12.6	pF	Measured
V_f	1.3	V	Measured
R_f	0.6	Ω	Measured
f_c	836	kHz	Calculated

contracts due to the current reversal limiting the switching frequency from below. The same effect is observed when the duty cycle is decreased. However, the duty cycle is only able to reach a maximum frequency range of 0.23. Moreover, the maximum losses in the feasible region when using a fixed duty cycle is higher than using a fixed dead time. More specifically, the analysis shows that a fixed dead time provides an expansion of up to 33% in the operating range for the same losses compared to using a fixed duty cycle, or up to a 59% decrease in reverse conduction losses for the same operating range compared to using a fixed duty cycle.

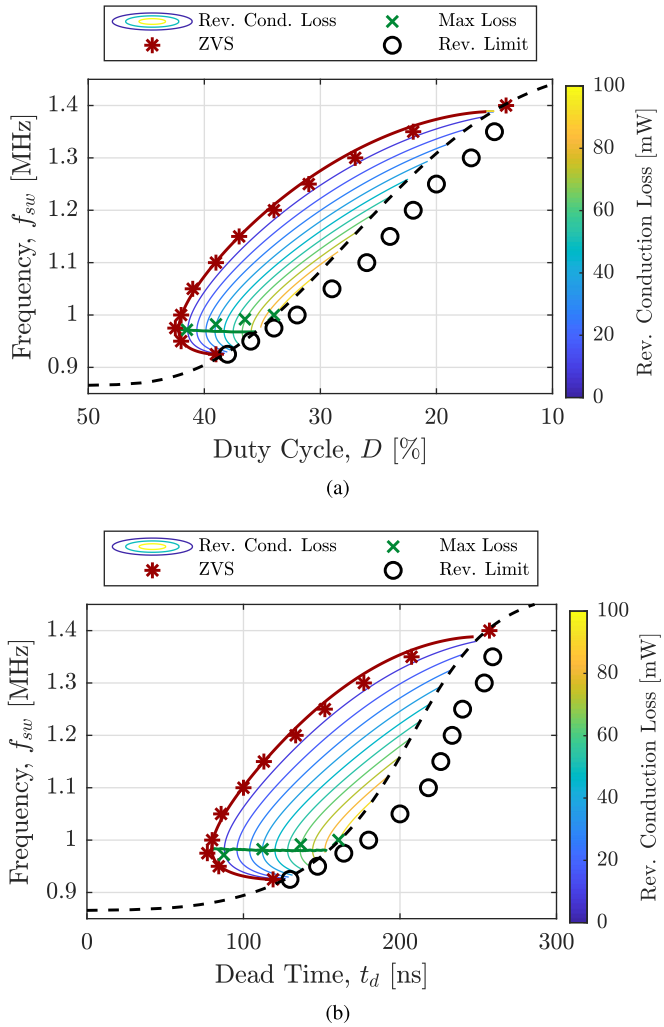

Fig. 6. Measured (points) and analytic (lines) results for the prototype converter. (a) Result for the fixed duty cycle. (b) Results for the fixed dead time.

V. EXPERIMENTAL VALIDATION

To validate the analysis findings, a 1-MHz class-D resonant converter prototype using GaNFETs [36] for the inverter switches is constructed. A complete characterization is performed on both the GaNFETs and the rectifier diodes using a Keysight B1505 A power device analyzer to obtain accurate data for the model. To characterize the output capacitance, the capacitance is measured for multiple bias voltages across the device going from 0 V to V_s. Then the average of the acquired capacitance values is calculated to get the time-related output capacitance $C_{\text{oss}_{(tr)}}$. The same approach is used to obtain the rectifier diode capacitance C_d with the only difference being that the bias voltage is limited to 250 V. The reverse conduction characteristic of the GaNFET is modeled as a diode using a forward voltage V_f and a resistor R_f. Fig. 5 shows the prototype and Table I shows the specifications and test conditions.

Points across both the ZVS curve and the current reversal curve are measured for encircling the feasible region and for comparison with the analysis. The measurements are performed by changing the converter's switching frequency and duty cycle until ZVS is observed. The same procedure is used for the current reversal. To determine the curve and size of the worst-case reverse conduction losses in the feasible region, an experiment is designed to map the response surface in the feasible region. Thus the reverse conduction losses are measured at multiple points inside the feasible region. A 4th order model is fitted from the measurements, and the maximum loss is derived from the estimated model.

Fig. 6(a) shows the measurement results (points) with the expected results from the analysis (lines) for a fixed duty cycle, and Fig. 6(b) shows the measurement results for the fixed dead time. Looking at Fig. 6, we find that the ZVS measurements and the location of the worst-case losses correspond to the theory. The ZVS measurements follow the theoretical curve exactly until 1.2 MHz, where the measurements start to fall slightly below the curve while the max loss points are measured to be at a slightly higher frequency than predicted. The reverse current limit follows the expected curve up to approximately 1 MHz from where the points are found at a greater dead time than expected. The discrepancy between the measurement and

TABLE II
DESIGN CRITERIA

	Value	Unit
V_o	150	V
V_s	300 ± 50	V
R_L	1000 ± 250	Ω

theory with the increasing switching frequency is partly due to the breakdown of the FHA method since the resonant current I_r no longer acts like a pure sinusoidal current. Furthermore, at higher switching frequencies, the model becomes more sensitive to the parasitic capacitance values in the GaNFETs and rectifier diodes.

The measured feasible region, both when using a fixed dead time and a fixed duty cycle, assimilates the shape of the corresponding theoretical region, with the main difference being the lower reverse current limit that expands the region slightly more. This suggests that the difference in performance identified in Section IV is valid and a fixed dead time in general is preferred.

Fig. 7 shows eight scope shots taken from the prototype when operating in the different regions as marked in Fig. 3. Fig. 7(a) and (b) shows the class-DE operation at the very top and bottom of the feasible region respectably. Fig. 7(b) and (d) shows ZVS for the same duty cycle but at two different frequencies proving that there can exist two ZVS points for the same duty cycle/dead time. Fig. 7(c) to (f) shows the switching behavior for regions 1 through 4. Finally, Fig. 7(g) and (h) shows the switching behavior of region 5 at the low and high frequency part, respectively.

From Fig. 7(a) and (b), it is clear to see that V_{sw} charges up with a decreasing slope and reaches the final voltage with almost zero slope, indicating that the resonant current is zero, i.e., ZCS is achieved, which implies class-DE operation. Lastly, we find that all the waveforms for all the tested operating points behave as expected from the analysis and match with the expected waveforms for each region provided in Fig. 2.

VI. DESIGN EXAMPLE

In this last section, an example is provided to show how the presented analysis can be applied in practice. For the example, the same prototype class-D SRC as in Section V is used, and we assume that it operates with a fixed dead time and frequency control. The design objective is to keep a stable output voltage, V_o, for a changing supply voltage V_s and load R_L. This needs to be achieved while staying within the feasible operating region at all times to minimize losses in the switching devices. The maximum variation on the supply voltage and load is assumed to be bounded. Table II shows the design criteria.

The design procedure can be summarized in the following three steps:

1) determine the lowest and highest switching frequency ($f_{\text{sw}_{\text{min}}}$ & $f_{\text{sw}_{\text{max}}}$) needed to stay at V_o for all possible perturbations:
2) derive the feasible operating regions for the perturbations resulting in $f_{\text{sw}_{\text{min}}}$ and $f_{\text{sw}_{\text{max}}}$;
3) find a common dead time that keeps the converter within each of the two feasible regions.

A. Determining Switching Frequencies

Using (25), it is possible to determine the output voltage of the converter under the FHA assumption [8], where η is the efficiency of the converter assumed to be 0.9

$$V_o = V_s \frac{\eta^2}{\sqrt{1 + Q^2\left(\omega_n - \omega_n^{-1}\right)^2}}. \tag{25}$$

The highest and lowest frequencies needed to stay at V_o are found in the corners of the perturbations, i.e., when V_s and R_L are at either the maximum or minimum. By sweeping ω_n, all obtainable output voltages for the converter can be determined. Fig. 8 shows the output voltage versus the normalized frequency for each corner. The dotted lines indicate the minimum $\omega_{n_{\text{min}}}$ and maximum $\omega_{n_{\text{max}}}$ normalized frequency needed to stay at V_o for the worst-case perturbations.

B. Deriving Feasible Operation Regions and Dead Time

In Section III-A, it is stated that the feasible operating region's only dependence on V_s is through the nonlinear parasitic capacitance $C_{\text{oss}(t)}$, and that within a local neighborhood of the nominal supply voltage, the capacitance change is negligible. From the design criteria in Table II we find that the supply varies with ± 50 V resulting in a ∓ 4.4 pF variation in $C_{\text{oss}(tr)}$. For the used converter and its defined load range, this variation in $C_{\text{oss}(tr)}$ turns out to be small enough to be disregarded. Thus only R_L needs to be considered when evaluating the feasible region.

Changing R_L will either expand or contract the feasible operating region due to the corresponding change in the resonant tank current's amplitude. When the load is increased, i.e., R_L is decreased, the feasible operating region expands up and down in frequency and towards lower dead times while the current reversal limit stays somewhat stationary. The expansion happens because a larger current is being processed in the converter, which provides more current for faster charging/discharging $C_{\text{oss}(t)}$. Hence, less dead time is needed. When the load is decreased, i.e., R_L is increased, the opposite happens, and the region contracts because less current is available for charging/discharging $C_{\text{oss}(t)}$. The change in the size of the feasible region, especially the contracting, vastly limits the size of realizable bounds on both V_s and R_L because the needed frequency range needs to fit within a smaller area. Fig. 9 shows the feasible operating regions for when the load is large and small.

The horizontal dotted lines on Fig. 9 indicate the frequency range that needs to be inside the feasible operating region. From Fig. 8, we know that $\omega_{n_{\text{max}}}$ needs to be in the feasible region for $R_L = 1250\,\Omega$ and $\omega_{n_{\text{min}}}$ in the feasible region for $R_L = 750\,\Omega$. This results in a needed normalized dead time of 0.33 and 0.7, respectively. Since the normalized dead time of 0.7 works for both feasible operating regions, it will work for all bounded perturbations. Henceforth, the minimum dead time needed to meet the criteria in Table II is 0.7. Moreover, the found dead time is the smallest possible and the one that will exhibit the fewest

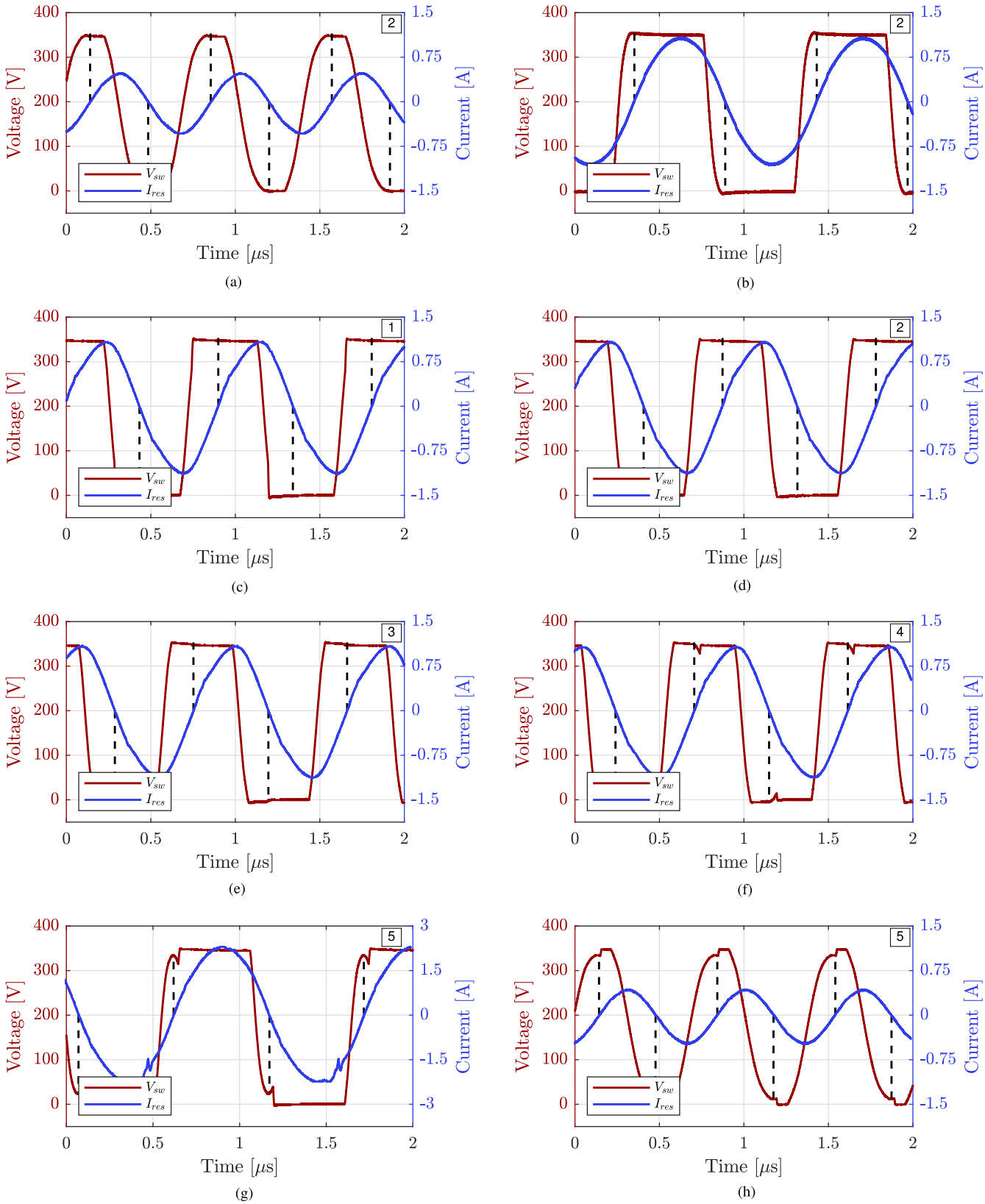

Fig. 7. Captured waveforms of the switching node V_{sw} and the resonant tank current I_r for the different operating regions. Frequency, dead time and duty cycle are noted for each plot. The dashed lines indicate the zero-crossing of the current. (a) Class-DE ZVS/ZVdS: 1.40 MHz, $t_d = 263$ ns/$D = 13.2\%$. (b) Class-DE ZVS/ZVdS: 926 kHz, $t_d = 130$ ns/$D = 38.0\%$. (c) Partial hard-switching: 1.10 MHz, $t_d = 60$ ns/$D = 43.4\%$. (d) ZVS; 1.1 MHz, $t_d = 105$ ns/$D = 38.5\%$. (e) Reverse conduction: 1.10 MHz, $t_d = 203$ ns/$D = 27.7\%$. (f) Current Reversal: 1.10 MHz, $t_d = 239$ ns/$D = 23.7\%$. (g) Partial hard-switching w/current reversal: 907 kHz, $t_d = 139$ ns/$D = 37.4\%$. (h) Partial hard-switching with current reversal: 1.43 MHz, $t_d = 287$ ns/$D = 9.0\%$.

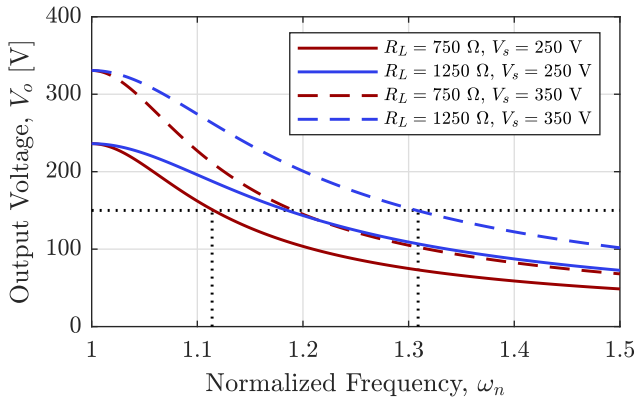

Fig. 8. Output voltage versus normalized frequency for each corner.

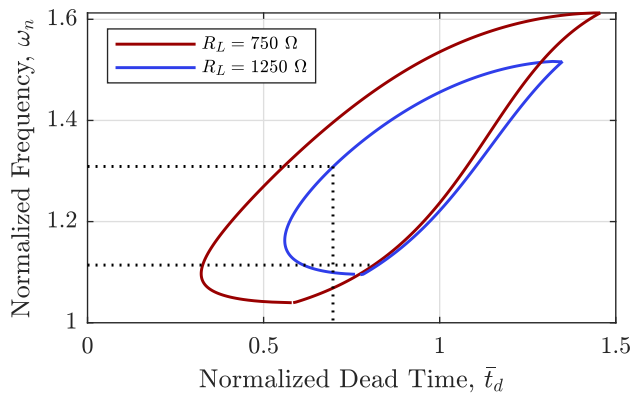

Fig. 9. Feasible operating region when the load is at the upper bound ($R_L = 750\,\Omega$) and the lower bound ($R_L = 1250\,\Omega$).

losses in the converter while keeping an FM-controlled converter inside the feasible region for all bounded perturbations. This is easily seen in Fig. 9 by the fact that the corner ($R_L = 1250\,\Omega$) is a ZVS point.

C. Validation

To validate the just found results, the prototype is measured at each corner and the nominal case to verify that the output voltage is as expected and within the feasible region. First, the normalized results are converted to the proper units

$$t_d = \bar{t}_d/\omega_c = 128\,\text{ns} \tag{26}$$

$$f_{\text{sw}_{\text{max}}} = \frac{\omega_{n_{\text{max}}}\omega_c}{2\pi} = 1.17\,\text{MHz} \tag{27a}$$

$$f_{\text{sw}_{\text{min}}} = \frac{\omega_{n_{\text{max}}}\omega_c}{2\pi} = 0.963\,\text{MHz}. \tag{27b}$$

Table III shows the measured output voltage for each of the corner cases and the nominal case, as well as the operating regions, when the dead time is $t_d = 128$ ns. As predicted, the corner ($R_L = 1250\,\Omega, V_s = 350$ V) is a ZVS point, and all other corners experience reverse conduction losses, indicating they are within the feasible operating region. Finally, we see that all the measured points are close to the target output voltage $V_o = 150$ V.

TABLE III
MEASURED SUPPLY, AND OUTPUT VOLTAGE FOR EACH CORNER AND THE NOMINAL CASE WHEN $t_d = 128$ NS

Conditions			Measured		
V_s [V]	R_L [Ω]	f_{sw} [MHz]	V_s [V]	V_o [V]	Operating Region
300	1000	1.05	300.1	149.7	Rev. Conduction
250	1250	1.05	250.0	152.3	Rev. Conduction
350	1250	1.17	350.9	146.6	ZVS
250	750	0.96	250.4	148.5	Rev. Conduction
350	750	1.03	350.6	144.4	Rev. Conduction

VII. CONCLUSION

This article presents an analysis of the different switching loss modes in a class-D SRC using either a fixed dead time or fixed duty cycle. A feasible operating region where the FETs in the inverter stage only exhibit reverse conduction losses is defined and fully enclosed by the ZVS curve and the reverse current limit. We find that class-DE operation is possible at both the top and bottom of the feasible region where the ZVS curve intersects with the reverse current limit. Furthermore, the impact of using a fixed dead time compared to a fixed duty cycle is investigated. It is concluded that using a fixed dead time is superior to using a fixed duty cycle since a broader operating range can be achieved for the same reverse conduction losses, or the same operating range can be achieved with lower losses. A reduction in the reverse conduction losses of up to 59% or an expansion of the operating range by 33% when using a fixed dead time rather than a fixed duty cycle is calculated. The analysis and modeling approach is validated on a 1-MHz class-D SRC prototype employing GaN switching devices, where the measurements followed the patterns predicted by the model. Lastly, we show how the presented analysis can be used to work out the frequency range and dead time for a frequency controller, such that the converter always stays within the feasible region, and the losses are minimized.

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