Letters

Hybrid Modular Multilevel Rectifier: A New High-Efficient High-Performance Rectifier Topology for HVDC Power Delivery

Jian Liu, *Student Member, IEEE*, Dong Dong, *Senior Member, IEEE*, and Di Zhang, *Senior Member, IEEE*

***Abstract*—This letter presents a novel three-phase rectifier topology, namely hybrid modular multilevel rectifier (HMMR) for medium or high voltage ac–dc power conversion applications. Compared with modular multilevel converter (MMC), up to 50% of the IGBTs and submodules (SMs) including capacitors can be replaced by simple high-efficient high-voltage line-frequency diode stacks. HMMR can keep the key benefits of MMC, such as modularity, reliability, and excellent harmonic performance, while significantly reducing the power losses, costs, and volume. Unlike the thyristor-based line-commutated converter (LCC) rectifier, HMMR can operate under different grid conditions and can even provide reactive power support, making it a strong candidate of rectifier unit for point-to-point MV and HV power delivery. The feasibility of proposed converter is verified by the simulation as well as experimental results.**

***Index Terms*—High power density, hybrid modular multilevel rectifier (HMMR), MV/ HV dc system.**

I. Introduction

MODULAR multilevel converter (MMC) has emerged as one of the most attractive topologies for medium voltage (MV) or high voltage (HV) dc applications due to its flexibility, modular structure, excellent power quality, and fault tolerant operation capability [1]. However, MMC-based HVdc systems still face some challenges. First, the number of IGBTs is doubled with the half-bridge (HB) submodule (SM) and quadrupled with full-bridge (FB) SM compared with the classic two-level voltage source converter. Second, SM capacitors occupy more than 50% of the weight and size of MMC [2], hence resulting in bulky converters and higher construction cost. This also hinders the MMC in weight or space sensitive applications, such as offshore wind power platform.

Compared to the MMC-based HVdc system (MMC-HVdc), line-commutated converter (LCC) based HVdc system (LCC-HVdc) reduces the cost, volume, and power conversion losses [3]. Nevertheless, LCC-HVdc is also limited by critical drawbacks, including large reactive power consumption, large amount of harmonic currents, and limited voltage regulation range [4]. The commutation process involves interactions with the grid, leading to commutation failure or reduced power capacity under weak-grid condition. In order to address these issues, various hybrid topologies have been proposed. The authors in [5] proposed to connect MMC in parallel with LCC or diode rectifier (DR) on ac sides to optimize the power distribution between two HVdc links. However, the parallel connection needs the MMC to withstand full nominal HVdc voltage and additional full-rating ac transformer with tertiary windings. In [6], a high-voltage cascaded FB branch is connected to MMC dc side to reduce MMC SM number. But, a large LC filter is required to constrain the high-frequency circulating current.

Given that the power flow of MV/HV dc power delivery systems is often unidirectional, a novel hybrid modular multilevel rectifier (HMMR) is proposed in this letter. Different from the aforementioned hybrid topology, HMMR integrates the diode bridge into and MMC directly as one unit. In the proposed topology, the key benefits of MMC are kept, such as modularity, excellent harmonic performance, high reliability and superior power regulation, and weak grid operation performance compared to LCC and DR. However, the arm voltage and current stress are significantly reduced compared with MMC. Particularly at unity power factor, HMMR can reduce SM numbers by 50% due to the utilization of high voltage diode. Thus, both the volume/size and construction cost could be reduced substantially compared with MMC. Similar idea was proposed in [7] and [8], which integrates the thyristor stacks and MMC together. However, compared with the topology in [8], HMMR can achieve even lower power losses and cost in unidirectional ac to dc power conversion, since reliable diodes operating at line-frequency switching are used instead of thyristor. And different from thyristor, diode does not need hold-off time for current commutation. So that the trapezoidal current allocation could be employed to avoid current step in [8] and the harmonics could be reduced. Besides, the HMMR can also work at nonunity power factor if the FB SMs are inserted to support the negative arm voltage stress. But when power factor is very small, the total device number is close to the traditional MMC, which mitigates the benefit of this topology. Besides, most HVdc rectifier stations need to produce active power instead of reactive power. Therefore, only high power factor cases are discussed in this letter.

The rest of this letter is organized as follows. In Section II, the HMMR-based HVdc system is presented, and single-phase operation principle, three-phase current allocation as well as a simple control scheme are presented. Section III shows the

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Jian Liu and Dong Dong are with the Virginia Tech, Blacksburg, VA 24061 USA (e-mail: jianl@vt.edu; dongd@vt.edu).

Di Zhang is with the Naval Postgraduate School, Monterey, CA 93943-5155 USA (e-mail: zhangdi@ieee.org).

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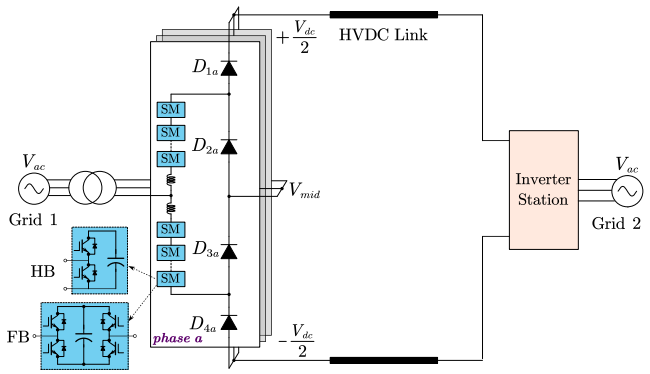

Fig. 1. Structure of HMMR-based HVdc system.

simulation results of a 200-MVA 200-kV HVdc case and the experimental results of a scale-down prototype. Finally, Section IV concludes the letter.

II. System Overview and Operation Principle

A. System Topology

Fig. 1 depicts the topology of proposed HMMR-based HVdc systems. Four HV diode stacks are added to each of original MMC topology, and three-phase midpoints are connected to construct a neutral point. In this way, the arm voltage is no longer determined by only ac voltage $V_{\rm ac}$ and dc voltage $V_{\rm dc}$ as in MMC. Instead, a freedom of midpoint voltage $V_{\rm mid}$ can be utilized to reshape the arm voltage, which makes it possible to reduce the maximum arm voltage.

Different from active switching device which can cut off the current actively [8], the state of diode is determined by the current polarity, controlled by the corresponding arm voltages. Therefore, as shown in Fig. 2, there are four possible working states: *PN* (positive-negative), *PZ* (positive-zero), *ZZ* (zero-zero), and *ZN* (zero-negative) states, for phase *a* of HMMR

$$\begin{aligned}
&V^*_{\rm pa} = 0.5V_{\rm dc} - V_a, V^*_{\rm na} = 0.5V_{\rm dc} + V_a (I_{\rm pa} > 0, I_{\rm na} > 0, PN)\\
&V^*_{\rm pa} = 0.5V_{\rm dc} - V_a, V^*_{\rm na} = V_a - V_{\rm mid} (I_{\rm pa} > 0, I_{\rm na} < 0, PZ)\\
&V^*_{\rm pa} = V_{\rm mid} - V_a, V^*_{\rm na} = V_a - V_{\rm mid} (I_{\rm pa} < 0, I_{\rm na} > 0, ZZ)\\
&V^*_{\rm pa} = V_{\rm mid} - V_a, V^*_{\rm na} = 0.5V_{\rm dc} + V_a (I_{\rm pa} < 0, I_{\rm na} > 0, ZN).
\end{aligned} \tag{1}$$

B. Current Allocation at Unity Power Factor

According to (1), the HMMR arm voltage stress will be minimum if this phase operates at *PZ* state under positive ac voltage and *ZN* state under negative ac voltage. So the polarity of upper and lower currents need to change at the same time with ac voltage, which is the case at unity power factor (PF = 1). Under such condition, a trapezoidal arm current different from [8] can be controlled to toggle the working state of the HMMR phase-leg. The three-phase configuration is presented in Fig. 3 and the corresponding six arm current and voltage waveforms are plotted in Fig. 4. It can be observed that the maximum arm voltage becomes only $0.5V_{\rm dc}$, which means the number of HB SMs can be reduced by half. And it can be easily proved that the current polarity condition can be satisfied for arbitrary modulation index. The sum of midpoint current $I_{\rm mid}$ keeps zero at any time, which means the midpoint voltage is balanced naturally.

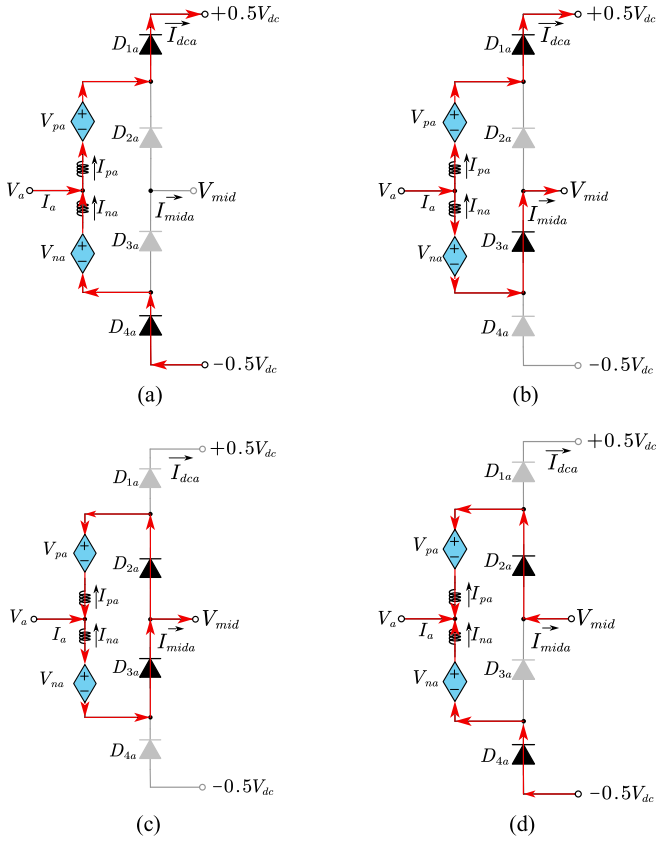

Fig. 2. Four working states of single phase HMMR. (a) PN state. (b) PZ state. (c) ZZ state. (d) ZN state.

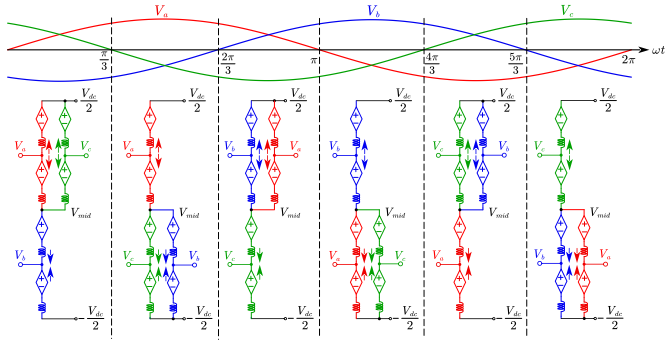

Fig. 3. Three-phase configuration of HMMR under unity power factor.

C. Current Allocation at Nonunity Power Factor

In some applications, it is desired for rectifier to support grid by providing reactive power. Take a specific phase angle difference $\varphi = \pi/6$ as an example. The ac voltage and current of phase *a* is expressed as

$$V_a = V_{\rm ac}\sin(\omega t), I_a = I_{\rm ac}\sin(\omega t + \pi/6) \tag{2}$$

where ωt is the voltage phase angle, and $I_{\rm ac}$ is the amplitude of ac current, respectively. Then the phase *a* arm current and the corresponding arm voltage waveforms gained from (1) are plotted in Fig. 5. It can be seen there is a period of *PN* state,

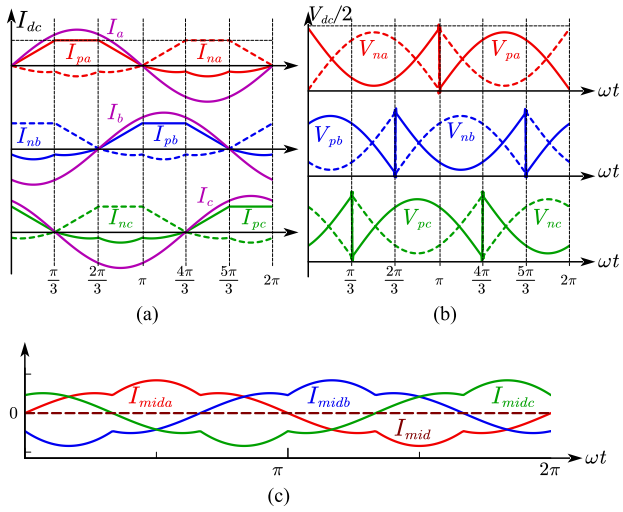

Fig. 4. Arm current, voltage, and midpoint current waveforms at unity power factor. (a) Arm currents. (b) Arm voltages. (c) Three–phase midpoint currents.

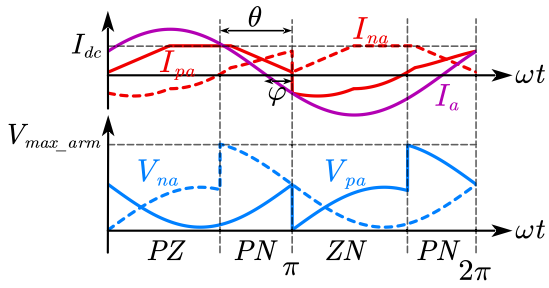

Fig. 5. Phase a arm waveforms at $\varphi = \pi/6$ using old current allocation scheme.

which lasts a duration of θ, and the arm voltage stress becomes

$$V_{\text{stress}} = V_{\text{max\_arm}} = 0.5V_{\text{dc}} + V_{\text{ac}} \sin(\theta)$$
$$\theta = \varphi + \text{a}\sin\left(\frac{I_{\text{dc}}}{I_{\text{ac}}}\right) = \varphi + \text{a}\sin\left[\frac{3M}{4} \cdot \cos(\varphi)\right] \quad (3)$$

where M is the modulation index defined by $2V_{\text{ac}}/V_{\text{dc}}$. So additional HB SMs are needed to provide the extra arm voltage stress, which is closely related to the duration of *PN* state. In order to mitigate the penalty of more SMs, another current allocation scheme is proposed. Take ωt from $\pi - \theta$ to π as an example, it can be divided into three segments. During the first segment ($\pi - \theta$, $\pi - \varphi$), the arm currents of phase a could be defined as (4) to work in *PZ* state instead of *PN* state

$$I_{\text{pa}} = \frac{(\pi - \varphi) - \omega t}{\text{a}\sin(I_{\text{dc}}/I_{\text{ac}})} \cdot I_{\text{dc}} \geq 0, \omega t \in (\pi - \theta, \pi - \varphi)$$
$$I_{\text{na}} = I_{\text{pa}} - I_{\text{ac}} \sin(\omega t + \pi/6) \leq 0. \quad (4)$$

After the determination of phase a arm currents, phase b and c arm currents could also be calculated as

$$I_{\text{pb}} = I_{\text{dc}} - I_{\text{pa}}, I_{\text{nb}} = I_{\text{dc}} - I_{\text{pa}} - I_b$$
$$I_{\text{pc}} = I_{\text{dc}} + I_c, I_{\text{nc}} = I_{\text{dc}}. \quad (5)$$

Then the same current allocation could be applied to the other two phases accordingly, and the three-phase currents are plotted in Fig. 6. When $\varphi = \pi/6$, and the modulation index is close to 1, θ is larger than $\pi/3$ and the difference is represented by $\gamma = \theta - \pi/3$. Since the phase a arm currents during ($\pi - \gamma$, π) have already been determined by phase c, the left range is ($\pi - \varphi$, $\pi - \gamma$). According to (1), a possible solution is

$$I_{\text{pa}} = I_{\text{ac}} \sin(\omega t + \pi/6), I_{\text{na}} \approx 0, \omega t \in (\pi - \varphi, \pi - \gamma). \quad (6)$$

During this period, phase a works as *ZZ* state. A negative arm voltage is required which can be realized by adding FB SMs. Such FB SMs could help improve the system dc fault tolerant capability. Through the same principle, six arm currents of whole cycle are depicted in Fig. 6. It can be seen that this current allocation method does not have any current step as in Fig. 5, so the current regulator design should be easier. Then the corresponding arm voltages could be plotted in Fig. 7, and the arm voltage stress is expressed as

$$V_{\text{stress}} = V_{\text{max\_arm}} - V_{\text{min\_arm}}$$
$$= 0.5V_{\text{dc}} + V_{\text{ac}} [\sin(\varphi) + \sin(\gamma)]. \quad (7)$$

The negative voltage determines the number of FB SMs

$$N_{FB} = V_{\text{ac}} \sin(\varphi)/V_{CSM} \quad (8)$$

where V_{CSM} is the rated dc link capacitor voltage of each SM. Then the number of HB SMs could be derived by subtracting FB part from the positive voltage

$$N_{\text{HB}} = [0.5V_{\text{dc}} + V_{\text{ac}} \sin(\gamma) - V_{\text{ac}} \sin(\varphi)]/V_{\text{CSM}}. \quad (9)$$

It can be seen that the HB number used in this method is smaller than the old current allocation method in (3). Above all, under nonunity power factor condition, the trapezoidal current allocation method uses only HB SM, which has superior modularity, but suffers from the current step and more devices at nonunity power factor. The second current allocation method uses both HB and FB SMs, which improves dc fault tolerant capability and has lower conduction loss.

In order to have the full dc fault blocking capability (e.g., pole-pole fault), all IGBTs are switched OFF and the FB capacitors of two series arms should withstand the ac side line-to-line voltage.

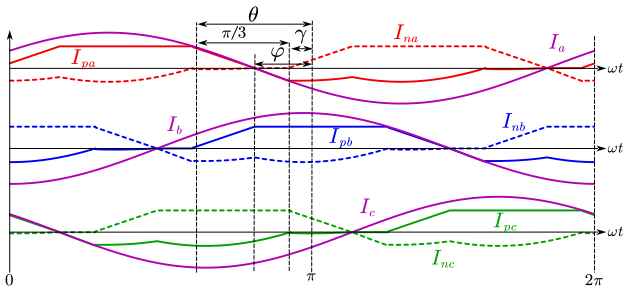

Fig. 6. Current waveforms of six arms with $\varphi = \pi/6$ using proposed method.

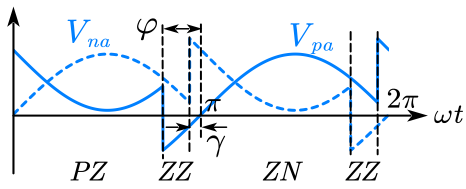

Fig. 7. Phase a arm current waveforms with $\varphi = \pi/6$ using proposed method.

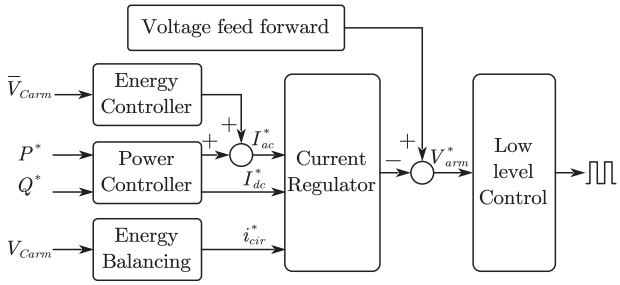

Fig. 8. Block diagram of employed control method.

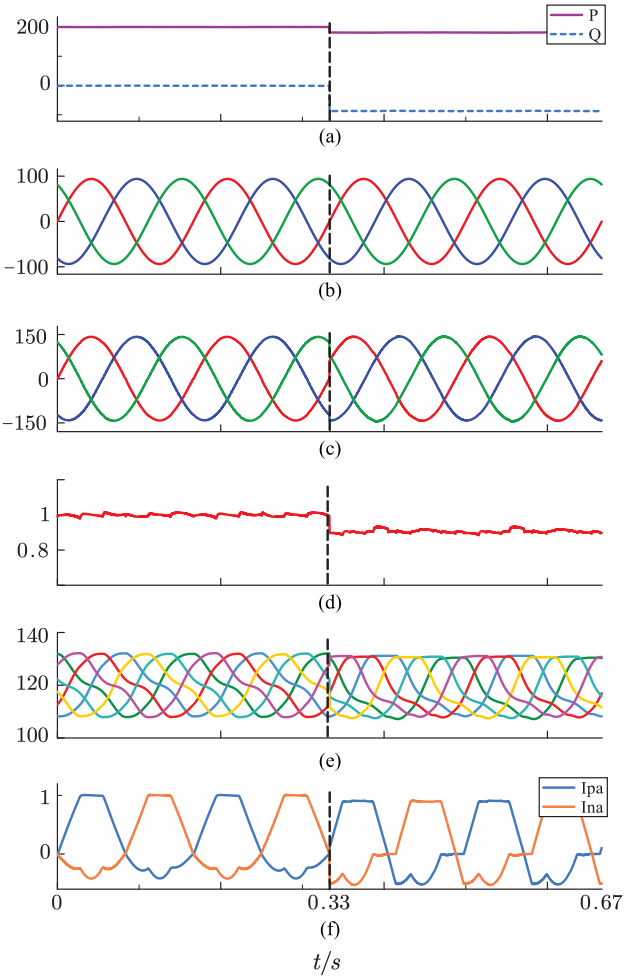

Fig. 9. Simulation waveforms and transition from PF = 1 to PF = 0.9. (a) Active and reactive power [MW]. (b) Input three phase voltages [kV]. (c) Input three phase currents [kA]. (d) Output dc current I_{dc} [kA]. (e) Sum of arm capacitor voltage v_{Carm} [kV]. (f) Arm current of phase a [kA].

So, the minimum FB SMs number will be

$$N_{\text{FB\_dc\_fault}} = \frac{\sqrt{3}V_{\text{ac}}}{2V_{\text{CSM}}}. \tag{10}$$

D. Control Method

Since this complex topology requires a specific paper to discuss the control strategy and parameter design, this letter only gives a general control scheme of HMMR as shown in

Fig. 8. The power controller and energy controller used to regulate the power exchanged with ac and dc grid is almost

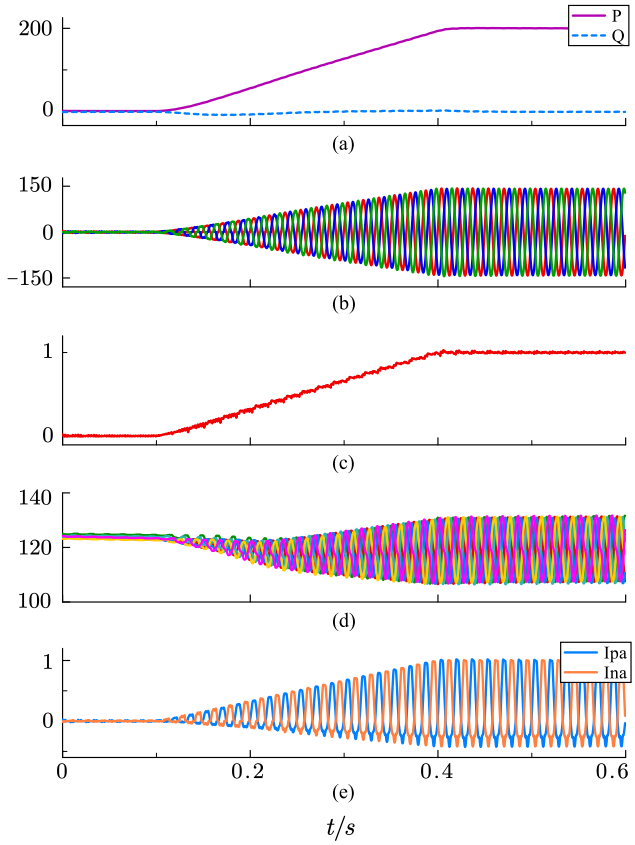

Fig. 10. Simulation waveforms of active power increasing process. (a) Active and reactive power [MW]. (b) Input three phase currents [kA]. (c) Output dc current I_{dc} [kA]. (d) Sum of arm capacitor voltage v_{Carm} [kV]. (e) Arm current of phase a [kA].

TABLE I
SPECIFICATIONS OF HMMR-BASED HVDC CONVERTER

Parameters	Values	Parameters	Values
Ac Voltage	115 kV	FB number per arm	38
Power rating	200 MVA	HB number per arm	22
Dc voltage	200 kV	SM capacitance	3 mF
Power factor	0.9 ~ 1	Arm inductor	5 mH
SM capacitor voltage	2 kV	Sampling frequency	15 kHz

the same with traditional MMC. But, the circulating current reference generated by arm energy balancing is different because the arm voltage of HMMR contains higher order harmonics. The current loop needs to track the reference shown in Fig. 6 and the arm voltage is synthesized by feed-forward voltage and current loop output. Then, the low level control is responsible for multilevel modulation and the SM capacitor voltage balancing.

III. SIMULATION AND EXPERIMENTAL RESULTS

To better illustrate the principle of the proposed HMMR and control method, an HVdc simulation case was performed and the electrical parameters are listed in Table I. The steady state waveforms at unity and 0.9 PF are shown in Fig. 9. The ac and dc currents are both satisfactory, and the arm currents fit well with the designed allocation shape in Fig. 6, which indicates the good performance of current controller. The transient process of ramping up active power is shown in Fig. 10. It can be seen that the capacitor voltage ripple increases under higher power operation conditions but the average value keeps the same,

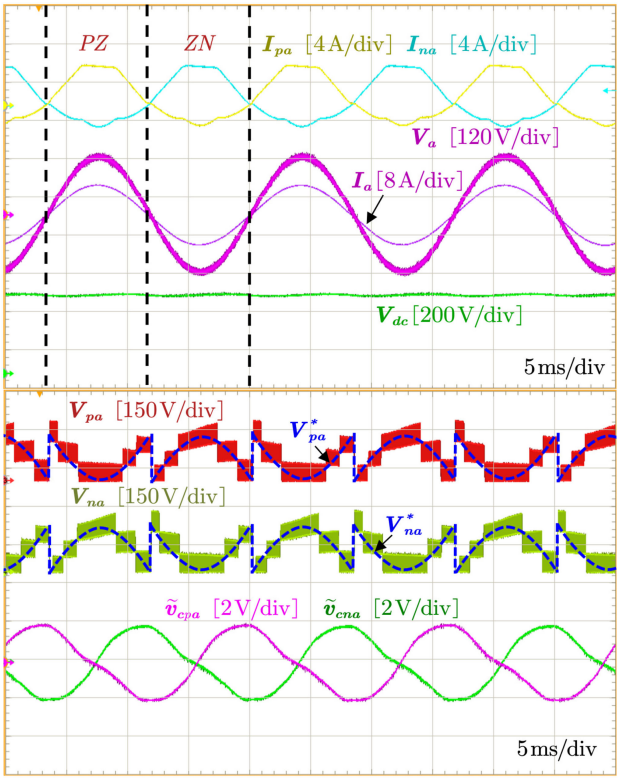

Fig. 11. Experimental waveforms of scale-down prototype phase *a*.

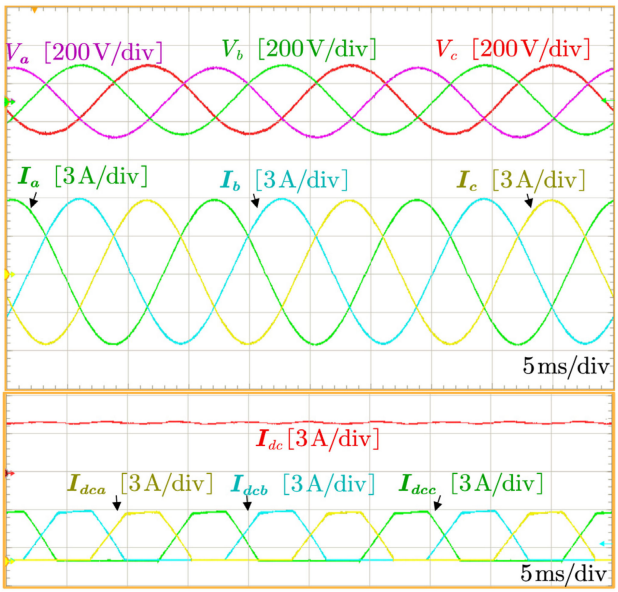

Fig. 12. Three-phase experimental waveforms.

which demonstrates the effectiveness of the proposed arm energy balancing algorithm.

In addition to the simulation, a scale-down prototype with dc resistor load was also built. The ac voltage amplitude is 180 V and output dc voltage is 400 V, each arm has three series HB SMs with 75 V dc-link voltage. The arm voltage and current waveforms of phase *a* are given in Fig. 11. The phase-shift (PS) modulation is employed to generate the four-level arm voltage. As explained earlier, this phase works in PZ and ZN state alternatively, which can reduce half voltage stress reduction seen in arm voltage reference waves. It should be noted that even if the number of SMs is half of MMC, the number of ac voltage level is still the same due to the extra three-level wave created by the diode stack and midpoint. The capacitor voltage ripple of one SM from upper and lower arms is also measured. And the dc bias is removed to highlight the ripple shape, which is same with simulation results in Fig. 9.

The three-phase voltage and current waveforms are shown in Fig. 12. The input ac currents I_a, I_b, and I_c have a very low THD. I_{dca}, I_{dcb}, and I_{dcc} are each phase output dc bus current shown in Fig. 2. It can be seen that they are trapezoidal shape with 120° phase shift, which keeps the sum dc output current stable and small ripple.

IV. Conclusion

This letter proposes a novel HMMR topology as an ac–dc rectifier for HVDdc power delivery and other unidirectional ac–dc power conversion applications. While retaining the advantages of traditional MMC, HMMR can save up to 50% IGBT SMs at unity power factor without sacrificing the ac side quality. The use of line-frequency commutated HV diodes in HMMR offers a significant improvement of efficiency, reliability, power-density, and cost reduction. By leveraging the SMs, the HV diodes commutation can be achieved without the involvement of grid-side voltage, and energy balancing can be still achieved. Even if at nonunity power factor, HMMR can still work with only HB SMs and save half of the required capacitors compared with MMC. And if the FB SMs are inserted, HMMR can support full reactive power to grid and have dc fault tolerant capability.

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