Fault Characteristics and Riding-Through Methods of Dual Active Bridge Converter Under Short-Circuit of the Load

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***Abstract*—The fault riding-through (FRT) capability is a key problem in the dc distribution network. In order to achieve the FRT, it is necessary to analyze the worst-case scenario (WCS) of the short-circuit transient process of distribution components. This article analyzes the whole fault characteristic in a dual active bridge (DAB) in the WCS when a short-circuit occurs on the load at different locations that has not been considered in the existing literature. The short-circuit in the WCS can cause various fault current in the whole circuit, introducing a risk of the overcurrent. In order to overcome this problem, FRT-based methods are proposed in this article. One of the methods is to block the power switches for a certain period and restart the circuit, and another is to add a series output inductor with a reasonable inductance. By these methods, the faulty branch can be cut off by the corresponding circuit breaker in time. The results are verified by the simulations on a 50-kW DAB by MATLAB/Simulink, and the experiments on a 3-kW prototype. The results presented in this article provide a theoretical reference for FRT of DABs.**

***Index Terms*—Dual active bridge (DAB), fault riding-through, short-circuit, transient process.**

NOMENCLATURE

FRT	Fault riding-through.
WCS	Worst-case scenario.
DAB	Dual active bridge.
DPS	Double phase shift.
VTR	Voltage transfer ratio k_v.
CB	Circuit breaker.
F1	Fault type 1 (Pole-to-pole fault).
F2	Fault type 2 (Cable-to-cable fault).
N	Transfer ratio of transformer.
v_2	Voltage of output capacitor.
V_1	Constant voltage of input capacitor.
V_2	Voltage of output capacitor in normal state.
k_v	Voltage transfer ratio $k_v = V_1/NV_2$.
f_s	Switching frequency.
T_s	Half of switching period.
i_L	Current of L_t.
n	Number of the load branches.
i_{si} $(i = 1, 2 \dots n)$	Current in load branch i.
i_s	Sum current of all loads.
i_2	AC output current before C_2.
I_2	Average value of i_2.
P_N	Maximum transmitted power of DAB.
I_{2N}	Maximum output current and basis value of normalization of DAB.
d_1	Inner phase-shift.
d_2	Outer phase-shift.
v_{AB}	AC side voltage of H1.
v_{CD}	AC side voltage of H2.
v_L	Voltage drop of L_t.
R_s	Short-circuit resistance.
t_a	Decay duration of v_2.
$t_0 \sim t_8$	Turning moment of i_L.
$P_s(k)$	Switching period in which fault occurs.
t_k	Fault moment.
$t_{k0} \sim t_{k8}$	Turning moment of i_L in $P_s(k)$.
$t_{k(s)}$	Duration between t_k and t_{k0}.
I_{tr+}	Transient maximum positive value of i_L.
I_{tr-}	Transient maximum negative value of i_L.
i_{dc}	DC bias current of i_L.
I_{dc}	Initial value I_{dc} of i_{dc}.
I_{trm}	Transient current stress.
G_{trm}	P.u. value of I_{trm}.
I_{s2}	Steady current stress.
G_{s2}	P.u. value of I_{s2}.
τ_t	Decay time constant of i_{dc}.
L_s	Inductance in short-circuit loop.
$I_{\max}$	Peak value of i_s.
R_e	Equivalent series resistor of D_4–D_8.
τ_s	Decay time constant of i_s.
I_B	Value of i_L when blocking.
t_{bd}	Blocking duration.
L_{se}	Series inductance.
L_{line}	Inductance of cable line.

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I. INTRODUCTION

IN THE dc power distribution system applications, a dc transformer supplies several branches of the load, so the reliability of the dc transformer is essential for sustainable operation,

especially when a short-circuit fault of the load occurs. To ensure the sustainable operation of the converter, it is necessary to apply the fault riding-through (FRT) method when facing the fault condition. Unlike the short-circuit protection, the purpose of FRT is to limit the fault current and cut off the fault load branch in time. After a fault is detected, the FRT process is not to shut down the system, but to provide a fault criterion current to cut off the fault load branch and restore the power supply as quickly as possible. When the FRT is considered, the fault current that is dangerous and not helpful for the FRT should be eliminated as soon as possible. Meanwhile, if the output current can be controlled within a certain range, it can be treated as a fault current criterion to trigger the circuit breaker (CB) so that the fault branch can be cut off, which is crucial for system restoring [1]–[3].

The proliferation of renewable and storage energies requires using a high-performance isolated bidirectional dc–dc converter as a dc transformer in the power distribution system [4], [5]. The DAB converter is suitable for constructing dc transformers due to its high power density, voltage step-up/down, bidirectional power flow, electrical isolation, and zero-switching capability [6], [7]. In order to achieve the FRT of a dc transformer built by DABs, it is necessary to analyze the fault characteristics and the FRT methods of the DAB in the WCS. The fault characteristics include the external and internal voltage, the external and internal current, which appear both in the fault transient process and in the fault steady state, respectively.

The transient process of a DAB can generate dc bias in the inductor current, and then, the risk of transient overcurrent occurs. The transient process caused by a short-circuit fault also has the same phenomenon. In the worst case, the current can saturate the magnetic cores of the transformer and inductor, thus leading to the converter failure [8]. In the steady state, putting a dc blocking capacitor in series with the transformer winding can eliminate the dc bias of inductor current caused by the mismatch of switching devices and the asymmetry of switching signals [9], but this capacitor is not helpful for suppressing the dc bias in the transient process. Meanwhile, it is unsuitable for high-power applications since they increase the volume and cost of the converter and slows down the dynamic response [10]. The dc bias current can be limited by reducing the voltage dc bias arising from the discretion of power semiconductors [11]. In the closed-loop control methods, duty cycles of phase-legs can be adjusted in diverse ways to reduce the dc bias and achieve the flux balance [12]–[19]. In [20], Yao *et al.* proposed the predictive bias suppression method to achieve both current and flux balance. It should be noted that all the mentioned works study only the sudden change in the phase-shift, which represents the transient conditions without a fault. However, there has been no detailed analysis of the transient process of DAB after a short-circuit fault. The transient process after a short-circuit fault differs significantly from that without a fault because the output voltage drops quickly in the fault condition, and it is impossible to use these methods in the transient process. The current-fed circuit can help to eliminate the output current harmonics and minimize the dc offset of the transformer [21], but the voltage-fed topologies are advantageous over the current-fed topologies with respect to reliability and cost [22].

As for the research of fault characteristics, in [23], all fault types that can occur in dc–dc converters were briefly summarized without providing a specific analysis. In [24]–[26], the prospects of a three-phase DAB to limit the short-circuit current in the future dc grids were analyzed. Furthermore, in [27], it was shown that the short-circuit fault clearance ability could be improved on the input side by adding the full-bridge circuits to the dc converter, but the fault at the output terminal was not considered. Both the pole-to-pole and the cable-to-pole dc short-circuit faults of a DAB were analyzed in [28] and [29]. On the one hand, in [28], the converter would be shut down immediately once a short-circuit happened, and only the transient process of the current in a power cable was considered. However, shutting down a DAB is not allowed in the FRT. Moreover, the results of [28] are not applicable to the condition of short-length power cables. On the other hand, in [29], the focus was on the surge current in a power cable without considering the internal circuit. In [30], the pole-to-pole short-circuit fault of a DAB was analyzed, and the root mean square (rms) of the internal current in the steady state after the fault was calculated. In [31], only the fundamental component of the internal current in the steady state after the fault was considered, while the transient process was ignored, too. In [32], a quasi-three-level modulation can be applied to achieve ZVS and ensure there is no overcurrent after the short-circuit fault, however, there is no solution to deal with FRT.

As for the research of FRT methods, using inductor on output terminals is an acceptable choice, since it can suppress the peak fault current [28], [29], [31]. However, the range of its inductance value has not been analyzed. TABLE I summarizes the existing countermeasures mentioned above for short-circuit fault. So far, to the best of authors' knowledge, there has been no detailed study on all the fault characteristics and the reveal of the WCS in DAB, and none short-circuit FRT-based method has been discussed in the literature.

The double phase shift (DPS) modulation is widely used in DABs because of its flexible adjustment capabilities and extensive optimization ranges [33]–[36]. Therefore, this article first analyzes the fault characteristics of the transient process of a DAB using the DPS modulation with different fault types, the pole-to-pole fault (F1), and the cable-to-cable fault (F2). Then, this article puts forward the FRT methods.

The situation where the short-circuit resistance is extremely small is assumed to obtain the WCS. The voltage close-loop controls are necessary for DAB. However, it is impossible to analyze the fault characteristics for all close-loop control types, and it has been recognized that all close-loop control types will undoubtedly increase the transmission power and inductor current after a fault occurs, thus increasing the risk of overcurrent. Therefore, the voltage controller should be shut down immediately when a fault is detected, so this article analyzes the fault characteristics under the open-loop control. During the fault, the transient process of the internal circuit is related to the falling slope of the output voltage, and different fault moments result

TABLE I
COMPARISON OF EXISTING COUNTERMEASURES FOR SHORT-CIRCUIT FAULT IN DC/DC CONVERTER

Schemes	Advantages	Disadvantages
Fault location on the cable [3][28]	The fault location can be achieved by using the inherent characteristics of RLC resonance	Only the external circuit is analyzed, and the internal circuit is ignored
No scheme is used since the final steady state is safe [24][30]	It shows the DAB characteristics of safety in steady state	The risk in fault transient process is ignored
Using DC reactor on the output terminal [28][29][31][37]	1. Constrain the peak fault current 2. Delay the occurrence of surge current through DAB diodes	1. Only external circuit was considered 2. The selection of inductance is various
Adding the full-bridge circuits [27]	The short-circuit fault clearance ability could be improved on the input side	The fault at the output side was ignored
A novel quasi-three-level modulation [32]	1. Realize ZVS 2. Ensure the phase angle to result in no overcurrent when fault occurs	No method to deal with removing the fault

in different fault characteristics, which introduces difficulties in the analysis of the transient process.

Based on the fault characteristics, this article puts forward three FRT methods. In the first method, the power switches are blocked for a few switching periods as soon as the fault was detected to decay the transient current, and the driving signals are restored thereafter for DAB to generate a fault criterion current, which can trigger the CB to cut off the fault branch. It should be noted that the block of the drive signals is not equal to the shutdown of converter. Shutdown means that the converter stops working completely and cannot output any voltage or current until the start command is received again. In contrast, the block of drive signals turns OFF the power switches for a few switching periods only, so the DAB can output desired current as soon as the drive signals are restored. In the second method, only a series inductor with a reasonable inductance is added to the output side, as a result, the internal risks are avoided, meanwhile, a fault criterion current is obtained to trigger the CB and the fault branch can be cut off, then the FRT can be achieved. The third method is putting a CLC filter on the output terminal and this is an extension of the second method.

The remaining of the article is organized as follows. Section II introduces a DAB and classifies the short-circuit types. Section III analyzes the transient process of the F1 fault, and Section IV analyzes the transient process of F2 fault. Section V introduces the methods of FRT, and Section VI validates the analysis results of the transient process of the F1 and F2 faults by simulations on a 50-kW, 1000/375-V DAB converter, and experiments on a 3-kW, 400/250-V prototype, respectively; the FRT scheme is also validated by the simulation. Finally, Section VII draws the conclusion.

II. SHORT-CIRCUIT FAULT TYPES OF DAB

The topology and short-circuit fault types of a DAB are shown in Fig. 1, where a high-frequency transformer T with a ratio of N:1 links two full-bridges denoted as H1 and H2, enabling the converter to conduct the dc–ac–dc conversion. The internal circuit includes the transmitted inductor L_t, the equivalent series resistor R_t, and two full-bridges H1 and H2,

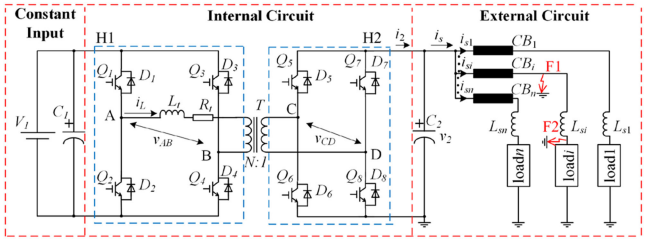

Fig. 1. Topology and short-circuit fault types of a DAB.

which are implemented by power switches Q_1–Q_4 and Q_5–Q_8, respectively, and their antiparallel diodes are D_1–D_8. The input side is connected to the dc grid, and the voltages of input capacitor C_1 are constant and denoted as V_1. There are n parallel branches of power cables connecting n load branches on the output side of the DAB; the voltage of output capacitor C_2 is denoted as v_2, and it is equal to V_2 in the normal state. The voltage transfer ratio (VTR) k_v of a DAB is expressed as V_1/NV_2. The switching frequency is denoted as f_s, and T_s represents half of the switching period. The current that flows through L_t is denoted as i_L, and in this article, it is named the internal current. The output current i_s represents the sum of all load branch currents, that is, $i_s = \sum i_{si}$ $(i = 1, 2, \ldots, n)$. A distribution unit is installed on the output side of the converter, which contains the CBs. Each load branch connects to the converter through a CB [36], [37].

There are four operating modes of DPS modulation due to different expressions of the transmitted power [4], which depends on a combination of the inner phase-shift ratio d_1 and the outer phase-shift ratio d_2, as given by (1). In (1), P_N denotes the maximum transmission power and also the base value used in the power normalization. The d_1 represents the phase-shift ratio between $Q_1(Q_5)$ and $Q_4(Q_8)$, and the d_2 represents the phase-shift ratio between Q_1 and Q_5. Further, the current before C_2 is denoted as i_2, and its average value is denoted as I_2, which can be regarded as a controlled current source controlled by the phase-shift ratios, as given by (2). Since the ac component of i_2 flows through C_2, the total output current is equal to I_2 in the steady state. The maximum value of I_2 is denoted as I_{2N}, and it represents the maximum output current of a DAB, which is also

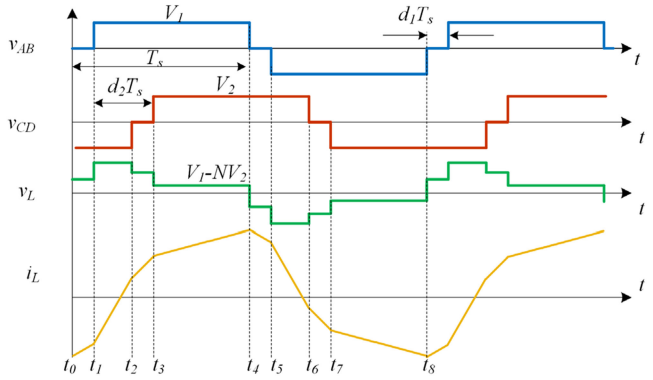

Fig. 2. Steady-state waveforms of a DAB in mode 2.

the base value for the current normalization. The expressions of P_N and I_{2N} are given by (3)

$$P = P_N \times \begin{cases} 2(1-d_2)(1+d_2-2d_1) & \text{Mode1}: d_2 > d_1, d_1+d_2 \geq 1 \\ 2\left(-d_1^2-2d_2^2+2d_2\right) & \text{Mode2}: d_2 > d_1, d_1+d_2 < 1 \\ 2(2-2d_1-d_2)\,d_2 & \text{Mode3}: d_2 \leq d_1, d_1+d_2 < 1 \\ 2(1-d_1)^2 & \text{Mode4}: d_2 \leq d_1, d_1+d_2 \geq 1 \end{cases} \tag{1}$$

$$I_2 = P/V_2 \tag{2}$$

$$\begin{cases} P_N = NV_1V_2/8L_tf_s \\ I_{2N} = NV_1/8L_tf_s. \end{cases} \tag{3}$$

The steady-state waveforms of a DAB in mode 2 are shown in Fig. 2, where v_{AB} represents the ac side voltage of H1, and v_{CD} represents the ac side voltage of H2. The voltage drop across L_t is denoted as v_L and expressed as $v_L = v_{AB} - Nv_{CD}$.

Before the fault, in the initial steady state, the dc bias of i_L is zero, and values of i_L at the turning points $t_0 - t_3$ in a half switching period are given by (4); the expressions of i_L at $t_4 - t_7$ can be obtained using the symmetry of the steady-state current waveform

$$\begin{cases} i_L(t_0) = [-V_1T_s(1-d_1) - NV_2T_s(d_1+2d_2-1)]/2L_t \\ i_L(t_1) = [-V_1T_s(1-d_1) - NV_2T_s(2d_2-d_1-1)]/2L_t \\ i_L(t_2) = [-V_1T_s(d_1-2d_2+1) - NV_2T_s(d_1-1)]/2L_t \\ i_L(t_3) = [-V_1T_s(-d_1-2d_2+1) - NV_2T_s(d_1-1)]/2L_t. \end{cases} \tag{4}$$

In power distribution systems, most of the short-circuit faults occur through cables, so the short-circuit loop contains cable inductance. However, there is still a possibility that the most extreme short-circuit fault occurs when the length of the power cable in the fault loop is near zero. Therefore, two types of short-circuit faults of a branch are considered in this article: the F1 and the F2 as illustrated in Fig. 1.

III. F1: Pole-to-Pole Short-Circuit

A. Transient Process of Output Circuit

The pole-to-pole short-circuit represents the case where short-circuit fault occurs on the terminals of C_2, and the inductance of a power cable in the short-circuit discharging loop is close to zero. When F1 occurs at branch i, the discharging loop is shown in Fig. 3.

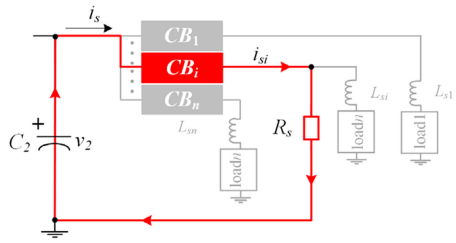

Fig. 3. Discharging loop of a DAB under F1.

In F1, R_s represents the short-circuit equivalent resistance, including the internal resistance of the capacitor C_2 and the bus. Since the loop impedance of branch i is the smallest, it can be approximated that $i_s = i_{si}$. The differential equation and the initial value of v_2 are given by (5), which can be used to derive the expressions of v_2 and i_s after the fault, which are given by (6). The speed of the discharging process is negatively correlated with the values of C_2 and R_s, and the peak value of the discharge current is positively correlated with them. With a fixed C_2, the smaller the value of R_s is, the faster the short-circuit process, and the higher the peak value of i_s will be. The comprehensive analysis of the impact of different values of R_s on the discharge process has been given in [28], and a detailed analysis will not be presented in this article.

This article focuses on the WCS, which means that the value of R_s is relatively small. In such a case, v_2 will decrease to zero instantaneously, so its decay time t_a is approximately zero; meanwhile, i_s will reach a large peak valued about $(V_2/R_s - I_2)$ in a short time. In the dc power distribution system, the normal mechanical breakers are used due to their low cost. A suitable current with a required duration is needed to trigger the beaker [31], and this current is denoted as a fault current criterion in this article. However, the discharge process of F1 is too rapid to trigger breaker CB_i. Therefore, if no FRT scheme is applied, it will be difficult to cut off the fault branch

$$\begin{cases} C_2(\mathrm{d}v_2/\mathrm{d}t) = i_2 - v_2/R_s \\ v_2(t_{k-}) = V_2 \end{cases} \tag{5}$$

$$\begin{cases} v_2(t) = i_2R_s + (V_2 - i_2R_s)\,e^{-(t-t_k)/R_sC_2} \\ i_s(t) = i_2 + (V_2/R_s - I_2)\,e^{-(t-t_k)/R_sC_2}. \end{cases} \tag{6}$$

B. Transient Process of Internal Circuit

As displayed in Fig. 3, when F1 occurs, the discharge current of C_2 will not flow through the internal circuit. However, the sudden drop of v_2 will cause a sudden change in v_L, which leads to the transient process of i_L. When the DPS modulation is used, there are four operating modes, each of which has eight switching states, so there will be 32 possibilities for the fault moments, resulting in different transient processes that should be fully considered.

Assume the fault occurred at a switch state of mode 2, as shown in Fig. 4, the short-circuit occurs in the fault switching period $P_s(k)$, the turning points of inductor current under the

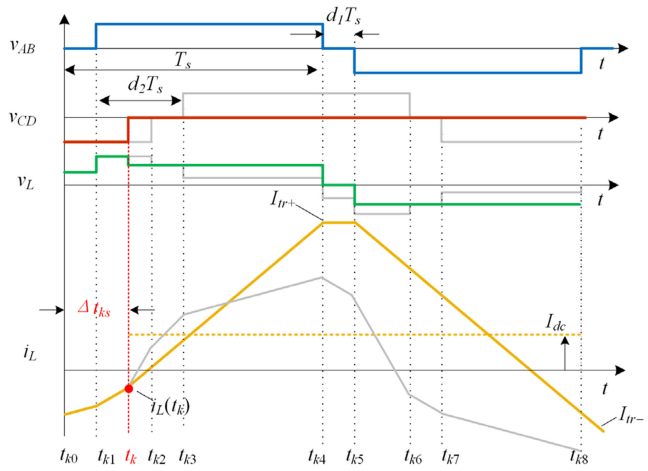

Fig. 4. Transient waveforms of a DAB after F1 in mode 2.

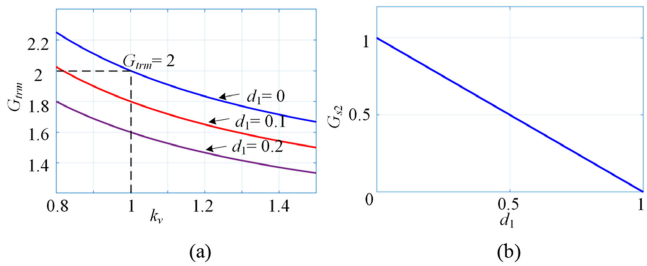

Fig. 5. Curve of p.u. current value. (a) G_{trm}. (b) G_{s2}.

steady state before fault are $t_{k0} - t_{k8}$, t_k represents the fault moment, and Δt_{ks} denotes the time between moments t_k and t_{k0}. When t_k is between t_{k1} and t_{k2}, the inductor current value at t_k is given by

$$i_L(t_k) = i_L(t_1) + (V_1 + nV_2)(t_k - t_{k1})/L_t. \tag{7}$$

Then, the value of v_L in $P_s(k)$ can be expressed by (8). Further, due to the polarity of v_L, i_L will reach the maximum positive value I_{tr+} at t_{k4}, and the maximum negative value I_{tr-} at t_{k8}, which is expressed by (9). Furthermore, the transient current stress of i_L denoted as I_{tr} is given by (10)

$$v_L = \begin{cases} V_1 & t_k \le t < t_{k4} \\ 0 & t_{k4} \le t < t_{k5} \\ -V_1 & t_{k5} \le t < t_{k8} \end{cases} \tag{8}$$

$$\begin{cases} I_{tr+} = \frac{nV_2}{2L_t}\left[T_s(1 - d_1 - 2d_2 - d_1k_v + k_v) + 2t_k\right] \\ I_{tr-} = \frac{nV_2}{2L_t}\left[T_s(1 - d_1 - 2d_2 + d_1k_v - k_v) + 2t_k\right] \end{cases} \tag{9}$$

$$I_{tr} = \max\left(|I_{tr+}|, |I_{tr-}|\right). \tag{10}$$

Due to the asymmetry of v_L in $P_s(k)$, the integral of i_L is not zero anymore. The dc bias current i_{dc} appears in $P_s(k)$, marking i_L enter the transient process, so the initial value of i_{dc}, which is denoted as I_{dc}, can be expressed by (11). Current i_{dc} is uncontrollable and decays naturally with the time constant of $\tau_t = L_t/R_t$ since v_{AB} is an ac quantity, as given by (12). Resistance R_t denotes the equivalent series resistance of inductor L_t

$$\begin{aligned} I_{dc} &= (I_{tr+} + I_{tr-})/2 \\ &= nV_2\left[T_s(1 - d_1 - 2d_2) + 2t_k\right]/(2L_t) \end{aligned} \tag{11}$$

$$i_{dc} = I_{dc}e^{-t/\tau_t}. \tag{12}$$

In this article, the period before a fault is considered as the initial steady state, and the period after the fault in which the peak of i_L is still changing dynamically is considered as the transient state. Finally, when i_L reaches a stable state again, that period is considered as the final steady state.

When the analysis is extended to all the situations, the results show that when t_k is between t_{k0} and t_{k4}, i_L always reaches the maximum positive value I_{tr+} at t_{k4}, and the maximum negative value I_{tr-} at t_{k8} due to the polarities of v_L. On the contrary, when t_k is between t_{k4} and t_{k8}, i_L always reaches the maximum negative value I_{tr-} at t_{k8}, and the maximum positive value I_{tr+} at t_{k4} in the next switching period. The expressions of I_{tr+}, I_{tr-}, and I_{dc} in all cases are derived, and they are listed in Table II; in these expressions, A, B, C, and M are given by (13). The corresponding expressions of $t_{k0} - t_{k8}$ are given in Table III.

In the final steady state, the value of i_L depends only on v_{AB}, so the steady current stress I_{s2} can be expressed and normalized as p.u. value G_{s2}, as given by (14). The value of G_{s2} is lower than one since $0 \le d_1 \le 1$, as shown in Fig. 5(b), indicating that there is no internal overcurrent in the final steady state, this conclusion is consistent with [24], [30]. However, it does not mean that there is no need to apply FRT method to DAB. According to expressions given in Table II, the maximum transient current I_{trm} is normalized as the p.u. value G_{trm}, as given by (15), and G_{trm} is defined by d_1 and k_v. The value of G_{trm} decreases with the increase in d_1 at constant k_v or increase in k_v at constant d_1. Generally, the rated power of a circuit is about 0.7 of the maximum power, that is $0.7P_N$, and the rated output current is set at $0.7I_{2N}$. In general, the semiconductor switches are selected according to twice of the rated condition, which is $1.4I_{2N}$. However, as shown in Fig. 5(a), the value of G_{trm} is greater than 1.4 in most cases, which indicates an internal overcurrent risk in the transient state. Besides, the value of I_{trm} and the decay duration of i_{dc} are two key factors for overcurrent evaluation. Since the decay time of i_{DC} is approximately equal to five times of τ_t, the smaller the value of R_t is, the longer the overcurrent will last, and the power switches will be subjected to more dangers. Meanwhile, if L_t is designed according to the steady state, it suffers from a

$$\begin{cases} A = 1 - d_1 - 2d_2 \\ B = 1 + d_1 + 2d_2 \\ C = -d_1k_v + k_v \\ M = NV_2/2L_t \end{cases} \tag{13}$$

$$\begin{cases} I_{s2} = V_1T_s(1 - d_1)/2L_t \\ G_{s2} = 1 - d_1 \end{cases} \tag{14}$$

$$\begin{cases} I_{trm} = NV_2T_s(1 - d_1)(1 + k_v)/2L_t \\ G_{trm} = (1 + 1/k_v)(1 - d_1) \end{cases} \tag{15}$$

TABLE II
TRANSIENT CURRENT STRESS AT DIFFERENT $T_{k(s)}$

I_{tr+}	I_{tr-}	I_{dc}
Mode 1		
$M\times\begin{cases} T_s(d_1-1)(1-k_v) & t_{k0}\le t_k<t_{k1}\\ [T_s(A+C)+2t_k] & t_{k1}\le t_k<t_{k3}\\ T_s(1-d_1)(1+k_v) & t_{k3}\le t_k<t_{k5}\\ [T_s(B+C)-2t_k] & t_{k5}\le t_k<t_{k7}\\ T_s(d_1-1)(1-k_v) & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} T_s(d_1-1)(1+k_v) & t_{k0}\le t_k<t_{k1}\\ [T_s(A-C)+2t_k] & t_{k1}\le t_k<t_{k3}\\ T_s(1-d_1)(1-k_v) & t_{k3}\le t_k<t_{k5}\\ [T_s(B-C)-2t_k] & t_{k5}\le t_k<t_{k7}\\ T_s(d_1-1)(1+k_v) & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} T_s(d_1-1) & t_{k0}\le t_k<t_{k1}\\ AT_s+2t_k & t_{k1}\le t_k<t_{k3}\\ T_s(1-d_1) & t_{k3}\le t_k<t_{k5}\\ BT_s-2t_k & t_{k5}\le t_k<t_{k7}\\ T_s(d_1-1) & t_{k7}\le t_k<t_{k8}\end{cases}$
Mode 2		
$M\times\begin{cases} [T_s(A+C)+2t_k] & t_{k0}\le t_k<t_{k2}\\ T_s(1-d_1)(1+k_v) & t_{k2}\le t_k<t_{k3}\\ [T_s(B+C)-2t_k] & t_{k3}\le t_k<t_{k6}\\ T_s(d_1-1)(1-k_v) & t_{k6}\le t_k<t_{k7}\\ [T_s(A+C-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} [T_s(A-C)+2t_k] & t_{k0}\le t_k<t_{k2}\\ T_s(d_1-1)(k_v-1) & t_{k2}\le t_k<t_{k3}\\ [T_s(B-C)-2t_k] & t_{k3}\le t_k<t_{k6}\\ T_s(d_1-1)(1+k_v) & t_{k6}\le t_k<t_{k7}\\ [T_s(A-C-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} (AT_s+2t_k) & t_{k0}\le t_k<t_{k2}\\ T_s(1-d_1) & t_{k3}\le t_k<t_{k3}\\ (BT_s-2t_k) & t_{k3}\le t_k<t_{k6}\\ T_s(d_1-1) & t_{k6}\le t_k<t_{k7}\\ [T_s(\mathrm{A}-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$
Mode 3		
$M\times\begin{cases} [T_s(A+C)+2t_k] & t_{k0}\le t_k<t_{k1}\\ T_s(1-d_1)(1+k_v) & t_{k1}\le t_k<t_{k3}\\ [T_s(B+C)-2t_k] & t_{k3}\le t_k<t_{k5}\\ T_s(d_1-1)(1-k_v) & t_{k5}\le t_k<t_{k7}\\ [T_s(A+C-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} [T_s(A-C)+2t_k] & t_{k0}\le t_k<t_{k1}\\ T_s(d_1-1)(k_v-1) & t_{k1}\le t_k<t_{k3}\\ [T_s(B-C)-2t_k] & t_{k3}\le t_k<t_{k5}\\ T_s(d_1-1)(1+k_v) & t_{k5}\le t_k<t_{k7}\\ [T_s(A-C-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} (AT_s+2t_k) & t_{k0}\le t_k<t_{k1}\\ T_s(1-d_1) & t_{k1}\le t_k<t_{k3}\\ (BT_s-2t_k) & t_{k3}\le t_k<t_{k5}\\ T_s(d_1-1) & t_{k5}\le t_k<t_{k7}\\ [T_s(\mathrm{A}-4)+2t_k] & t_{k7}\le t_k<t_{k8}\end{cases}$
Mode 4		
$M\times\begin{cases} T_s(d_1-1)(1-k_v) & t_{k0}\le t_k<t_{k1}\\ [T_s(A+C)+2t_k] & t_{k1}\le t_k<t_{k2}\\ T_s(1-d_1)(1+k_v) & t_{k2}\le t_k<t_{k5}\\ [T_s(B+C)-2t_k] & t_{k5}\le t_k<t_{k6}\\ T_s(d_1-1)(1-k_v) & t_{k6}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} T_s(d_1-1)(1+k_v) & t_{k0}\le t_k<t_{k1}\\ [T_s(A-C)+2t_k] & t_{k1}\le t_k<t_{k2}\\ T_s(1-d_1)(1-k_v) & t_{k2}\le t_k<t_{k5}\\ [T_s(B-C)-2t_k] & t_{k5}\le t_k<t_{k6}\\ T_s(d_1-1)(1+k_v) & t_{k6}\le t_k<t_{k8}\end{cases}$	$M\times\begin{cases} T_s(d_1-1) & t_{k0}\le t_k<t_{k1}\\ AT_s+2t_k & t_{k1}\le t_k<t_{k2}\\ T_s(1-d_1) & t_{k2}\le t_k<t_{k5}\\ BT_s-2t_k & t_{k5}\le t_k<t_{k6}\\ T_s(d_1-1) & t_{k6}\le t_k<t_{k8}\end{cases}$

TABLE III
EXPRESSION AT EACH MOMENT OF DPS

	Mode 1	Mode 2	Mode 3	Mode 4
t_{k0}	0	0	0	0
t_{k1}	$(d_1+d_2-1)\,T_s$	$d_1\,T_s$	d_2T_s	$(d_1+d_2-1)\,T_s$
t_{k2}	$d_1\,T_s$	d_2T_s	$d_1\,T_s$	d_2T_s
t_{k3}	d_2T_s	$(d_1+d_2)\,T_s$	$(d_1+d_2)\,T_s$	$d_1\,T_s$
t_{k4}	T_s	T_s	T_s	T_s
t_{k5}	$(d_1+d_2)\,T_s$	$(d_1+1)\,T_s$	$(d_2+1)\,T_s$	$(d_1+d_2)\,T_s$
t_{k6}	$(d_1+1)\,T_s$	$(d_2+1)\,T_s$	$(d_1+1)\,T_s$	$(d_2+1)\,T_s$
t_{k7}	$(d_2+1)\,T_s$	$(d_1+d_2+1)\,T_s$	$(d_1+d_2+1)\,T_s$	$(d_1+1)\,T_s$
t_{k8}	$2\,T_s$	$2\,T_s$	$2\,T_s$	$2\,T_s$

high risk of saturation since the values of dc bias and transient current will increase with i_L. Once the saturation of L_t happens, i_L will reach a very large value, and the whole converter will be damaged or shut down by the protection circuit.

In summary, when F1 occurs in the circuit, the internal current will generate a dc bias due to sudden voltage drop, causing risks of the internal overcurrent and more serious inductor saturation. Therefore, FRT method is expected to avoid the internal overcurrent and provide a more reliable selection basis for semiconductor switches. Based on this, the corresponding FRT strategies would be given in Section V.

Besides, the discharging speed of capacitor C_2 slows down with the increase in the short-circuit resistance, and its impact on i_L is also different from the one presented in this section; namely, in that case, it behaves similarly as in the cable-to-cable short-circuit case, which is presented in the following section.

IV. F2: CABLE-TO-CABLE SHORT-CIRCUIT

The cable model used in the single-strand cable routing can be represented by the π-equivalent circuit [39], in which the parallel capacitance can be ignored compared to C_2, so the cable can be considered as an inductor. When the material and diameter of cables are fixed, the cable inductance depends on its length. Hence, when F2 occurs at branch i, the discharging loop contains C_2, line inductance L_s, and short-circuit resistor R_s, as shown in Fig. 6(a).

A. Transient Process of Output Circuit

There can occur three resonance types when C_2 discharges: underdamped, critical damped, and overdamped attenuation

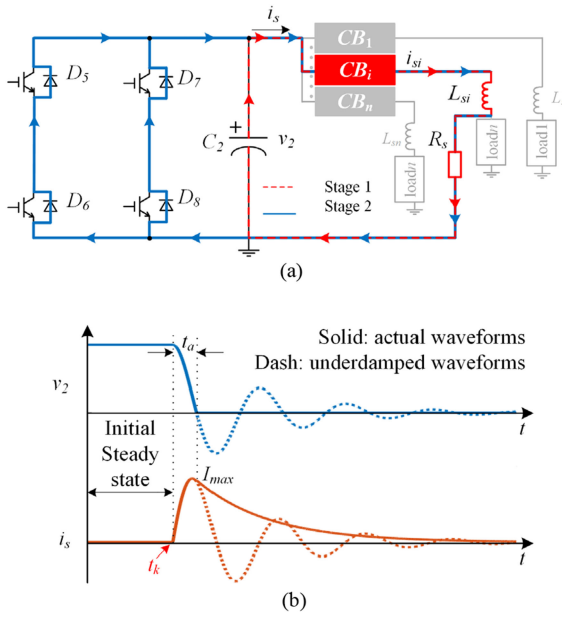

Fig. 6. Case of F2 fault. (a) Discharging loops in different stages. (b) Discharging waveforms.

[28]. This article analyzes the short-circuit process of underdamped resonance as the WCS. Since the antiparallel diodes of the switches on H2 have a negative voltage clamping effect on v_2, once v_2 reaches a negative value, the overdamped attenuation resonance ends. However, current i_s still exists, and it has to freewheel through diodes D_5–D_8 of H2. Therefore, the discharge process of the output circuit can be divided into two stages, the first stage represents the decay stage of v_2, and the second stage represents the decay stage of i_s, as shown in Fig. 6(a).

1) Stage 1: v_2 Decays to Zero: In this stage, the discharge loop is represented by a dashed line in Fig. 6(a). The differential equations and the initial values of v_2 and i_s are given by (16), where t_k denotes the fault moment. Accordingly, v_2 and i_s can be derived and expressed by (17), where the parameters are as follows: $\delta = R_s/2L_s$, $\omega_0 = \sqrt{1/L_sC_2}$, $\omega = \sqrt{\omega_0^2 - \delta^2}$, and $\beta = \arctan(\omega/\delta)$

$$\begin{cases} C_2\left(\mathrm{d}v_2/\mathrm{d}t\right) = I_2 - i_s \\ L_s\left(\mathrm{d}i_s/\mathrm{d}t\right) = v_2 - R_s i_s \\ v_2\left(t_{k-}\right) = V_2 \\ i_s\left(t_{k-}\right) = I_2 \end{cases} \tag{16}$$

$$\begin{cases} v_2(t) = \omega_0 V_2 \mathrm{e}^{-\delta(t-t_k)} \sin\left[\omega\left(t-t_k\right)+\beta\right]/\omega \\ i_s(t) = V_2 \mathrm{e}^{-\delta(t-t_k)} \sin\left[\omega\left(t-t_k\right)\right]/\omega L_s + I_2. \end{cases} \tag{17}$$

At first, v_2 decays as i_s increases. Once v_2 reaches the value of zero, i_s reaches the peak value $I_{\max}$ that is expressed by (18). The duration of the first stage, which represents the decay time t_a of v_2 can be calculated by (19)

$$I_{\max} = V_2 \mathrm{e}^{-\delta(\pi-\beta)/\omega} \sin\left(\pi-\beta\right) \Big/ \omega L_s + I_2 \tag{18}$$

$$t_a = (\pi - \beta)/\omega. \tag{19}$$

2) Stage 2: i_s Decays to I_2: In this stage, i_s freewheels through diodes D_5–D_8 of H2, and the discharge loop is drawn by a solid line in Fig. 6(a). In Stage 2, i_s will decay naturally to I_2 with the time constant of $\tau_s = L_s/R_e$, as given by (20), where R_e represents the summation of the resistances of all diodes and a short-circuit resistor. Then, the duration of the second stage, which represents the decay time of i_s can be calculated by

$$i_s(t) = \left(I_{\max} - I_2\right) \mathrm{e}^{-R_e(t-t_k-t_a)/L_s} + I_2 \tag{20}$$

$$t_b = 5\tau_s = 5L_s/R_e. \tag{21}$$

Combining these two stages, the waveforms of v_2 and i_s in the total discharge process can be obtained, and they are shown by solid lines in Fig. 6(b), where can be noted that there is no risk of overvoltage during the discharge process, but the resonance peak current and the discharge time of i_s will cause the external overcurrent to last for a long duration.

B. Transient Process of Internal Circuit

Due to the existence of L_s, the decay process of v_2 is slowed down, which makes the internal transient process different from that of F1. The transient process of the internal current i_L must be classified according to t_a, which represents the decay time of v_2. This article considers that the DAB works in mode 2 and assume that a short-circuit fault occurs at time t_{k2} because the fault moment can cause the most severe internal overcurrent in F1. The transient process is decided by t_a, so there are three situations considered in this article, and they are shown in Fig. 7.

1) Situation 1: $\mathrm{t_a} \le \mathrm{d_1T_s}$: When the value of L_s is small, the discharging speed of C_2 is still fast. As shown in Fig. 7(a), while v_2 decays to zero within interval $t_{k2} - t_{k3}$, whose duration is d_1T_s, that situation can be approximately treated as that of F1 since v_L is equal to that in F1.

2) Situation 2: $\mathrm{d_1T_s} \le \mathrm{t_a} \le \mathrm{2T_s}$: As the value of L_s increases, the decay time t_a becomes longer than d_1T_s. Compared to the F1 case, v_L lacks the shaded area in the Fig. 7(b) and (c), reducing the dc bias current of i_L. Both I_{dc} and I_{tr+} are smaller than those of F1. Since v_L and i_L change simultaneously, it is difficult to establish the corresponding analytical formula, but this can be conservatively approximated to F1.

3) Situation 3: $\mathrm{t_a} \ge \mathrm{2T_s}$: When t_a is longer than one switching period due to larger L_s, v_2 can be regarded as constant in one switching period, the asymmetry of v_L is negligible, and then the dc bias current of i_L is neglectable. Therefore, i_L changes from the initial steady state to the final steady state without dc bias appears when v_2 decays slowly.

According to these three cases, t_a increases as L_s increases, while the dc bias of i_L gradually decreases. When t_a is greater than one switching period, the dc bias of the internal current can be neglected, which means that there is no internal overcurrent in this case.

V. Methods for Fault Riding-Through

The whole fault characteristics when the output is short-circuited have been analyzed in the previous sections, and this

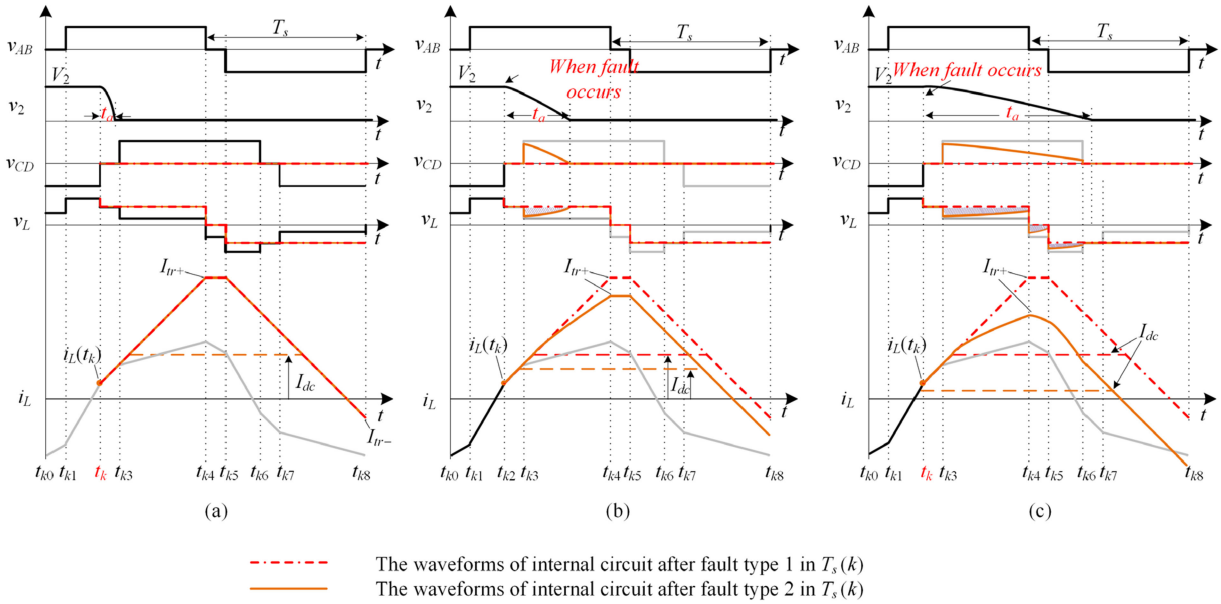

Fig. 7. Transient process of the internal circuit at slow discharging speed. (a) $t_a \leqslant d_1 T_s$ (b) $d_1 T_s \leqslant t_a \leqslant T_s$ (c) $T_s \leqslant t_a \leqslant 2T_s$.

section proposes the FRT-based methods for a DAB. The FRT strategy includes the four following steps:

1) detect the short-circuit fault;
2) avoid or eliminate the overcurrent;
3) provide a fault criterion current to the fault branch;
4) cut off the fault branch by the breaker and restore the power supply.

According to the previous analysis, there is an internal overcurrent risk, and the external current can be limited by the cable inductance. Based on the fault characteristics, this article proposes three FRT methods for a DAB. The first method is blocking the switching signals to eliminate the internal transient current when the fault is detected, then restoring the switching signals to generate the fault criterion current. In the second method, only a series inductor with a reasonable inductance is added to the output side. As a result, the internal overcurrent risks are avoided. Meanwhile, a fault criterion current is obtained to trigger the CB and the fault branch can be cut off. The third method is an extension of the second, the CLC pi filter is added on the output terminal.

A. Power Switches Blocking Method

In a DAB, the internal overcurrent during the fault transient process needs to be eliminated. Changing d_1 and d_2 can adjust the internal current in the steady-state condition, however, the change in d_1 and d_2 can only be performed at the next switching period, which cannot help for the current switching cycle. Moreover, the mechanism of eliminating dc bias by changing d_1 and d_2 is to generate a new transient dc bias to cancel the original transient dc bias. Since the transient dc bias cannot be directly measured by the sample circuit, it cannot be guaranteed that the transient current can be canceled in all the cases. To address this problem, this article proposes an FRT scheme for a DAB based on the blocking of all power switches. When a fault is detected, first, the switching signals are blocked to eliminate the internal overcurrent, and then the DAB restarts to provide a fault criterion current to the fault load branch. Finally, the fault branch is cut off by the breaker, and the power supply is restored. The flowchart of the FRT strategy is displayed in Fig. 8.

1) Fault Detection: Generally, the converter operates under rated conditions, and the rated power is about 70% of the maximum power. Before a fault occurs, the output voltage is equal to V_2, the total output current i_s is approximately $0.7I_{2N}$, and the current in each load branch is smaller than $0.7I_{2N}$. The maximum output current of a DAB is I_{2N}, so when it is detected that v_2 is lower than $0.6V_2$ and i_s exceeds I_{2N}, it can be determined that a fault occurred on the output side.

2) Power Switches Blocked for Overcurrent Elimination: According to the fault characteristics analyzed in Section IV, the internal overcurrent risk increases when F1 occurs. Due to the unpredictability and randomness of a fault, it is essential to block power switches for a certain time to eliminate the possible internal overcurrent risks when a fault is detected. Meanwhile, to control and recover the circuit quickly, the shortest blocking duration must be set appropriately.

In a DAB, once the drive signals of all power switches are blocked, i_L will freewheel through different loops depending on the polarity of i_L, as given in Table IV and Fig. 9(a) and (b). Fig. 9(a) shows the freewheel loop when polarity of i_L is positive, and Fig. 9(b) shows it when polarity of i_L is negative.

The equivalent circuits of the two cases are unified and represented in Fig. 9(c), where L_t is directly connected to the input voltage to attenuate i_L. Therefore, i_L will decay according to (22), where I_B denotes the value of i_L when blocking is used. When I_B is equal to the fault current stress I_{trm}, the longest decay time is given by (23). The most reliable blocking duration

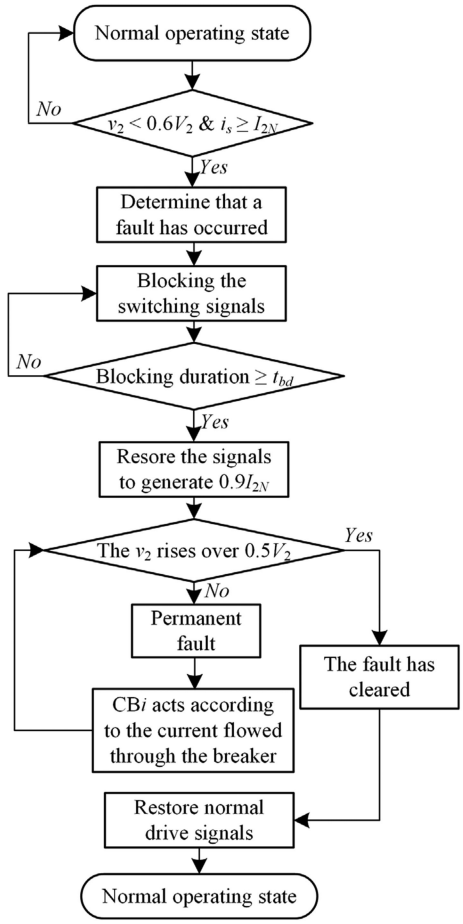

Fig. 8. Flowchart of the FRT strategy based on the signal blocking.

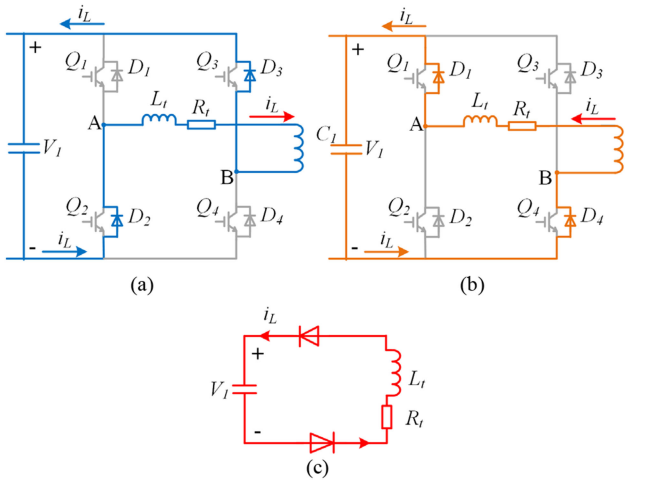

Fig. 9. Freewheeling loop after blocking (a) when i_L is positive, (b) when i_L is negative, and (c) equivalent circuit.

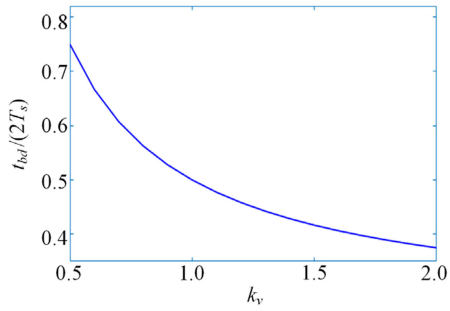

Fig. 10. t_{bd} curve.

TABLE IV
FREEWHEELING DEVICE TYPES

Polarity of i_L	Freewheeling device
Positive (+)	D_2 and D_3
Negative (-)	D_1 and D_4

t_{bd} is expressed by (24), considering that d_1 is zero

$$i_L = I_B - V_1 t / L_t \tag{22}$$

$$\Delta t_m = T_s\,(1 - d_1)\,(1 + 1/k_v)/2 \tag{23}$$

$$t_{bd} = T_s(1 + 1/k_v)/2. \tag{24}$$

The curve of t_{bd} with respect to k_v is shown in Fig. 10, where i_L would decay fully within one switching period when the range of k_v is 0.5–2.0. To facilitate the digital control and the restart of a circuit, t_{bd} can be set to one switching period.

3) Fault Criterion Current: After blocking all the switching signals for t_{bd}, the switching signals must be recovered to generate a fault criterion current immediately. Since the maximum output capacity of a DAB is I_{2N}, the fault criterion current can be set to $0.9I_{2N}$.

4) Fault Branch Cut Off and System Restore: Almost the entire fault criterion current flows through the faulty branch because the impedance of this branch is the smallest among all the branches. The breaking action value of the mechanical CB can be set at $0.8I_{2N}$. If the output voltage restores and the branch current cannot exceed $0.8I_{2N}$ with a certain time, a fault is considered as a self-recoverable fault, which is possible in distribution networks. In this case, the switching signals return to normal, and the circuit recovers the power supply. Once the current flowed through CBi exceeds $0.8I_{2N}$ and last over a certain interval, the fault branch can be cut off by a breaker, and after the fault branch is cut off, the output voltage can be restored again, and then the power supply can be recovered.

This method is an effective and simple solution because the short-circuit occurs at random. By conducting these four steps, the FRT on the DAB output side is completed.

B. Series Inductance-Based Method

Using inductor on output terminals is a feasible choice in the converters, and according to the analysis of F2 fault, a large inductor in the fault loop not only can avoid internal dc components but also can limit the external current effectively. Therefore, adding an additional inductor L_{se} in series at the output terminal of a DAB can be used as a solution for the FRT without blocking the signals. The scheme includes the following steps: 1) detect the fault; 2) locate the faulty branch according to the current of each branch; 3) cut off the fault branch using the

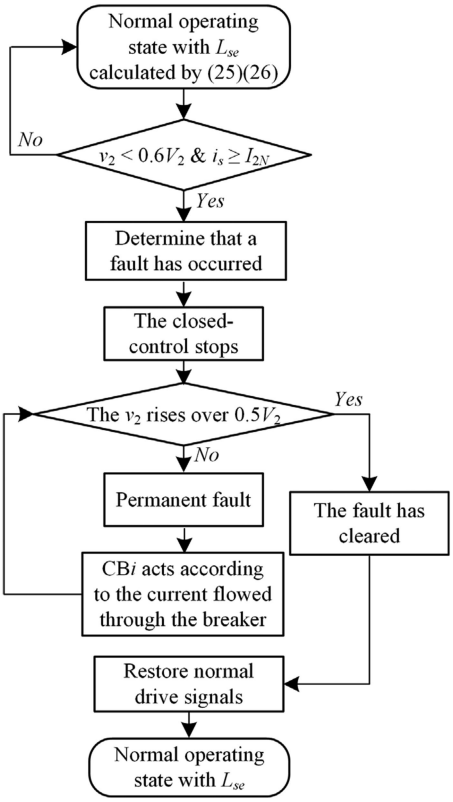

Fig. 11. Flowchart of the FRT strategy using the series inductor.

breaker and restore the system. The corresponding flowchart is presented in Fig. 11.

The selection of the inductor must satisfy the two following conditions: 1) avoid the internal transient overcurrent of a DAB; 2) ensure the external current is larger than the fault criterion to trigger the CB.

1) Avoid the Internal Transient Overcurrent: When the length of a power cable is close to zero, the short-circuit inductance L_s is equal to the series inductance L_{se}. Considering the worst case, the short-circuit resistance $\mathrm{R_s}$ is approximately zero. According to the analysis result of Section IV-B, if $t_a \geq 2T_s$ can be guaranteed in this situation, the internal transient overcurrent can be avoided regardless of the power cable length. According to (19), L_{se} should be selected according to the following criterion:

$$L_{se} \geq 16T_s^2/C_2\pi^2 = 4/\left(C_2\pi^2 f_s^2\right). \tag{25}$$

2) Ensure the Current Exceeds the Fault Current Criterion: When the power cable length is long, the short-circuit inductance L_s in the discharging circuit represents the sum of the line inductance L_{line} and the series inductance L_{se}: $L_s = L_{se} + L_{line}$. Also, $I_{\max}$ can be calculated by (18). The breaking current of the CB is set at $0.8I_{2N}$. If $I_{\max}$ can meet condition $I_{max} \geq 0.8I_{2N}$, i_s will reach the fault current criterion regardless of the distance between the fault point and the output terminal, and the fault load branch can be cut off by the breaker. Therefore, the range of L_{se} can be obtained as

$$L_{se} \leq 100C_2V_2^2L_t^2f_s^2/\left(N^2V_1^2\right) - L_{line}. \tag{26}$$

Once the valid range of L_{se} is determined, the smallest value should be chosen. Therefore, a possible compromise can be achieved between reliability and cost-efficiency to ensure the FRT capability of a DAB.

However, this scheme can be used only as an additional scheme due to its high cost and volume, and also, the specific inductance value of a power cable must be known. Besides, there is a possibility that the range of L_s is invalid.

C. CLC Filter Method

The third method is an extension of the second, CLC pi filter has a better limited current performance than with only one inductor. The drop of the output voltage and its change rate are small, which means a low overcurrent risk. However, the method also has the disadvantage of the cost and volume, therefore, this article will not discuss the method in detail.

It must be mentioned that the first method is the main FRT method, and the other two are both alternatives.

It should be noticed that the transient overcurrent has the risk of damaging the devices through increased thermal stress. The thermal stress of devices is decided by the current stress and the rms current flowed through it. Both the current stress and the rms current on the devices would increase significantly after the fault, which would result in large thermal stress in power devices. However, it should be mentioned that whether devices fail also depends on device selection. However, the selection criterion of power switches has not been strictly defined, and it should be conducted based on particular design goals and control methods, e.g., different efficiency optimization algorithms. The evaluation of all these factors cannot be included in this article due to the length of the article. For the other side, the result of the overcurrent analysis in this article represents an important reference for device selection. Meanwhile, the proposed FRT method of blocking drive signals can avoid the overcurrent in all situations and thus prevent the devices from the impact of the overcurrent thoroughly.

VI. Simulation and Experimental Results

A. F1 Fault

1) Simulation of F1: The DAB parameters of the F1 fault simulated by MATLAB/Simulink are presented in Table V.

In order to analyze the influence of fault moments on i_L, two different values of t_k were used. The enlarged waveforms of v_2, v_L, and i_L are given in Fig. 12(a) and (b). The DAB operated in mode 2 with the phase shift angles of $d_1 = 0.1$ and $d_2 = 0.2$ in the initial steady state. As shown in Fig. 12(a), where $t_k = t_2$, a positive current surge of 208.4 A of i_L was achieved, and as displayed in Fig. 12(b), where $t_k = t_6$, a negative current surge of -187.7 A of i_L was obtained; the time of 0.015 s denoted the beginning of the switching period. The results indicated that different fault moments had different influences on the internal overcurrent since the I_{2N} was only 133.3 A.

TABLE V
SIMULATED PARAMETERS OF F1 FAULT

Parameter	Value
V_1/V_2	1000 V/ 375 V
N/k	2 / 1.333
P_N	50 kW
f_s	10 kHz
L_t	187.5 uH
I_{2N}	133.3 A
R_s	1 mΩ

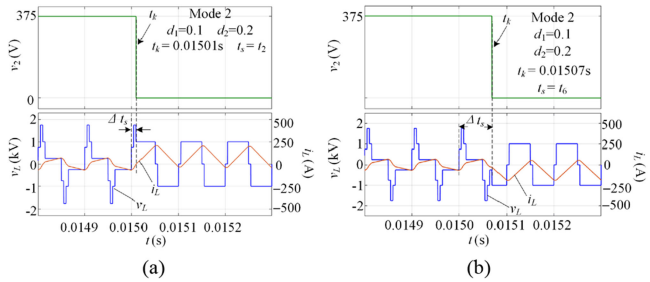

Fig. 12. Enlarged waveforms of v_2, v_L, and i_L. (a) $t_k = 0.01501$ s, $t_s = t_2$. (b) $t_k = 0.01507$ s, $t_s = t_6$.

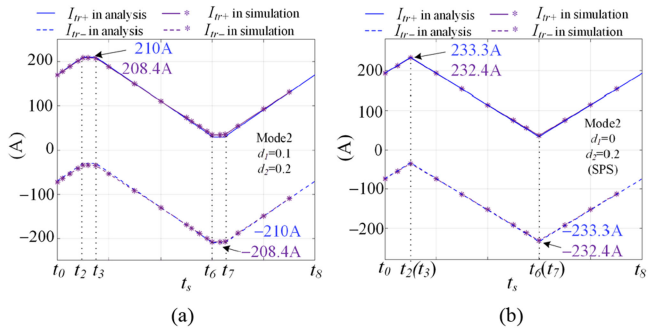

Fig. 13. Comparison of I_{tr+}, I_{tr-}, and I_{dc} in mode 2. (a) $d_1 = 0$, and $d_2 = 0.2$. (b) $d_1 = 0.1$, and $d_2 = 0.2$.

In order to verify the accuracy of the transient current expression given in Table II, two initial steady states with $d_1 = 0.1$, $d_2 = 0.2$, and $d_1 = 0$, $d_2 = 0.2$ were used to simulate the F1 fault for several groups of fault moments to record I_{tr+}, I_{tr-}, and I_{dc}. The comparisons of simulation records and the calculation results in Table II are illustrated in Fig. 13. In Fig. 13(a), the DAB that operated with $d_1 = 0.1$ and $d_2 = 0.2$ in the initial steady state is presented, and in Fig. 13(b), the DAB that operated with the phase-shift angles $d_1 = 0$ and $d_2 = 0.2$ in the initial steady state is presented; the lines with "$*$" denote the simulation records, and the lines without "$*$" denote the calculation results from Table II.

The subtle error was caused because, in the simulation, the circuit resistor was considered while it was ignored in deriving the expressions given in Table II. The comparison results showed that the formulas provided in Table II are accurate enough to predict the possibility of internal overcurrent.

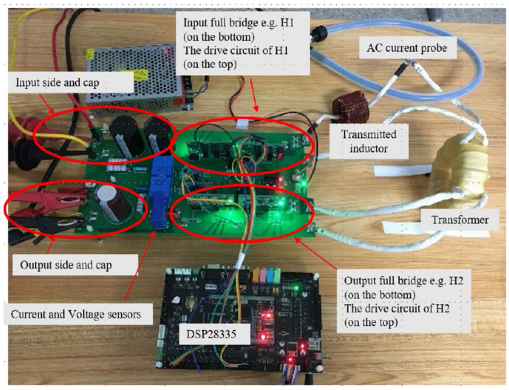

Fig. 14. Photograph of the experimental prototype.

TABLE VI
EXPERIMENT PARAMETERS OF DAB

Parameter	Value
V_1/V_2	400 V/ 250 V
N/k	2 / 0.8
P_N	3.125 kW
f_s	10 kHz
L_t	800 uH
I_{2N}	12.5 A
R_s	1 mΩ (F1) / 0.1Ω (F2)

2) Experiment of F1: The experimental prototype is shown in Fig. 14, and the experimental parameters of the DAB are shown in Table VI.

The experimental results without FRT are shown in Fig. 15, in which t_k referred to the fault moment. As seen in the waveforms, v_2 decayed rapidly and i_s surged a pulse current when the fault occurred, and the transient dc bias current in i_L appeared at once, resulting in the transient current stress. The discharging process is too rapid to trigger the CB on the fault branch. Then, transient current decreased with the decay of dc bias current. It can be seen that the transient current stress reached $I_{tr} = 25.8$ A; however, I_{2N} is only 12.5 A. The peak current in final steady current valued 10.8 A is smaller than I_{2N}, it is still necessary to apply FRT method because it took a long time (about 90 switching cycles) to decay the transient dc bias.

It is not rational to wait for the process to end without doing anything, since the fault branch needs to be cut off then the circuit can be restored.

B. F2 Fault

The experiments on F2 are also based on the parameters in Table VI. From 100 to 1000 μH, with 100 μH as the spacing, ten groups of inductors with different values were selected to imitate L_s to perform the experiments of F2 fault. The four groups of experimental waveforms about v_2, i_s, and i_L at $L_s = 100$, 200, 300, and 400 μH are shown in Fig. 16(a)–(d), where it is shown that, before the fault, the DAB operated in the initial steady state with $v_2 = 250$ V, and $i_s = 8.5$ A. Next, the fault occurred at t_k, leading to a decrease in v_2, and an increase in i_s during t_a, which

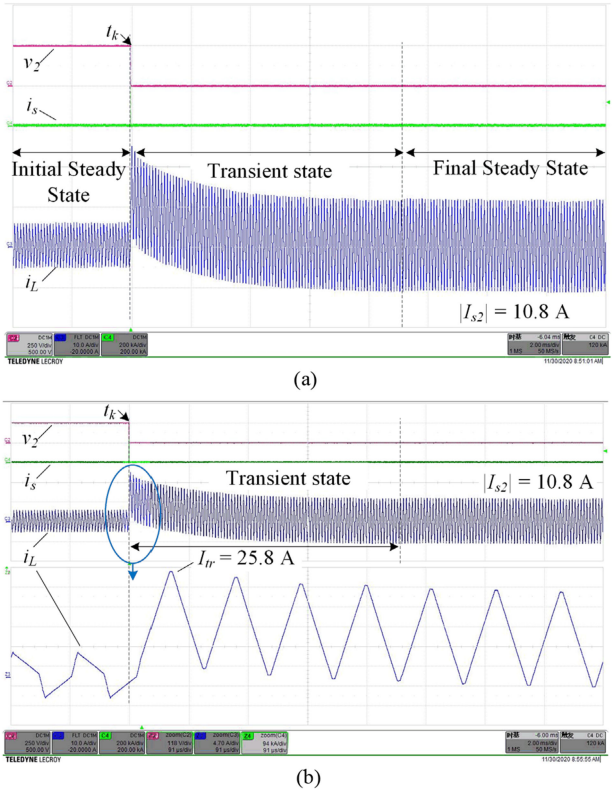

Fig. 15. Transient waveforms of v_2, v_L, and i_L in F1 without FRT method. (a) Overall waveforms. (b) Enlarged waveforms of i_L

indicated an underdamped resonance between C_2 and L_s; then, i_s decreased during t_b, which indicated the energy decay process of L_s. Meanwhile, i_L changed from the initial steady state to the final steady state slowly during t_a, and neither overcurrent nor dc bias in i_L appeared. As for the influence of L_s value on the transient process, it is obvious that, when L_s increased, the capacitor discharging process became slower, so t_a and t_b increased while $I_{\max}$ decreased. Fig. 17 shows the experimental data of $I_{\max}$, t_a, and t_b with L_s. According to the results in Fig. 17, the accuracy of the theoretical analysis model is validated, while the errors between the solid and dashed lines originated from the inevitable impedance in the real circuit.

The experimental results prove the accuracy of the theoretical analysis of the F2 fault presented in this article.

C. FRT Methods Verification

The FRT scheme was verified by MATLAB/Simulink, and the simulated waveforms are drawn in Fig. 18. The DAB supplied load branches 1–3, and the short-circuit fault occurred in branch 3 at $t = 0.03$ s; then, v_2 dropped and i_s increased so that the fault could be detected. Once the fault was detected, the switching signals were blocked to eliminate the overcurrent in the internal circuit, and the transient overcurrent of i_L was avoided. After the blocking one switching period, the circuit restarted to provide the fault criterion current $0.9I_{2N}$ to the fault branch. When the current of the branch was larger than $0.8I_{2N}$ for 6 ms, the CB was

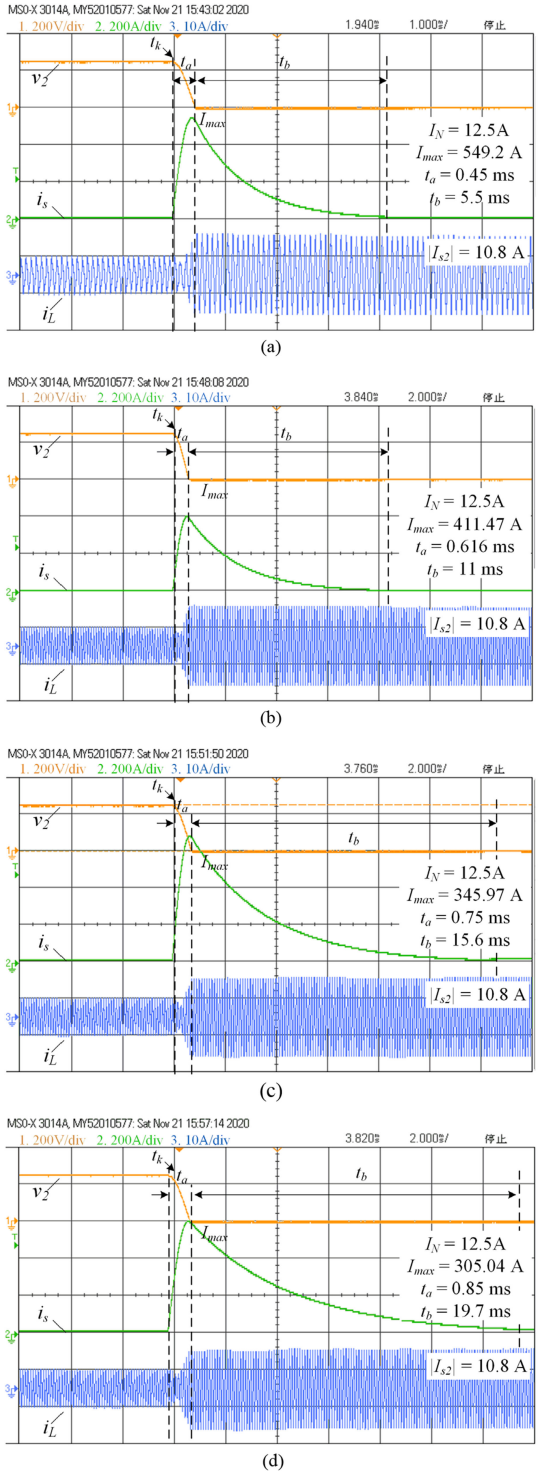

Fig. 16. Experimental results of the F2 fault. (a) $L_s = 100$ μH. (b) $L_s = 200$ μH. (c) $L_s = 300$ μH. (d) $L_s = 400$ μH.

triggered to cut off the fault branch. Finally, the output voltage was restored, and the FRT was achieved.

Compared with Fig. 15, the FRT scheme can protect the internal circuit and provide the required fault current to the fault branch and triggered the breaker, which demonstrates its effectiveness and reliability.

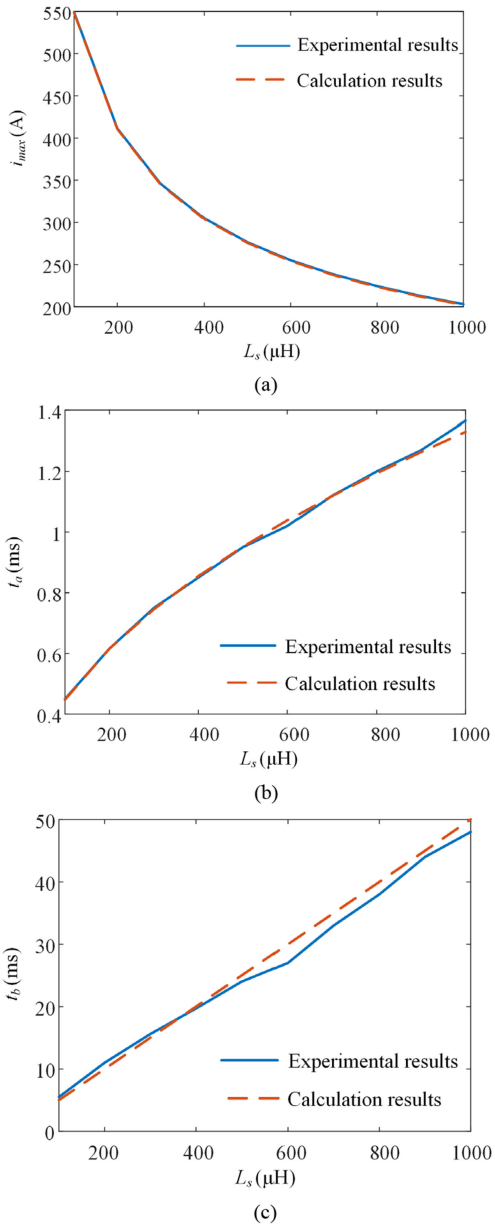

Fig. 17. Experimental results compared to the theoretical analysis results of (a) $I_{\max}$, (b) t_a, and (c) t_b.

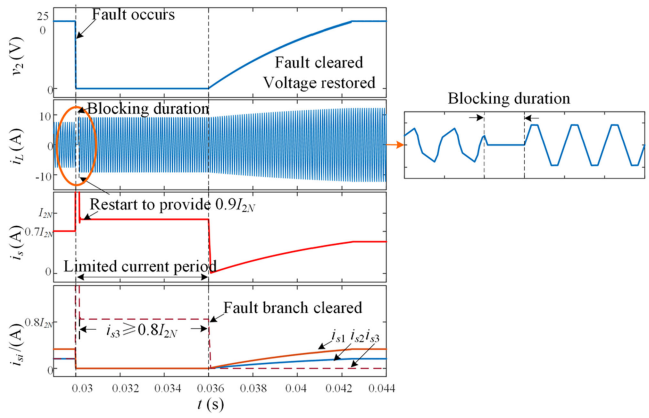

Fig. 18. Waveforms when the FRT scheme is applied.

VII. Conclusion

In a dc distribution network, a short-circuit fault can occur on the output, which can cause the overcurrent. This article provides a comprehensive analysis of the fault process of a DAB, which reveals the overcurrent phenomenon after the short-circuit faults, and puts forward three methods to achieve the FRT. One method is to block the power switches for a certain period and then recover the switching signals to generate a fault criterion current to trigger the breaker, and another is to add a series inductor with a reasonable inductance on the output side, and then cut off the faulty branch by the breaker. The third method is an extension of the second, CLC pi filter is added on the output terminal. The first method is the main FRT method because it is simple and effective, and the second and third are both alternatives because of their high cost.

The simulation and experimental results validate the accuracy of the theoretical analysis results of the fault characteristics and the FRT effectiveness. The safety and the clearance capability are guaranteed, which provides strong support to the dc power distribution network.

The research results in this article provide a theoretical basis for the development of the DAB overcurrent protection, CB selection, and FRT methods. Based on the research in this article, the fault characteristics and FRT methods of dc transformers can be further studied.

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