Efficiency Optimization Based Parameter Design Method for the Capacitive Power Transfer System

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***Abstract*—In this article, a parameter design method is proposed to improve the dc–dc efficiency of the capacitive power transfer (CPT) system. Similar to the inductive power transfer (IPT) system, the capacitive coupler is analyzed by using a T-type model, giving direct insight into the impedance refracted from the secondary side. Compared to the IPT system, the external capacitor of the capacitive coupler introduces extra design freedom, making it easy to realize the optimal load condition by adjusting the external capacitance. To quantify the relationship between the optimal load and the external capacitance, the impedance characteristic of the rectifier is discussed. Then, the efficiency analysis is conducted in detail. Considering the impact of the resonant frequency, and the external capacitance that determines the coupling coefficient, a parameter design method is proposed to improve the dc–dc efficiency. Although the design example is conducted with the double-sided *LC* compensated CPT system, the analysis and design process can be extended to other compensation networks easily. The effectiveness of the proposed design method is verified with a 100-W output CPT system. The experimental results show that the dc–dc efficiency can reach 89.39% with 10-W output, and reach 93.02% with 100-W output.**

***Index Terms*—Capacitive power transfer (CPT) system, efficiency optimization, parameter design method, T-type model.**

I. Introduction

DURING the past few years, much effort has been put into the study of the capacitive power transfer (CPT) system [1]–[24]. Compared to the other implementation methods of the wireless power transfer (WPT) systems, the CPT system has the following outstanding advantages: the ability to transfer power across metal barriers [1]–[3], low electromagnetic interference [4], [5], low eddy current loss [6]–[8], and low cost and weight of the capacitive coupler [9]–[10].

Due to its outstanding advantages, the CPT system has been widely used in many applications, including the portable device [11], the power generation excitation system [12], the biomedical device [13], [14], and the electric vehicle [15], [16]. No matter what the application is, efficiency is always a research hotspot.

To improve the efficiency of the CPT system, many researchers have done a lot of work around the parameter design method [17]–[20]. In [17], the optimal load of the double-sided *LC* compensated CPT system was analyzed. However, the optimal load could only improve the ac–ac efficiency of the resonant network, which was not comprehensive enough to improve the dc–dc efficiency, leading to a dc–dc efficiency of 74.8% with 109.3-W output.

To avoid the impact of the inductance detuning, the compensation inductance was designed by limiting the variation of the output current, the power factor, and the voltage across the external capacitor [19]. However, the power factor to improve the dc–ac efficiency of the inverter was an empirical value, which lacked a quantitative analysis to study the impact of the parameter on the dc–ac efficiency. The experimental results showed that the dc–dc efficiency could reach 91.8% with 368.5-W output. In [20], a multiobjective optimization algorithm was proposed for the parameter design, aiming at the optimization of the output power, efficiency, and the total harmonic distortion. However, the algorithm only considered the loss of the resonant components, leading to a good performance in the ac–ac efficiency, but not in the dc–dc efficiency. The experimental results showed that the dc–dc efficiency could reach 87.1% with 252.3-W output. Although a lot of work has been done to improve the efficiency, it still needs to further discuss the impact of the parameter on the dc–dc efficiency, constructing a direct relationship between the parameter and the dc–dc efficiency.

For the CPT system, the mutual capacitance and the input and output working conditions are determined by the application. Thus, the designable parameter consists of the resonant frequency and the external capacitance that determines the coupling coefficient.

Normally, the resonant frequency f_s can vary from 480 kHz [1] to 6.78 MHz [11], which is a wide design range. The choice of f_s directly influences the capacitive and inductive reactance of the compensation components, which determines the design of the compensation parameters. Moreover, due to the parasitic capacitor of the power device, both the inverter and the rectifier cannot be simply equivalent to a pure resistance when f_s is up to 1 MHz. The impedance characteristics determined by the parasitic capacitor and f_s have a great impact on the optimal load

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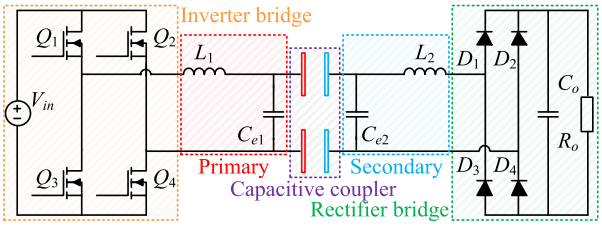

Fig. 1. Typical circuit diagram of the CPT system.

and the compensation parameters, which should be considered when designing the parameter.

Moreover, different from the inductive power transfer (IPT) system, there exists an external capacitor in the CPT system, which is added to increase the equivalent self-capacitance of the capacitive coupler. The external capacitance introduces extra design freedom, making the parameter design more complex and flexible. Thus, it is necessary to discuss the impact of the external capacitor on efficiency.

It is well known that the ac–ac efficiency η_r is in a positive correlation with the coupling coefficient k_C. However, the dc–dc efficiency, $\eta_{\rm DC}$, is determined by not only η_r but also the dc–ac efficiency $\eta_{\rm inv}$, and ac–dc efficiency of the rectifier $\eta_{\rm rec}$. That is, to improve $\eta_{\rm DC}$, the impact of k_C on $\eta_{\rm inv}$ and $\eta_{\rm rec}$ should also be discussed.

In this article, considering the impact of the resonant frequency, and the external capacitance that determines the coupling coefficient, a parameter design method is proposed to improve the dc–dc efficiency. There are three main contributions in this article. First, using the T-type model, the similarity and the difference between the IPT and the CPT systems are revealed. Then, a novel method is proposed for the CPT system to realize the optimal load condition by adjusting the external capacitance. Second, to quantify the relationship between the optimal load and the external capacitance, the impedance characteristic of the rectifier is analyzed. Then, the efficiency analyses of the inverter, the resonant network, and the rectifier are conducted in detail, constructing a direct relationship between the designable parameter and the dc–dc efficiency. Third, considering the impact of the designable parameter, a parameter design method is proposed to improve the dc–dc efficiency. The experimental results show that the dc–dc efficiency can reach 89.39% with only 10-W output, and reach 93.02% with 100-W output.

II. Analysis of the Resonant Network Using the T-Type Model

Fig. 1 shows the typical circuit diagram of the double-sided *LC* compensated CPT system, which is composed of the inverter, the rectifier, and the resonant network that consists of the *LC* compensation network and the capacitive coupler, where $V_{\rm in}$ is the dc input voltage, Q_1–Q_4 are MOSFETs that constitute the inverter, D_1–D_4 are diodes that constitute the rectifier, L_1 and L_2 are the primary and secondary compensation inductors, respectively, C_{e1} and C_{e2} are the primary and secondary external capacitors, respectively, C_o is the output filter capacitor, and R_o is the load resistance.

Fig. 2. Models of the capacitive coupler. (a) Π-type model. (b) T-type model.

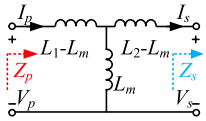

Fig. 3. T-type model of the inductive coupler.

A. T-type Model of the Capacitive Coupler

In the CPT system, the capacitive coupler is normally equivalent to a Π-type model, which is shown in Fig. 2(a), where Z_p represents the primary input impedance, Z_s represents the secondary output impedance, and C_1 and C_2 are the equivalent self-capacitors that can be obtained by the following equations:

$$C_1 = C_{e1} + C_{s1} \tag{1}$$

$$C_2 = C_{e2} + C_{s2} \tag{2}$$

where C_{s1} and C_{s2} are the internal self-capacitors of the capacitive coupler.

According to the reciprocal two-port network, the Π-type model can be equivalently transferred into the T-type mode, which is shown in Fig. 2(b). Then, the voltage and current relationships can be expressed as follows:

$$\begin{bmatrix} V_p \\ V_s \end{bmatrix} = \frac{1}{j\omega\left(C_1C_2 - C_m^2\right)} \begin{bmatrix} C_2 & -C_m \\ C_m & -C_1 \end{bmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} = \begin{bmatrix} Z'_1 & -Z'_m \\ Z'_m & -Z'_2 \end{bmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} \tag{3}$$

where ω is the resonant angular frequency and C_m is the mutual capacitance.

Then, the refraction relationship between Z_p and Z_s can be expressed as follows:

$$Z_p = Z'_1 + \frac{|Z'_m|^2}{Z'_2 + Z_s}. \tag{4}$$

From (4), it can be noted that the T-type model provides an easier method to obtain Z_p, making the analysis more directly and concisely.

B. Similarity and Difference Between the IPT and CPT Systems

From Fig. 2(b), it can be noted that the T-type model of the capacitive coupler is similar to that of the inductive coupler as shown in Fig. 3. Similar to (3), the voltage and current relationship can be expressed as follows:

$$\begin{bmatrix} V_p \\ V_s \end{bmatrix} = j\omega \begin{bmatrix} L_1 & -L_m \\ L_m & -L_2 \end{bmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} \tag{5}$$

TABLE I
MAPPING RELATIONSHIPS BETWEEN THE INDUCTIVE AND CAPACITIVE COUPLERS

	Capacitive	Inductive
Z'_1	$\frac{C_2}{j\omega\left(C_1C_2-C_m^2\right)}$	$j\omega L_1$
Z'_2	$\frac{C_1}{j\omega\left(C_1C_2-C_m^2\right)}$	$j\omega L_2$
Z'_m	$\frac{C_m}{j\omega\left(C_1C_2-C_m^2\right)}$	$j\omega L_m$

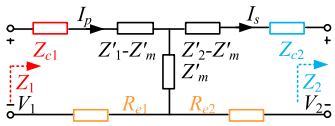

Fig. 4. Typical S/S compensation network.

TABLE II
UNIFIED EXPRESSIONS OF THE IPT AND CPT SYSTEMS

	T-type	IPT	CPT
Z_{c1}	$-Z'_1$	$\frac{1}{j\omega C_1}=-j\omega L_1$	$j\omega L_1=\frac{-C_2}{j\omega\left(C_1C_2-C_m^2\right)}$
Z_{c2}	$-Z'_2$	$\frac{1}{j\omega C_2}=-j\omega L_2$	$j\omega L_2=\frac{-C_1}{j\omega\left(C_1C_2-C_m^2\right)}$
G_v	$-\frac{Z_2}{Z'_m}$	$-\frac{Z_2}{j\omega L_m}$	$-\frac{j\omega\left(C_1C_2-C_m^2\right)Z_2}{C_m}$

where L_m is the mutual inductance.

Then, the mapping relationship between the capacitive and inductive couplers can be given in Table I.

To further show the effectiveness and necessity of the proposed T-type model in studying the CPT system, the typical series/series (S/S) compensation network is shown in Fig. 4, where Z_1 and Z_2 are the primary and secondary port impedances, respectively, Z_{c1} and Z_{c2} are the primary and secondary compensation components, respectively, and R_{e1} and R_{e2} are the equivalent series resistors (ESRs) of the resonant components.

According to [17] and [21], to ensure that Z_1 is purely resistive, the required Z_{c1} and Z_{c2} are given in Table II. Combining the mapping relationships in Table I, Z_{c1} and Z_{c2} can be expressed by Z'_1, Z'_2, and Z'_m, and they are unified in the IPT and CPT systems. Moreover, the voltage gain $G_v = V_2/V_1$ is also unified by using the T-type model.

Except for Z_{c1} and Z_{c2}, R_{e1} and R_{e2} are also key parameters in the analysis, which are produced by the ESR of the compensation component and the coupler. The ESR of the compensation component can be directly measured by the *LCR* measurement instrument, whereas that of the coupler needs to be measured by making some changes in the circuit.

For the inductive coupler, the ESR of the primary port can be measured by making the secondary port open as shown in Fig. 5(a), and vice versa. Then, the ESR of the inductive coupler can be expressed by that of L_1 and L_2. Similarly, the ESR of the

Fig. 5. Measuring method for the ESR of the coupler. (a) Inductive coupler. (b) Capacitive coupler.

capacitive coupler can be measured by making the secondary port short as shown in Fig. 5(b). Then, the ESR of the capacitive coupler can be expressed by that of C_1 and C_2. Therefore, R_{e1} and R_{e2} are the same in both the IPT and CPT systems, which can be expressed as follows:

$$R_{e1} = \frac{\omega L_1}{Q_L} + \frac{1}{\omega C_1 Q_C} \tag{6}$$

$$R_{e2} = \frac{\omega L_2}{Q_L} + \frac{1}{\omega C_2 Q_C} \tag{7}$$

where Q_L is the quality factor of L_1 and L_2 and Q_C is the quality factor of C_1 and C_2.

Thus, all parameters of the IPT and CPT systems in Fig. 4 are unified by (6), (7), and Table II. Using the unified parameters, the existing technologies can be shared between the IPT and CPT systems.

From Fig. 4, the efficiency of the primary side η_1 and secondary side η_2 can be expressed as follows:

$$\eta_1 = \frac{1}{1+R_{e1}/\mathrm{Re}\left(\frac{|Z'_m|^2}{Z_{c2}+Z'_2+Z_2}\right)} \tag{8}$$

$$\eta_2 = \frac{1}{1+R_{e2}/\mathrm{Re}\left(Z_2\right)}. \tag{9}$$

From (8), it can be noted that η_1 is maximized when parameters are designed to satisfy the following equation:

$$Z_{c2} + Z'_2 + j\mathrm{Im}\left(Z_2\right) = 0. \tag{10}$$

Then, η_r can be expressed as follows:

$$\eta_r = \eta_1\eta_2 = \frac{1}{1+\frac{R_{e1}R_{e2}}{|Z'_m|^2}+\frac{R_{e1}\mathrm{Re}(Z_2)}{|Z'_m|^2}+\frac{R_{e2}}{\mathrm{Re}(Z_2)}} \le \eta_{r\max} \tag{11}$$

$$\eta_{r\max} = \frac{1}{\left(1+\sqrt{\frac{R_{e1}R_{e2}}{|Z'_m|^2}}\right)^2}. \tag{12}$$

From (11), it can be noted that η_r can reach a maximum value $\eta_{r\max}$, when the compensation network and the capacitive coupler are designed to satisfy the optimal load in the following equation:

$$\mathrm{Re}\left(Z_2\right) = \sqrt{\frac{|Z'_m|^2 R_{e2}}{R_{e1}}}. \tag{13}$$

According to (13), even the optimal load conditions in the IPT and CPT systems is the same, there are three typical differences between these two systems, which are summarized as follows:

1) Z'_m in the inductive coupler is only determined by L_m, whereas that in the capacitive coupler can be adjusted by changing C_1 and C_2 rather than only determined by C_m.
2) R_{e1} and R_{e2} in the inductive coupler are determined by the structure and the material of the coupler, whereas that in the capacitive coupler can be adjusted by changing C_1 and C_2.
3) Z_2 in the IPT system can be simplified as a pure resistance, whereas that in the CPT system is capacitive due to the parasitic capacitor of the power device and the high f_s.

That is, different from the IPT system, C_1 and C_2 determined by C_{e1} and C_{e2} and the capacitive coupler make it possible for the CPT system to realize the optimal load condition without changing Z_2.

C. Novel Method to Realize the Optimal Load Condition

To simplify the analysis, define the relationships between C_m and C_1/C_2 as follows:

$$C_1 = k_1 C_m \tag{14}$$

$$C_2 = k_2 C_m \tag{15}$$

where k_1/k_2 is the ratio of C_m and C_1/C_2, and k_1k_2 is equal to $1/{k_C}^2$ according to the definition of the coupling coefficient.

Substituting the conditions in (14), (15), and Table II into (3), (6), and (7), Z'_m, R_{e1}, and R_{e2} can be rewritten as follows:

$$Z'_m = \frac{1}{j\omega\left(k_1k_2 - 1\right)C_m} \tag{16}$$

$$R_{e1} = \frac{k_2}{\omega\left(k_1k_2 - 1\right)C_mQ_L} + \frac{k_2}{\omega k_1k_2C_mQ_C} \tag{17}$$

$$R_{e2} = \frac{k_1}{\omega\left(k_1k_2 - 1\right)C_mQ_L} + \frac{k_1}{\omega k_1k_2C_mQ_C}. \tag{18}$$

To ensure the optimal load condition in (13), the relationship between k_1 and k_2 should satisfy the following equation:

$$\frac{R_{e1}}{R_{e2}} = \left|\frac{Z'_m}{\mathrm{Re}\left(Z_2\right)}\right|^2 = \frac{k_2}{k_1}. \tag{19}$$

According to (16), $|Z'_m|$ is determined by k_1k_2. Thus, keeping k_1k_2 constant, the optimal load condition can be realized by adjusting the ratio of k_1 and k_2 according to (19).

However, as mentioned above, Z_2 in the CPT system is capacitive due to the parasitic capacitor of the power device and the high f_s. It needs to further analyze the impedance characteristic of the rectifier to obtain the accurate Re(Z_2). Besides, the impedance characteristic of the inverter is also analyzed to meet the design requirement for the soft-switching.

III. Impedance Analyses of the Inverter and the Rectifier

To reveal the impact of the inverter and the rectifier, the impedance characteristics are discussed in this section. Based on the impedance characteristics, the efficiency analyses of the inverter and the rectifier are conducted to provide theoretical support for studying η_{DC}.

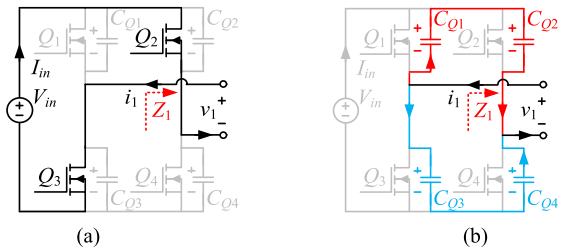

Fig. 6. Equivalent circuits of the inverter. (a) Conduction mode. (b) Commutation mode.

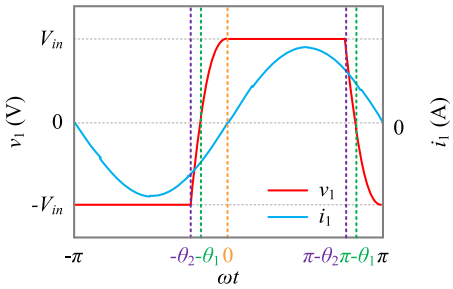

Fig. 7. Key waveforms of the inverter.

A. Impedance Characteristic of the Inverter

Due to the existence of the parasitic capacitor in the MOSFETs, the inverter has two working modes in one switching period as shown in Fig. 6. In the figure, C_{Q1}–C_{Q4} are the output junction capacitances of Q_1–Q_4, respectively, and they can be simplified as $C_Q = C_{Q1} = C_{Q2} = C_{Q3} = C_{Q4}$.

To illustrate the operation analysis, Fig. 7 shows the key waveforms in one switching period. To simplify the analysis, i_1 is defined as follows:

$$i_1 = \sqrt{2}I_1 \sin\left(\omega t\right) \tag{20}$$

where I_1 is the root mean square (rms) of i_1.

Since the operation analysis of [-π, 0] and [0, π] is similar, only the operation analysis of [-π, 0] is conducted.

Stage I. Conduction Mode [$-\pi$, $-\theta_2$]

During this stage, Q_2 and Q_3 conduct, making v_1 equal to $-V_{in}$ as shown in Fig. 6 (a). This stage ends at $\omega t = -\theta_2$ when Q_2 and Q_3 are turned OFF.

Stage II. Commutation Mode [$-\theta_2$, 0]

After Q_2 and Q_3 are turned OFF, i_1 keeps its flow direction. That is, i_1 discharges C_{Q1} and C_{Q4} while it charges C_{Q2} and C_{Q3} as shown in Fig. 6(b). In the ideal situation, when this stage ends at $\omega t = 0$, i_1 increases to 0, and v_{CQ1} and v_{CQ4} decrease to 0. During this stage, v_1 can be expressed as follows:

$$v_1 = -V_{\mathrm{in}} + \frac{\sqrt{2}I_1}{\omega C_Q}\left(\cos\left(\omega t\right) - \cos\left(\theta_2\right)\right). \tag{21}$$

According to (21), θ_1 and θ_2 can be obtained by letting v_1 be equal to 0 and V_{in}, thus

$$\theta_1 = \arccos\left(\frac{1 + \cos\left(\theta_2\right)}{2}\right) \tag{22}$$

$$\theta_2 = \arccos\left(1 - \frac{\sqrt{2}\omega C_Q V_{\text{in}}}{I_1}\right). \tag{23}$$

According to the definition of the impedance angle, the input impedance angle θ_{in} is equal to θ_1. Then, v_1 can be expressed by the fundamental wave as follows:

$$v_1 = \sqrt{2} V_1 \sin(\omega t + \theta_1) \tag{24}$$

where V_1 is the fundamental component of v_1.

Since $\sin(\omega t+\theta_1)$ is small in $[-\theta_1, 0]$ and $[\pi\text{-}\theta_2, \pi-\theta_1]$, V_1 is mainly determined by V_{in} and can be approximated as follows:

$$\begin{aligned} V_1 &= \frac{\sqrt{2}}{\pi}\int_{-\theta_1}^{\pi-\theta_1} v_1 \sin(\omega t + \theta_1)\, d\omega t \\ &\approx \frac{\sqrt{2}}{\pi}\int_{-\theta_1}^{\pi-\theta_1} V_{\text{in}} \sin(\omega t + \theta_1)\, d\omega t = \frac{2\sqrt{2}}{\pi} V_{\text{in}}. \end{aligned} \tag{25}$$

Ignoring the loss in the inverter, the input power provided by the dc source is equal to the output power of the inverter. Then, I_1 can also be expressed as follows:

$$I_1 = \frac{V_{\text{in}} I_{\text{in}}}{V_1 \cos(\theta_1)}. \tag{26}$$

Substituting (26) into (22) and (23), I_1, θ_1, and θ_2 can be expressed as follows:

$$I_1 = \frac{\pi I_{\text{in}}}{2\sqrt{2}} + \frac{\omega C_Q V_{\text{in}}}{\sqrt{2}} \tag{27}$$

$$\theta_1 = \arccos\left(\frac{1}{1 + 2\omega C_Q R_{\text{in}}/\pi}\right) \tag{28}$$

$$\theta_2 = \arccos\left(\frac{2}{1 + 2\omega C_Q R_{\text{in}}/\pi} - 1\right) \tag{29}$$

where R_{in} is the equivalent input resistance and can be obtained by $R_{\text{in}} = V_{\text{in}}/I_{\text{in}}$.

According to (27)–(29), Z_1 required for realizing the soft-switching can be expressed as follows:

$$\text{Re}(Z_1) = R_1 = \frac{I_{\text{in}}^2 R_{\text{in}}}{I_1^2} = \frac{\sin^2(\theta_2)}{\pi\omega C_Q} \tag{30}$$

$$\text{Im}(Z_1) = X_1 = R_1 \tan(\theta_1). \tag{31}$$

As given in (31), the inverter requires an extra inductance for ensuring that Z_1 is inductive enough to realize the soft-switching.

Moreover, the conduction loss and the turn-OFF loss of the inverter are directly related to I_1 and θ_1, which affects η_{inv}. That is, it is necessary to consider the impact of the impedance characteristic of the inverter when discussing efficiency.

B. Impedance Characteristic of the Rectifier

Same as the inverter, the rectifier has two working modes in one switching period as shown in Fig. 8, where C_{D1}–C_{D4} are the output junction capacitances of D_1–D_4, respectively, and they can be simplified as $C_D = C_{D1} = C_{D2} = C_{D3} = C_{D4}$.

To illustrate the operation analysis, Fig. 9 shows the key waveforms in one switching period. Since the analysis of the impedance characteristic of the rectifier is almost the same as

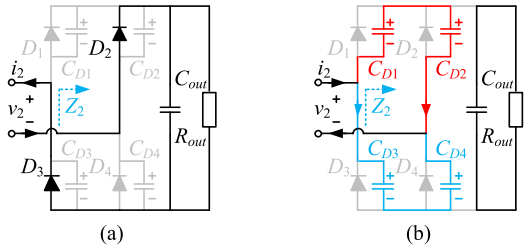

Fig. 8. Equivalent circuits of the rectifier. (a) Conduction mode. (b) Commutation mode.

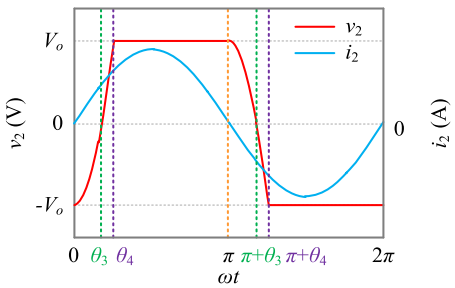

Fig. 9. Key waveforms of the rectifier.

TABLE III
ANALYSIS RESULTS OF THE IMPEDANCE CHARACTERISTIC OF THE RECTIFIER

	Expression
Impedance angle	$\theta_3 = \arccos\left(\frac{1}{1+2\omega C_D R_o/\pi}\right)$
Z_2	$\text{Re}(Z_2) = R_2 = \frac{1}{\frac{\pi^2}{8R_o} + \frac{\omega^2 C_D^2 R_o}{2} + \frac{\omega\pi C_D}{2}}$
	$\text{Im}(Z_2) = X_2 = -R_2 \tan(\theta_o)$

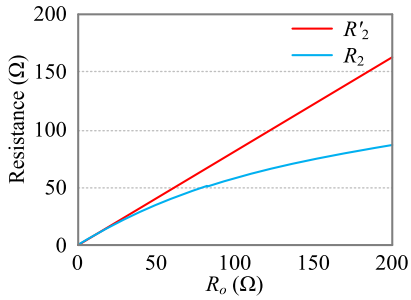

Fig. 10. Calculation results of R_2 and R'_2 against R_o.

that of the inverter, Table III gives the analysis results directly to reduce the repeated analysis.

Define R_2 obtained by the traditional method as $R'_2 = 8R_o/\pi^2$. Then, the calculation results of R_2 and R'_2 against R_o are shown in Fig. 10, where the calculation parameters are $C_D = 470$ pF, $V_o = 100$ V, and $f_s = 1$ MHz.

From Fig. 10, it can be noted that R_2 deviates a lot from R'_2 with R_o increasing, which has a great impact on the optimal load condition in (19). That is, it is necessary to consider the impact of the impedance characteristic of the rectifier when discussing efficiency.

C. Impact of the Impedance Characteristics on Efficiency

Considering the impact of the impedance characteristics, the efficiency is analyzed in detail, including $\eta_{\rm inv}$, $\eta_{r\max}$, and $\eta_{\rm rec}$.

1) DC–AC Efficiency: In the inverter, since the soft-switching of the MOSFETs is realized, the turn-ON loss can be ignored. Thus, the inverter loss, $P_{\rm inv}$, consists of the conduction loss $P_{\rm cond}$ and the turn-OFF loss $P_{\rm OFF}$.

According to Fig. 7, the rms of the current flowing through the MOSFETs during the switching period can be expressed as follows:

$$I_{\rm cond}=\sqrt{\frac{1}{2\pi}\int_0^{\pi-\theta_2}\left(\sqrt{2}I_1\sin(\omega t)\right)^2 d\omega t}=\sqrt{\frac{I_1^2\left(2\pi-2\theta_2-\sin(2\theta_2)\right)}{4\pi}}. \tag{32}$$

Thus, $P_{\rm cond}$ can be expressed as follows:

$$P_{\rm cond}=\frac{I_1^2R_{\rm dsON}\left(2\pi-2\theta_2-\sin(2\theta_2)\right)}{4\pi} \tag{33}$$

where $R_{\rm dsON}$ is the drain-to-source ON resistance.

According to Fig. 7, it can be noted that the turn-OFF current is $i_1(-\theta_2)$. Then, the turn-OFF loss, $P_{\rm OFF}$, can be expressed as follows:

$$P_{\rm OFF}=\frac{\pi I_1^2t_Ff_sR_1\sin(\theta_2)}{6\left(1+\cos(\theta_2)\right)} \tag{34}$$

where t_F is the fall time.

Since $P_{\rm inv}$ is equal to $4(P_{\rm cond}+P_{\rm OFF})$, the equivalent loss resistance of the inverter, $R_{\rm inv}$, can be expressed as follows:

$$R_{\rm inv}=\frac{R_{\rm dsON}\left(2\pi-2\theta_2-\sin(2\theta_2)\right)}{\pi}+\frac{2\pi t_Ff_sR_1\sin(\theta_2)}{3\left(1+\cos(\theta_2)\right)}. \tag{35}$$

Thus, $\eta_{\rm inv}$ can be expressed as follows:

$$\eta_{\rm inv}=\frac{R_1}{R_1+R_{\rm inv}}=\frac{1}{1+2\omega R_{\rm dsON}C_Qm+\frac{\omega t_Fn}{3}} \tag{36}$$

$$m=\frac{\pi-\theta_2}{\sin^2(\theta_2)}-\cot(\theta_2) \tag{37}$$

$$n=\frac{\sin(\theta_2)}{1+\cos(\theta_2)}. \tag{38}$$

Furthermore, the derivative of m and n with respect to θ_2 can be obtained by the following equations:

$$\frac{dm}{d\theta_2}=-\frac{2\left(\pi-\theta_2\right)\cos(\theta_2)}{\sin^3(\theta_2)}<0 \tag{39}$$

$$\frac{dn}{d\theta_2}=\frac{1+\cos(\theta_2)}{1+\cos^2(\theta_2)}>0. \tag{40}$$

With θ_2 increasing, the proportion of the conduction mode in the switching period decreases, leading to a decrement in $P_{\rm cond}$. Therefore, m caused by $P_{\rm cond}$ is in a negative correlation with θ_2.

Different from the conduction mode, the proportion of the commutation mode in the switching period increases with θ_2 increasing, leading to an increment in $P_{\rm OFF}$. That is, n caused by $P_{\rm OFF}$ is in a positive correlation with θ_2.

In [0, π/2], with θ_2 increasing, $dm/d\theta_2$ increases from $-\infty$ to 0, and $dn/d\theta_2$ shows a trend of first increasing and then decreasing in the range of (1, 1.21). That is, the denominator of $\eta_{\rm inv}$ shows a trend of first decreasing and then increasing, which makes $\eta_{\rm inv}$ show a trend of first increasing and then decreasing.

Substituting the impedance relationship of the resonant network into (29) and (30), θ_2 can be rewritten as follows:

$$\theta_2=\arcsin\sqrt{\frac{\pi\omega C_Q|Z'_m|^2}{R_2}}=\arcsin\sqrt{\frac{\pi C_Q}{C_m^2(k_1k_2-1)^2}\left(\frac{\pi}{16R_of_s}+\pi C_D^2R_of_s+\frac{\pi C_D}{2}\right)}. \tag{41}$$

Thus, $\eta_{\rm inv}$ is determined by f_s and k_1k_2 together. To improve $\eta_{\rm DC}$, the impact of the parameter on $\eta_{\rm inv}$ should be considered.

2) AC–AC Efficiency: As discussed before, L_1 is designed to ensure the soft-switching of the inverter, and L_2 is designed to maximum η_1. Thus, according to (31) and Tables II and III, L_1 and L_2 can be expressed as follows:

$$L_1=\frac{C_2}{\omega^2\left(C_1C_2-C_m^2\right)}+\frac{R_1\tan(\theta_1)}{\omega} \tag{42}$$

$$L_2=\frac{C_1}{\omega^2\left(C_1C_2-C_m^2\right)}+\frac{R_2\tan(\theta_3)}{\omega}. \tag{43}$$

Since L_1 and L_2 are mainly determined by the first term, R_{e1} and R_{e2} can still be expressed as (17) and (18). Then, $\eta_{r\max}$ can be rewritten as follows:

$$\eta_{r\max}=\frac{1}{\left(1+\sqrt{k_1k_2}\left(\frac{1}{Q_L}+\frac{k_1k_2-1}{Q_Ck_1k_2}\right)\right)^2}\approx\frac{1}{\left(1+\sqrt{k_1k_2}\left(\frac{1}{Q_L}+\frac{1}{Q_C}\right)\right)^2}. \tag{44}$$

That is, with k_1k_2 increasing, C_1C_2 increases and $\eta_{r\max}$ decreases. Moreover, Q_L and Q_C are determined by f_s, which should be discussed when designing the parameter.

3) AC–DC Efficiency: Different from $\eta_{\rm inv}$ and $\eta_{r\max}$, η_{rec} is determined by R_o, P_o, and the diode itself, which can be expressed as follows:

$$\eta_{rec}=\frac{1}{1+2V_F\sqrt{1/\left(R_oP_o\right)}} \tag{45}$$

where V_F is the forward voltage that can be obtained in the datasheet of the diodes.

As discussed above, the parameter has a great impact on efficiency. It is necessary to analyze the design of the parameter, improving $\eta_{\rm DC}$.

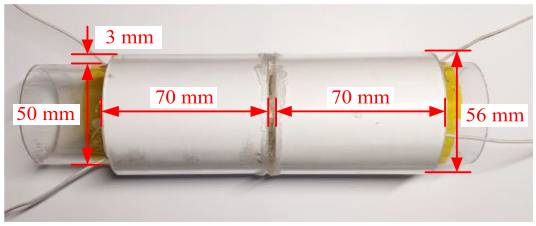

Fig. 11. Experimental capacitive coupler.

TABLE IV
CIRCUIT PARAMETERS DETERMINED BY THE APPLICATION AND THE POWER DEVICE

C_m	24 pF	air gap	3 mm
R_o	100 Ω	P_o	100-W
GaN	GS66508T	t_F	15 ns
R_{dsON}	50 mΩ	C_Q	364 pF
Diode	V30202C	V_F	0.65 V
C_D	470 pF		

IV. PARAMETER DESIGN METHOD TO IMPROVE THE DC–DC EFFICIENCY

Based on the efficiency analyses, a parameter method is proposed in this section to improve η_{DC}. First, the circuit parameter determined by the application and the power device is analyzed to provide basic support for the design method. Second, the voltage stress of the external capacitor is analyzed as the constraint condition for the design method. Then, a parameter design method is proposed and discussed in detail, improving η_{DC}.

A. Circuit Parameters Determined by the Application and the Power Device

As mentioned above, C_m, R_o, and P_o are determined by the application. In this article, the capacitive coupler is made of copper, and its structure is shown in Fig. 11. The measured C_m is 24 pF, which is given in Table IV. Moreover, R_o and P_o are set to be 100 Ω and 100-W, respectively.

Besides the circuit parameter determined by the application, the circuit parameter of the power device is also important in the design process. The MOSFETs used in the inverter are GS66508T, and the diode used in the rectifier is V30202C. The related circuit parameter is also given in Table IV. However, it should be noted that C_Q and C_D cannot be directly obtained in the datasheet. Using the charge equivalent model in [22], C_Q and C_D can be expressed as follows:

$$C_Q = \frac{1}{V_{\text{in}}}\int_0^{V_{\text{in}}} C_Q\left(v_{ds}\right)dv_{ds} \tag{46}$$

$$C_D = \frac{1}{V_o}\int_0^{V_o} C_D\left(v_r\right)dv_r \tag{47}$$

where v_{ds} is the drain-to-source voltage of the MOSFETs, and v_r is the reverse voltage of the diode.

Since V_o is 100 V, C_D is calculated to be 470 pF. From Table II, it can be noted that G_v is determined by f_s, C_1, and C_2 together, making V_{in} vary with different designable parameters. Considering that G_v is normally in the range of (0.5, 1.5), C_Q is set to be the average value of $C_Q|_{V\text{in}=50\text{ V}}$ and $C_Q|_{V\text{in}=150\text{ V}}$, which is calculated to be 364 pF.

B. Voltage Constraint of the External Capacitor

In the CPT system, the voltage across the external capacitor can be up to several hundred or thousand volts, which is an important constraint condition in the parameter design.

According to (3), the voltage stresses of the external capacitor, V_p and V_s, can be expressed as follows:

$$V_p = \frac{Z'_1\left(Z'_2 + j\omega L_2 + R_2 + jX_2\right) - Z'^2_m}{Z'm} \times\left(\frac{\pi I_o}{2\sqrt{2}} + \frac{\omega C_D V_o}{\sqrt{2}}\right) \tag{48}$$

$$V_s = \left(j\omega L_2 + R_2 + jX_2\right)\left(\frac{\pi I_o}{2\sqrt{2}} + \frac{\omega C_D V_o}{\sqrt{2}}\right). \tag{49}$$

Considering that C_D is only 470 pF, and the optimal load condition in (19), $|V_p|$, and $|V_s|$ can be simplified as in the following equations:

$$|V_p| = \left(\frac{\pi I_o}{2\sqrt{2}} + \frac{\omega C_D V_o}{\sqrt{2}}\right)\frac{\sqrt{k_1k_2+R_2}}{\omega(k_1k_2-1)C_mR_2} \approx \frac{\pi I_o}{2\sqrt{2}C_m}\sqrt{\frac{1}{k_1k_2}\left(1+\frac{R_2}{k_1k_2}\right)\left(\frac{C_D^2R_o}{2}+\frac{\pi C_D}{2\omega}+\frac{\pi^2}{8R_o\omega^2}\right)} \tag{50}$$

$$|V_s| = \left(\frac{\pi I_o}{2\sqrt{2}} + \frac{\omega C_D V_o}{\sqrt{2}}\right)\sqrt{R_2^2 + k_1k_2R_2} \approx \frac{\pi I_o}{2\sqrt{2}}\sqrt{R_2^2 + k_1k_2R_2}. \tag{51}$$

That is, with f_s increasing, R_2 decreases and ω increases, leading to a decrement in both $|V_p|$ and $|V_s|$. Similarly, with k_1k_2 increasing, $|V_p|$ decreases and $|V_s|$ increases. Therefore, by adjusting f_s and k_1k_2 according to (50) and (51), $|V_p|$ and $|V_s|$ can be limited in a reasonable voltage range. Since the rated voltage of the C0G capacitor is 2000 Vdc, the limited voltage is set to be 1000 Vac.

C. Parameter Design Method to Improve the DC–DC Efficiency

As discussed in Section III, η_{DC} consists of three parts, η_{inv}, $\eta_{r\max}$, and η_{rec}. Different from η_{inv} and $\eta_{r\max}$, η_{rec} is determined by R_o, P_o, and V_F, and has no relationship with f_s and k_1k_2. That is, η_{rec} is calculated to be 98.72%. Then, the impact of f_s and k_1k_2 on η_{inv} and $\eta_{r\max}$ is discussed to realize the parameter design.

Since the capacitive reactance of C_1 and C_2 is also affected by f_s, the design of f_s is first discussed. From (41), It can be noted that the variation trend of θ_2 against f_s is determined by whether f_s is larger than $1/4R_oC_D$ or not. Using the circuit parameters in Table IV, $1/4R_oC_D$ is calculated to be 5.3 MHz, which is larger

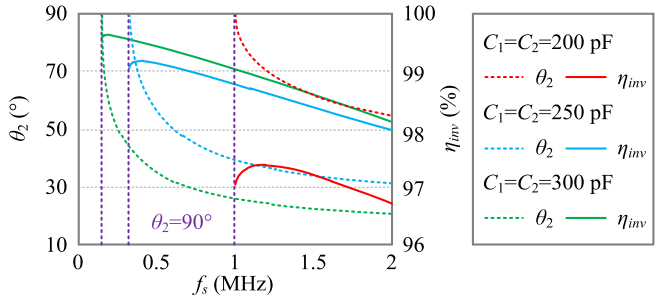

Fig. 12. Calculation results of θ_2 and $\eta_{\rm inv}$ against f_s.

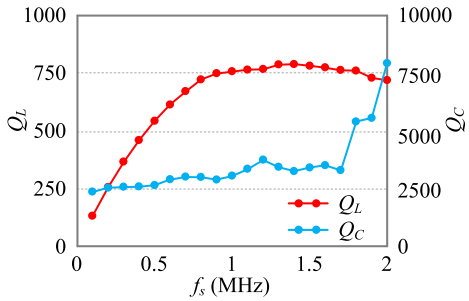

Fig. 13. Variation of Q_L and Q_C against f_s.

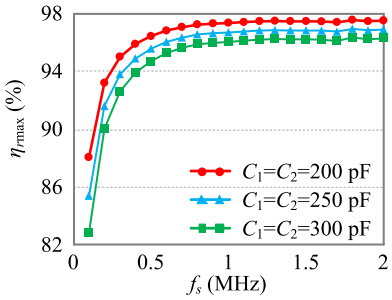

Fig. 14. Calculation results of $\eta_{r\max}$ against f_s.

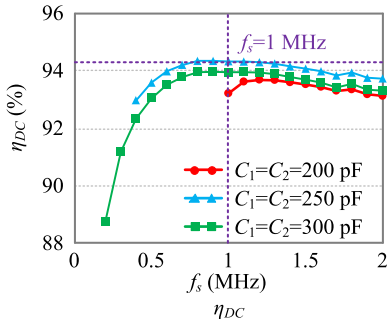

Fig. 15. Variation of $\eta_{\rm DC}$ against f_s.

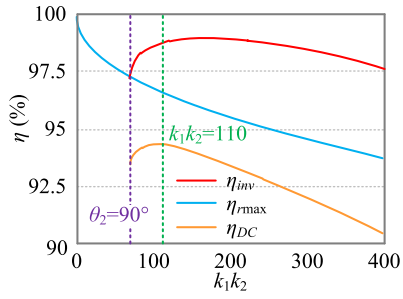

Fig. 16. Calculation results of $\eta_{\rm inv}$, $\eta_{r\max}$, and $\eta_{\rm DC}$ against k_1k_2.

than f_s. Thus, with f_s increasing, θ_2 decreases, making $\eta_{\rm inv}$ show a trend of first increasing and then decreasing.

Taking $C_1 = C_2 = 200/250/300$ pF as examples, Fig. 12 shows the variation of θ_2 and $\eta_{\rm inv}$ against f_s. The minimum $f_{s\min}$ is limited by the critical condition that $\theta_2 = 90°$, which is indicated with the purple dotted line. Moreover, with C_1 and C_2 increasing, $f_{s\min}$ decreases as shown in Fig. 12, which is also in coincidence with (41).

As shown in Fig. 12, $\eta_{\rm inv}$ shows a trend of first increasing and then decreasing in the range of ($f_{s\min}$, 2 MHz). With the given f_s, $\eta_{\rm inv}$ decreases with C_1 and C_2 decreasing. Thus, to improve $\eta_{\rm inv}$, it is necessary to choose a suitable f_s for the given C_1 and C_2, and vice versa.

To discuss the impact of f_s on $\eta_{r\max}$, the variation of Q_L and Q_C against f_s should be discussed. In this article, L_1 and L_2 are made of the 500-strand AWG 46 Litz-wire, C_1 and C_2 consist of the C0G capacitor and the capacitive coupler is made of copper. Fig. 13 shows the variation of Q_L and Q_C against f_s.

As shown in Fig. 13, it can be noted that Q_L varies a lot with different f_s when f_s is smaller than 1 MHz. Using (44), Fig. 14 shows the calculation results of $\eta_{r\max}$ against f_s. With f_s increasing, $\eta_{r\max}$ increases and approaches the asymptote. Different from $\eta_{\rm inv}$, $\eta_{r\max}$ increases with C_1 and C_2 decreasing.

Based on the above analysis, the variation of $\eta_{\rm DC}$ against f_s can be obtained, which is shown in Fig. 15. With f_s increasing, $\eta_{\rm DC}$ shows a trend of first increasing and then decreasing. With C_1 and C_2 increasing, the variation of $\eta_{\rm DC}$ is the same as that with f_s increasing. That is, to maximum $\eta_{\rm DC}$, C_1 and C_2 should be designed to be around 250 pF, and then f_s should be designed to be 1 MHz.

It should be noted that the design value of C_1 and C_2 is only an approximate range. Moreover, to ensure that η_r is equal to $\eta_{r\max}$, C_1 and C_2 should be designed to satisfy the optimal load condition in (19). Thus, the design of C_1 and C_2 should be further discussed.

Since f_s is designed to be 1 MHz, the measured value of Q_L is 760, and that of Q_C is 3092. Using the optimal load condition in (19), Fig. 16 shows the variation of $\eta_{\rm inv}$, $\eta_{r\max}$, and $\eta_{\rm DC}$ against k_1k_2. Similar to Fig. 12, the minimum k_1k_2 is limited by the critical condition that $\theta_2 = 90°$, which is indicated with the purple dotted line. From the figure, it can be noted that the maximum $\eta_{\rm DC}$ appears at $k_1k_2 = 110$.

As discussed above, $|V_p|$ and $|V_s|$ are important constraints in the parameter design. According to (50) and (51), k_1k_2 should be in the design range of (80, 173), which covers the optimization point that $k_1k_2 = 110$. If the optimization point is out of the design range determined by the voltage constraint, f_s can be increased to expand the design range of k_1k_2. Then, repeat the design process until it covers the optimization point.

In this design, k_1k_2 is chosen to be 110, which meets the requirement of efficiency optimization and the voltage constraint. Then, k_1 is calculated to be 9.9, and k_2 is calculated to be 11.1

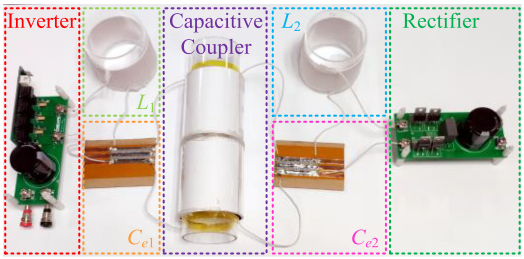

Fig. 17. Experimental prototype of the CPT system.

TABLE V
DESIGNED AND MEASURED CIRCUIT PARAMETERS

	Designed	Measured		Designed	Measured
k_1k_2	110	117	k_C	9.5%	9.2%
C_1	237.6 pF	244.4 pF	C_2	266.4 pF	276.2 pF
L_1	109.2 μH	107.3 μH	L_2	98.4 μH	96.2 μH

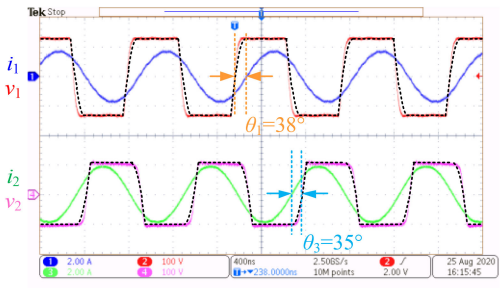

Fig. 18. Input and output experimental waveform using $k_pk_s = 117$.

according to (19). Using (14) and (15), C_1 and C_2 are calculated to be 237.6 and 266.4 pF, respectively.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed circuit parameters design method, the experiment is conducted using a 100-W double-sided *LC* compensated CPT system. Fig. 17 shows the photograph of the experimental prototype.

A. Experiments Using the Optimized Circuit Parameters

Using the circuit parameters in Table V, Fig. 18 shows the input and output experimental waveforms with full load, where the black dotted line represents the theoretical waveforms of V_1 and V_2 as analyzed in Section III. From the figure, it can be noted that the theoretical waveforms are almost in coincidence with the experimental waveforms, which verifies the accuracy of the analysis in the impedance characteristics.

Fig. 19 shows the measured efficiency with 10% load and full load. From the measurement results, it can be noted that $\eta_{\rm DC}$ can reach 89.39% with 10-W output and 93.02% with 100-W output, which verifies that the proposed circuit parameters design method can realize high $\eta_{\rm DC}$.

Fig. 20 shows the calculated and measured θ_1 and θ_3 with different P_o. From the figure, it can be noted that $\theta_{3\_\rm mea}$ is almost in coincidence with $\theta_{3\_\rm cal}$, and the small deviation is caused by the difference of C_D between the device and the datasheet.

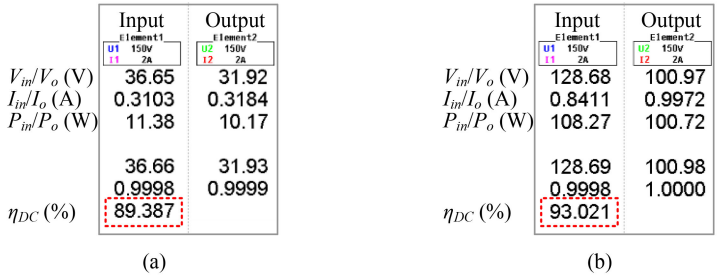

Fig. 19. Measured efficiency. (a) With 10% load. (b) With full load.

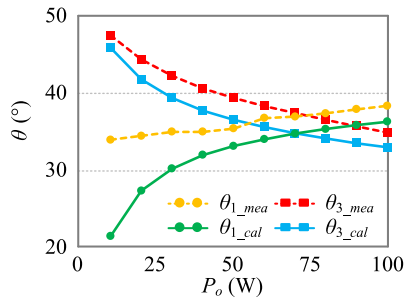

Fig. 20. Calculated and measured θ_1 and θ_3 with different P_o.

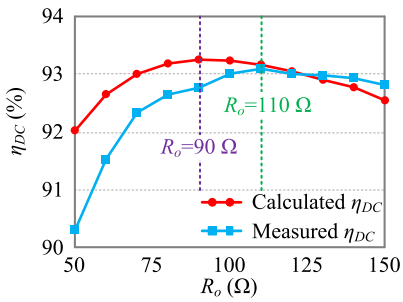

Fig. 21. Calculated and measured $\eta_{\rm DC}$ against R_o.

Different from θ_3, θ_1 is determined by both C_Q and C_D. From the datasheet, it can be noted that C_Q and C_D vary sharply when $V_{\rm in}$ and V_o are small, making it hard to obtain the accuracy capacitance. Therefore, the deviation between $\theta_{1\_\rm mea}$ and $\theta_{1\_\rm cal}$ increases with P_o decreasing as shown in Fig. 20.

To verify the realization of the optimal load, experiments are conducted against R_o. Fig. 21 shows the calculated and measured $\eta_{\rm DC}$ with different R_o. From the figure, it can be noted that both the calculated and measured $\eta_{\rm DC}$ show a trend of first increasing and then decreasing with R_o increasing. The maximum value of the calculated $\eta_{\rm DC}$ appears at $R_o = 90\ \Omega$, whereas that of the measured $\eta_{\rm DC}$ appears at $R_o = 110\ \Omega$, which is in coincidence with the designed optimal load $R_o = 100\ \Omega$. However, with R_o increasing, the deviation of calculated and measured $\eta_{\rm DC}$ increases from -1.7% to 0.26%, which is caused by the variation of V_F against I_o. Due to the constant P_o, I_o is in a negative correlation with R_o, making V_F be in a negative correlation with R_o as well. Thus, with R_o increasing, the increment of the measured $\eta_{\rm rec}$ is larger than that of the calculated $\eta_{\rm rec}$, resulting in the deviation of calculated and measured $\eta_{\rm DC}$.

Moreover, using the constant $V_{\rm in} = 129$ V, Fig. 22 shows the variation of I_2 against R_o. The nominal I_2 at $R_o = 100\ \Omega$

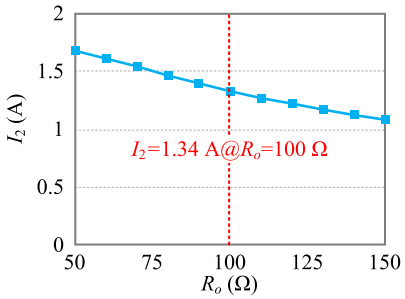

Fig. 22. Variation of I_2 against R_o.

TABLE VI
PARAMETERS FOR THE EXPERIMENTS WITH DIFFERENT F_S

	Designed	Measured		Designed	Measured
f_s	0.8 MHz	0.82 MHz	η_{DC}	92.06%	91.97%
L_1	169.15 μH	168.21 μH	L_2	151.56 μH	150.76 μH
θ_1	39°	40°	θ_3	30°	33°
V_p	905 V	1140 V	V_s	913 V	963 V
f_s	1 MHz	1.02 MHz	η_{DC}	93.24%	93.02%
θ_1	37°	38°	θ_3	33°	35°
V_p	871 V	774 V	V_s	754 V	799 V
f_s	1.5 MHz	1.52 MHz	η_{DC}	91.24%	90.82%
L_1	49.56 μH	49.75 μH	L_2	45.02 μH	45.55 μH
θ_1	31°	34°	θ_3	38°	42°
V_p	809 V	625 V	V_s	565 V	582 V

is 1.34 A, while the minimum value $I_{2\min} = 1.09$ A appears at $R_o = 150\ \Omega$, and the maximum value $I_{2\max} = 1.7$ A appears at $R_o = 50\ \Omega$. That is, even R_o varies in such a wide range, the variation of I_2 is still maintained within $\pm 30\%$.

B. Experiments to Verify the Design of f_s

Keeping k_1k_2 constant, experiments are conducted with $f_s =$ 0.8/1.5 MHz to verify its impact on the efficiency. Using the circuit parameters in Table VI, Fig. 23 shows the input and output experimental waveforms with different f_s. From Figs. 18 and 23, it can be noted that θ_2 decreases with f_s increasing, which is in coincidence with the variation trend in Fig. 12. Moreover, θ_2 is in a negative correlation with f_s, which satisfies the variation trend in (41).

Fig. 24 shows the voltage stress of the external capacitor. From the measured $|V_p|$ and $|V_s|$, it can be noted that $|V_p|$ and $|V_s|$ decrease obviously with f_s increasing, which is in coincidence with the analysis in Section IV.

Table VI gives the designed and measured parameters for the experiments with different f_s. From the measured results, it can be noted that $\eta_{\rm DC}$ measured with $f_s = 1$ MHz is larger than that with $f_s = 0.8/1.5$ MHz, which verifies the necessity and effectiveness of the design in f_s. Moreover, the measured values of θ_1, θ_3, and $\eta_{\rm DC}$ have good coherence to the designed ones, which verifies the accuracy of the impedance and efficiency analysis. Although the designed and measured $|V_p|$ or $|V_s|$ decrease with f_s increasing, the deviation between the designed and the measured value is up to 26%. Such a large deviation is caused by the parasitic capacitance of the voltage probe, which can be several or tens of picofarad, affecting the circuit resonance.

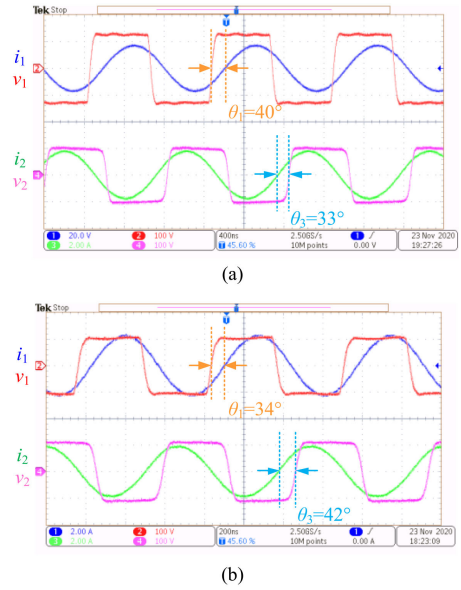

Fig. 23. Input and output experimental waveforms. (a) $f_s = 0.8$ MHz. (b) $f_s = 1.5$ MHz.

TABLE VII
DESIGNED AND MEASURED CIRCUIT PARAMETERS OF THE CONTRAST POINT

	Designed	Measured		Designed	Measured
k_1k_{2A}	90	95	k_{CA}	10.5%	10.3%
C_{1A}	175.5 pF	183.9 pF	C_{2A}	295.4 pF	297.1 pF
L_{1A}	148.9 μH	149.1 μH	L_{2A}	92 μH	95.4 μH
k_1k_{2B}	130	131	k_{CB}	8.8%	8.7%
C_{1B}	305.7 pF	308.5 pF	C_{2B}	245 pF	245.3 pF
L_{1B}	85.7 μH	88.3 μH	L_{2B}	109.9 μH	109.2 μH

Fig. 25 shows the loss breakdown of the CPT system with different f_s. From the figure, it can be noted that with f_s increasing, $P_{\rm inv}$ increases, and P_r that consists of P_{L1}, P_{L2}, P_{C1}, and P_{C2} decreases, which is in coincidence in the analysis in Section IV. Using the proposed design method, f_s is designed to be 1 MHz, which performs well in both $P_{\rm inv}$ and P_r.

C. Experiments to Verify the Design of k_1k_2

As shown in Fig. 16, the maximum $\eta_{\rm DC}$ appears at $k_1k_2 = 110$. To verify the accuracy of the optimized k_1k_2, two typical points $k_1k_2 = 90$ and 130 are chosen as contrast designed parameters. The first typical point $k_1k_2 = 90$ performs well in $\eta_{\rm rmax}$ but badly in $\eta_{\rm inv}$. The second typical point $k_1k_2 = 130$ performs well in $\eta_{\rm inv}$ but badly in $\eta_{\rm rmax}$. Table VII shows the designed and measured circuit parameters of the contrast point.

To verify the impact of k_1k_2 on the efficiency, experiments are conducted with the circuit parameters in Table VII. Fig. 26 shows the calculated and measured $\eta_{\rm DC}$ with different k_1k_2 and P_o. In the situation that $k_1k_{2\rm A} = 95$, η_r increases because k_{CA} is larger than k_C. However, it also leads to a decrement in $\eta_{\rm inv}$, which makes $\eta_{\rm DC}$ smaller than that with k_1k_2. Similarly, in the situation

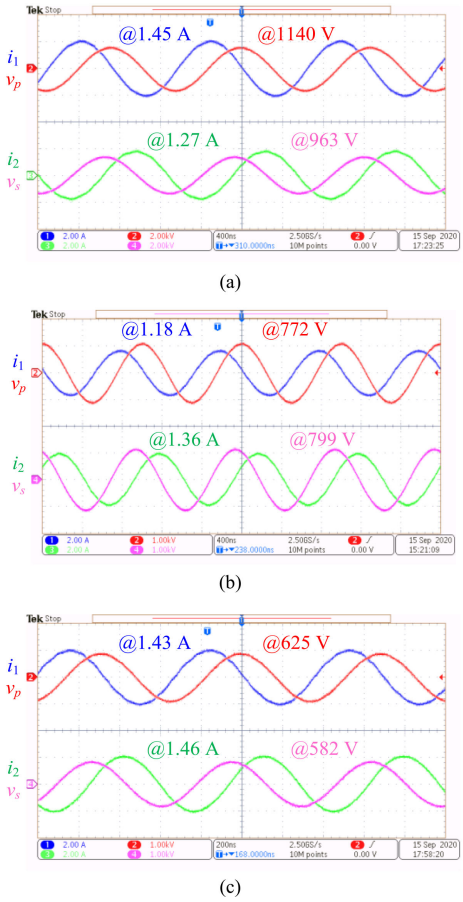

Fig. 24. Voltage stress of the external capacitor. (a) $f_s = 0.8$ MHz. (b) $f_s = 1$ MHz. (c) $f_s = 1.5$ MHz.

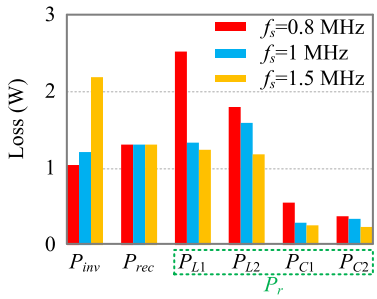

Fig. 25. Loss breakdown of the CPT system with different f_s.

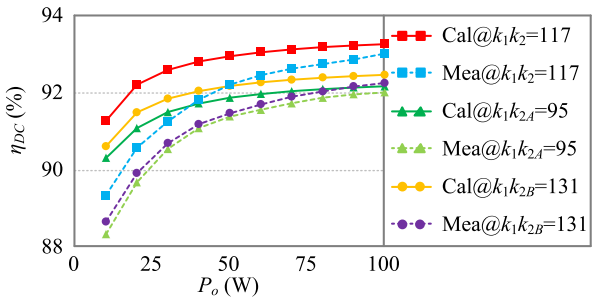

Fig. 26. Calculated and measured $\eta_{\rm DC}$ with different k_1k_2 and P_o.

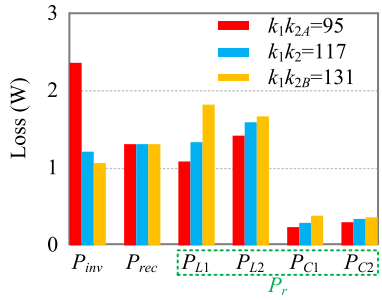

Fig. 27. Loss breakdown of the CPT system with different k_1k_2.

that $k_1k_{2\rm B} = 131$, $\eta_{\rm inv}$ increases, and η_r decreases, leading to a smaller $\eta_{\rm DC}$ compared to that with k_1k_2. The comparative results of the calculated and measured $\eta_{\rm DC}$ verify the necessity and effectiveness of the design in k_1k_2.

Similar to that in Fig. 25, the loss breakdown of the CPT system with different k_1k_2 is shown in Fig. 27. From the figure, it can be noted that with k_1k_2 increasing, $P_{\rm inv}$ decreases, and P_r increases, which is in coincidence in the analysis in Section IV. Using the proposed design method, k_1k_2 is designed to be around 110, which performs well in both $P_{\rm inv}$ and P_r.

VI. Conclusion

This article presents a parameter design method to improve the dc–dc efficiency of the double-sided *LC* compensated CPT system. The capacitive coupler is analyzed by using a T-type model, giving direct insight into the impedance refracted from the secondary side. Using the T-type model, the CPT system can realize the optimal load condition easily by adjusting the external capacitance. To quantify the relationship between the optimal load and external capacitance, the impedance characteristics of the inverter and the rectifier are discussed. Then, the efficiency analyses of the inverter, the resonant network, and the rectifier are conducted in detail. To improve the dc–dc efficiency, a parameter design method is proposed, which limits the external capacitor to ensure that the voltage stress is in a reasonable range. Although the design example is conducted with the double-sided *LC* compensated CPT system, the analysis and design process can be extended to other compensation networks easily. The effectiveness of the proposed design method is verified with a 100-W output CPT system. The experimental results show that the dc–dc efficiency can reach 89.39% with 10-W output, and reach 93.02% with 100-W output.

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