Common-Mode Current Reduction at DC and AC Sides in Inverter Systems by Passive Cancellation

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***Abstract*—It is well known that PWM inverters generate common-mode (CM) voltages, which may cause the CM electromagnetic interference and leakage current in the applications such as photovoltaic or motor drive systems. The CM noise issue becomes more severe with the application of silicon-carbide devices, which have higher *dv/dt* than silicon devices. In this article, a passive cancellation method is proposed by inserting two CM transformers (CMT) into the input and output side of the inverter, respectively. The selection of the turns ratio for two CMTs is analyzed and revealed to achieve the best CM noise cancellation, and the influence of the parasitics in the CMT is investigated as they limit the bandwidth for CM noise cancellation. Compared to the passive filter, floating filter, and the active cancellation method, the proposed method could reduce the CM noise at both sides simultaneously regardless of the CM impedance of the source or the load. A single-phase inverter is built, and the proposed method achieves 40 dB reduction at both sides, which verifies the effectiveness of the proposed method.**

***Index Terms*—Common-mode noise, inverter system, leakage current, passive cancellation.**

I. Introduction

FOR photovoltaic (PV) and motor drive systems, the pulsewidth modulation (PWM) inverter is an essential unit to achieve dc to ac inversion with high efficiency and high quality waveforms. As the switches in the inverter turn ON and OFF periodically with high switching frequency, the displacement current is generated in the parasitic capacitances between the high *dv/dt* nodes in the circuit and the ground, which causes common-mode (CM) noise. With the application of fast-switching silicon-carbide (SiC) devices in PWM inverters, the CM noise issue becomes more severe, as the *dv/dt* in the circuit is much higher than that in silicon (Si) device-based circuits.

For the PV inverter system shown in Fig. 1(a) [1], [2], the CM current entering the grid is referred as the leakage current, which may cause safety hazards. For the motor drive system shown in Fig. 1(b) [3], the CM current drawing from the dc power supply via the input power cables may cause conducted

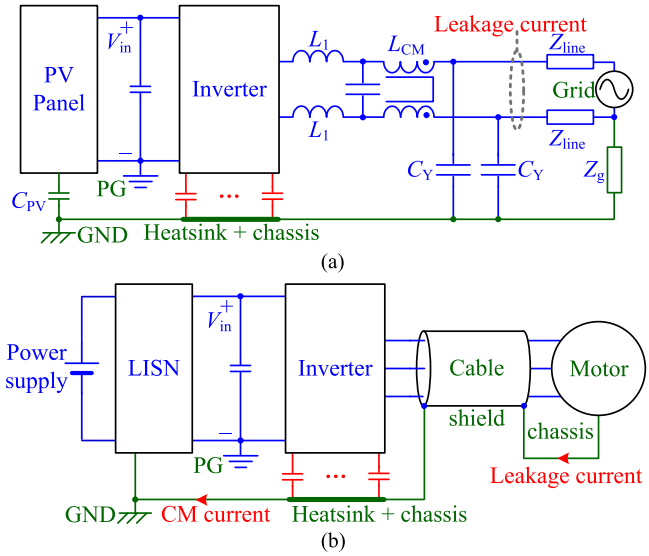

Fig. 1. Typical inverter systems. (a) Single phase PV inverter system [1]. (b) Three-phase motor drive system [3].

electromagnetic interference (EMI), and the CM current going into the motor (also referred as the leakage current), may result in bearing damage and insulation breakdown. Therefore, how to effectively reduce the CM EMI and the leakage current in an inverter system is always a concerned issue [4]–[7].

The methods for reducing CM EMI and leakage current in an inverter system can be categorized into the following groups, including the passive filter [8]–[11], active filter [3], topology [12]–[17], modulation [18]–[21], balancing [22], [23], and CM noise cancellation [24]–[28]. The passive filter attenuates the CM noise by placing the CM inductors along the CM noise propagation path to increase the impedance, and adding Y capacitors to bypass the noise into the ground. As the filter design for both sides is coupled because of the CM loop, the attenuation of CM noise at one side could make the CM noise at the other side even worse as the Y capacitors change the impedance of the CM loop [10]. To handle this issue, floating EMI filter is proposed in [11] by connecting the ac side Y capacitors to the midpoint of the dc-link for designing the filters independently. On the other hand, the active filter attenuates the CM noise with active devices for sensing and compensating the CM noise. The CM impedance of the source and the load must be considered for designing the passive or active filter, as they affect the CM noise attenuation of the filter.

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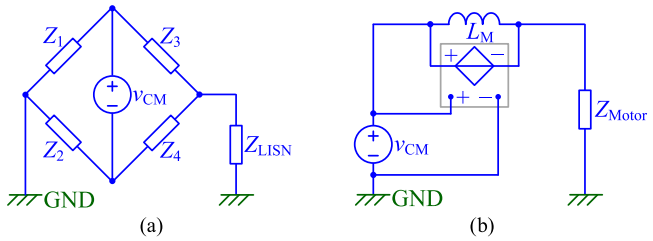

Fig. 2. CM noise reduction method. (a) Balancing technique. (b) CM noise cancellation.

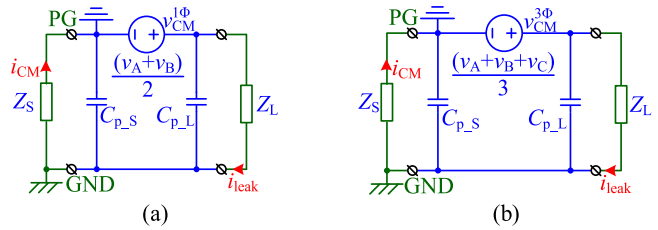

Fig. 3. Generalized CM noise model. (a) Single phase inverter system. (b) Three-phase inverter system.

At the topology level, it is revealed that the CM noise is essentially attributed to the CM voltage of the inverter, and the topology with constant CM voltage inherently has no CM noise/current generation. For PV inverter systems, various inverter topologies with constant CM voltage have been proposed [12]–[14]. For motor drive systems, relevant topologies can also be found in [15]–[17].

Instead of altering the circuit configuration, advanced modulation strategies of PWM converters can modify the CM voltage spectra and reduce its harmonic amplitude, hence attenuating the CM noise [18]–[21]. The CM noise reduction is usually coupled with other issues such as switching loss, output voltage harmonics, and neutral point voltage balance, so the design tradeoffs need to be addressed. As the CM voltage spectra is reduced, the topology and advanced modulation could reduce the CM current at both sides. However, the increased hardware cost and low frequency harmonics should be concerned when applying these methods.

The principle of CM noise reduction via balancing is shown in Fig. 2(a) [22], [23], where $v_{\rm CM}$ is the CM voltage of the inverter, $Z_{\rm LISN}$ is the equivalent impedance for the CM noise at the line impedance stabilization network (LISN) side, and Z_1–Z_4 are impedances of the related branches along the CM noise propagation path. As long as the impedances Z_1–Z_4 are matched ($Z_1/Z_2 = Z_3/Z_4$), the CM noise appeared at the LISN side is eliminated.

The principle of CM noise cancellation is shown in Fig. 2(b), where $Z_{\rm motor}$ is the CM impedance of the motor, and a CM transformer (CMT) with a magnetizing inductance of L_m is used to sense the CM voltage and inject the same amount of voltage with opposite polarity to cancel the CM voltage. Therefore, it reduces the CM noise in a feed-forward way. The CM noise cancellation could be implemented either by active circuits or passive circuits. In [24], an active cancellation circuit is proposed to eliminate the CM current in the motor drive system, where a single CMT with 1:1 turns ratio is placed at the load side. The corresponding realization by a passive circuit can be also found in [25]. The CM noise cancellation methods in [24] and [25] could greatly reduce the CM noise of an inverter system at the load side, while the CM noise reduction at the source side is not significant.

In this article, a generalized CM noise model of an inverter system is presented. By analyzing the CM noise model, a passive cancellation method is proposed by inserting two CMTs into the inverter input and output side, respectively. This article has provided guidance on the turns ratio selection for the two CMTs as a main contribution. The influence of the parasitics in the CMT is also investigated as they limit the bandwidth for CM noise cancellation. Compared to the passive filter, floating filter, and active cancellation, the proposed method could reduce the CM noise at both sides simultaneously regardless of the CM impedances of the source or the load.

The rest of this article is organized as follows. In Section II, a generalized CM noise model of the inverter system is presented. In Section III, the principle of the passive cancellation method is proposed, and the design considerations are presented. In Section IV, the passive cancellation method is explained from the current balance viewpoint. In Section V, the considerations for practical applications are also discussed, and the comparison between the passive filter, floating filter, the active cancellation method, and the proposed method is given. In Section VI, a single-phase inverter is built, and the CM current at the input side and the output side are measured and compared, which validates the proposed passive cancellation method. Finally, Section VI concludes this article.

II. Generalized Inverter CM Noise Model

The PV and motor drive inverters are two typical inverter systems that are widely used, and the CM noise model for each of them had been presented in [2] and [3] with well-known modeling approach. This section summarizes these models and provides a generalized CM noise model, as shown in Fig. 3, where, Z_S and Z_L are the equivalent CM impedance of the source and load side, respectively. The voltage source is the CM voltage $v_{\rm CM}$ of the inverter, and v_A, v_B, and v_C are the phase voltages of the inverter.

In Fig. 3, the capacitances $C_{\rm p\_S}$ and $C_{\rm P\_L}$ are related with the CM parasitic capacitances of the inverter, and they are given by

$$C_{\rm p\_S} = \sum_{\rm i=1} C_{\rm Si} \tag{1}$$

$$C_{\rm p\_L} = \sum_{\rm i=1} C_{\rm Di} \tag{2}$$

where $C_{\rm Si}$ is the parasitic capacitance between the positive or negative terminals of the dc bus and GND. $C_{\rm Di}$ is the parasitic capacitance between the midpoint of each phase leg and GND. Take a single phase PV inverter in Fig. 4 as an example, its CM noise circuit is given in Fig. 3(a), and $C_{\rm p\_S}$ and $C_{\rm p\_L}$ are equal

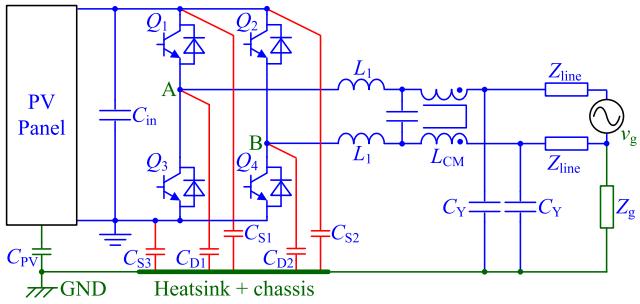

Fig. 4. Single phase PV inverter with critical CM parasitic capacitances.

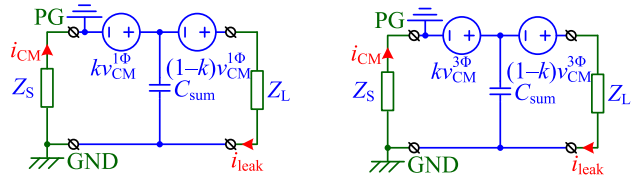

Fig. 5. Equivalent CM circuit. (a) Single phase. (b) Three-phase.

to

$$C_{\mathrm{p\_S}} = C_{\mathrm{S1}} + C_{\mathrm{S2}} + C_{\mathrm{S3}} \tag{3}$$

$$C_{\mathrm{p\_L}} = C_{\mathrm{D1}} + C_{\mathrm{D2}}. \tag{4}$$

The CM parasitic capacitances mainly exist between the power switches and the heatsink, so their value depends on the area of corresponding terminal, insulation material, and its thickness between the power switches and the heatsink.

III. Derivation of the Passive Cancellation Method

The CM noise circuits in Fig. 3(a) and (b) indicate that the CM noise results from the CM voltage of the inverter, and cancelling the CM voltage will eliminate the CM current i_{CM} and the leakage current i_{leak}. For better derivation of the cancellation method, the circuits in Fig. 3 are transformed into their equivalent circuits as shown in Fig. 5, where the network of the inverter with Δ connection is changed into Y connection.

The proof for this transformation is provided in Appendix A. In Fig. 5, C_{sum} and the coefficient k are given by

$$C_{\mathrm{sum}} = C_{\mathrm{p\_S}} + C_{\mathrm{p\_L}} \tag{5}$$

$$k = C_{\mathrm{p\_L}} \cdot (C_{\mathrm{sum}})^{-1}. \tag{6}$$

As seen from (6), the coefficient k is determined by the capacitance ratio, which is in the range of (0, 1).

Referring to Fig. 5, the passive cancellation method can be directly derived. Because there are two voltage sources in the circuit, two cancellation voltage sources can be inserted in the circuit to cancel the voltage of each loop individually, as shown in Fig. 6. In order to nullify the noise current i_{CM} and i_{leak}, the cancellation voltage v_{comp1} and v_{comp2} are expected to be

$$v_{\mathrm{comp1}} = kv_{\mathrm{CM}} \tag{7}$$

$$v_{\mathrm{comp2}} = (1-k)\, v_{\mathrm{CM}}. \tag{8}$$

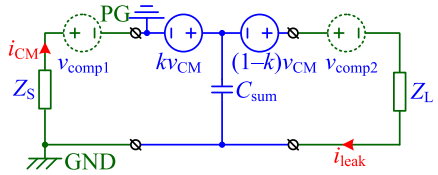

Fig. 6. Cancellation principle.

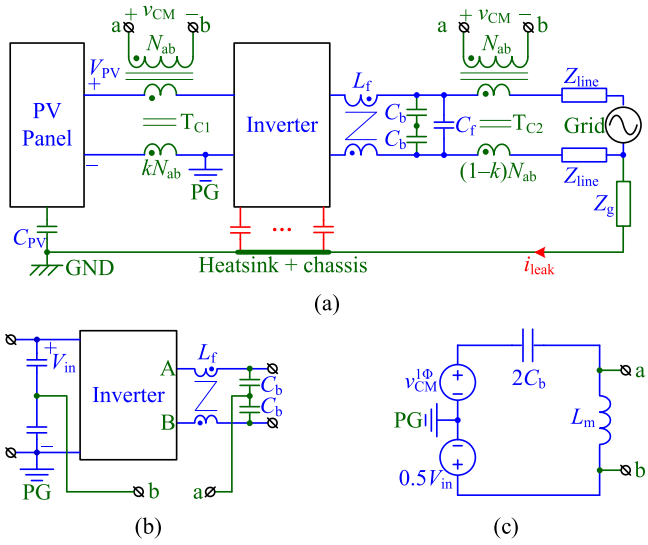

Fig. 7. Realisation of the passive cancellation method. (a) CMT in PV inverter system. (b) CM voltage sensing circuit for single-phase inverter [24]. (c) Equivalent circuit for CM voltage sensing circuit in single-phase inverter without the parasitics of CMT.

According to [24]–[27], the cancellation voltage can be realized by CMT as shown in Fig. 7(a). The CM voltage v_{CM} of the inverter is injected to the winding ab at the top of T_{C1} and T_{C2}, and the cancellation voltages are induced by the other windings. The injecting winding turns in T_{C1} and T_{C2} are kN_{ab} and $(1-k)N_{\mathrm{ab}}$, respectively, referring to (7) and (8).

The sensing circuit for the CM voltage of the single-phase inverter is given in Fig. 7(b). Part of the output filtering capacitance is split as two capacitors C_b in series [10], so that the harmonic filter design and the CM voltage sensing circuit design are decoupled. The capacitors C_b works with the coupled inductor L_{f} to sense the CM voltage of the inverter. The CM impedance of L_f can be neglected as its two windings are differentially coupled. The equivalent series inductance (ESL) of C_b should be small, so that C_b has negligible effect on the higher frequency range for cancellation. Fig. 7(c) shows the equivalent circuit for the sensing and injecting circuit of CM voltage in single-phase inverter, where L_m is the paralleled magnetizing inductance of T_{C1} and T_{C2}. Since the CM voltage contains the switching frequency f_S component and its harmonics, the impedance of L_m at the frequencies higher than f_S should be much larger than the capacitor branch, so v_{ab} is close to v_{CM} as desired. Therefore, the resonant frequency f_r of L_m and $2C_b$ is much lower than f_S to pass the spectrum of v_{CM}. Meanwhile, f_r should be much higher than the power frequency f_0 to avoid the interaction between L_m and dc-link capacitors. The higher cut-off frequency for cancellation

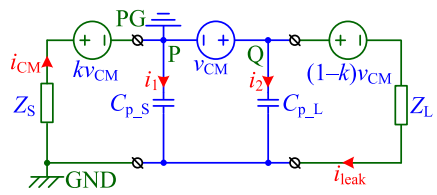

Fig. 8. Passive cancellation from the current balance viewpoint.

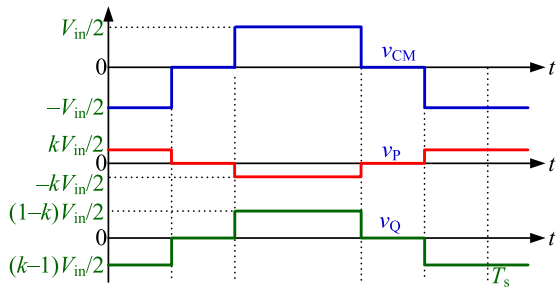

Fig. 9. Typical electric potential of P and Q in a switching period.

is limited by the parasitics of CMT, which will be discussed in Section V. For three-phase inverter system, the CM voltage sensing and injecting circuit is similar. The proposed method is passive cancellation as the sensing and injecting circuit for the CM voltage is realised only by passive components.

As discussed above, the passive cancellation for CM noise in inverter systems requires a CM voltage sensing circuit consisting of a coupled inductor and two (three) capacitors for single-phase (three-phase) inverter, which can be reused as the output filtering circuit. Besides, two CMTs are required for injecting the CM voltage at the dc and ac side. The considerations for implementing the passive cancellation method will be discussed in Section V.

IV. Current Balance Viewpoint of the Passive Cancellation Method

In this section, the passive cancellation method in this article is revisited from the current balance viewpoint, in order to understand the noise cancellation mechanism in the inverter when the passive cancellation method is applied.

Fig. 8 shows the equivalent CM noise circuit of the inverter, which adopts the passive cancellation method. By selecting the ground node GND as the electrical potential reference, the typical waveform for the CM voltage $v_{\rm CM}$ of a single-phase inverter is given in Fig. 9. The dc component in $v_{\rm CM}$ is removed because it does not affect the CM noise. In addition, $i_{\rm CM}=0$ and $i_{\rm leak}=0$ can be expected when the passive cancellation method is applied. Thus, Fig. 9 also shows the electric potential of P and Q with respect to the GND.

According to Fig. 8, the sum of i_1 and i_2 is given by

$$i_1+i_2=C_{\rm p\_S}\frac{d}{dt}v_{\rm P}+C_{\rm p\_L}\frac{d}{dt}v_{\rm Q}. \tag{9}$$

In Fig. 8, $v_{\rm P}$ and $v_{\rm Q}$ are equal to

$$v_{\rm P}=-kv_{\rm CM} \tag{10}$$

$$v_{\rm Q}=(1-k)\,v_{\rm CM}. \tag{11}$$

By substituting (6), (10), and (11) into (9), the sum of i_1 and i_2 is 0, so the current i_1 and i_2 cancel each other. Therefore, the generated CM noise current is confined within the inverter, other than flowing into the source side or the load side.

The passive cancellation method [29] had been proposed to cancel the CM EMI in power converters: A branch consisted of a compensation voltage source and a capacitor is in parallel with the power converter, and an out-of-phase current is generated to cancel the CM noise current from the power converter. For the proposed method in the inverter applications, instead of injecting the compensation current using external branch, the electric potential of the inverter is modified in a way to make the net current flowing through the CM parasitic capacitances in the inverter being 0.

V. Considerations in Practical Application

In this section, the considerations for implementing the passive cancellation method are discussed, which covers the restriction of current, balancing capacitor, the influence of parasitics, and the comparison with the existing methods.

A. Restriction of Input and Output Current

As the injecting windings are inserted into the dc and ac sides, the proposed method is preferred in low current applications so that the corresponding winding dimensions are not significantly large.

B. Balancing Capacitor

In (6), the coefficient k is determined by capacitance ratio, and the capacitance takes arbitrary value within a reasonable range. So the turns $kN_{\rm ab}$ and $(1-k)N_{\rm ab}$ of two CMTs might not be an integer in a general case. To handle this issue, a balancing capacitor could be added and connected in parallel with one of the parasitic capacitance, in order to adjust the capacitance ratio and make $kN_{\rm ab}$ and $(1-k)N_{\rm ab}$ being an integer.

In some cases, balancing capacitor is not required. For the switches using discrete MOSFETs, the dominant CM parasitic capacitance is between the drain of each MOSFET and the heatsink. As long as the same insulation material with equal thickness is inserted between each MOSFET and the heatsink, these parasitic capacitances are equal. According to (1), (2), and (6), the coefficient k is 0.5 regardless of the capacitance, and the turns $kN_{\rm ab}$ and $(1-k)N_{\rm ab}$ could be integer as a result.

C. Influence of Parasitics in CMT

The CMT is a critical component for sensing and injecting CM voltage, and its parasitics have profound effect on CM current reduction at high frequencies. As shown in Fig. 10(a) and (b), the magnetizing inductance $L_{\rm m1}(L_{\rm m2})$ and the parasitic capacitance $C_{\rm pri1}$ ($C_{\rm pri2}$) across the primary winding, as well as the leakage inductance $L_{\sigma{\rm p}1}, L_{\sigma{\rm s}1}(L_{\sigma{\rm p}2}, L_{\sigma{\rm s}2})$ of the windings in $T_{\rm C1}(T_{\rm C2})$ are considered, while the leakage inductance between the injecting windings is neglected. Take a single-phase inverter as an example, Fig. 10(c) shows the equivalent circuit for the inverter using passive cancellation, by combining Figs. 7(a)

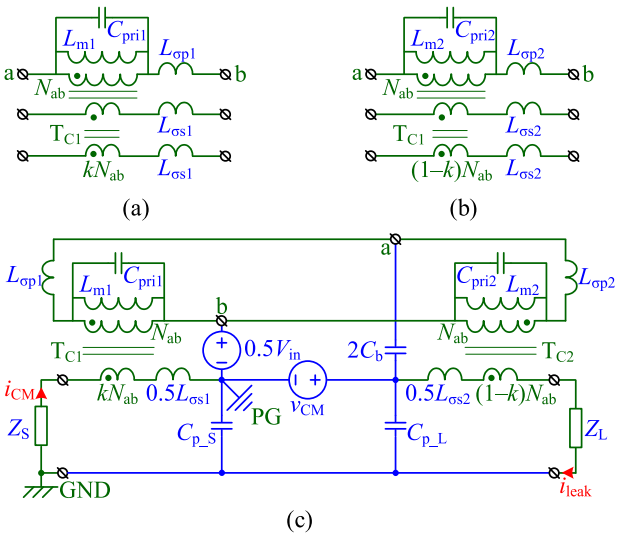

Fig. 10. Equivalent circuit. (a) CMT for T_{C1} with parasitics. (b) CMT for T_{C2} with parasitics. (c) Inverter with passive cancellation method.

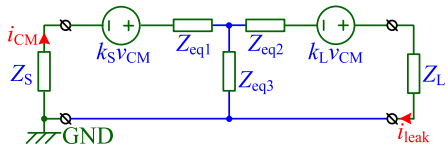

Fig. 11. Simplified CM noise circuit.

and (c), 8, and 10(a) and (b). The $0.5L_{\sigma s1}$ and $0.5L_{\sigma s2}$ is the inductance for CM current because two $L_{\sigma s1}$ ($L_{\sigma s2}$) in T_{C1} and T_{C2} are essentially in parallel for CM current.

Referring to Appendix B, the simplified circuit of Fig. 10(c) is given in Fig. 11. As seen, the CM current can be eliminated if the voltages are zero, yields

$$k_S = k_L = 0. \tag{12}$$

According to (12) and (B2), it is required that

$$s^2 L_{\sigma p1} C_{pri1} + 1 + L_{\sigma p1} (L_{m1})^{-1} = 1 \tag{13}$$

$$s^2 L_{\sigma p2} C_{pri2} + 1 + L_{\sigma p2} (L_{m2})^{-1} = 1. \tag{14}$$

Referring to (13) and (14), the leakage inductance $L_{\sigma p1}$ and $L_{\sigma p2}$ should be far smaller than the magnetizing inductance L_{m1} and L_{m2}, respectively. Moreover, the upper frequency f_H for effective passive cancellation is far lower than (roughly from 1/5 to 1/3) the resonant frequencies of $L_{\sigma p1}$ with C_{pri1} and $L_{\sigma p2}$ with C_{pri2}, as these parasitics affect the frequency dependent terms as the frequency goes higher. Therefore, the bandwidth for passive cancellation is within (f_S, f_H), and f_H is given by

$$f_H \ll \min\left\{ \left(2\pi\sqrt{L_{\sigma p1} C_{pri1}}\right)^{-1}, \left(2\pi\sqrt{L_{\sigma p2} C_{pri2}}\right)^{-1} \right\}. \tag{15}$$

As discussed above, the leakage inductance and parasitic capacitance of the sensing (primary) winding in the CMT should be as small as possible to achieve wide frequency range of noise reduction. Considering these requirements, sandwiched winding structure is preferred to realise the CMT, which could achieve tight coupling and small parasitic capacitance of the primary winding at the same time.

D. Comparison With Other Methods

The passive filter, floating filter [11], active cancellation method [24], and passive cancellation method in this article are compared regarding the used components, bandwidth, and noise attenuation, as shown in Table I. The equivalent circuits for these existing methods are shown in Fig. 12. The lower cut-off frequency f_L for these methods is required to be much lower than the switching frequency, which can be realised by choosing proper parameters. The higher cut-off frequency f_H of passive filter and floating filter is limited by the equivalent parallel capacitance (EPC) of CM inductors and the ESL of CM capacitors. For the active and passive cancellation method, f_H is given by (15), as CMT is used in both methods.

The noise attenuation and component volume of active and passive cancellation method is first compared. Based on the experimental results in [24] and this article, the ac side CM current is significantly reduced by both methods. For the dc side CM current, the active cancellation gives a reduction of 20 dB, and the passive cancellation reaches a reduction of 40 dB. Because two CMTs are used in the passive method, the volume of passive components is larger than that in the active method. However, the volumetric density of the system depends on the total volume of passive components, active devices, and the associated cooling parts, which changes with the applications.

For comparing the noise attenuation and the component volume of passive filter, floating filter, and passive cancellation method, the CM inductances of L_{CM1} and L_{CM2} in Fig. 12 are assumed to be equal to the magnetizing inductance of the CMT at the input and output side in the passive cancellation method, respectively. This assumption makes the component volume and the copper loss of the CM inductors or transformers being the same, which take up most of the volume in these methods. Because the noise attenuation of passive filter and floating filter is affected by the CM impedance of the source and the load, the noise attenuation of these methods varies with the situations.

1) If Z_S and Z_L are far lower than the impedance of L_{CM1} and L_{CM2}, the attenuation of passive filter or floating filter could be stronger than the passive cancellation because the mismatch of impedance is guaranteed in this case.
2) If Z_S or Z_L is close to or even larger than the impedance of L_{CM1} and L_{CM2}, the insertion loss of the passive filter or floating filter would be lower than the passive cancellation method, as the mismatch of impedance is not satisfied in this case.

As a conclusion, compared to the passive filter, floating filter, and active cancellation, the passive cancellation reduces the CM noise at both sides simultaneously, regardless of the CM impedance of the source or the load.

VI. Experimental Verification

In order to verify the effectiveness of the proposed passive cancellation method, a single-phase SiC inverter is built, and the

TABLE I
COMPARISON BETWEEN PASSIVE FILTER, FLOATING FILTER, ACTIVE, AND PASSIVE CANCELLATION METHODS

		Passive filter	Floating filter	Active cancellation	Passive cancellation
Components	Active	0	0	2 power transistors	0
	Passive	2 CM inductors	2 CM inductors, 4 Y caps	1 CMT	2 CMTs
Bandwidth	f_L	The lower cut-off frequency f_L is designed to be far lower than the switching frequency f_S			
	f_H	f_H is limited by the equivalent parallel capacitance (EPC) of CM inductors and the ESL of CM capacitors.		As given in (15), f_H is far lower than the resonant frequency of the leakage inductance and parasitic capacitance of the sensing winding in the CMT.	
Noise Attenuation	AC side	If Z_S and Z_L are far lower than the impedance of CM inductors in Fig. 12(a) and (b), strong attenuation of CM current can be achieved. Otherwise, the attenuation is not significant.		Yes, Strong	Yes, Strong (40 dB for the experiment in this paper)
	DC side			Yes, Medium (20 dB in [24])	

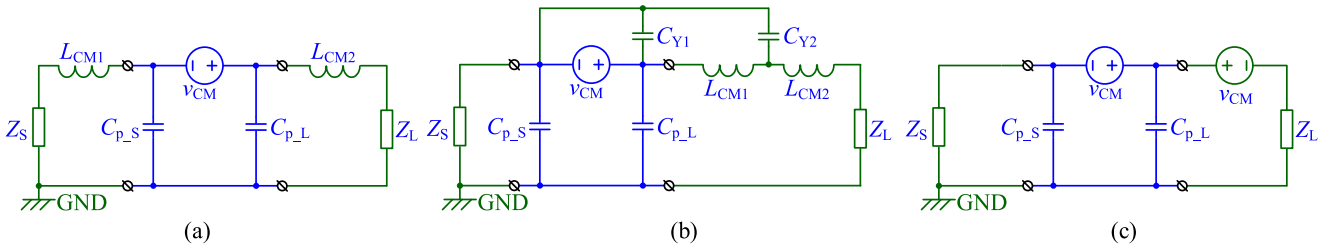

Fig. 12. Equivalent circuits for the existing methods. (a) Passive filter. (b) Floating filter. (c) Active cancellation method.

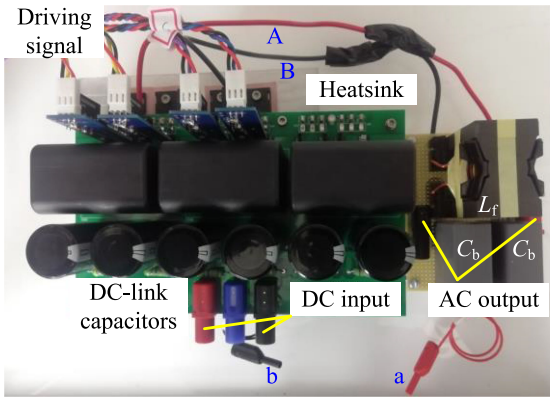

Fig. 13. Photograph of the SiC inverter prototype.

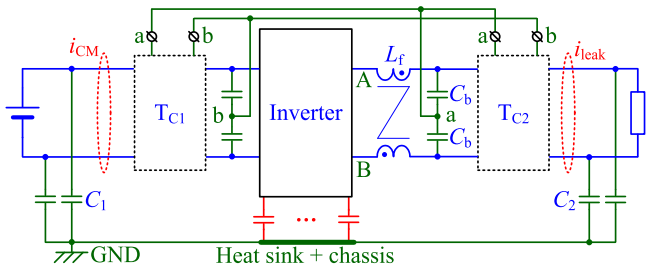

Fig. 14. Measurement setup for the CM current.

TABLE II
MAIN CIRCUIT PARAMETERS AND CM PARASITIC CAPACITANCES

DC input voltage	400 V	DC-link capacitor	220 μF
Load Resistance	50 Ω	Filter inductance L_f	520μH
Nominal Power	1 kW	Filter capacitance C_b	6.8 μF
Output line frequency	50 Hz	Parasitic cap. C_p	38 pF
Switching frequency	80 kHz	Input side cap. C_1	0.1 μF
Modulation	Diploid SPWM	Output side cap. C_2	1 nF

CM current at the dc and ac sides are measured and compared to the case without the passive cancellation method.

Fig. 13 shows the prototype, including the inverter and the output filter. The main switches Q_1–Q_4 adopt SiC MOSFETs (CREE: C2M0040120D), and the output filtering capacitance uses two C_b in series. Fig. 14 shows the measurement setup for the CM current. Two capacitors C_1 (C_2) are connected between the input power cords (loads) and the GND. In addition, the heatsink is also connected to GND. Table II lists the parameters of the inverter. The parasitic capacitance C_p between the drain of each MOSFET and the heatsink is measured by an impedance analyzer (WAYNE KERR 6500B) with MOSFETs disconnected from the inverter, and the test frequency for C_p is 100 kHz. As shown in Fig. 14, the current i_{CM} and i_{leak} are measured with high-bandwidth current probes (Agilent 1147A) under three conditions, including the original case without transformers T_{C1} and T_{C2}, inserting T_{C1} and T_{C2} and leaving their winding ab open (T_{C1} and T_{C2} act as CM inductors), inserting T_{C1} and T_{C2}, and connecting them according to Fig. 14 (T_{C1} and T_{C2} act as CMT in this case).

The photo and winding structure of T_{C1} and T_{C2} are shown in Fig. 15. Sandwiched winding structure is adopted to reduce the leakage inductance and equivalent parasitic capacitance in parallel with the injection winding. Table III lists the parameters

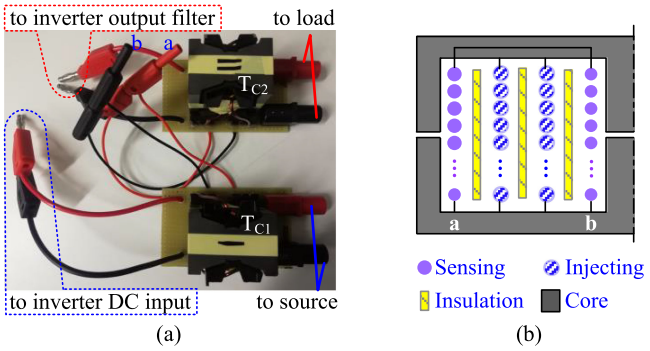

Fig. 15. CMT for T_{C1} and T_{C2}. (a) Photograph of the CMTs. (b) Winding structure.

TABLE III
PARAMETERS OF MAGNETIC COMPONENTS

	L_f	T_{C1}	T_{C2}
Core	PQ50/50	PQ40/40	
Turns	22 : 22	30 : 15 : 15	
Magnetizing inductance	130 μH, 130 μH	3.13 mH	3.32 mH
Primary leakage inductance $L_{\sigma p}$		1.30 µH	1.36 µH
Secondary leakage inductance $L_{\sigma s}$		0.48 µH	0.46 µH
Parasitic capacitance C_{pri}		27.4 pF	28.1 pF

of the magnetic component L_f, T_{C1}, and T_{C2}. As seen, the turns ratio of T_{C1} and T_{C2} are both 2:1:1 ($k = 0.5$), because the equivalent parasitic capacitance C_{p_S} and C_{p_L} are both equal to $2C_p$ as discrete MOSFETs are used. By measuring the impedance curve of each winding in the CMT (the other windings are open), the leakage inductance and the parasitic capacitance can be extracted, as given in Table III. The resonant frequency between $L_{\sigma p}$ and C_{pri} of T_{C1} and T_{C2} is 26.67 and 25.75 MHz, respectively.

A. Test of CM Voltage Sensing and Injecting Circuit

To evaluate the performance of CM voltage sensing and injecting circuit, the input impedance of the left side port in the circuit shown in Fig. 16(a) is measured by an impedance analyzer. During the measurement, the right sides of T_{C1} and T_{C2} are left open. Fig. 16(b) shows the measured impedance from 50 Hz to 30 MHz. As seen, the impedance has one resonant peak and two resonant valleys. The peak is created by the resonance between the magnetizing inductance L_m and parasitic capacitance C_{pri} of CMT, the lower valley is the resonance between the filter capacitance $2C_b$ and L_m, and the higher valley is the resonance between the leakage inductance $L_{\sigma p}$ and C_{pri} of CMT. Because of the leakage inductance of filtering inductor L_f, the resonant frequency of the higher valley is a little bit lower than that between $L_{\sigma p}$ and C_{pri} of each CMT. According to Fig. 16(b), the effective frequency range for noise cancellation is roughly from 3 kHz to 10 MHz. In order to validate the 10 MHz higher cut-off frequency, an 80 kHz square wave is injected into the left port

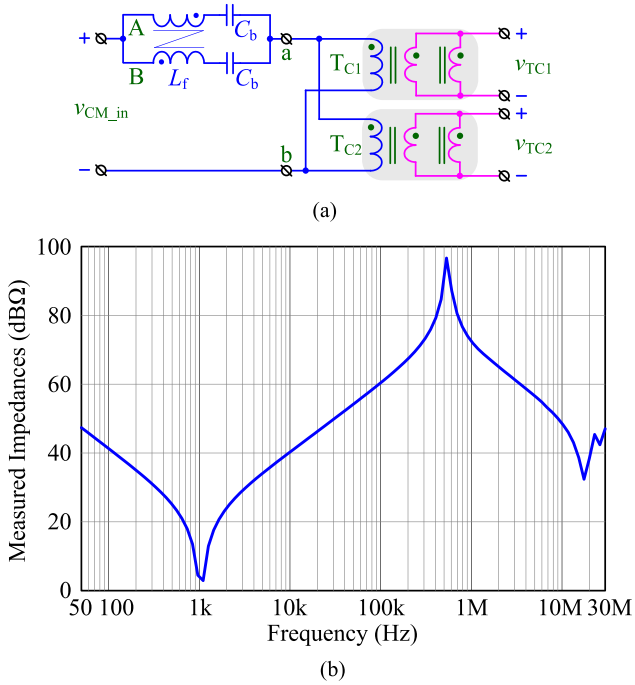

Fig. 16. CM voltage sensing and injecting circuit. (a) Connection for the test. (b) Measured input impedance of the circuit from the left port.

in Fig. 16(a) by a signal generator, and the right sides of T_{C1} and T_{C2} are both open. The signals v_{CM_in}, v_{TC1}, and v_{TC2} are recorded by an oscilloscope. The spectra of these signals are then calculated with fast Fourier transformation (FFT) in MATLAB (using rectangular window), as shown in Fig. 17. As seen, the spectrum of the response signal is 6 dB lower than that of the excitation signal for the frequencies below 10 MHz, which corresponds to the 2:1:1 turns ratio and the impedance measurement in Fig. 16.

Fig. 18 shows the measured voltages for the circuit in Fig. 14 when the inverter outputs nominal power, where v_{CM} is measured across the port ab, and the injected voltage v_{CM_TC1} and v_{CM_TC2} is measured across the injection windings of T_{C1} and T_{C2}, respectively. As seen, their waveforms are generally similar, and have amplitude ratio of 2:1:1 as expected. The major difference in their waveforms occurs when the voltage has step changes, which is caused by the parasitics of the CMT that limits the bandwidth for sensing the CM voltage.

B. Verification of CM Current Reduction

Fig. 19 compares the time-domain waveforms of i_{CM} and i_{leak} under the aforementioned three cases. Please note the scales for the CM and leakage current (i_{CM}, i_{leak}) are 10 A/div, 500mA/div, and 200 mA/div for the three cases, respectively. In Fig. 19(a), i_{CM} and i_{leak} are similar, because the impedance of C_1 and C_2 are far smaller than that of C_p at switching harmonic frequencies. Referring to Fig. 8(a), the current flowing through $2C_p$ can be neglected compared with i_{CM} and i_{leak}, so the circuit can be simplified as a serial circuit without C_p. In addition, the CM current for this original case (without CMTs, Case I) has the largest amplitude. After inserting the CM inductors (Case

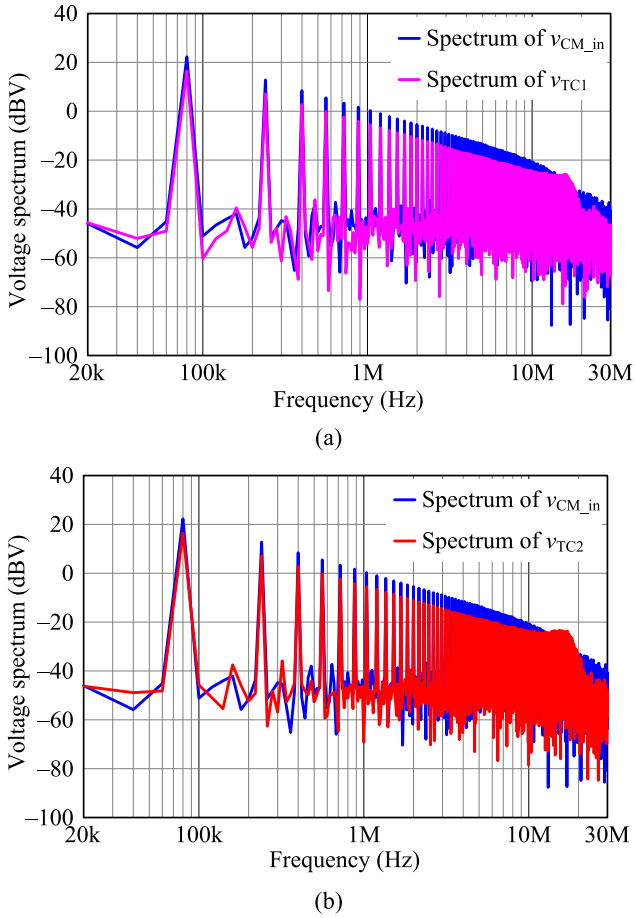

Fig. 17. Spectra of the excitation and response signals. (a) DC side. (b) AC side.

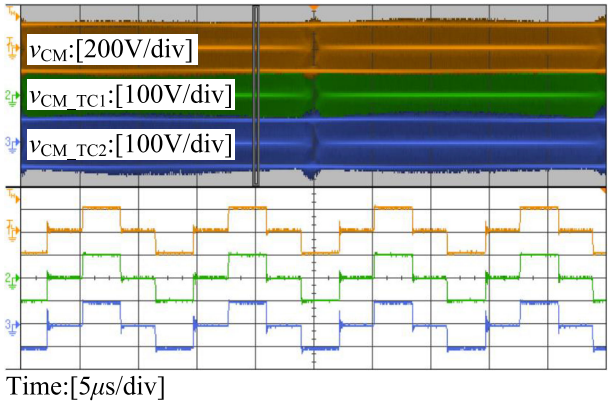

Fig. 18. CM voltage of the inverter and the injected voltages from CMTs T_{C1} and T_{C2}.

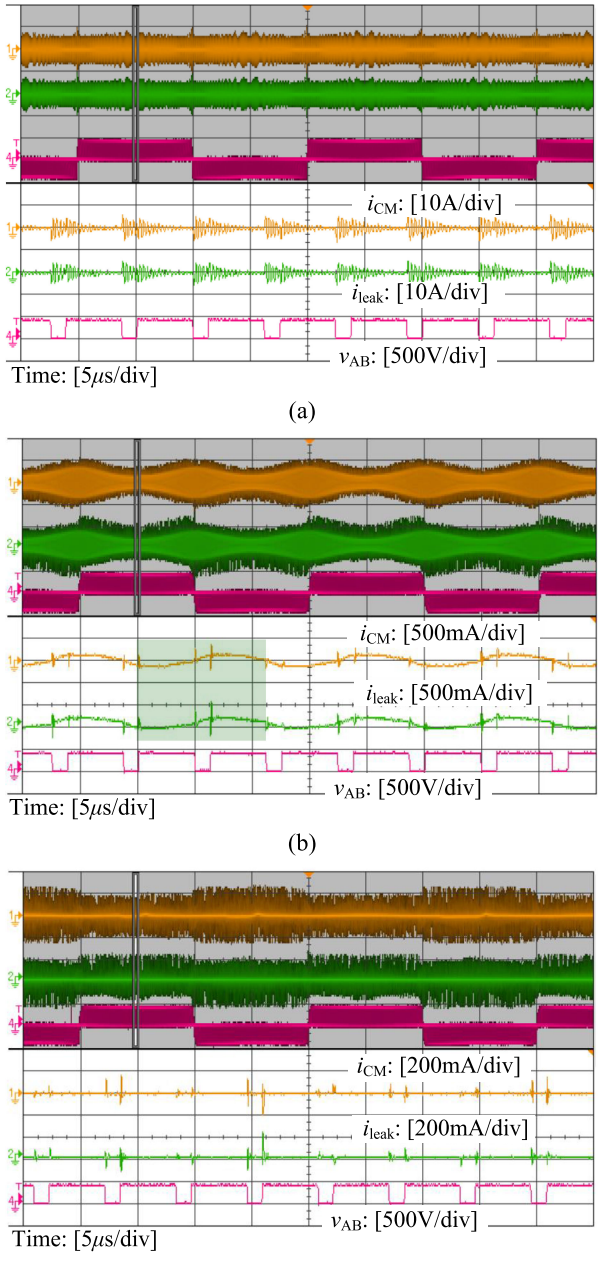

Fig. 19. Comparison of CM current at the dc and ac side. (a) Original case. (b) With CM inductors at the dc and ac side. (c) With CMTs at both sides.

II), the amplitude of i_{CM} and i_{leak} is significantly reduced in Fig. 19(b), but the switching frequency component in i_{CM} and i_{leak} can still be observed, as highlighted in Fig. 19(b). This is because the impedance of CM inductors at the switching frequency is small, and the attenuation of i_{CM} and i_{leak} by CM inductance is not significant. In Fig. 19(c), by inserting the CMTs (Case III), the amplitude of i_{CM} and i_{leak} is further reduced. Because the parasitic capacitance between Q_1–Q_4 and GND is not exactly the same, the CM noise cancellation is not perfect as expected, and there are little spikes in i_{CM} and i_{leak}. As the leakage current is higher than the 30 mA standard [31], the passive cancellation method in this article cannot guarantee that the attenuated current meets the standard. However, the amplitude of these spikes is lower than that in Fig. 19(a) and (b), which verifies the effectiveness of this method. Various methods can be combined to further reduce the high frequency CM noise, e.g., adding passive filters to reduce the high frequency components, adopting variable switching frequency modulation [32] to spread the noise spectrum, or using active gate driver [33], [34] for smoothing the switching transients. These can

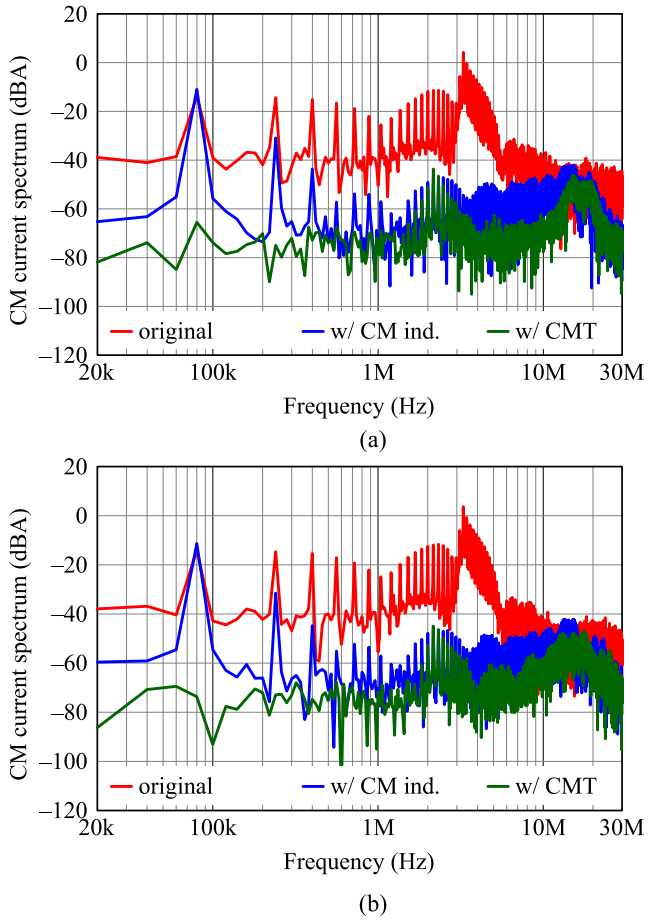

Fig. 20. Comparison of CM current spectra at the dc and ac side with 50 μs time length. (a) DC side. (b) AC side.

help tackle MHz+ frequency harmonics, where the passive cancellation may not perform well in this frequency range due to the high-frequency parasitic effects of the CMT.

Fig. 20 compares the CM current spectra of i_{CM} and i_{leak} under the three cases. The CM current data is collected by the digital oscilloscope (Agilent MSO-X 3054A), and then sent to MATLAB for calculating the CM current spectra using FFT (rectangular window is selected). The time length for FFT is supposed to be 20 ms for covering a complete line cycle, which yields a spectrum ranges only from 0 to 1.56 MHz due to limited sampling points of the oscilloscope. To observe the high frequency components, a 50 μs time length of CM current data is recorded when the output voltage is crossing zero. In this way, the harmonic amplitude of the inverter CM voltage is the same under the three cases, and the higher frequency range of FFT could be extended as well. As seen in Fig. 20, the harmonic spectra of i_{CM} and i_{leak} for the original case (Case I) are the highest. There are clear spikes at the switching frequency and its odd harmonics, because the CM voltage of a single phase inverter with diploid SPWM control is a square wave with 50% duty cycle when the output voltage is crossing zero. After inserting the CM inductors (Case II), the harmonic amplitude i_{CM} and i_{leak} see a reduction at high frequencies due to the impedance of CM inductors. However, the harmonic amplitude around the switching frequency is still high, because the impedance of the CM inductors is not sufficiently larger than that of C_2. Finally, by applying the CMT (Case III), the spectra of i_{CM} and i_{leak} are further reduced. Compared to the original results, nearly 40 dB reduction from 20 kHz to 10 MHz is achieved by adopting the passive cancellation. The higher cut-off frequency for effective cancellation is 10 MHz, which corresponds to the experimental results in Section VI-A. Thus, the proposed passive cancellation method is verified.

VII. Conclusion

In this article, a generalized CM noise model for inverter systems is presented, which can be equivalent to a Y-connected network using generalized Thevenin's theorem for a two-port network. With this equivalent network, the passive cancellation method is derived. A CM voltage sensing circuit comprising a coupled inductor and two (three) capacitors for single-phase (three-phase) inverters is required to sense the CM voltage, and two CMTs are required to inject the CM voltage into the dc input power cable and ac output cable. The turns ratio of the sensing winding and injecting winding are determined by the parasitic capacitance ratio of the inverter, and the bandwidth of this method is limited by the resonant frequency of the leakage inductance and parasitic capacitance of the sensing winding in the CMT. With this method, the CM currents of the input and output sides can be reduced, especially for fast-switching wide-bandgap converters, where high *dv/dt* will induce increased level of CM problems. Compared to the passive filter, floating filter, and the active cancellation method, the passive cancellation method reduces the CM noise at both sides simultaneously, regardless of the CM impedance of the source or the load. A single phase full-bridge inverter has been built, the CM voltage sensing and injection circuit works up to 10 MHz, and 40 dB reduction for the CM current spectra at both sides is achieved by applying the passive cancellation method.

Appendix

A. Equivalent Δ and Y Connection With Voltage Sources

This appendix proves the equivalence between the network in Fig. 21(a) and the network in Fig. 21(c) with Y connection, where Z_1 and Z_2 take arbitrary values for general discussion.

The generalized Thevenin's theorem for a two-port network is used here to effectively remove the independent sources inside the network and insert the equivalent sources outside [30]. First, with both ports open, the open-circuit voltages v_{oc1} and v_{oc2} in Fig. 21(a) are expressed by

$$\begin{cases} v_{\mathrm{oc1}} = -kV_{\mathrm{CM}} \\ v_{\mathrm{oc2}} = (1-k)\,V_{\mathrm{CM}} \end{cases} \tag{A1}$$

where the coefficient k is given by

$$k = Z_1 \cdot (Z_1 + Z_2)^{-1}. \tag{A2}$$

By making the inside voltage source zero and inserting the equivalent sources v_{oc1} and v_{oc2} outside, the equivalent circuit of Fig. 21(a) is obtained, as shown in Fig. 21(b). By simplifying

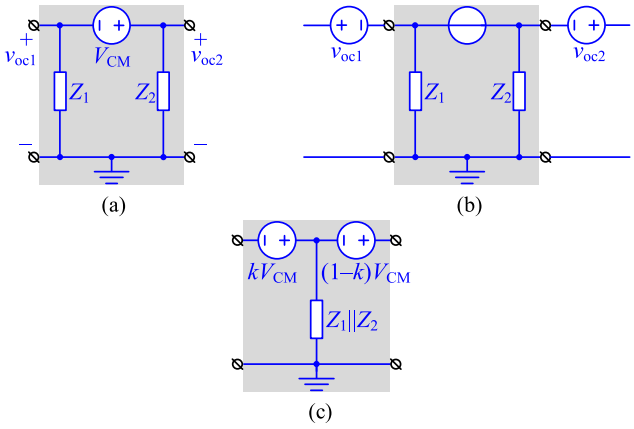

Fig. 21. Equivalent networks. (a) With Δ connection. (b) With equivalent sources moving to the outside. (c) With Y connection.

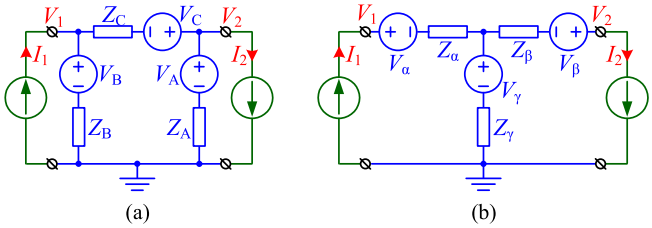

Fig. 22. Two equivalent circuits. (a) Δ connection. (b) Y connection.

this circuit, the network with Y connection is finally derived, as shown in Fig. 21(c).

As an extension, the equivalent Δ and Y connection with independent voltage sources in Fig. 22 for a general case is provided. Two current sources are used for ease of proving their equivalence. As long as the voltages V_1 and V_2 across two current sources in Fig. 22(a) are equal to the respective voltages in Fig. 22(b), the Δ and Y connection are equivalent.

First, based on superposition, by shorting all the voltage sources, the response of V_1 and V_2 excited by I_1 and I_2 should be identical for these two circuits, respectively. Therefore, the internal impedances in these two circuits must satisfy the Δ-Y transformation for impedance. Second, by opening all the current sources, the open-circuit voltage in these two circuits should be equal to each other, respectively. The relationship of these parameters can be established with this requirement.

From Δ connection to Y connection, the equations are given in (A3), where, V_γ is a free variable

$$\begin{cases} V_\alpha = V_B - Z_B(Z_A+Z_B+Z_C)^{-1}(V_B+V_C-V_A) - V_\gamma \\ V_\beta = V_A + Z_A(Z_A+Z_B+Z_C)^{-1}(V_B+V_C-V_A) - V_\gamma. \end{cases} \tag{A3}$$

From Y connection to Δ connection, the equations are given in (A4), where V_C is a free variable

$$\begin{cases} V_A = V_\beta + V_\gamma - Z_\gamma \cdot Z_\alpha^{-1} \cdot (V_\alpha - V_\beta + V_C) \\ V_B = V_\alpha + V_\gamma + Z_\gamma \cdot Z_\beta^{-1} \cdot (V_\alpha - V_\beta + V_C). \end{cases} \tag{A4}$$

B. Simplification of Fig. 10(c)

In Fig. 10(c), for the frequencies above f_S, the impedance of $2C_b$ is so small that it can be treated as short circuit. Meanwhile,

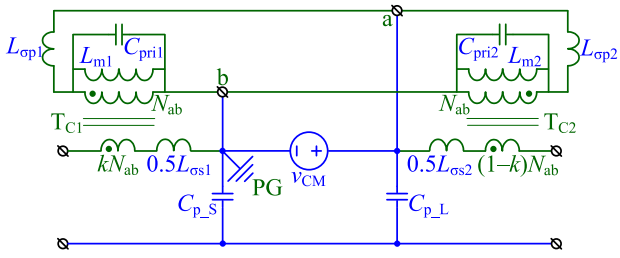

Fig. 23. Equivalent circuit of Fig. 10(c) when the frequency is above f_S.

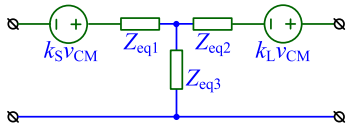

Fig. 24. Simplified network using general Thevenin's theorem.

the dc voltage source $0.5V_{in}$ can be shorted in this frequency range. Therefore, the two-port network between Z_S and Z_L in Fig. 10(c) is redrawn in Fig. 23. By following the steps of generalized Thevenin's theorem, the open-circuit voltages across each side and the internal impedance of the network with the internal voltage source being zero can be calculated and combined, yielding the simplified network shown in Fig. 24. The related impedances are given by

$$\begin{cases} Z_{eq1} = \frac{sL_{\sigma s1}}{2} + k^2\left[sL_{\sigma p1}||sL_{m1}||(sC_{pri1})^{-1}\right] \\ Z_{eq2} = \frac{sL_{\sigma s2}}{2} + (1-k)^2\left[sL_{\sigma p2}||sL_{m2}||(sC_{pri2})^{-1}\right] \\ Z_{eq3} = \left[s\left(C_{p\_S}+C_{p\_L}\right)\right]^{-1}. \end{cases} \tag{B1}$$

The coefficients regarding the voltage sources are given by

$$\begin{cases} k_S = k\left[1-\left(s^2L_{\sigma p1}C_{pri1}+1+\frac{L_{\sigma p1}}{L_{m1}}\right)^{-1}\right] \\ k_L = (1-k)\left[1-\left(s^2L_{\sigma p2}C_{pri2}+1+\frac{L_{\sigma p2}}{L_{m2}}\right)^{-1}\right]. \end{cases} \tag{B2}$$

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