Coded PWM Based Switching Ripple Communication Applied in Visible Light Communication

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***Abstract*—Visible light communication (VLC) system integrates LED lighting with wireless communication. Conventionally, power conversion and communication are designed separately. The circuitry added for communication helps to achieve a high bit rate, but increases costs and impacts the efficiency. On the other hand, power conversion and communication can also be designed together by applying switching ripple communication (SRC), where no additional devices are needed. However, SRC is usually achieved by broadband modulation methods, which means that the bandwidth is much lower than the switching frequency. By applying information theory to pulsewidth modulation, this article proposes a novel VLC scheme that applies baseband modulation to SRC in order to achieve a high bit rate with a relatively low switching frequency. In addition, power control and communication are decoupled, so that they do not influence each other. In the experiments, GaN MOSFETs are used to achieve a 1.25 Mb/s VLC system with a code error ratio of less than 10^{-6}. Moreover, the scheme shows good performance under the duty cycle from 70% to 30%, and under the output power from 100% to 7.5% of the rated value.**

***Index Terms*—Baseband, encoding, switching ripple communication (SRC), visible light communication (VLC).**

I. Introduction

WIRELESS communication has changed the way people connect to the world, and new wireless schemes are still emerging. LED lighting, widely used for high-efficiency illumination, can also be applied to wireless communication, i.e., visible light communication (VLC). Due to the ability of LEDs to operate at the frequency of megahertz [1]–[3], VLC is capable of achieving a high bit rate, and has become a promising wireless communication scheme.

Since VLC was first introduced in 2004 [4], various VLC schemes have been proposed. In VLC systems, power conversion and communication are conventionally designed separately. The circuitry for illumination should be modified by adding circuitry for communication [5]–[8], so that advanced modulation methods can be used to achieve a high bit rate. However, the volume and cost of the circuitry are increased, and communication can influence the efficiency of power conversion [6]–[8].

On the other hand, power conversion and communication can also be designed together. Communication is realized by applying dedicated methods to modulate data on the LED current perturbation, and no changes are necessary for the lighting circuitry. The current perturbation can be introduced by adding a signal reference into the control loop [8], [9], and it can also be the output current switching ripple [10]–[12]. In general, the latter can make use of a higher communication bandwidth than the former, so that methods that employ the switching ripple as a data carrier, termed as the switching ripple communication (SRC), can provide a higher bit rate.

SRC uses the input/output voltage/current switching ripples of the converter as carrier waves for communication. By modulating the digital data on the gate signals for switching devices, the information can be delivered by the ripples. Based on this idea, digital modulation methods such as amplitude-shift keying (ASK), differential phase-shift keying (DPSK), and frequency-shift keying (FSK) have already been applied to SRC systems [10]–[19]. While the ASK scheme can only be applied to interleaved topologies by shifting the phase difference between converters [10], [11], and is not applicable to single buck/boost topologies, DPSK and FSK can be applied to all topologies. Therefore, they are more useful in SRC systems.

However, due to the low bandwidth utilization, the bit rate of SRC is still limited. Under FSK modulation, the bit rate achieved is less than 10 kb/s [15]–[19], and under DSPK modulation, the converter can only achieve a bit rate of more than 100 kb/s [12]–[14]. Comparing with the bit rate of some commonly used communication protocols such as half-speed USB1.1 with 1.5 Mb/s and Bluetooth LDAC protocol with 0.99 Mb/s, a bit rate of more than 1 Mb/s is needed to be compatible with existing communication protocols, and to have a better Internet access. The bit rate increase is usually achieved by increasing the switching frequency in SRC systems. However, referring to the ratio of bit rate to switching frequency in previous literature [12]–[19], a switching frequency of about 10 MHz is required for a bit rate of more than 1 Mb/s. Although wide-bandgap devices such as GaN and SiC transistors can afford the frequency [20],

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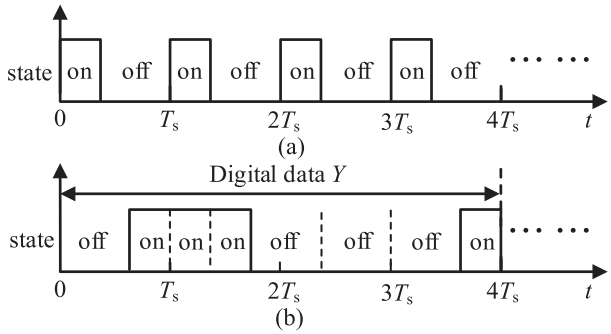

Fig. 1. Gate signal of (a) conventional PWM control and (b) proposed VLC scheme.

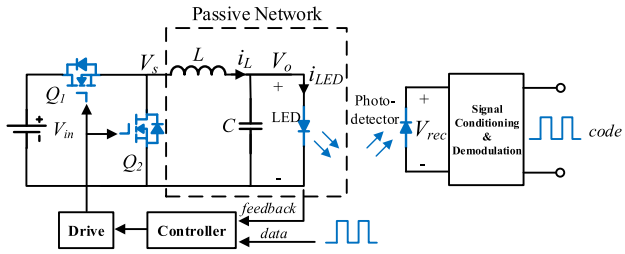

Fig. 2. Schematic of the VLC system.

[21], the low ratio brings additional switching losses and hinders further improvements on the bit rate.

In general, SRC schemes are broadband modulation schemes, which means that the communication bandwidth is much lower than the carrier frequency. In order to achieve a high bit rate and maintain a relatively low switching frequency, a novel baseband communication scheme based on information theory is proposed. This baseband scheme can achieve a bit rate of more than 1 Mb/s with a relatively low switching frequency. In addition, power control and communication can be independent.

The contributions of this article are as follows. First, a coded pulsewidth modulation (PWM) control scheme is presented. It integrates the coding method with PWM control to achieve communication and dimming functions simultaneously in the VLC system. Second, the new VLC system can achieve a high bit rate compared with conventional SRC systems, and power control and communication can be decoupled.

The rest of this article is organized as follows. In Section II, the principle of coded PWM scheme is proposed, and the signal transmission process is analyzed. Besides, the decoupling analysis of power control and communication is discussed. In Section III, the basic concepts about encoding are explained, and a novel encoding method is proposed. In Section IV, simulation and experiment results are presented to verify the feasibility of the scheme. Finally, Section V concludes this article.

II. Principles of Coded PWM Scheme

A. Basic Symbol for Communication

The gate signal of the conventional PWM control is shown in Fig. 1(a), and it controls MOSFETs to turn ON and OFF. The "ON" and "OFF" states are alternate in the gate signal, and their duration is determined by the duty cycle, so the gate signal is a regular square wave when the duty cycle keeps constant. But according to information theory, a definite signal cannot carry a message. Thus, in order to embed the information in the gate signal, it is necessary to disturb the distribution of "ON" and "OFF," and the distribution should be determined by the digital data, as shown in Fig. 1(b). As a result, the data can be modulated on the gate signal, and the baseband communication can be achieved.

According to the information theory, self-information of x_1 is defined as (1), where $P(x_1)$ is the possibility that x_1 will happen, and $I(x_1)$ is the quantity of information of x_1

$$I\left(x_1\right) = -\log_2\left(P\left(x_1\right)\right). \tag{1}$$

If x_1 is not the only circumstance of event X, and the event has multiple circumstances such as $x_1, x_2, x_3, \ldots, x_n$, then the average quantity of information that can be derived from event X is the entropy of X. Based on (1), the entropy $H(X)$ can be expressed as the expectation of self-information, which is shown in (2).

$$\begin{aligned} H\ (X) &= E\left[I\left(x_i\right)\right] \\ &= -\sum_{i=1}^{n} \log_2\left(P(x_i)\right) \cdot P(x_i). \end{aligned} \tag{2}$$

Take the state of a MOSFET as event X, then the entropy of the event is

$$H\ (X) = -\log_2\left(P\left(\text{on}\right)\right) \cdot P\left(\text{on}\right) - \log_2\left(P\left(\text{off}\right)\right) \cdot P\left(\text{off}\right) \tag{3}$$

It represents the average quantity of information of a MOSFET state, and it is obvious that according to (3), $H(X)$ has a maximum value of 1 when $P(\text{on}) = P(\text{off}) = 0.5$. So, if MOSFET states are used as basic elements for baseband communication, the bit rate increase can be achieved by increasing $H(X)$, and the maximum bit rate will occur when the possibilities of "ON" and "OFF" are equal. Moreover, if all the events are independent, every state can represent a binary number.

However, the above analysis takes MOSFET states as discrete events, and does not consider about the characteristics of the time domain. Thus, in order to apply this theory to practical circuits, the duration of the state should be defined. Suppose the duration of the "ON" state and the "OFF" state are T_{on} and T_{off}, respectively, and can have different values. For simplicity, the state "ON" with duration T_{on} is defined as symbol "1"and the state "OFF" with duration T_{off} is defined as symbol "0." Then, "1" and "0" are the basic symbols of baseband communication.

B. Analysis of Signal Transmission

The LED drive in the proposed VLC system is a buck converter, and the schematic is shown in Fig. 2. The receiver includes a photodetector whose output signal is proportional to its received light intensity. Fig. 3 shows the characteristics of the LED used in the experiment. According to Fig. 3(a), the voltage variation is proportional to the current variation within a small range of I_F, so the LED can be equivalent to a resistive load [22]

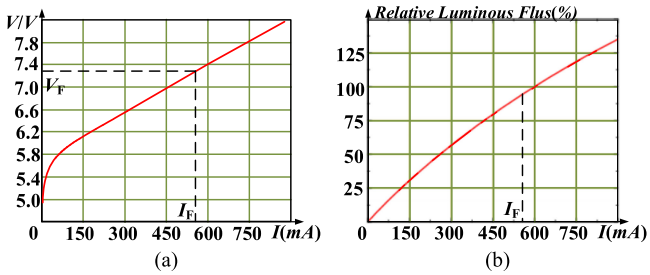

Fig. 3. (a) *V–I* curve of the LED. (b) Light intensity-*I* curve of the LED.

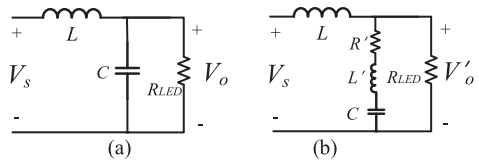

Fig. 4. (a) Equivalent passive network. (b) Improved equivalent passive network.

in the range, and the equivalent circuit of the passive network is shown in Fig. 4(a). Moreover, according to Fig. 3(b), the light intensity is proportional to the current when the current is near I_F, so the received signal $V_{\rm rec}$ is proportional to V_o.

The transfer function from V_s to V_o in Fig. 4(a) is

$$T(s) = \frac{R_{\rm LED}}{s^2 R_{\rm LED} LC + sL + R_{\rm LED}}. \tag{4}$$

The unit step response of T(s) is

$$\begin{cases} h(s) = \frac{R_{\rm LED}}{s^3 R_{\rm LED} LC + s^2 L + s R_{\rm LED}} = \frac{1}{s} + \frac{A}{s+a} + \frac{B}{s+b} \\ h(t) = g(t) + L^{-1}\left[\frac{A}{s+a} + \frac{B}{s+b}\right] \end{cases} \tag{5}$$

$$\begin{cases} A, B = \pm \frac{1}{2R_{\rm LED} C \sqrt{\frac{1}{R_{\rm LED}^2 C^2} - \frac{4}{LC}}} - \frac{1}{2} \\ a, b = \frac{\frac{1}{R_{\rm LED} C} \pm \sqrt{\frac{1}{R_{\rm LED}^2 C^2} - \frac{4}{LC}}}{2} \end{cases} \tag{6}$$

where $g(t)$ is the unit step signal, L^{-1} is the inverse Laplace transformation, and the expression of $L^{-1}[\frac{A}{s+a} + \frac{B}{s+b}]$ depends on the values of a and b.

Considering V_s is a square wave, which can be seen as a sequence of symbols, so it can be expressed as the sum of step signals shown in (7), where g_i(t) is the ith unit step signal, A_i is its amplitude and T_i is its start moment

$$V_s(t) = \sum_{i=1}^{\infty} A_i g_i(t - T_i). \tag{7}$$

Then, according to (5) and (7), V_o can be expressed as

$$V_o(t) = \sum_{i=1}^{\infty} \left\{ A_i g_i(t - T_i) + A_i L^{-1} \left[e^{-T_i s} \left(\frac{A}{s+a} + \frac{B}{s+b} \right) \right] \right\}. \tag{8}$$

Since the values of C and $R_{\rm LED}$ are usually tens to hundreds of microfarad and several ohms, respectively, if step signals occur at the frequency of megahertz, $L^{-1}[e^{-T_{n-1}s}(\frac{A}{s+a} + \frac{B}{s+b})]$ will be surely to have a great influence on the nth step signal response. Thus, in the received signal $V_{\rm rec}$, the term

$$\sum_{i=1}^{n-1} A_i L^{-1} \left[e^{-T_i s} \left(\frac{A}{s+a} + \frac{B}{s+b} \right) \right] \tag{9}$$

is the intersymbol interference (ISI) of the nth symbol, and it will heavily influence communication. As a result, the passive network in Fig. 4(a) is not suitable for baseband communication.

In order to avoid the ISI, the improved passive network is proposed in Fig. 4(b), and the transfer function from V_s to V'_o is

$$T'(s) = \frac{1}{\frac{s^2 L}{s^2 L' + sR' + 1/C} + \frac{sL}{R_{LED}} + 1}. \tag{10}$$

R' and L' are the equivalent series resistor (ESR) and the equivalent series inductor (ESL) of the capacitor C, respectively, and their values are small enough that (11) can be satisfied at a low frequency, so they will not influence power control

$$T'(s) \approx T(s). \tag{11}$$

Considering the values of the ESR and the ESL, if the frequency is within a range from hundreds of kilohertz to a megahertz, the capacitor and the ESR will be dominant compared with the ESL, and $sCR' >> 1$, so (10) can turn to

$$T'(s) \approx \frac{R_{\rm LED} R'}{sL(R_{\rm LED} + R')}. \tag{12}$$

According to (7) and (12), the expression of V'_o is

$$V'_o(t) = \sum_{i=1}^{\infty} \frac{A_i R_{\rm LED} R'}{L(R_{\rm LED} + R')} (t - T_i) g_i(t - T_i). \tag{13}$$

In (13), there is no ISI term as (9), and the waveform is either an ascending slope or a descending slope. Thus, after sampling the received signal $V_{\rm rec}$, the gradient can be calculated by subtracting two adjacent sample values, and the symbol can be derived directly from the gradient. So, the baseband communication can be achieved through the passive network shown in Fig. 4(b).

If the frequency is low and $sCR' >> 1$ cannot be satisfied, the baseband communication may fail. When the frequency is over the resonance frequency of the capacitor, and the ESL cannot be ignored, the baseband communication may still be achieved. But, it is a complicated circumstance, and will not be discussed in this article.

Considering (12), the capacitor can only be ignored at a high frequency that can satisfy $sCR' >> 1$. However, under low frequencies, the output capacitor plays an important role in power conversion, so it cannot be removed from the circuit.

C. Decoupling of Power Control and Communication

From the point of view of power control, the distribution of "1"s and "0"s should not be entirely random depending on the possibility, because there may be consecutive "1"s or "0"s

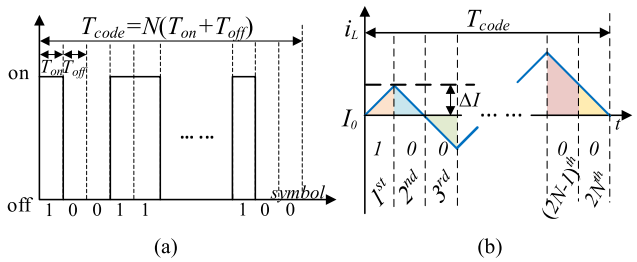

Fig. 5. (a) Symbols in $T_{\rm code}$. (b) Inductor current in $T_{\rm code}$.

that will have a significant impact on the amplitude of output current. Thus, $T_{\rm code}$ is introduced to decouple power control and communication, and within $T_{\rm code}$, the distribution of "1"s and "0"s can be random. In order to ensure that the possibilities of "1" and "0" are equal, the numbers of "1" and "0" in $T_{\rm code}$ should be the same, and suppose there are N "1"s and N "0"s in $T_{\rm code}$, as shown in Fig. 5(a).

In conventional PWM control, the switching period is constant and the duty cycle is employed to control the output power. Similarly, in the proposed scheme, $T_{\rm code}$ is predetermined before the circuit design, and the definition of duty cycle is shown in (14), where $(T_{\rm on}+T_{\rm off})$ is determined, because the values of $T_{\rm code}$ and N are determined. This definition is the same as that in PWM control, so power control can be achieved using existing control methods

$$D = \frac{NT_{\rm on}}{T_{\rm code}} = \frac{T_{\rm on}}{T_{\rm on}+T_{\rm off}}. \tag{14}$$

As a result, when the converter is under a steady state, the inductor current at the beginning of $T_{\rm code}$ should be equal to that at the end of $T_{\rm code}$, as shown in Fig. 5(b). This means that the current changes brought by a "1" and a "0" are equal, and assume the value is ΔI.

Then, the expression of the average current in $T_{\rm code}$ is

$$I_{\rm avg} = \frac{1}{T_{\rm code}} \int_0^{T_{\rm code}} i_L(t)\, dt. \tag{15}$$

It can be calculated using areas surrounded by current $i_L(t)$ and I_0, as shown in Fig. 5(b), where I_0 is the initial value of the current, and the colored region is the area of each symbol. Suppose the areas above I_0 are positive, and areas below I_0 are negative, then the area of the ith symbol is

$$S_i = \begin{cases} \Delta I T_{\rm on}\left(\frac{1}{2}+\sum_{j=1}^{i-1} x_j\right), & \text{if the } i\text{th symbol is "1"} \\ \Delta I T_{\rm off}\left(-\frac{1}{2}+\sum_{j=1}^{i-1} x_j\right), & \text{if the } i\text{th symbol is "0"} \end{cases} \tag{16}$$

where

$$\begin{cases} x_i,\ x_j = 1, & \text{if the } i\text{th, } j\text{th symbol is "1"} \\ x_i,\ x_j = -1, & \text{if the } i\text{th, } j\text{th symbol is "0"} \end{cases}$$

Thus, (15) can be written as

$$I_{\rm avg} = I_0 + \frac{1}{T_{\rm code}} \sum_{i=1}^{2N} S_i. \tag{17}$$

Based on the equal possibilities of "1" and "0," no matter what the symbol distribution is, the possibility is the same for a negative value of the total area, where "1"s and "0"s are inverted. Thus, the expectation of the total area is equal to zero, and the expectation of the average current is

$$E\ [I_{\rm avg}] = I_0 + E\left[\frac{1}{T_{\rm code}} \sum_{i=1}^{2N} S_i\right] = I_0. \tag{18}$$

Equations (17) and (18) show that although the average current within each $T_{\rm code}$ varies, the variation can be seen as harmonics at the frequency of $1/T_{\rm code}$, and can be filtered by a low-pass filter during the sampling process. After being filtered, the average current is constant despite the distribution of $2N$ symbols in each $T_{\rm code}$. As communication is achieved by controlling the distribution, it can be concluded that communication will not influence power control, which means the decoupling of power control and communication is realized.

III. Encoding Method Design

A. Basic Concepts About Encoding

The symbol sequence representing digital data is defined as the code, and the number of symbols in a code is defined as the code length N_c. If there are totally M distribution patterns, which means M codes, then the codes can represent digital data from 0 to M-1, and this is an M-ary encoding method. According to (2), if the possibilities of all the codes are equal, the entropy of a code shall be $\log_2 M$. For the bit rate is the quantity of information that transfers in a unit time, its expression is

$$\text{bit rate} = \frac{\log_2 M}{T_{\rm code}}. \tag{19}$$

In order to evaluate the performance of the encoding method, some important parameters should be introduced. Since the bit rate can be easily increased by increasing the switching frequency in broadband modulation methods such as PSK and FSK, the ratio of bit rate to average switching frequency is introduced in (20), where $f_{\rm avs}$ is the average switching frequency, N_s is the number of switching operations within $T_{\rm code}$, which is the sum of the changes from "1" to "0" and from "0" to "1," and N_c is the code length

$$\begin{cases} R_{b\_\rm avs} = \frac{\text{bit rate}}{f_{\rm avs}} \\ f_{\rm avs} = \frac{N_s}{2T_{\rm code}} = \frac{N_s}{2T_r N_c} \end{cases}. \tag{20}$$

Besides, the bit rate can also be increased by applying M-ary broadband modulation, which requires higher modulation resolution. For example, in 8PSK, the phase can only be changed by an integer multiple of $\pi/4$, so the modulation resolution is 1/8 of the switching period, and in 256PSK, it is 1/256 of the switching period. Modulation resolution represents the shortest $T_{\rm on}$ and $T_{\rm off}$ that can be used by the converter, and a higher resolution can bring a higher bit rate. Thus, R_{b_r} is introduced to reflect this feature, and defined as the product of bit rate and modulation resolution T_r, as shown in the following equation:

$$\begin{cases} R_{b\_r} = \text{bit rate} \times T_r \\ T_r = \frac{T_{\rm on}+T_{\rm off}}{2} \end{cases}. \tag{21}$$

TABLE I
CODE LIST WHEN N_s IS 4 AND N_c IS 8

code	code	code	code	code
11101000	11100100	11100010	11011000	11001100
11010001	11001001	11000101	10110001	01100110
10100011	10010011	10001011	01100011	00110011
01000111	00100111	00010111	11000110	10011001
10001110	01001110	00101110	10001101	
00011101	10011100	01011100	00011011	
00111010	00111001	10111000	00110110	
01110100	01110010	01110001	01101100	

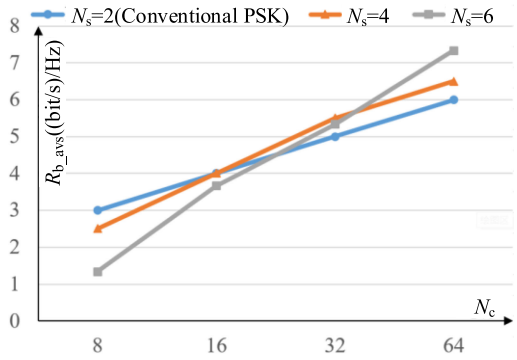

Fig. 6. Relationship of R_{b_avs} with N_c and the N_S.

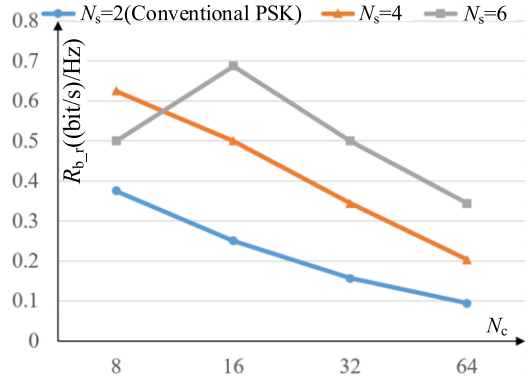

Fig. 7. Relationship of R_{b_r} with N_c and the N_S.

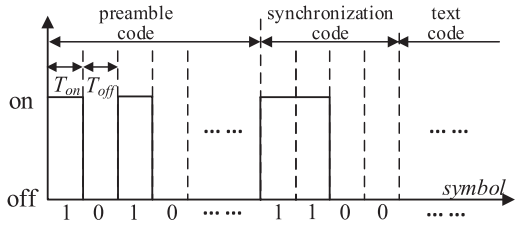

Fig. 8. Proposed synchronization strategy.

B. Encoding Method Design

According to (19), when the value of T_{code} is fixed in the proposed VLC scheme, the only way to increase the bit rate is to increase the code entropy, which can be achieved by increasing the number of codes.

Suppose there are four "1"s and four "0"s in T_{code}, which means N_c is 8. If there are two switching operations in T_{code} ($N_s = 2$), then only eight codes can be found, and this is similar to PSK, so N_s should be increased. Set $N_s = 4$, and all the codes are listed in Table I.

There are 36 codes that can be used to encode to represent numbers from 0 to 35, and the code entropy is $\log_2 36 \approx 5.17$ b. If a 32-ary encoding method is required, then 32 codes should be chosen from the 36 codes to represent numbers from 0 to 31, and the code entropy is $\log_2 32 = 5$ b.

In order to evaluate the performance of this scheme, the bit rate is compared with the theoretical maximum bit rate of PSK, which uses only one cycle to represent a phase. Suppose the duration of "1" and "0" is 500 ns, then the relationship between R_{b_avs}, N_c, and N_s is shown in Fig. 6, and the relationship between R_{b_r}, N_c, and N_s is shown in Fig. 7.

According to Fig. 6, larger N_c brings larger R_{b_avs}, which means if the average switching frequency f_{avs} remains constant, larger N_c will bring a higher bit rate. It seems to be a good performance because the increase in the bit rate does not result in additional switching losses. However, large N_c causes other problems, such as a large amplitude of the output ripple. Under the condition of $N_s < N_c/2$, increasing N_s can increase R_{b_avs}, and also reduce the maximum amplitude of the ripples, which benefits the converter's performance. But large N_s means high f_{avs}, which leads to more switching losses. So, the value should be carefully considered by balancing the ripple amplitude and the switching losses.

According to Fig. 7, when the modulation resolution remains constant and $N_s < N_c/2$, larger N_s will bring larger R_{b_r}, and larger N_c will bring smaller R_{b_r}. It shows that small N_c and large N_s can bring high bit rates under constant modulation resolution, but R_{b_avs} decreases under this condition. Therefore, R_{b_r} and R_{b_avs} should be balanced.

Generally, from the perspective of R_{b_r} and R_{b_avs}, the proposed encoding method performs much better than the best theoretical performance of PSK under proper N_c and N_s.

C. Symbol Synchronization

At the receiver, the signal is demodulated by referring to the predetermined values of T_{on} and T_{off}. But according to (14), the predetermined values are different under different duty cycles, even if the codes are the same. Besides, if the duration of the sent symbols deviates from the predetermined values while communicating, the code will be misread and the communication will be affected. Thus, at the beginning of the data frame, the receiver should be synchronized with the sender by updating the values of T_{on} and T_{off}, and the values should remain constant throughout the frame.

The strategy for synchronization is designed as shown in Fig. 8. At the beginning of communication, the converter sends a preamble code, which is the sequence "1010 ...." During the same time, the values of T_{on} and T_{off} are measured and

TABLE II
SYSTEM PARAMETERS

System parameters	
L	$12.8\mu H$
C	$100\mu F$(Electrolytic capacitor)
R_{LED}	3.1Ω
Q_1,Q_2	EPC2045
V_{in}	15V
V_{out}	7.3V
Output Power	4W
T_{code}	$4\mu s$
f_{avs}	500kHz
T_r	500ns
Photodetector	BPW34BS
Analog to Digital Converter (ADC)	10MHz
Sampling Frequency Controller (FPGA)	EP4CE10F17C8N

TABLE III
EXPERIMENTAL CODE LIST

Code	Data	Code	Data	Code	Data
11101000	31	00100111	20	10111000	9
11010001	30	01001110	19	01110001	8
10100011	29	10011100	18	11011000	7
01000111	28	00111001	17	10110001	6
10001110	27	01110010	16	01100011	5
00011101	26	11100010	15	11000110	4
00111010	25	11000101	14	10001101	3
01110100	24	10001011	13	00011011	2
11100100	23	00010111	12	00110110	1
11001001	22	00101110	11	01101100	0
10010011	21	01011100	10		

recorded by the receiver, and they are applied as criteria in the following communication process. After that, the converter sends a synchronization code, which is the sequence "1100," to mark the end of the preamble code. Text codes will be sent immediately after the synchronization code, and the receiver will divide the received symbols into codes according to the predetermined N_c.

IV. SIMULATION AND EXPERIMENT

A. VLC Scheme Simulation

The design guideline is provided as follows. The modulation resolution T_r, which is determined by the controller, should be set first. Next, the average switching frequency $f_{\text{avs}} = \frac{N_s}{2T_r N_c}$, which relates to the converter efficiency, should be decided. Then, proper N_c should be selected, and N_s is determined consequently. Large N_c is better because the bit rate can be promoted by increasing N_c. However, when $N_c > 64$, the large N_c makes it hard to distinguish a single symbol, and there will be an extremely large code list, so the value of N_c should be smaller than 64 in practical design. On the other side, as there will be $(N_c - N_s + 2)$ consecutive "1"s when communicating, large N_c will bring large inductor current ripple and output ripple, which leads to a larger inductance and increases the volume. Thus, the inductance L and N_c should be traded OFF. Finally, according to Figs. 6 and 7, R_{b_r} and R_{b_avs} should be balanced by the fine adjustment of N_c and N_s. The output capacitance should satisfy the equation $sCR' >> 1$.

To verify the feasibility of the proposed VLC scheme, a simulation analysis is carried out on the basis of the schematic in Fig. 2. The buck converter powers the LED, and the output current is sampled for closed-loop control. The controller generates the gate signal for the MOSFET drive according to the control loop and the sending data, so it works as an encoder and dc controller. Simulation parameters of the passive network are listed in Table II, and the codes are listed in Table III. For the method requires a high resonant frequency of the output capacitor, tantalum electrolytic capacitors are used in the experiment. According to the datasheet, the resonant frequency of the capacitor is more than 1 MHz, so the ESL is ignored, and the measured ESR value is 170 mΩ.

Simulation results are shown in Fig. 9. In Fig. 9(a), CH1 is the waveform of V_s, which stands for the code, and CH2 is the waveform of the LED current. It is clear that the LED current changes immediately when a switching operation occurs, and the relationship between CH1 and CH2 is in accordance with (13). Besides, Fig. 9(b) shows that the dc component of the LED current is well controlled and is not affected by communication, which means that power control and communication are decoupled. The proposed VLC scheme, therefore, realizes both power transmission and baseband communication at the same time.

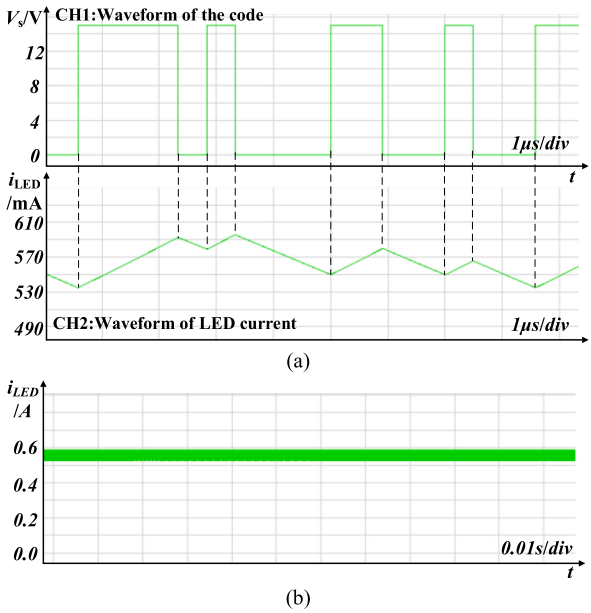

Fig. 9. (a) Simulation waveforms in small time scale. (b) Simulation waveform in large time scale.

B. Experiment Results

An experimental system prototype is established to verify the performance of the proposed scheme, which is shown in Fig. 10, and GaN MOSFETs are used to improve the high-frequency performance. The system parameters for experiments and the code list are given in Tables II and III, respectively.

Fig. 11 shows the LED current i_{LED} (CH1) and the output voltage V_o (CH2) of the converter. The current is 550 mA and the voltage is 7.3 V. The peak-to-peak amplitude of the current ripple is 56 mA, and peak-to-peak amplitude of the voltage ripple is 175 mV.

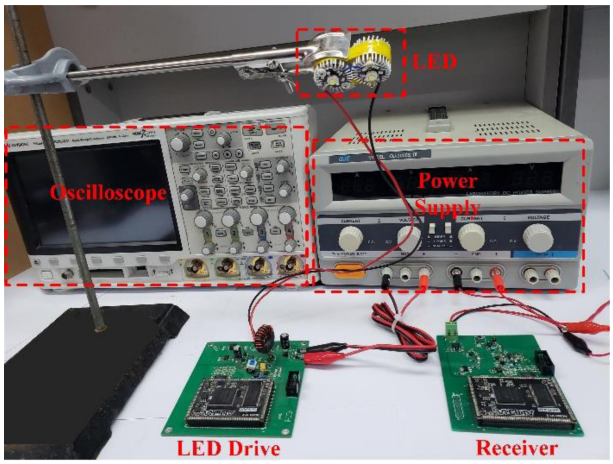

Fig. 10. Experimental system prototype.

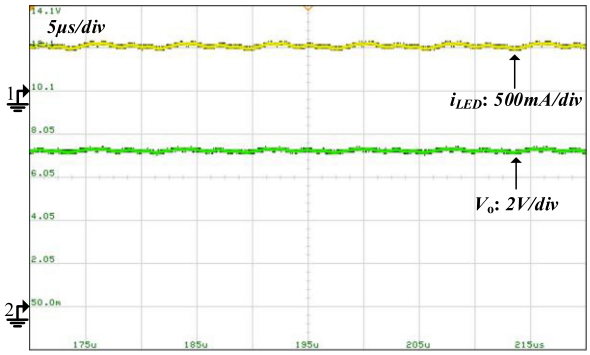

Fig. 11. Output current and output voltage of the buck converter.

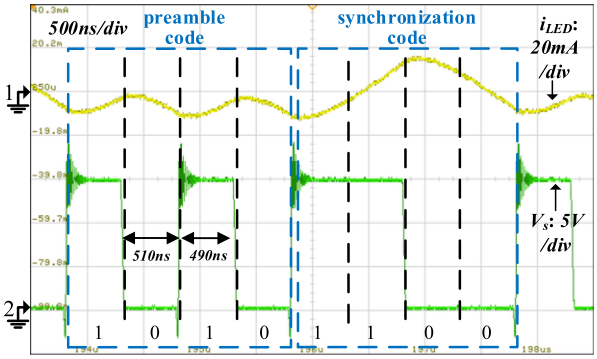

Fig. 12. Output current and sending symbols during synchronization.

In Fig. 12, CH1 is the LED current i_{LED} and CH2 is the waveform of V_s. The preamble code "1010" is sent at the beginning of communication. The measured durations of "1" and "0" are 490 and 510 ns, respectively. The synchronization code used in the experiment is "1100," and the symbol after "1100" is the first text code symbol. For the code length being predetermined, the receiver starts decoding when eight symbols are received after synchronization.

Fig. 13 shows the LED current i_{LED} (CH1), V_s (CH2), and the demodulation output of the FPGA V_{FPGA} (CH3) when

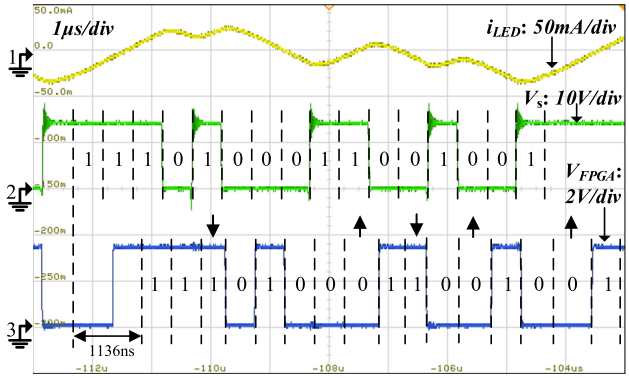

Fig. 13. Output current, V_s voltage, and the digital output of FPGA when communicating.

communicating. CH2 is the code sent by the converter, and CH3 is the code received by the receiver. Code demodulation is achieved by calculating the gradient of the received signal. Since N_c is 8, there are two codes in the figure, which are "11101000" and "11001001," and digital data 31 and 22 can be derived by looking up Table III.

The up and down arrows in CH3 mean that the duration of the symbol is larger or smaller than the criteria measured in the preamble code. Discrepancies are introduced by the nonideal characteristics of the signal channel and by the demodulation resolution, but their values are too small to bring an error code.

The demodulation resolution is determined by the sampling frequency, which can be conveniently controlled by the FPGA. Moreover, the demodulation adjustment can be achieved by updating the software. Besides, the time delay of the communication is only 1136 ns, so the communication can be considered as strictly real time. Thus, the FPGA demodulation scheme is convenient and has a good performance.

The duration thresholds are set to 50% of the duration criteria, which means that if the measured duration of the "ON" state is less than 50% of the criterion, it will be ignored. If the duration is within 50%–150% of the criterion, it will be considered as a symbol "1," and if the duration is within 150%–250% of the criterion, it will be considered as two symbol "1"s. Thus, the demodulation error is more likely to exceed the threshold if the criteria values are small. The results of the above experiment are carried out under the condition of $D = 0.49$, which is close to the optimum value of 0.5. In order to demonstrate overall performance, experiments under the duty cycle of 30% and 70% are carried out. The change in duty cycle is achieved by changing the input voltage while maintaining the same output power. The preamble code and the synchronization code are sent before text codes in every data frame to the receiver to confirm the duty cycle. The results are shown in Figs. 14 and 15.

In the experiment, all codes are demodulated correctly, and there is no symbol whose duration is close to the threshold value. Obviously, the amplitude of the current ripple changes according to the duty cycle, which will influence the sampled value for demodulation, but it can be compensated by using software, and as not to influence communication. Besides, the electrical parameters designed for the duty cycle of 49% can tolerate a

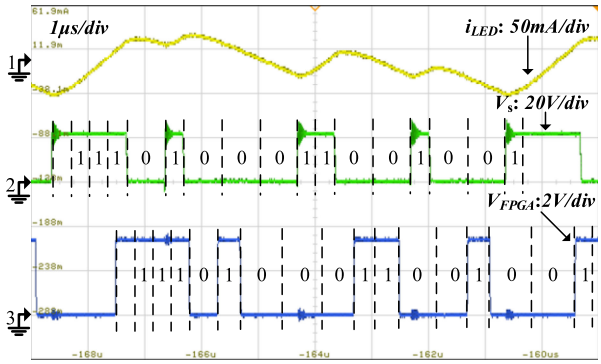

Fig. 14. Output current, V_s voltage, and the digital output of FPGA under the duty cycle equals to 30% when communicating.

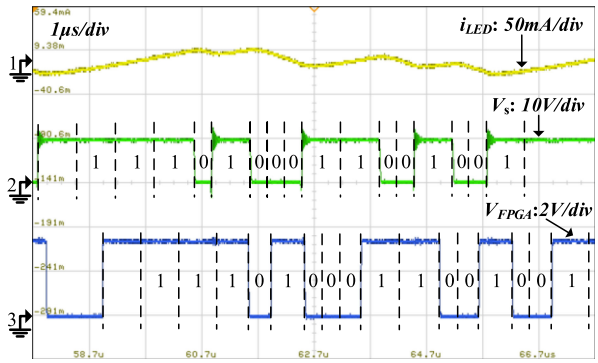

Fig. 15. Output current, V_s voltage, and the digital output of FPGA under the duty cycle equals to 70% when communicating.

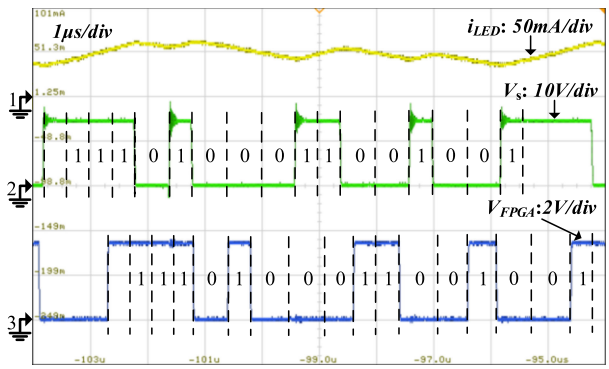

Fig. 16. Output current, V_s voltage, and the digital output of FPGA under the under the converter's output power of 0.2 W.

large variation of duty cycle, which shows the robustness of the VLC system.

The output power is the same for the above experiments while dimming is a basic function for the LED drive. Thus, the dimming experiment is performed and the results are shown in Fig. 16. The output power of the converter is only 0.3 W, which is 7.5% of the rated power of 4 W, and the communication function still operates normally. It can be concluded that the new scheme can be applied to the LED drive that achieves both dimming and communication. The efficiency of the converter is shown

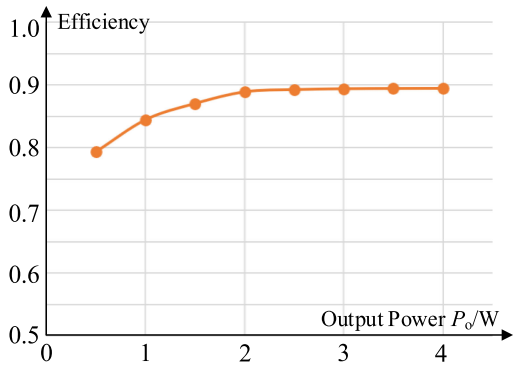

Fig. 17. Efficiency-output power curve of the converter.

in Fig. 17, which shows a good performance on the efficiency for a 4-W buck converter. The power loss mainly consists of the switching loss, the MOSFETs conducting loss, and the ESR loss of the inductor.

The code error ratio (CER) is tested in the indoor illumination environment, which has a stronger noise and is more similar to the practical application compared with the dark room. The distance between the sender and receiver is 30 cm. After the amplifiers and filters, the measured amplitude of a symbol and the background noise is 500 and 80 $mV_{p\text{-}p}$, respectively. The converter sends 10^7 codes and only three error codes are received, so the tested CER is less than 10^{-6}.

The experiment achieves a bit rate of 1.25 Mb/s with an average switching frequency of 500 kHz and a modulation resolution of 500 ns. If 8PSK has the same resolution, the theoretical maximum of bit rate is 750 kb/s. In commercial PSK communication schemes, usually more than ten cycles are used to represent one phase, and even in laboratory PSK schemes, several cycles are needed, so the bit rate will be much lower than 750 kb/s. Thus, the proposed scheme is much faster than the conventional PSK scheme.

V. Conclusion

This article proposes a novel coded PWM based VLC scheme that combines LED lighting with baseband communication. The scheme is designed by applying information theory to PWM control. Not only does it realize the decoupling of power control and communication but also achieves a bit rate higher than the conventional PSK modulation. Moreover, the scheme presents a novel view that information theory can be applied to a power converter, which helps to push power electronics and communication engineering closer. The experiments are carried out on a buck converter, and a bit rate of 1.25 Mb/s with a 500 kHz average switching frequency and a 500 ns modulation resolution is achieved, which is much faster than the existing SRC systems under the same condition.

However, some electrical features are sacrificed in this scheme. The output ripple is magnified and gets irregular, so the electromagnetic interference of the output power increases compared with conventional LED drives. Besides, the duty cycle can influence the communication performance. Extreme duty cycles are more likely to cause error codes to the receiver. In

addition, compared with the VLC systems that power conversion and communication are designed separately, the proposed method is more likely to be influenced by noises and has a shorter communication distance, because of the smaller signal amplitude.

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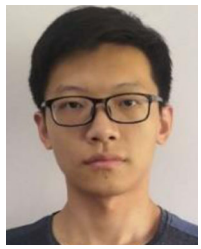

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