# CSI7: Novel Three-Phase Current-Source Inverter With Improved Reliability

Fazal Akbar, *Student Member, IEEE*, Honnyong Cha, *Senior Member, IEEE*, and Duc-Tuan Do, *Member, IEEE*

***Abstract*—Unlike voltage-source inverters (VSI), the power decoupling element in current-source inverters (CSI) is inductor. Inductor has a long lifetime and makes the CSI more reliable. However, the traditional CSIs suffer from open-circuit problem and dangerous voltage spikes are generated if the input inductor current is intermitted. Therefore, to avoid the voltage spikes, overlap-time should be inserted in the gate signals. But these intervals distort the output currents and reduce the current source utilization. To address these issues, a novel three-phase CSI is proposed in this article. The proposed inverter is originated from the conventional seven-switch CSI named CSI7 by adding only two small film capacitors. The film capacitors along with the pre-existing diodes of the CSI7 ensure that there is always a path for the inductor current, and thus the open-circuit issue is resolved. The elimination of open-circuit issue enhances the reliability and allows to minimize the overlap-time. This will improve the quality of output currents as well. Moreover, simulation and experimental results are provided at the output power of 950 W to verify the effectiveness of the proposed inverter.**

***Index Terms*—CSI, overlap-time, reliability.**

## I. Introduction

POWER inverters are mainly classified into voltage-source inverters (VSIs) and current-source inverters (CSIs) [1]. VSIs perform buck function and are used in many industrial applications. However, to achieve boost function, VSIs need an additional step-up converter or transformer. Besides, VSIs require large electrolytic capacitors for power decoupling. The electrolytic capacitors have a short lifetime [2] and thus reduce the VSIs reliability. The current shoot-through problem is another worry for the reliability of VSIs [3]. It occurs when switches in the same leg of VSI are turned-ON simultaneously and is depicted in Fig. 1(a). However, vast research has been carried out to resolve this issue. Many different topologies based on dual-buck structure [4], like buck-boost inverter [5], dual-buck split-source inverter [6], multilevel inverter [7], and three-phase inverter [8] are proposed to eliminate the current shoot-through problem of VSIs. All these inverters eliminate the current shoot-through problem because inductors appear in the current path even if the switches of the same leg are turned-ON.

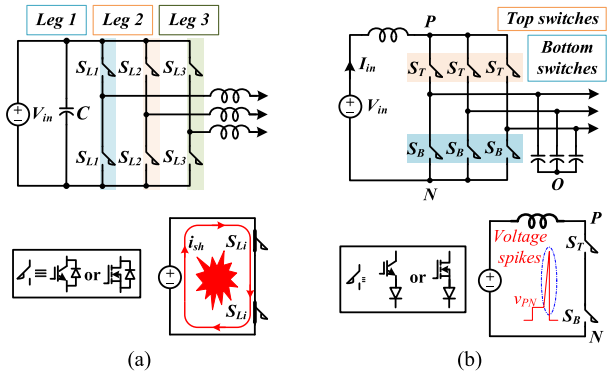


Fig. 1. Reliability issues. (a) Current shoot-through problem in VSIs. (b) Open-circuit problem in CSIs.

Alternatively, CSIs achieve step-up function in a single stage, draw smooth current from the input source, eliminate electrolytic capacitors, utilize inductors to limit the current ripple on the dc side, and have inherent short-circuit protection capability. Inductors have a much longer lifetime than electrolytic capacitors and therefore CSIs are more reliable [9]. Meanwhile, CSIs have achieved significant attention in various fields, such as photovoltaic grid-tied inverters [10], wind energy conversion systems [11], power electric drives [12], [13], and utility interfacing for superconducting magnetic energy storage systems [14].

In addition to all these advantages, the conventional six-switch CSI [15] represented by CSI6 also has some limitations such as limited operation range, lower efficiency, bulky input inductor, and open-circuit problem [16]. Similar to the current shoot-through issue in VSI, the open-circuit issue as depicted in Fig. 1(b) has a major impact on CSI reliability [17]. It takes place when the inductor current is suddenly interrupted due to turning off either top and/or bottom switches in CSI simultaneously. Several efforts have been made in the literature to resolve the limitations and improve the performance of CSIs. One of the impressive attempts is to add one more switch and hence resulting in seven-switch CSI represented by CSI7. To improve the operation range, Gao *et al.* proposed buck-boost CSI7 which is shown in [18, Fig. 2]. Similarly, to improve the dynamic

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Fazal Akbar and Honnyong Cha are with the Kyungpook National University, Daegu 41566, South Korea (e-mail: fazalakbar923@gmail.com; chahonny@knu.ac.kr).

Duc-Tuan Do is with the Thai Nguyen University of Technology, Thai Nguyen 24131, Vietnam (e-mail: doductuan-tdh@tnut.edu.vn).

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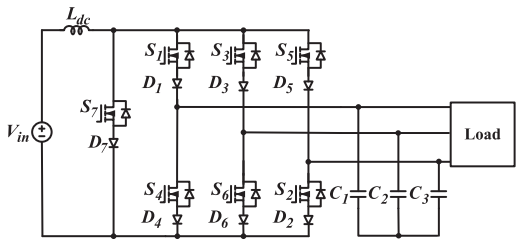



Fig. 2. CSI7 with hybrid switches [21].

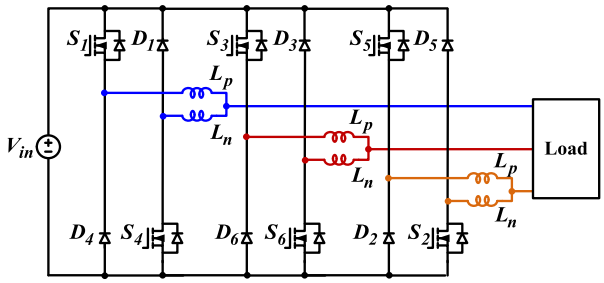



Fig. 3. Three-phase dual-buck inverter.

performance, a tri-state CSI7 is proposed in [19]. This inverter removes the zero in the right-half-plane of the control-to-output transfer function by using an additional null state obtained from the additional switch. Another grid-tied CSI7 with improved efficiency is proposed in [20]. In this topology, each null state vector is generated by turning ON the switch $S_7$ only, which results in reduced conduction losses. However, the lack of reverse blocking capability of the switch $S_7$ may cause interphase short-circuit problems. Another interesting and efficient CSI7 as shown in Fig. 2, is proposed in [21]. In this topology, the switch $S_7$ is silicon carbide while the remaining switches are silicon type (Si). The diode in series with the switch $S_7$ eliminates the risk of interphase short-circuit fault. Moreover, two modulation schemes are proposed to ensure zero-current switching in the Si switches $S_1 - S_6$, which results in boosting efficiency. Apart from this, efforts are also made in [22] to reduce the size of the dc-link inductor with the help of new space vector modulation (SVM).

Despite all these improvements, the open-circuit problem continues to be a major concern for CSIs. Therefore, caution must be taken to prevent the sudden disruption of the input inductor current. In normal operation, to avoid the open-circuit problem, overlap-time is introduced in the gating signals of switches. But the problem is that the overlap-time distorts the output current waveforms [23]. Some efforts are made in [16] and [24] to compensate for the distortions caused by overlap-time. However, these researches are based on CSI6 and increase the complexity of modulation strategy by adding the compensation stage. Furthermore, dead-time may still appear in the top three switches and $S_7$, or in the bottom three switches and $S_7$ due to electromagnetic interference (EMI) or gate driver fault, etc. Under these conditions, the inductor current will have no path to flow, and enormous voltage spikes will be produced, that can easily kill the semiconductor devices.

Therefore, in this article, a new three-phase CSI7 is proposed. The proposed inverter has no open-circuit problem, which results in increased reliability. In addition, the overlap-time can be reduced, which will improve the quality of output waveforms.

## II. Motivation for the Proposed CSI7

The discussion towards the unique relationship between the current-source converter (CSC) and the voltage-source converter (VSC) can be traced back to the 1970s. According to numerous works in the literature, the CSC and VSC share a dual relationship in such a way that a dual component occurs in the VSC for each component of the CSC [25]. Many CSC topologies are derived from VSC by using the duality theorem. In VSC, switches connected across the voltage source should not be switched-ON simultaneously. By doing so, the dc source is short-circuited and the switching devices can be easily damaged due to the current shoot-through problem. Similarly, according to the duality theorem, the switches connected to the current source should not be turned-OFF simultaneously. By doing so, the current path will be blocked and huge voltage spikes will be generated across the switches.

To prevent the current shoot-through problem in the VSC, overlap-time is strictly forbidden and thus dead-time is added among the switches. However, dead-time causes distortion in the output voltage waveforms and also reduces the voltage source utilization. Conversely, to prevent voltage spikes in the CSC, dead-time is strictly forbidden and thus overlap-time is added among the switches. However, overlap-time distorts the output current waveforms and reduces the current source utilization. Moreover, despite inserting dead-time in the VSC, the risk of overlap-time still exists due to faulty conditions. During the overlap-time, the current shoot-through problem will occur and the switching devices might blow up. To avoid the current shoot-through problem and improve the output voltage waveforms by minimizing the dead-time, dual-buck structures are introduced in numerous VSC topologies [4]–[8]. The basic structure of a three-phase dual-buck inverter is shown in Fig. 3. In this inverter, the small inductors $L_p$ and $L_n$ are used to protect against the current shoot-through problem during faulty conditions.

Conversely, CSI suffers from the open-circuit problem, but negligible attention is paid to it so far. Therefore, the key motivation is to develop a new CSI topology that can eliminate the open-circuit problem and as a result minimize the overlap-time. One obvious way of doing this is to find the dual structure of three-phase dual-buck inverter of Fig. 3. However, it is not feasible because the duality theorem does not apply directly to nonplanar structures. Anyhow, the key concept obtained from dual-buck inverters is that: in dual-buck inverters, inductors are used to limit the current when switches across the voltage source are turned-ON simultaneously. Now taking help from the duality theorem, one can anticipate that: in CSI, capacitors can be used to limit the voltage when switches connected to the current source are turned-OFF simultaneously. In this article, the same concept

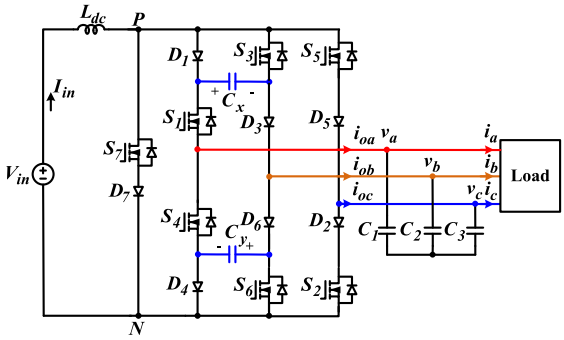



Fig. 4. Proposed three-phase CSI7.

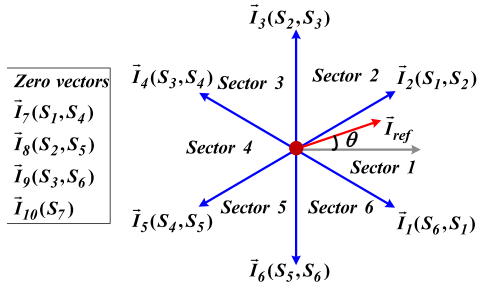



Fig. 5. Space vector diagram of the proposed CSI.

is used in the development of the proposed inverter to avoid the open-circuit problem.

## III. Proposed CSI7

### A. Topology

The proposed CSI7 is shown in Fig. 4. It is obtained from the conventional CSI7 shown in Fig. 2 by making the following modifications: 1) the positions of $S_1$, $D_1$ and $S_6$, $D_6$ are interchanged, 2) two small reliable film capacitors $C_x$ and $C_y$ are added. The inductor $L_{dc}$ draws smooth dc current $I_{in}$ from the input voltage source $V_{in}$ and limits the low-frequency current ripple appearing on it. The capacitors $C_x$ and $C_y$ along with the diodes $D_1$, $D_3$, $D_4$, and $D_6$ ensure that there is always a path for the inductor current $I_{in}$. It means that, if the top switches $(S_1, S_3, S_5)$ along with $S_7$, and/or the bottom switches $(S_4, S_6, S_2)$ along with $S_7$ are all turned OFF, the inductor current $I_{in}$ can still flow through the capacitors $C_x$ and $C_y$. That is why, in the proposed CSI7, there is no open-circuit problem and the voltage overshoot is limited by the added capacitors. Furthermore, due to the elimination of the open-circuit issue, overlap-time can be reduced, which results in improving the quality of output current waveforms.

### B. Modulation Strategy

Different SVM strategies can be adapted for the proposed CSI7. The commonly used SVM strategy applied to CSI is based on double triangular synthesis mode and consists of seven segments [16]. Two different strategies named superior-output-performance and minimal-switching-count modulation strategies are derived from the seven-segment sequence in [21] and can be applied to the proposed CSI7. Although the seven-segment schemes are good in terms of input inductor current ripple but are a little complex and consist of more switching commutations. Therefore, in this article, a simple and typical three-segment SVM strategy [26] is adapted for the proposed CSI7. The other modulation strategies are considered beyond the scope of this article.

The typical space vector diagram for the proposed CSI7 is shown in Fig. 5, where $\vec{I}_1$ to $\vec{I}_6$ are active vectors and $\vec{I}_7$ to $\vec{I}_{10}$ are zero vectors. The space vector can be mathematically expressed by

$$\vec{I}\ (t) = \frac{2}{3}\left[i_{oa}\,(t)\,e^{jo} + i_{ob}\,(t)\,e^{j2\pi/3} + i_{oc}\,(t)\,e^{j4\pi/3}\right] \quad (1)$$

where $i_{oa}$, $i_{ob}$, and $i_{oc}$ are the pulsewidth-modulation (PWM) currents through each phase, as shown in Fig. 4. Every space vector corresponds to a switching state, e.g., the vector $\vec{I}_1$ $[S_6, S_1]$ implies that the switches $S_6$ and $S_1$ are in ON states and the remaining switches are in OFF states. For the active state $[S_6, S_1]$, the PWM currents are

$$\begin{aligned} i_{oa}\ (t) &= I_{in}, \\ i_{ob}\ (t) &= -I_{in}, \text{ and } i_{oc}\ (t) = 0. \end{aligned} \quad (2)$$

Using (2) in (1) and simplifying the results, space vector $\vec{I}_1$ is obtained and is given by

$$\vec{I}_1 = \frac{2}{\sqrt{3}}\, I_{in} e^{-j\pi/6}. \quad (3)$$

The remaining space vectors, $\vec{I}_2$ to $\vec{I}_{10}$, are obtained similarly and are drawn in Fig. 5. The current reference vector $\vec{I}_{ref}$ can be synthesized by two nearby active vectors and the zero vectors. However, to reduce the conduction losses, only the zero vector $\vec{I}_{10}$ is used for the proposed CSI7. After defining the active and zero vectors for the synthesis of $\vec{I}_{ref}$, the corresponding dwell times are then calculated by

$$\left.\begin{aligned} t_{a1} &= M * \sin\left[\pi/6 - \{\vartheta - (k-1)\,\pi/3\}\right] T_s \\ t_{a2} &= M * \sin\left[\pi/6 + \{\vartheta - (k-1)\,\pi/3\}\right] T_s \\ t_z &= T_s - t_{a1} - t_{a2} \end{aligned}\right\} \quad (4)$$

where $t_{a1}, t_{a2}$, and $t_Z$ are the dwell times of two active and one zero vectors, $T_s$ is the sampling period, $M$ is the modulation index, and $\vartheta$ is the angular displacement of $\vec{I}_{ref}$. The value of $k$ is equal to 1, 2, . . . , 6 for sectors 1, 2, . . . , 6, respectively. The typical three-segment switching sequence for generating $\vec{I}_{ref}$ is illustrated in Fig. 6. The red-colored rectangular regions in Fig. 6 represent overlap-time between two switching states.

### C. Mode Analysis

Fig. 6 illustrates that there are six sectors and each sector is then subdivided into different switching combinations. The key waveforms of the proposed CSI7 are shown in Fig. 7. The

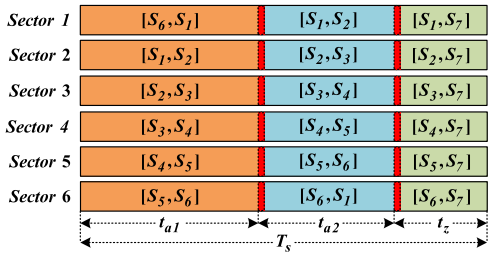



Fig. 6. Illustration of switching pattern for the proposed CSI7 during all six sectors.

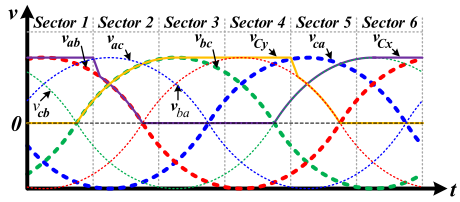



Fig. 7. Output line-to-line voltages and voltages of the capacitors $C_x$ and $C_y$.

current paths during different modes of operation are shown in Figs. 8 and 9. The red-colored lines represent the main current loops, while the blue-colored lines represent the minor current paths. For analysis, the diodes and switches are considered ideal and the load is considered resistive. The capacitor $C_x$ is charged when current flows through diodes $D_1$, $D_3$, and $C_x$ while it is discharged when current flows through switches $S_3$, $S_1$, and $C_x$. This implies that if at least one diode $D_1$ (or $D_3$) is reverse biased, the capacitor $C_x$ cannot be charged. Similarly, if at least one switch $S_1$ (or $S_3$) is OFF, the capacitor $C_x$ cannot be discharged. Likewise, the capacitor $C_y$ is charged through $D_4$ and $D_6$ while discharged through $S_4$ and $S_6$. The detailed mode analysis of the proposed CSI7 is provided as follows.

1) *Mode 1* $[S_1, S_6]$*:* In this mode, $S_1$ and $S_6$ are ON and it appears during sectors 1 and 6. Since $S_3$ is OFF and $D_3$ is reverse biased by $v_{ab} - v_{Cx}$, current cannot flow through the capacitor $C_x$. Similarly, $C_y$ is neither charged nor discharged because $S_4$ is OFF and the current $I_{in}$ flows through $S_6$. According to Fig. 6, there are two possibilities when $S_6$ is ON, (1) $v_{Cy} > 0\ V$, (2) $v_{Cy} = 0\ V$. If $v_{Cy} > 0\ V$, $D_4$ is reverse biased and the current flows through $S_6$. If $v_{Cy} = 0\ V$, $D_4$ is ideally forward biased but the current still flows through $S_6$ rather than $C_y$. The reason is that $C_y$ and $S_6$ appears in parallel and ideally, the voltage across switch is zero volt when it is ON. It means $v_{Cy}$ is also zero volt and no current flows through it. The current direction is shown in Fig. 8(a).
2) *Mode 2* $[S_6, S_1, S_2]$*:* In this mode, $S_1$, $S_2$ and $S_6$ are ON and it appears during sector 1 in the overlap-time. Since $S_3$ is OFF and $D_3$ is reverse biased by $v_{ab} - v_{Cx}$, the capacitor $C_x$ is neither charged nor discharged. If $v_{bc}$ is negative, $D_6$ is reverse biased and the current flows through $S_2$ and $D_2$. The capacitor $C_y$ is neither charged nor discharged because $S_4$ is OFF and $D_6$ is reverse biased. The current direction is shown in Fig. 8(b). On the other hand, if $v_{bc}$ is positive, $D_2$ is reverse biased and the current flows through $S_6$ and $D_6$. The current direction in this case is similar to Fig. 8(a).
3) *Mode 3* $[S_1, S_2]$*:* This mode appears during sectors 1 and 2. The capacitor $C_x$ is neither charged nor discharged because $S_3$ is OFF and $D_3$ is reverse biased. The capacitor $C_y$ is not discharged because $S_4$ and $S_6$ are OFF. However, it can be charged depending on the condition of line voltage $v_{bc}$ and capacitor voltage $v_{Cy}$. If $v_{bc} = v_{Cy}$ , the diodes $D_4$ and $D_6$ are forward biased and the capacitor $C_y$ starts charging. During this condition, $C_y$ is connected across the phase b and c. However, the capacitor $C_y$ is very small as compared to the filter capacitors ($C_1, C_2$, and $C_3$). Therefore, the current through capacitor $C_y$ is negligible. The current flow in this condition is shown in Fig. 8(c). On the other hand, if $v_{bc} < v_{Cy}$, both diodes $D_4$ and $D_6$ are not forward biased and $C_y$ cannot be charged. The current flow in this case is similar to Fig. 8(b).
4) *Mode 4* $[S_1, S_2, S_3]$*:* This mode appears during the overlap-time in sector 2. The diode $D_1$ is reverse biased when $v_{Cx} > 0$ and diode $D_3$ is reverse biased when $v_{Cx} > v_{ab}$. It means if $v_{Cx} > 0$ and $v_{Cx} > v_{ab}$, diodes $D_1$ and $D_3$ are reverse biased. Consequently, the capacitor $C_x$ is discharged as shown in Fig. 8(d). At the time $v_{Cx}$ becomes equal to $v_{ab}$, the main current is shifted to $D_3$ as shown in Fig. 8(e). However, when $v_{Cx}$ reaches to zero volt and $v_{ab}$ becomes negative, $D_1$ is forward biased and $D_3$ is reverse biased. The current path is then shown in Fig. 8(c). Fig. 8(c), (d), and (e) shows that small current is always flowing through $C_y$. However, this is only the case when $v_{bc} = v_{Cy}$ . If $v_{bc} < v_{Cy}$, no current will flow through the capacitor $C_y$.
5) *Mode 5* $[S_2, S_3]$*:* This mode occurs during sectors 2 and 3. The diode $D_3$ is forward biased and $D_1$ is reverse biased. The capacitor $C_x$ is neither charged nor discharged because $S_1$ is OFF and current $I_{in}$ flows through $S_3$. When $v_{bc} = v_{Cy}$ , the diodes $D_6$ and $D_4$ are forward biased and capacitor $C_y$ is charged by small current. The current flow is shown in Fig. 8(f). On the other hand, the capacitor $C_y$ is neither charged nor discharged if $v_{bc} < v_{Cy}$. The current flow in this case is shown in Fig. 8(g).
6) *Mode 6* $[S_2, S_3, S_4]$*:* This mode appears during sector 3. In this mode, $C_x$ and $C_y$ are neither charged nor discharged. The reason is, that $S_1$ and $S_6$ are OFF, $D_6$ is reverse biased and current $I_{in}$ flows through $S_3$ rather than $D_1$. The diode $D_6$ is reverse biased by $v_{ba} - v_{Cy}$. If $v_{ca}$ is negative, $D_2$ is reverse biased and the current flows through $S_4$ as shown in Fig. 8(h). However, if $v_{ca}$ is positive, $D_4$ is reverse biased and the current flows through $S_2$. The current flow in this case is similar to Fig. 8(g).
7) *Mode 7* $[S_3, S_4]$*:* This mode appears during sectors 3 and 4. The capacitors $C_x$ and $C_y$ are neither charged nor discharged and the current flow is similar to Fig. 8(h).

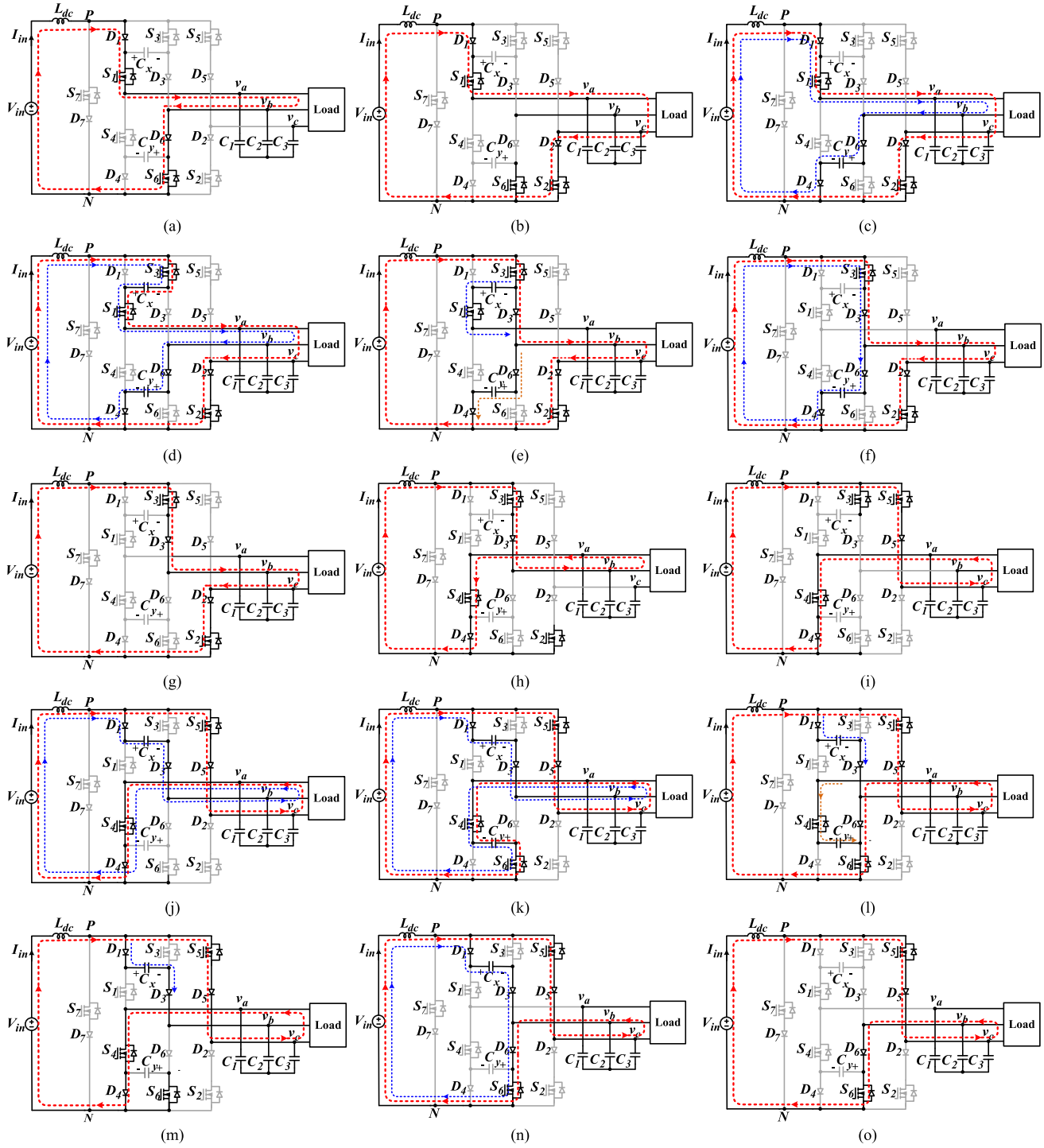



Fig. 8. Current paths during different modes of operations. (a) Modes 1, 2, and 12. (b) Modes 2 and 3. (c) Modes 3 and 4. (d) Mode 4. (e) Mode 4. (f) Mode 5. (g) Modes 5 and 6. (h) Modes 6, 7, and 8. (i) Mode 8. (j) Mode 9. (k) Mode 10. (l) Mode 10. (m) Mode 10. (n) Mode 11. (o) Modes 11 and 12.

8) *Mode 8* $[S_3, S_4, S_5]$*:* This mode appears during sector 4. It can be observed from sector 4 of Fig. 7 that $v_{Cx} = 0$ if $v_{cb} < 0$, and $v_{Cx} = v_{cb}$ if $v_{cb} > 0$. In the former case, $D_3$ is reverse biased by $v_{cb}$ while in the latter case $D_1$ is reverse biased by $v_{Cx}$. Moreover, diode $D_6$ is reverse biased by $v_{ba} - v_{Cy}$. Consequently, capacitors $C_x$ and $C_y$ are neither charged nor discharged. If $v_{bc}$ is positive, $D_3$ is reverse biased and the current flows through $S_5$ as shown in Fig. 8(i). However, if $v_{bc}$ is negative, $D_5$ is reverse biased and the current flows through $S_3$. The current direction in this case is similar to Fig. 8(h).

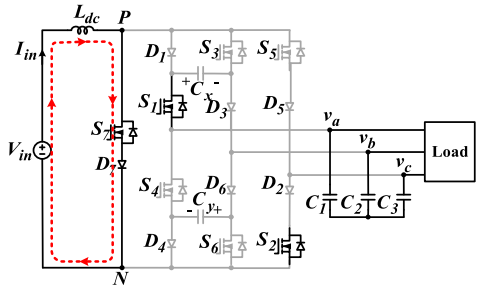



Fig. 9. Operation during mode 13.

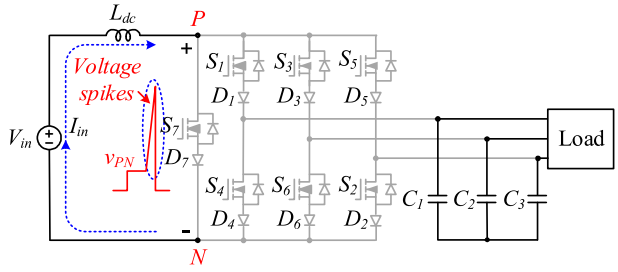



Fig. 10. Interruption of inductor current and voltage spikes generation in CSI7 during fault condition.

9) *Mode 9* $[S_4, S_5]$*:* This mode appears during sectors 4 and 5. The capacitor $C_y$ is neither charged nor discharged. When $v_{cb} = v_{Cx}$ , the capacitor $C_x$ is charged by a small current. The current direction is shown in Fig. 8(j). However, if $v_{cb} < v_{Cx}$, no current flows through the capacitor $C_x$ .
10) *Mode 10* $[S_4, S_5, S_6]$*:* This mode appears during sector 5. When $v_{Cy} > 0$ and $v_{Cy} > v_{ba}$, $D_4$ is reverse biased by $v_{Cy}$ and $D_6$ is reverse biased by $v_{ba} - v_{Cy}$. Consequently, capacitor $C_y$ is discharged as shown in Fig. 8(k). When $v_{Cy} > 0$ and $v_{Cy} = v_{ba}$ , the main current is shifted to $D_6$ as shown in Fig. 8(l). However, when $v_{Cy}$ reaches zero volt and $v_{ba}$ becomes negative, the diode $D_6$ is reverse biased and $D_4$ is forward biased. Therefore, the current flows through $S_4$ and $D_4$. The capacitor $C_y$ is neither charged nor discharged and remains at zero volt. The reason is that $C_y$ and $D_4$ appear in parallel and ideally, the voltage across diode is zero volt when it is forward biased. The current direction is shown in Fig. 8(m). Fig. 8(k)–(m) shows that small current is flowing through $C_x$. However, this is only the case when $v_{cb} = v_{Cx}$ . If $v_{cb} < v_{Cx}$, no current flows through the capacitor $C_x$.
11) *Mode 11* $[S_5, S_6]$*:* This mode occurs during sectors 5 and 6. $C_y$ is neither charged nor discharged because $S_4$ is OFF and the current $I_{in}$ flows through $S_6$. When $v_{cb} = v_{Cx}$, the capacitor $C_x$ is charged as shown in Fig. 8(n). When $v_{cb} < v_{Cx}$, the current direction is shown in Fig. 8(o).
12) *Mode 12* $[S_5, S_6, S_1]$*:* This mode appears during sector 6. The capacitor $C_x$ is neither charged nor discharged because $S_3$ is OFF and $D_3$ is reverse biased by $v_{ab} - v_{Cx}$. Similarly, $C_y$ is neither charged nor discharged because $S_4$ is off and the current $I_{in}$ flows through $S_6$. When $v_{ca} > 0$, $D_5$ is reverse biased and the current direction is similar to Fig. 8(a). When $v_{ca} < 0$, $D_1$ is reverse biased and the current direction is similar to Fig. 8(o).
13) *Mode 13:* In this mode, the input inductor $L_{dc}$ stores energy while the load current is supplied by the filter capacitors $(C_1, C_2, C_3)$. This mode is the result of any one of the following switching combinations: (a) $[S_1, S_2, S_7]$, (b) $[S_1, S_7]$, (c) $[S_2, S_3, S_7]$, (d) $[S_2, S_7]$, (e) $[S_3, S_4, S_7]$, (f) $[S_3, S_7]$, (g) $[S_4, S_5, S_7]$, (h) $[S_4, S_7]$, (i) $[S_5, S_6, S_7]$, (j) $[S_5, S_7]$, (k) $[S_6, S_1, S_7]$, (l) $[S_6, S_7]$. As an example, the current direction for the switching combination $[S_1, S_2, S_7]$ is shown in Fig. 9.

## IV. Reliability Consideration and Operation of the Proposed CSI7 in Fault Conditions

As stated earlier, CSIs generally require finite overlap-time for safe commutation. However, if there are some delays or mismatches in the gate drive signals, there is an open-circuit problem and the switching devices are damaged by overvoltage because the input inductor current is blocked suddenly. The open-circuit problem may also be caused by EMI noise's misgating-off. For example, in the conventional CSIs [see Figs. 1(b) and 2], if the top and/or the bottom switches along with the switch $S_7$ are all OFF accidently, the inductor current $I_{in}$ is suddenly interrupted and high $di/dt$ in the input inductor will cause dangerous voltage spikes. To summarize, the open-circuit problem in conventional CSI7 is caused by the following three fault conditions: (a) when all the switches are OFF; (b) when $S_1$, $S_3$, $S_5$, and $S_7$ are OFF; and (c) when $S_4$, $S_6$, $S_2$, and $S_7$ are OFF. As an example, Fig. 10 shows the interruption of inductor current and voltage spikes generation in conventional CSI7 during fault condition (a).

Conversely, in the proposed CSI7, the capacitors $C_x$ and $C_y$ always provide a path for the inductor current in fault conditions. As a result, the inductor current is not interrupted abruptly and the open-circuit issue is eliminated. In other words, it can also be stated that the proposed CSI7 is more reliable than the conventional CSIs. The reason is that the reliability of conventional CSIs is adversely affected by the open-circuit issue [17]. The current flow during the fault condition (a), is shown in Fig. 11(a). In this case, both capacitors $C_x$ and $C_y$ provide a path for inductor current to limit the voltage spikes effectively. Similarly, the current flow during the fault conditions (b) and (c) is shown in Fig. 11(b) and (c) respectively. In the former case, the capacitor $C_x$ provides a path for inductor current, while in the latter case, the capacitor $C_y$ provides a path for inductor current. As can be seen in Fig. 11, depending on the fault conditions, the input current $I_{in}$ flows through the capacitors $C_x$ and/or $C_y$. The input current charges the capacitors and the rise in capacitors' voltages are given by

$$\left.\begin{aligned} \Delta V_{Cx} &= \tfrac{I_{in}}{C_x}\,\Delta t_f \\ \Delta V_{Cy} &= \tfrac{I_{in}}{C_y}\,\Delta t_f \end{aligned}\right\} \tag{5}$$

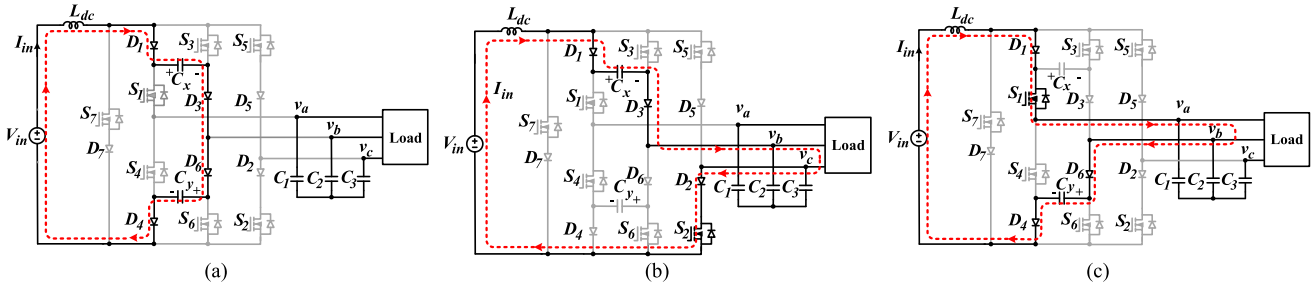



Fig. 11. Current flow in fault conditions. (a) All switches are OFF. (b) Top switches and $S_7$ are OFF. (c) Bottom switches and $S_7$ are OFF.

TABLE I
VOLTAGE STRESSES OF THE SWITCHES

| Voltage stresses | Normal conditions | Fault conditions |
|---|---|---|
| $V_{DS1}$ | $max\ \{v_{Cx} - v_{ab}, v_{ca}\}$ | $max\ \{{v_{Cx}}^f - v_{ab}\}$ |
| $V_{DS2}$ | $max\ \{v_{ca}, v_{cb}\}$ | $max\ \{{v_{Cy}}^f - v_{bc}\}$ |
| $V_{DS3}$ | $max\ \{v_{Cx}, v_{cb}\}$ | $max\ \{{v_{Cx}}^f\}$ |
| $V_{DS4}$ | $max\ \{v_{Cy} + v_{ab}, v_{ac}\}$ | $max\ \{{v_{Cy}}^f + v_{ab}\}$ |
| $V_{DS5}$ | $max\ \{v_{ac}, v_{bc}\}$ | $max\ \{{v_{Cx}}^f + v_{bc}\}$ |
| $V_{DS6}$ | $max\ \{v_{Cy}, v_{bc}\}$ | $max\ \{{v_{Cy}}^f\}$ |
| $V_{DS7}$ | $max\{v_{ab}, v_{ac}, v_{ba}, v_{bc}, v_{ca}, v_{cb}\}$ | $max\ \{{v_{Cx}}^f + {v_{Cy}}^f\}$ |

TABLE II
ELECTRICAL SPECIFICATIONS

| | | | |
|---|---|---|---|
| Output power | 950 $W$ | Dc-link inductor ($L_{dc}$) | 6 $mH$ |
| Input voltage ($V_{in}$) | 160 $V$ | Capacitors ($C_1, C_2, C_3$) | 20 $\mu F$ |
| Line-to-line voltage | 277 $V_{peak}$ | Capacitors ($C_x, C_y$) | 0.2 $\mu F$ |
| Switching frequency | 20 $kHz$ | Switches | IPW60R040C7 |
| Output frequency | 60 $Hz$ | Diodes | RHRG3060 |

where $\Delta V_{Cx}$ and $\Delta V_{Cy}$ represent the increase in voltages of capacitors $C_x$ and $C_y$, respectively, while $\Delta t_f$ represents the time duration of fault conditions. Therefore, after the fault conditions, the capacitors' voltages can then be calculated as

$$\left.\begin{aligned} {v_{Cx}}^f &= v_{Cx} + \Delta V_{Cx} \\ {v_{Cy}}^f &= v_{Cy} + \Delta V_{Cy} \end{aligned}\right\} \tag{6}$$

where ${v_{Cx}}^f$ and ${v_{Cy}}^f$ represent, respectively, the voltages of the capacitors $C_x$ and $C_y$ with fault conditions. Furthermore, Fig. 11 implies that in fault condition in Fig. 11 (a) both $C_x$ and $C_y$ are charged, whereas in the condition in Fig. 11 (b) only $C_x$ and in condition (c) only $C_y$ is charged. However, as it can be found later on, that the voltage stresses of the switches in fault conditions depend on the voltages of both capacitors. Therefore, fault condition (a) is the worst case and is considered for further analysis.

Before finding voltage stresses of the switches in fault conditions, it is better to find them in normal conditions. Taking an example of the switch $S_1$, it can be deduced from Fig. 4 that when $S_3$ is ON and $S_5$ is OFF, the drain-to-source voltage $v_{DS1}$ of the switch $S_1$ is equal to $v_{Cx} - v_{ab}$. Similarly, when $S_3$ is OFF and $S_5$ is ON, then $v_{DS1} = v_{ca}$ . It means that the voltage stress $V_{DS1}$ of the switch $S_1$ is found by selecting the maximum value between $v_{Cx} - v_{ab}$ and $v_{ca}$. The maximum value between $v_{Cx} - v_{ab}$ and $v_{ca}$ is denoted by $\max\{v_{Cx} - v_{ab},\ v_{ca}\}$. The voltage stresses of the remaining switches are calculated similarly and are listed in Table I. While looking at Table I and the waveforms in Fig. 7, it can be deduced that ideally the voltage stresses of all switches are equal to the peak value of line-to-line voltages.

The voltage stresses of the switches in fault condition (a), which is the worst case, can be deduced from Fig. 11(a) and are listed in Table I. The other fault conditions are omitted because in those cases, the voltage stresses of only top or bottom switches are changed while the remaining switches operate like normal conditions. Moreover, Table I shows that voltage stresses of the switches in normal and fault conditions are not identical. As an example, in normal conditions, the voltage stress of switch $S_7$ is the peak value of the line-to-line voltage, while in fault conditions it is equal to $\max\ ({v_{Cx}}^f + {v_{Cy}}^f)$.

## V. SIMULATIONS AND EXPERIMENTAL RESULTS

In this section, both simulations and experimental results are provided to verify the operation and performance of the proposed CSI7. The system parameters for simulations and experiments are listed in Table II. The selection of capacitors $C_x$ and $C_y$ is explained in the upcoming subsection. The input dc-link inductor $L_{dc}$ provides impedance to suppress the input current ripple. Low current ripple enables the inverter PWM algorithm to regulate the amplitude and frequency of three-phase output currents accurately. Based on [27], the expression for the value of $L_{dc}$ is given by

$$L_{dc} = \frac{\sqrt{3}.V_{ph}}{4.f_{sw}.\Delta i_L} \tag{7}$$

where $V_{ph}$ is the peak value of phase voltage, $f_{sw}$ is the switching frequency, and $\Delta i_L$ is the maximum allowable inductor current ripple. A common approach is to keep $\Delta i_L$ smaller than $20\%$ of the rated input current $I_{in}$.

Similarly, the CSI's output filter capacitors $(C_1, C_2,\ C_3)$ are designed to keep the line-to-line voltage ripple smaller than $5\%$ of rated line-to-line voltage. The values of filter capacitors can be found by

$$C_1,\ C_2,\ \ C_3 = \frac{I_{in}}{4.f_{sw}.\Delta v_C} \tag{8}$$

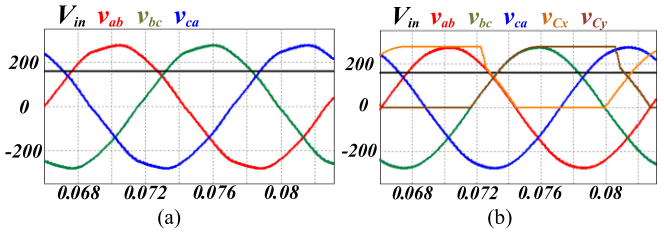



Fig. 12. (a) Input voltage $V_{in}$ and line-to-line voltages $v_{ab}$, $v_{bc}$, $v_{ca}$ of conventional CSI7. (b) Input voltage $V_{in}$, line-to-line voltages $v_{ab}$, $v_{bc}$, $v_{ca}$, and voltages of capacitors $v_{Cx}$, $v_{Cy}$ of proposed CSI7.

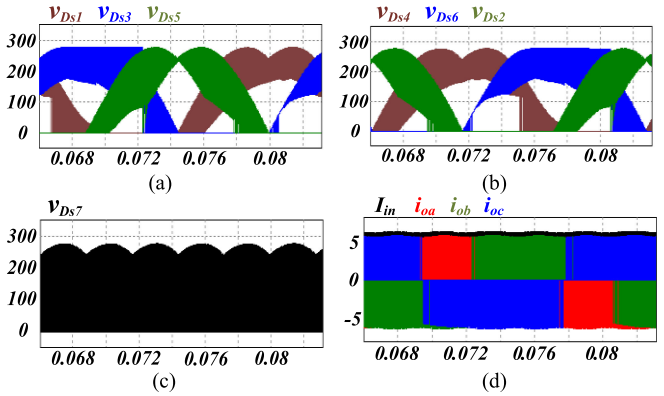



Fig. 13. (a) Drain-to-source voltages of top switches $v_{Ds1}$, $v_{Ds3}$, $v_{Ds5}$. (b) Drain-to-source voltages of bottom switches $v_{Ds4}$, $v_{Ds6}$, $v_{Ds2}$. (c) Drain-to-source voltage of switch $S_7$. (d) Input current $I_{in}$ and PWM currents $i_{oa}$, $i_{ob}$, and $i_{oc}$.

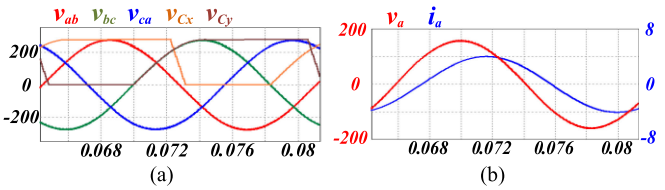



Fig. 14. Waveforms with inductive load. (a) Line-to-line voltages $v_{ab}$, $v_{bc}$, $v_{ca}$ and voltages of capacitors $v_{Cx}$, $v_{Cy}$. (b) Phase voltage $v_a$ and phase current $i_a$.

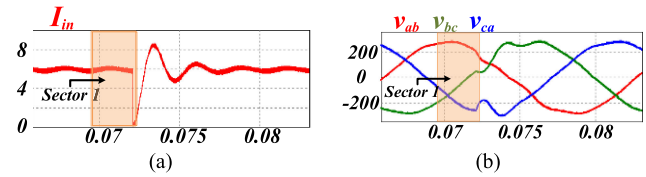



Fig. 15. Waveforms of conventional CSI and CSI7 in fault conditions during sector 1. (a) Input inductor current. (b) Line-to-line voltages.

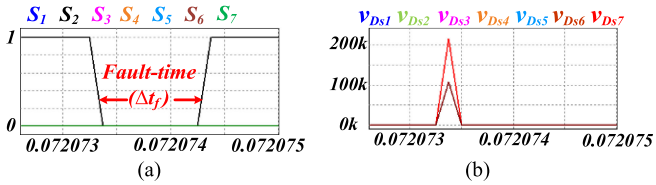



Fig. 16. (a) Gate signals of switches during fault-condition. (b) Drain-to-source voltages of switches in conventional CSI and CSI7.

where $\Delta v_C$ is the maximum allowable voltage ripple across the filter capacitors [27].

### A. Simulation Results

Simulations are performed for both conventional and proposed CSI7 using PSIM software. The conventional CSI7 has open-circuit problem and therefore 2 $\mu$s overlap-time is inserted in the gate signals. The overlap time in conventional CSI7 cannot be reduced too much. The reason is that the shorter the overlap time, the possibility of the input inductor current interruption is higher due to the characteristics of the switching devices, resulting in reduced reliability of the inverter [16]. However, the proposed CSI7 has no open-circuit problem, and the overlap-time is reduced to 0.4 $\mu$s. The input voltage and line-to-line voltages of conventional CSI7 are shown in Fig. 12(a). The input voltage, line-to-line voltages, and voltages across the capacitors $v_{Cx}$, $v_{Cy}$ of the proposed CSI7 are shown in Fig. 12(b). Due to the reduction of overlap-time in the proposed CSI7, the waveforms in Fig. 12(b) are smooth and have less distortion as compared to the waveforms in Fig. 12(a). The drain-to-source voltages of the proposed CSI7 are shown in Fig. 13(a)–(c). These waveforms show that the voltage stresses of the switches in normal operation are equal to the peak value of line-to-line voltage which is 277 V. The unipolar PWM currents $(i_{oa}, i_{ob}, i_{oc})$ and input current $I_{in}$ are shown in Fig. 13(d). Although the analysis and simulation results until now are for resistive load, the proposed inverter can also provide reactive power. Fig. 14 shows simulation results with a partly inductive load while keeping the apparent power equal to 950 W. The load is star-connected and the value of resistor and inductor per phase are 32 Ω and 60 mH. The line-to-line voltages and voltages across the capacitors $(v_{Cx}, v_{Cy})$ are shown in Fig. 14(a), while the phase voltage $v_a$ and phase current $i_a$ are shown in Fig. 14(b).

Moreover, to show the effectiveness of the proposed CSI7 in fault conditions, all the switches are turned-OFF for 1 $\mu$s in sector 1. Fig. 15 shows the inductor current and line-to-line voltages of the conventional CSI and CSI7. In Fig. 15(a), due to fault conditions, the inductor current has no path and is suddenly reduced to zero. This high $di/dt$ of the input inductor generates huge voltage spikes across the switches. Fig. 16 shows gate signals and drain-to-source voltages of switches during fault conditions. Voltage spikes of 214 kV is generated across the switch $S_7$, while 107 kV is generated across the switches $S_1, S_2, \ldots, S_6$. Conversely, in the proposed CSI7, no voltage spikes are generated in the fault conditions. The input inductor current and line-to-line voltages of the proposed CSI7 are shown in Fig. 17(a) and (b), respectively. Fig. 17 implies that, during fault conditions, the input inductor current in the proposed CSI7 is continuous and is not suddenly interrupted like the conventional CSI/CSI7. This is because the inductor current flows through the capacitors $C_x$ and $C_y$ in the proposed CSI7. The increase in voltages of capacitors $(\Delta v_{Cx}, \Delta v_{Cy})$ are shown in Fig. 18. The line-frequency waveforms are shown in Fig. 18(a), while the waveforms zoomed at fault conditions

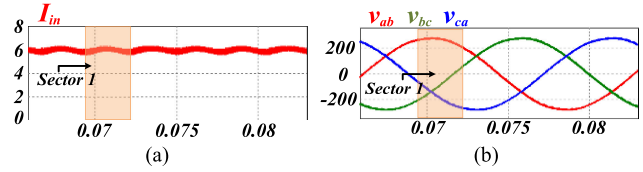



Fig. 17. Waveforms of the proposed CSI7 in fault conditions during sector 1. (a) Input inductor current. (b) Line-to-line voltages.

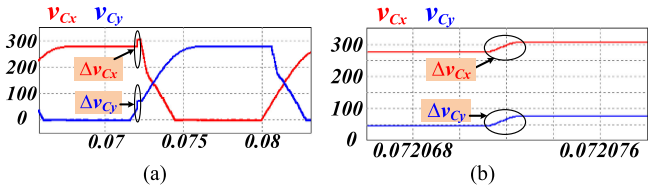



Fig. 18. Voltages across the capacitors $C_x$ and $C_y$. (a) At line frequency with fault conditions in sector 1. (b) Zoomed waveforms at fault condition only.

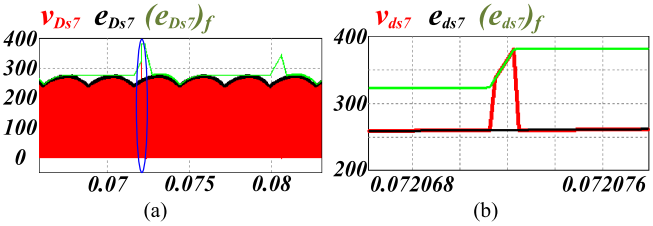



Fig. 19. Drain-to-source voltage of the switch $S_7$ and its upper envelope in normal and fault conditions. (a) Line frequency waveforms. (b) Waveforms zoomed at fault conditions.

are shown in Fig. 18(b). It can be observed that during fault conditions according to (5), the voltages of capacitors $v_{Cx}$ and $v_{Cy}$ are increased by 30 V. $v_{Cx}$ is increased from 277 to 307 V, while $v_{Cy}$ is increased from 47 to 77 V. The drain-to-source voltage of the switch $S_7$ and its zoomed waveforms during fault conditions are shown in Fig. 19(a) and (b) respectively. The blue circle is used to highlight the region of fault conditions. $e_{ds7}$ and $(e_{ds7})_f$ represent the upper envelopes of the drain-to-source voltage of the switch $S_7$ in normal and fault conditions, respectively. The envelopes are obtained from Table I with the help of C-block in PSIM software. Fig. 19(b) shows that, in normal conditions $v_{ds7}$ follows $e_{ds7}$ while in fault conditions it follows $(e_{ds7})_f$.

The drain-to-source voltages of the remaining switches and their upper envelopes are shown in Fig. 20. Simulation results show that the peak drain-to-source voltages of the switches $S_1, S_2$, and $S_6$ are 277 V, while the peak drain-to-source voltages of the switches $S_3, S_4$, $S_5$ and $S_7$ are 307, 288, 352, and 380 V, respectively. These results assure that the capacitors $C_x$ and $C_y$ limit the rise in drain-to-source voltages of the switches during fault conditions and the dangerous voltage spikes are eliminated.

Further, simulation results show that due to fault conditions in sector 1, the peak drain-to-source voltages of the switches $S_3, S_4$, $S_5$, and $S_7$ are increased while the remaining switches are unchanged. This is because the peak drain-to-source voltages across the switches also depend on the location of fault

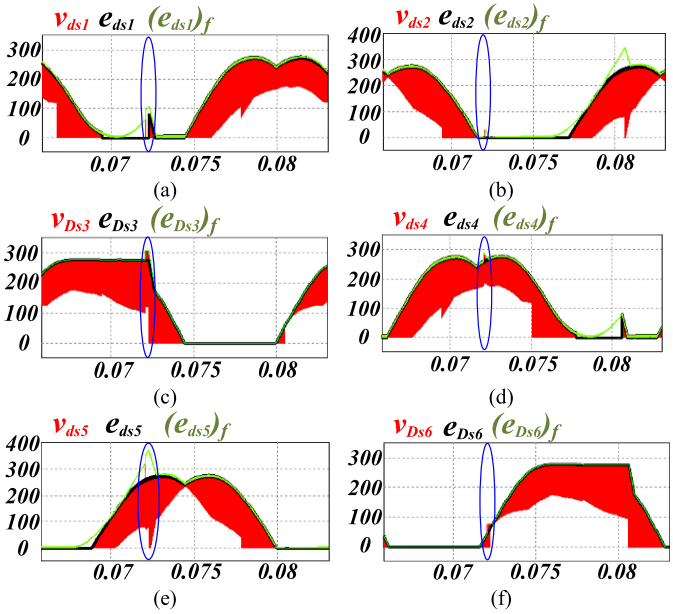



Fig. 20. Drain-to-source voltages and their upper envelopes in normal and fault conditions (a) Switch $S_1$. (b) Switch $S_2$. (c) Switch $S_3$. (d) Switch $S_4$. (e) Switch $S_5$. (f) Switch $S_6$.

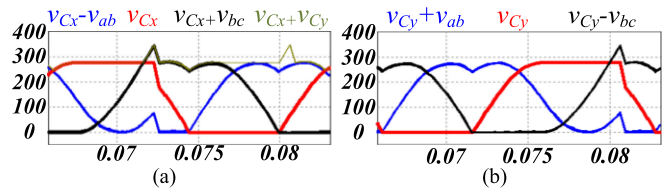



Fig. 21. (a) Waveforms of $(v_{Cx} - v_{ab})$, $v_{Cx}$, $v_{Cx} + v_{bc}$, $v_{Cx} + v_{Cy}$. (b) Waveforms of $v_{Cy} + v_{ab}$, $v_{Cy}$, and $v_{Cy} + v_{bc}$.

conditions. As an example, due to fault conditions in sector 1, the peak drain-to-source voltage of $S_3$ is increased from 277 to 307 V. However, if the fault conditions appear in sector 3, the peak drain-to-source voltage of $S_3$ will not increase and will be equal to 277 V. The reason is that switch $S_3$ is always on in sector 3 and after fault conditions, $v_{ds3}$ is reduced to "0 V" again. Besides, the fault conditions might appear in any sector and for each sector the peak drain-to-source voltages of the switches are not identical. Therefore, to select switches, it is necessary to find the maximum possible voltages that should appear across the switches. As an example, the voltage stress of switch $S_7$, which is also shown in Table I is given by

$$V_{ds7} = \max\left({v_{Cx}}^f + {v_{Cy}}^f\right) . \tag{9}$$

Putting (6) in (9), we get

$$V_{ds7} = \max\left(v_{Cx} + v_{Cy}\right) + \Delta V_{Cx} + \Delta V_{Cy}. \tag{10}$$

In (10), $v_{Cx}$ and $v_{Cy}$ vary with time and therefore $\max(v_{Cx} + v_{Cy})$ can be obtained from the plot shown in Fig. 21(a), which is 347 V. After that, $\Delta V_{Cx}$ and $\Delta V_{Cy}$ are determined by the following equation:

$$\Delta V_{Cx} + \Delta\, V_{Cy} = V_{sw,br} - \max\left(v_{Cx} + v_{Cy}\right). \tag{11}$$

TABLE III
VOLTAGE STRESSES OF THE SWITCHES IN FAULT CONDITIONS

| $V_{ds1}$ | $V_{ds2}$ | $V_{ds3}$ | $V_{ds4}$ | $V_{ds5}$ | $V_{ds6}$ | $V_{ds7}$ |
|---|---|---|---|---|---|---|
| 307 V | 377 V | 307 V | 307 V | 377 V | 307 V | 407 V |

Where $V_{sw,br}$ is the maximum breakdown voltage of the switch and can be obtained from the datasheets. For simplicity, the capacitors $C_x$ and $C_y$ are considered to be identical and therefore according to (5), $\Delta V_{Cx} = \Delta V_{Cy}$ . Putting these values in (11), $\Delta V_{Cx}$ and $\Delta V_{Cy}$ are then determined by

$$\Delta V_{Cx} = \Delta V_{Cy} = \frac{V_{sw,br} - \max(v_{Cx} + v_{Cy})}{2}. \quad (12)$$

Moreover, according to (5), $\Delta V_{Cx}$ and $\Delta V_{Cy}$ also depend on values of capacitors $C_x$ and $C_y$. Therefore, the capacitors can be chosen to guarantee, the voltage stress of the switch under fault conditions is always lower than $V_{sw,br}$. Rearranging (5), the capacitors $C_x$ and $C_y$ are given by

$$\left.\begin{aligned} C_x &> \tfrac{I_{in}}{\Delta V_{Cx}} \Delta t_f \\ C_y &> \tfrac{I_{in}}{\Delta V_{Cy}} \Delta t_f \end{aligned}\right\}. \quad (13)$$

The voltage stresses of the other switches can be obtained similarly from Table I, and are given by

$$\left.\begin{aligned} V_{ds1} &= \max(v_{Cx} - v_{ab}) + \Delta V_{Cx} \\ V_{ds2} &= \max(v_{Cy} - v_{bc}) + \Delta V_{Cy} \\ V_{ds3} &= \max(v_{Cx}) + \Delta V_{Cx} \\ V_{ds4} &= \max(v_{Cy} + v_{ab}) + \Delta V_{Cy} \\ V_{ds5} &= \max(v_{Cx} + v_{bc}) + \Delta V_{Cx} \\ V_{ds6} &= \max(v_{Cy}) + \Delta V_{Cy} \end{aligned}\right\}. \quad (14)$$

As $v_{Cx}$, $v_{Cy}$, $v_{ab}$, and $v_{bc}$ vary with time. Therefore, in (14), $\max(v_{Cx} - v_{ab})$, $\max(v_{Cy} - v_{bc})$, $\max(v_{Cx})$, $\max(v_{Cy} + v_{ab})$, $\max(v_{Cx} + v_{bc})$, and $\max(v_{Cy})$ are obtained from the plots shown in Fig. 21(a) and (b). The plots show that the maximum values are 277, 347, 277, 277, 347, and 277 V, respectively. Apart from this, after selecting $C_x$ and $C_y$ based on (12) and (13), $\Delta V_{Cx}$ and $\Delta V_{Cy}$ are calculated from (5). Then putting these values in (10) and (14) gives voltage stresses of the switches in fault conditions. Consider as an example, the breakdown voltages of the switches are 600 V and $\Delta t_f = 1\ \mu$s. Putting these values in (12) and then using (13), implies that $C_x$ and $C_y$ should be greater than 48 $n$F. Selecting a little higher value of capacitances reduce $\Delta V_{Cx}$ and $\Delta V_{Cy}$ which in terms reduce the voltage stresses of switches as well. In the proposed inverter, $C_x = C_y = 0.2\ \mu$F and $\Delta t_f = 1\ \mu$s. Therefore, according to (5), $\Delta V_{Cx} = \Delta V_{Cy} = 30$ V. Putting these values in (10) and (14), voltage stresses of the switches are obtained which are listed in Table III.

### B. Experimental Results

For experimental verification, a 950-W hardware prototype, with electrical specifications similar to Table II, is built and tested with resistive load. Experimental results with inductive load are not provided due to the unavailability of big value inductors. Anyhow, the simulation results confirmed the functionality of the proposed CSI7 with the inductive load as well. Experiments are first performed in normal conditions with overlap-time of 0.4 $\mu$s and then followed by fault conditions. Film capacitors with part number MKP10-.1/630/5P22 are used for both $C_x$ and $C_y$. The photograph of prototype is shown in Fig. 22.

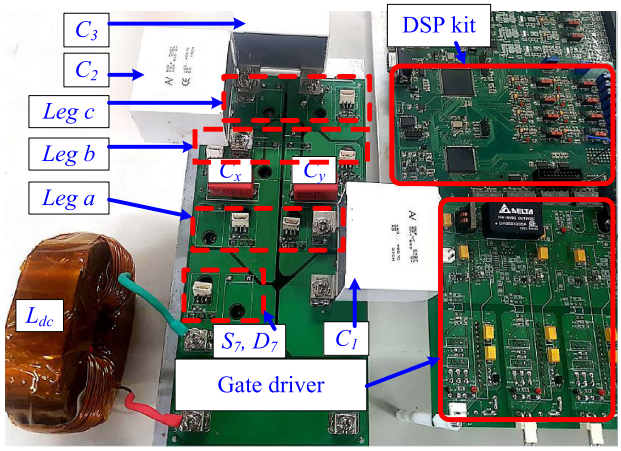
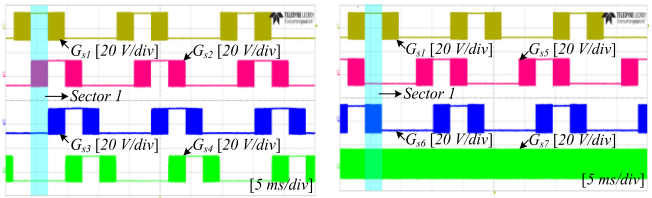
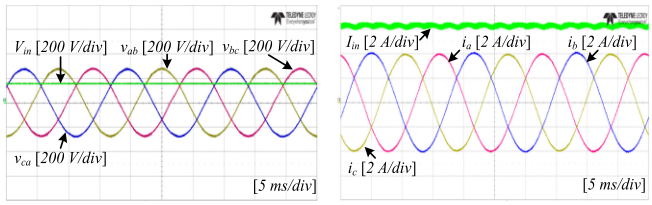



Fig. 22. Prototype picture of proposed inverter.




(a) (b)

Fig. 23. Gate driving signals of switches. (a) $G_{s1}, G_{s2}, G_{s3}, G_{s4}$. (b) $G_{s1}, G_{s5}, G_{s6}, G_{s7}$.




(a) (b)

Fig. 24. (a) Input voltage $V_{in}$ and line-to-line voltages $v_{ab}, v_{bc}$, and $v_{ca}$.(b) Input current $I_{in}$ and phase currents $i_a$, $i_b$, and $i_c$.

The gate driving signals $(G_{s1}, G_{s2}, \ldots, G_{s7})$, generated with the help of digital signal controller TMS320F28335 are shown in Fig. 23. The pale-blue colored highlighted region in Fig. 23 represent sector 1. As explained earlier, it can be observed during sector 1 that the switches $S_2$, $S_6$, and $S_7$ operates at high frequency, $S_1$ is continuously ON, while the remaining switches are continuously off. The input voltage and line-to-line voltages of the proposed CSI7 are shown in Fig. 24(a) while the input current and phase currents are shown in Fig. 24(b). Voltages across the capacitors $v_{Cx}, v_{Cy}$ and drain-to-source voltages of the switches in normal conditions are shown in Fig. 25. As seen, voltage stresses of the switches in normal conditions are equal to the peak value of line-to-line voltages.

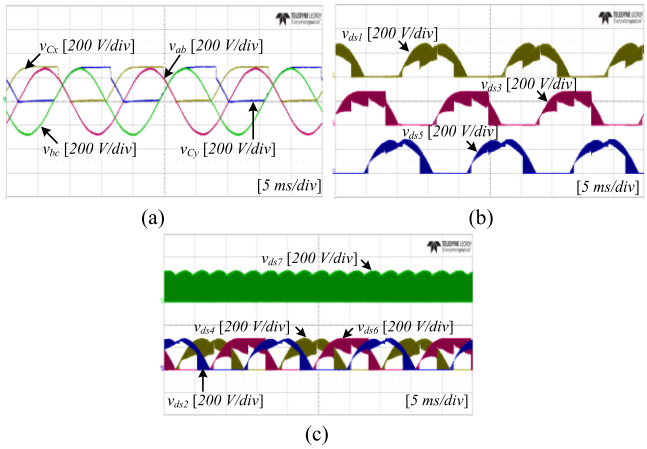



Fig. 25. (a) Voltages across the capacitors $v_{Cx}, v_{Cy}$ and line voltages $v_{ab}$, $v_{bc}$. (b) Drain-to-source voltages $v_{ds1}$, $v_{ds3}$, and $v_{ds5}$. (c) Drain-to-source voltages $v_{ds4}$, $v_{ds6}$, $v_{ds2}$, and $v_{ds7}$.

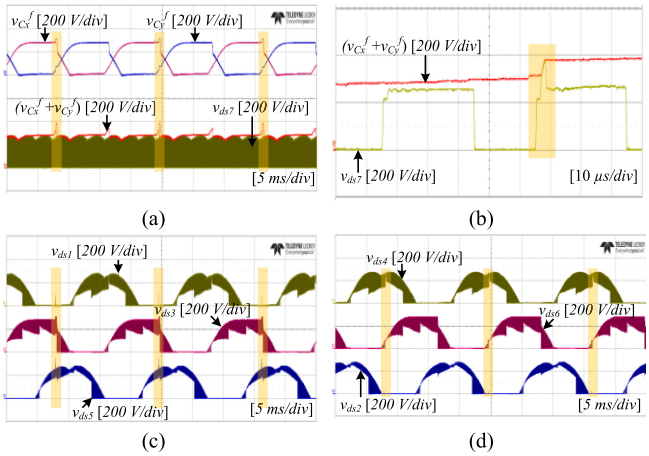



Fig. 26. Key waveforms of proposed CSI7 with fault conditions in sector 1. (a) Drain-to-source voltage $v_{ds7}$, voltages across the capacitors $v_{Cx}{}^f$, $v_{Cy}{}^f$ and their summation $(v_{Cx}{}^f + v_{Cy}{}^f)$. (b) Waveforms of $v_{ds7}$ and $(v_{Cx}{}^f + v_{Cy}{}^f)$ zoomed at fault conditions. (c) Drain-to-source voltages $v_{ds1}$, $v_{ds3}$, and $v_{ds5}$. (d) Drain-to-source voltages $v_{ds4}$, $v_{ds6}$, and $v_{ds2}$.

Moreover, to ensure the operation of the proposed CSI7 in fault conditions, all the switches are turned-OFF for 1 $\mu$s once in sector 1 deliberately. The key waveforms of the proposed CSI7 during fault conditions are shown in Fig. 26. The fault conditions are highlighted by the orange-colored rectangular regions. The drain-to-source voltage $v_{ds7}$, voltages across the capacitors $v_{Cx}{}^f$, $v_{Cy}{}^f$ and their summation $(v_{Cx}{}^f + v_{Cy}{}^f)$ are shown in Fig. 26(a). The superscript "$f$" in $v_{Cx}{}^f$ and $v_{Cy}{}^f$ is for the fault conditions. As expected, the voltage $v_{Cx}{}^f$ is increased from 280 to 310 V while the voltage $v_{Cy}{}^f$ is increased from 40 to 70 V in the fault conditions. The waveforms $v_{ds7}$ and $(v_{Cx}{}^f + v_{Cy}{}^f)$ are zoomed at fault conditions and are shown in Fig. 26(b). As stated earlier, the drain-to-source voltage of the switch $S_7$ in fault conditions is equal to $(v_{Cx}{}^f + v_{Cy}{}^f)$. Therefore, as shown in Fig. 26(b), $v_{ds7}$ becomes equal to $(v_{Cx}{}^f + v_{Cy}{}^f)$ in fault conditions. Similarly, the drain-to-source voltages of the switches $S_1$, $S_3$, and $S_5$ are shown in Fig. 26(c) while the drain-to-source voltages of the remaining switches are shown in Fig. 26(d). It can be deduced from Fig. 26 that during fault conditions, the peak drain-to-source voltages $v_{ds7}$, $v_{ds5}$, and $v_{ds3}$ are limited by the capacitors to 380, 350, and 310 V respectively. On the other hand, the drain-to-source voltages of the remaining switches are increased momentarily during fault conditions but their peak values are not increased and are equal to the peak value of line-to-line voltages. Furthermore, it is not possible to take experimental results of the conventional CSI and CSI7 during the fault conditions because of huge voltage spikes generation across the switches. Besides, both the simulations and experimental results closely match each other and also with the theoretical analysis, which confirms the validity of the proposed CSI7.

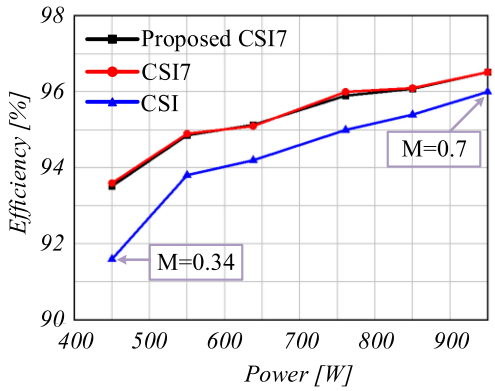



Fig. 27. Measured efficiencies of proposed and conventional CSIs at different output power.

Eventually, efficiency and total harmonic distortion (THD) are measured using YOKOGAWA WT-1800 power analyzer. Since the purpose of this article is to investigate and provide a solution for the open-circuit problem of conventional CSIs, the power semiconductors were not chosen to maximize efficiency. Anyhow, to provide a fair comparison with conventional CSIs, the same hardware setup and modulation strategies are used. The power loss $P_{c-xy}$ due to additional capacitors $C_x$ and $C_y$ can be calculated as

$$P_{c-xy} = I^2{}_{Cx-rms}\,.ESR_x + I^2{}_{Cy-rms}.ESR_y \tag{15}$$

where $ESR_x, ESR_y, I_{Cx-rms}$, and $I_{Cy-rms}$ are the equivalent series resistances and rms currents of capacitors $C_x$ and $C_y$. The rms currents $I_{Cx-rms}$ and $I_{Cy-rms}$ are given by

$$\left.\begin{aligned} I_{Cx-rms} &= \sqrt{\frac{1}{T_{LF}}\int_0^{T_{LF}} i^2{}_{Cx}\,(t)\,dt} \\ I_{Cy-rms} &= \sqrt{\frac{1}{T_{LF}}\int_0^{T_{LF}} i^2{}_{Cy}\,(t)\,dt} \end{aligned}\right\}. \tag{16}$$

where $T_{LF}$ is the time period of the line frequency. From the manufacturer's datasheet, the value of ESR is 30 m$\Omega$. While based on (16), the values of $I_{Cx-rms}$ and $I_{Cy-rms}$ are 0.14 A each. Thus, according to (15), the losses in capacitors $C_x$ and $C_y$ are considerably small. The efficiencies of conventional CSI6, CSI7, and proposed CSI7 are measured at different output power and the results are plotted in Fig. 27. The same three-segment switching scheme is applied to both conventional and proposed

TABLE IV
AMPLITUDES OF HARMONICS IN LOAD CURRENT $i_a$ OF CONVENTIONAL AND PROPOSED CSI7

| Topology | Harmonic (n) | | | | | | | | | | | | | | | THD (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | |
| Conventional CSI7 | 3.97 | 0.031 | 0.056 | 0.035 | 0.04 | 0.047 | 0.028 | 0.009 | 0.001 | 0.008 | 0.009 | 0.015 | 0.014 | 0.009 | 0.001 | 2.6 |
| Proposed CSI7 | 3.98 | 0.017 | 0.041 | 0.015 | 0.017 | 0.019 | 0.011 | 0.005 | 0.001 | 0.003 | 0.008 | 0.001 | 0.004 | 0.003 | 0.001 | 1.4 |

TABLE V
COMPARISON OF CONVENTIONAL AND PROPOSED CSIS

| Topology | Switches | Diodes | Overlap time | Open circuit problem | THD | Reactive power capability | Efficiency |
|---|---|---|---|---|---|---|---|
| CSI6 [15] | 6 | 6 | Yes | Yes | Medium | Yes | Medium |
| CSI7 [19] | 7 | 6 | Yes | Yes | Medium | limited | Highest |
| CSI7 [10], [20] | 7 | 7 | Yes | Yes | Medium | Yes | Higher |
| Four-leg CSI [9] | 8 | 8 | Yes | Yes | Medium | Yes | Medium |
| Proposed CSI7 | 7 | 7 | Can be minimized | No | Lower | Yes | Higher |

CSIs. The efficiency of conventional CSI6 is measured by turning OFF the switch $S_7$ and generating null states from space vectors $\vec{I}_7$, $\vec{I}_8$ and $\vec{I}_9$. Furthermore, similar to [21], the input current and the output voltage is kept constant while the output power is varied by changing the modulation index. Fig. 27 shows that efficiencies of conventional and proposed CSI7 are almost equal but they are better than that of CSI6. This is because only one switch and diode conduct during the null state in CSI7. The efficiency of conventional four-leg CSI [9] is not measured but according to [28], it will be almost equal to CSI6. Similarly, the harmonic spectra and THD of phase current $i_a$ for both conventional and proposed CSI7 are included in Table IV. It can be observed that the THD of proposed CSI7 is less than conventional CSI7.

In the end, a brief comparison among basic and proposed CSIs is shown in Table V. CSI6 has the minimum number of components and is comparatively good in terms of cost. CSI7 presented in [20] has one more switch than CSI6 but it is more efficient because input current flows through only one switch during the null state. However, the limitation is that it can only operate with power factor close to one. CSI7 presented in [10] and [21] has a diode in series with the switch $S_7$ and thus its reactive power capability is not limited. It is also good in terms of efficiency because the input current flows through one switch and diode during the null state. Four-leg CSI [9] has the highest number of components but the good feature is that it can eliminate high-frequency component from common-mode voltage by connecting the grid neutral to the midpoint of split capacitors on the input side. Besides their respective advantages, the conventional CSIs have open-circuit problem and therefore overlap-time is necessary. However, overlap-time causes distortion in the output current waveforms. In the proposed CSI7, there is no open-circuit problem and the overlap-time can be minimized. As a result, the THD of output current is reduced. Moreover, the proposed CSI7 can achieve better efficiency as compared to conventional CSI6 and four-leg CSI.

## VI. CONCLUSION

This article has presented a novel three-phase CSI7. The proposed inverter is reliable because it successfully solves the open-circuit problem, which occurs in conventional CSI and CSI7. Moreover, due to the absence of open-circuit problem, the overlap-time is minimized, which results in improved output waveforms. The theoretical analysis and performance of the proposed CSI7 are verified through both simulations and experimental results as well.

It should be noted that this article mainly focused on three-level three-phase CSI with a three-segment SVM strategy. The other strategies like five and seven segments modulation schemes and the extension of the proposed concept to multilevel three-phase CSIs are the subjects of future research.

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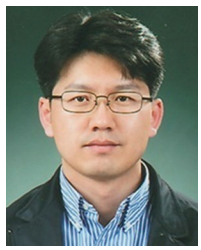
**Fazal Akbar** (Student Member, IEEE) received the B.S. degree in electrical engineering from the University of Engineering and Technology, Peshawar, Pakistan, in 2015, and the M.S. and Ph.D. degrees in power electronics from the School of Energy Engineering, Kyungpook National University, Daegu, South Korea, in 2018 and 2021, respectively.

His current research interests include high-frequency magnetics design, grid-tied inverters, and ac–ac converters.

Dr. Akbar was a recipient of scholarships from NICT R&D Fund Pakistan, and Kyungpook National University.



**Honnyong Cha** (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical engineering from Michigan State University, East Lansing, MI, USA, in 2009.

From 2001 to 2003, he was a Research Engineer with the Power System Technology Company, Ansan, South Korea. From 2010 to 2011, he was a Senior Researcher with the Korea Electrotechnology Research Institute, Changwon, South Korea. In 2011, he was with the School of Energy Engineering, Kyungpook National University. In 2017, he was with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. His current research interests include high-power dc–dc converters, dc–ac inverters, Z-source inverters, and power conversion for electric vehicles and wind power generation.

**Duc-Tuan Do** (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Thai Nguyen University of Technology (TNUT), Vietnam, in 2008 and 2012, respectively, and the Ph.D. degree from the School of Energy Engineering from Kyungpook National University, Daegu, South Korea, in 2021.

He is currently a Lecturer with the Faculty of Electrical Engineering, TNUT. His current research interests include high efficiency bidirectional dc–dc converters, automation systems, and dc–ac inverters.