Accuracy of Three Interterminal Capacitance Models for SiC Power MOSFETs Under Fast Switching

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***Abstract*—This article presents a comprehensive analysis of nonlinear voltage-dependent capacitances of vertical silicon carbide power MOSFETs with lateral channel, focusing specifically on fast switching transients. The capacitance-voltage (*C-V*) device characteristics, (C_{gs}, C_{gd}, C_{ds}), being dependent on both V_{gs} and V_{ds}, are extracted by means of two-dimensional technology computer aided design simulations for a commercially available device in both OFF- and ON-state modes. Different compact models for the power MOSFET are investigated, each employing a three interterminal capacitance model as typically used in power electronics. The performed analysis provides a detailed explanation for the importance of taking into account the dependence of C_{gd}, C_{gs}, and C_{ds} on both of the voltages V_{gs} and V_{ds}. This is especially important for fast switching transients (in the range of 10 ns) in order to accurately predict switching losses, driver losses, current, and voltage slopes, as well as current and voltage delays. As direct measurements for C_{gd}, C_{gs}, and C_{ds} in dependence of both V_{gs} and V_{ds} are highly demanding, the results presented in this article increase the understanding of both the underlying effects as well as of the tradeoffs between accuracy and computational complexity made by simplifying device models. In turn, this information is highly beneficial for enabling accurate and computationally efficient automated design procedures for power electronics.**

***Index Terms*—Compact device modeling, fast switching, power MOSFET capacitances, silicon carbide (SiC) power MOSFET.**

I. Introduction

THE INCREASING demands for electrification and highly efficient energy conversion are driving the adaption of wide bandgap power semiconductor devices in advanced power electronic (PE) systems [1]. Silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) have shown to be a promising switching device for high voltage and high temperature PE applications. As unipolar power devices, SiC MOSFETs enable fast switching operation with lower power losses compared to their silicon counterparts, insulated gate bipolar transistors (IGBTs), and hence, lead to higher power density and higher efficiency power conversion. Design for fast switching operation is one of the requirements that comes along with the employment of SiC power devices [2]. Dynamic device response carries information not only about the device capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics, but also information on frequency-dependent circuit and package parasitics. Moreover, it is very challenging to separate the effects of distributed layout and device properties in the measured switching waveforms containing high frequency ringing. Therefore, device simulations and electromagnetic modeling are frequently used for assessing and optimizing PE systems.

It was shown that nonlinear voltage-dependence of interterminal MOSFET capacitances determine the dynamic performance of power MOSFETs. Their implementation in compact models is of a high importance for an accurate prediction of the switching waveforms [3]–[6]. Compact device models have been used by engineers for simulations of power electronic circuits, demanding a compromise between computational complexity and modeling accuracy. Compact models of power MOSFETs are typically based on three interterminal capacitors: gate-source capacitor C_{gs}, gate-drain capacitor C_{gd}, and drain-source capacitor C_{ds}, connected to MOSFET terminals, as shown in Fig. 1(a). The capacitance values of these capacitors can be obtained experimentally. However, it should be noted that these capacitors represent a simplification of the distributed capacitance within

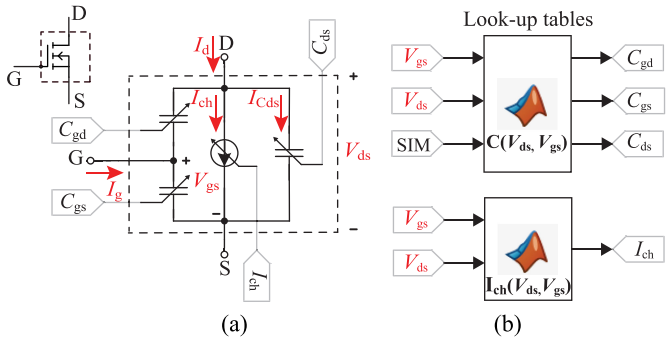

Fig. 1. Compact model of power MOSFET: (a) equivalent circuit implemented in MATLAB Simulink, and (b) the look-up tables used to determine the values of two-voltage dependent capacitors, C_{gs}, C_{ds}, C_{gd}, and current source I_{ch} in circuit simulations based on the voltages across the MOSFET terminals, V_{gs} and V_{ds}. The extracted current and voltage waveforms are marked in red. The MOSFET symbol used in circuit simulations shows the terminals related to the terminals of the MOSFET model implemented in the circuit simulator, i.e., MATLAB Simulink. The pin SIM is used to define which type of *C-V* dependence for C_{gs}, C_{ds}, and C_{gd} is used: two-voltage-/single-voltage-dependent/constant.

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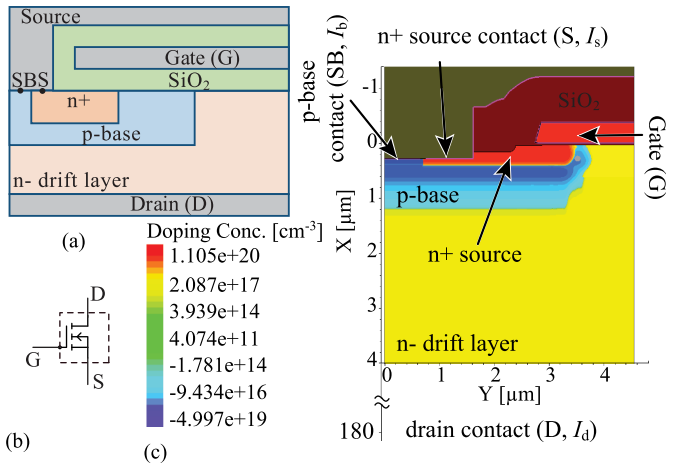

Fig. 2. Modeling of an active cell in SiC power MOSFET: (a) schematics of the half-cell structure, (b) the MOSFET electrical model used in circuit simulations showing the terminals related to the terminals in the TCAD model, and (c) two-dimensional TCAD model of a MOSFET active cell with a p-base contact simulated in Synopsys Sentaurus S-Device, visualizing only first $X = 4$ μm of an $X = 180$ μm active cell [13].

the actual power MOSFET device structure. The main challenge of compact models is to achieve a good accuracy for various operating points defined by a surrounding circuit. In practice, simplifications of the voltage-dependent capacitances are used, as information on the two-voltage dependence of the interterminal capacitances of power devices is typically not available and requires additional characterization steps. The most commonly adopted simplification is based on ($C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$) being recalculated from datasheet input, $C_{\rm iss}$, output, $C_{\rm oss}$, and reverse, $C_{\rm rss}$, device capacitances as: $C_{\rm gd} = C_{\rm rss}$, $C_{\rm gs} = C_{\rm iss} - C_{\rm rss}$, $C_{\rm ds} = C_{\rm oss} - C_{\rm rss}$, which are provided only for the device in the OFF-state ($V_{\rm gs} = 0$). Further simplifications are made by adopting $C_{\rm gs} =$ const. and single voltage dependent $C_{\rm gd}(V_{\rm gd})$ and $C_{\rm ds}(V_{\rm ds})$, or even $C_{\rm ds}$ is constant [2]. The importance of using two-voltage dependent ($C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$) and their experimental characterization for power MOSFETs have been extensively investigated in recent literature [3]–[10]. However, the exact impact of $C_{\rm gs}$; $C_{\rm gd}$; $C_{\rm ds}(V_{\rm gd}, V_{\rm ds})$ in general, and specifically for SiC power MOSFETs, has not been shown in a comprehensive way so far. Circuit simulations performed in technology computer-aided design (TCAD) software including physics-based device models can be highly useful to gain a deep insight in the device switching behavior [11], but require the knowledge of device design beyond datasheet information often not available publicly. TCAD simulation tools provide physics-based modeling of distributed intrinsic MOSFET capacitances and a possibility of characterizing interterminal capacitors even in the presence of layout parasitics [12]. An example of a SiC MOSFET cell simulated in the Synopsys Sentaurus TCAD package is shown in Fig. 2(c), where the source, drain, and gate contacts correspond to the terminals of the compact model shown in Fig. 2(b). The base contact (electrically connected to the source contact) in TCAD simulations is used to extract the current between drain and source not flowing via the channel, which would most closely correspond to $I_{\rm Cds}$ in the compact model.

Starting from a calibrated TCAD model of a commercially available SiC power MOSFET developed in-house [13], the main aim of this article is to evaluate the accuracy of power MOSFET compact models commonly used in power electronics for predictive modeling of fast switching operation, distinguishing the impact of the device *C-V* modeling, the *I-V* modeling, and the circuit layout modeling. The simplifications such as, e.g., constant gate-source capacitance [10] and single-voltage dependent OFF-state gate-drain and drain-source capacitance [3], [4] available in datasheets, are evaluated with respect to modeling accuracy. Namely, the impact of these simplifications on predicting the device dynamic performance is investigated in detail using several compact models with different *C-V* settings. The results shown in this article increase the knowledge about the errors associated with the simplified models of power MOSFETs, which has not been addressed in literature in a comprehensive way until now.

The rest of this article is organized as following. Section II presents a comprehensive literature survey on the characterization of MOSFET capacitances, pointing towards numerical semiconductor device modeling as a useful tool to avoid the side-effects introduced by measurement equipment and to evaluate the accuracy of compact models in a more comprehensive way. TCAD modeling of power MOSFET *C-V*s are then explained in Section III using an example of 1.2 kV, 80 mΩ planar-gate SiC power MOSFET. In Section IV, MATLAB-Simulink switching simulations based on a three interterminal capacitance model with *C-V* and *I-V* look-up tables extracted from the proposed TCAD device simulations are presented and compared to the TCAD switching simulations. A comprehensive analysis of commonly adopted modeling assumptions for MOSFET capacitances is performed by comparing TCAD device simulations of switching transients and the MATLAB Simulink simulation results for the varied MOSFET capacitance models. In Section V, the simulation results of the switching transients are compared with the experimental results from double-pulse test (DPT) measurements of the same 1.2 kV, 80 mΩ SiC power MOSFET, confirming the challenges of predicting the fast switching performance of power semiconductor devices accurately. Finally, the conclusion is summarized in Section VI.

II. MOSFET Capacitances Characterization: State-of-the-Art

The distributed intrinsic MOSFET capacitances are typically characterized by a three interterminal capacitance model, i.e., three differential capacitors connected between the gate (g), drain (d), and source (s) terminals, $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$. These interterminal capacitors are voltage dependent and their behavior is governed by the p-n semiconductor junctions within the device cell structure and/or the oxide-semiconductor interfaces. As illustrated in Fig. 3, the drain-source terminal capacitance $C_{\rm ds}$ is mainly determined by the junction between p+ well (body region) and n-drift layer. The gate-source capacitance $C_{\rm gs}$ is formed by the oxide capacitances between gate and source electrodes ($C_{\rm ov2}$), between the gate electrode and the source n+ contact ($C_{\rm ov1}$), between the gate electrode and the

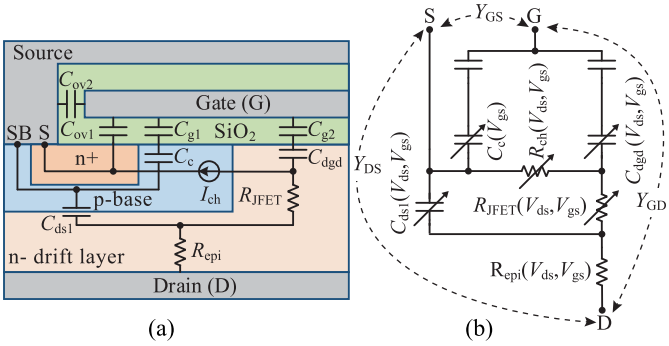

Fig. 3. (a) MOSFET structure schematic with a simplified model of MOSFET capacitances, and (b) a simplified small-signal electrical circuit of distributed resistances and capacitances of a SiC power MOSFET describing the voltage-dependent behavior of small-signal complex admittances $Y_{\rm gs}$, $Y_{\rm gd}$, and $Y_{\rm ds}$.

channel ($C_{\rm g1}$), as well as the semiconductor capacitance of p well ($C_{\rm c}$) depending on the applied terminal voltages. Finally, the gate-drain capacitance $C_{\rm gd}$ consists of the MOS interface capacitance between the gate electrode ($C_{\rm g2}$) and the JFET area and the semiconductor capacitance of JFET area ($C_{\rm dgd}$), i.e., a depletion capacitance depending on the applied terminal voltages, connected in series.

The measurements of the OFF-state *C-V* characteristics, ($C_{\rm iss}$, $C_{\rm oss}$, $C_{\rm rss}$), are commonly performed using semiconductor curve tracers [14], [15]. It has been shown in literature that $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are dependent on both terminal voltages: $V_{\rm gs}$ and $V_{\rm ds}$ [6], [8], [9], [16]–[18]. The standard curve tracers such as a Keithley Parametric Curve Tracer 2600-PCT-4B [15] and a Keysight B1505 A with integrated ultrahigh-current unit [14], enable pulse-based measurements at high voltage bias and current conduction [2]. However, they have limited output range, i.e., the Keithley 2600-PCT-4B and the Keysight B1505 A have the limitations of 40 V/100 A/4 kW and 60 V/1500 A/22.5 kW, respectively, and hence, they cannot be used to extract $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ for all operating points. To the authors' best knowledge no commercial curve tracer systems exists that allows capacitance characterization of a 1.2 kV SiC power MOSFETs in all operating points, e.g., during the switching transients at the nominal dc voltage of 800 V. Therefore, the verification of capacitance models is frequently shown only for the OFF-state *C-V* characteristic measurements, as, e.g., in [19], and extended measurements [8], [9] are required to characterize the MOSFET terminal capacitance for the operating points ($V_{\rm gs}$, $V_{\rm ds}$) during the device ON-state.

In [8], S-parameter measurements of three-terminal WBG power devices using custom-designed bias tees were employed to extract the nonlinear voltage dependence of $C_{\rm gs}$ and $C_{\rm gd}$. These *C-V* measurements require a precise synchronization between a current pulse and the capacitance measurement units. The most challenging part is to select a low measurement frequency (in order to avoid the effects of package parasitics) and keep the duration of the current pulse as short as possible to avoid the self-heating. The *C-V* measurements in [8] were performed at 1 MHz, which does not allow the package parasitics to be fully avoided. A compact behavioral model of SiC power MOSFETs was proposed in [9], where S-parameter measurements were used to parameterize the capacitance model $C_{\rm gs}(V_{\rm gs}, V_{\rm ds})$ and $C_{\rm gd}(V_{\rm gs}, V_{\rm ds})$. The bias tees used to measure S-parameters of ON-state SiC MOSFETs in [9] were designed to a maximum current of 2 A, which limited the parameter extraction up to $V_{\rm gs} \approx 6$ V. When using the S-parameter measurements, the influence of parasitics at higher frequencies has to be considered either by de-embedding the S-parameters of the package from the measurement results [9] or by performing the measurements at frequencies below 1 MHz [20]. Another approach of extracting the nonlinear voltage dependence of power MOSFET's $C_{\rm gs}$ and $C_{\rm gd}$ is by means of the dynamic *I-V* waveforms [5], [10], [17], [21]. In comparison to Si-IGBTs, the gate-source voltage $V_{\rm gs}$ of Si-super junction (SJ) and SiC power MOSFETs is nonconstant during the so-called Miller phase of the switching transients, i.e., the phase characterized by the change of the drain-source voltage $V_{\rm ds}$ [10], [22]. The nonconstant $V_{\rm gs,Miller}$, neglected in certain compact models [5], makes the extraction of nonlinear $C_{\rm gd}$ based on the switching transients more challenging, as described in [23]. In [10], dynamic *C-V* characteristics of SJ Si-MOSFETs are calculated from the gate-charge curves measured by a DPT setup, assuming constant $C_{\rm gs}$. In [21], MOSFET interterminal capacitances were characterized by current and voltage measurements of the device using a closed-loop gate control to ensure constant $V_{\rm gs}$ during the $\mathrm{d}V_{\rm ds}/\mathrm{d}t$ voltage commutation.

The extraction of *C-V* characteristics from the dynamic *I-V* waveforms relies on an accurate interpretation of the measurement results influenced by the layout and package parasitics. The accuracy of fast switching measurements for WBG power devices strongly depends on the bandwidth of current and voltage probes, as well as deskewing of the probes [24]–[26]. Therefore, the measurements of fast switching transients and time-delays between $V_{\rm ds}(t)$, $V_{\rm gs}(t)$, and $I_{\rm d/s}(t)$ signals suffers from inaccuracies, which are hard to avoid. Furthermore, the measurement effects are superimposed to the device and layout effects, and hence, hard to be distinguished. Switching loss energies should be ideally determined individually for each combination of power devices, gate driver unit, and power circuit layout. Calorimetric measurement setups represent a way to measure the switching and conduction losses of fast switching power devices with the relative error as high as 15%, which is significantly better than the DPT measurements [27].

In contrast to compact device models, numerical simulation of semiconductor devices in TCAD tools provides a more accurate modeling of device physics, and a deeper insight into the device performance, which can neither be gained accurately by DPT nor by calorimetric measurements. The 2-D and 3-D TCAD simulations of a single device cell are typically performed to predict and evaluate device performance. While 3-D TCAD simulations can capture the device physics more accurately for certain device geometries [28], 2-D TCAD simulations are computationally less expensive and frequently provide a good approximation of device physics. Mixed-mode TCAD simulations coupling 2-D device models of fast and slow switching super-junction Si-MOSFETs with a broadband electromagnetic (PCB and package) layout model were presented in [11] for the first time. Even though highly computationally demanding, the TCAD mixed-mode simulations including an active MOSFET cell with a

termination structure provide a highly valuable information how accurate the device power losses can be estimated based on the TCAD modeling tools in comparison to the measurements.

In the following section, a detailed insight into the interterminal capacitances of a planar-gate SiC power MOSFET using TCAD simulations is presented. Here, TCAD device modeling allows us a more precise verification of the standard three interterminal MOSFET capacitance model and a separation of the effects originating from measurement probes, circuit layout, and the power MOSFET itself.

III. MOSFET Capacitance Extraction Using 2-D TCAD Modeling

Based on in-house investigations and a re-engineering report of a commercial 1.2 kV, 80 mΩ planar-gate SiC power MOSFET (C2M0080120D) [29], [30], a 2-D TCAD model of a half-device active cell [31] was developed using the Synopsys Sentaurus TCAD package, i.e., Sentaurus Device (S-Device) and Process simulators. The 2-D TCAD model was calibrated to match the *I-V* and *C-V* device characteristics as close as possible, while observing the performance variation between several C2M0080120D devices. A more detailed description of the MOSFET structure shown in Fig. 2 was presented in [13].

The proposed TCAD simulations showed that during fast switching transients both at turn-ON and turn-OFF, the maximum temperature increase within the device is less than 5 K, if self-heating is considered in the simulation setup, which was also reported in [10]. Hence, the influence of self-heating on *I-V* device waveforms during fast switching transients (i.e., high measurement frequencies) can be neglected. Accordingly, the TCAD simulations and all investigations presented in this article were performed at the same constant temperature (namely, a standardized room temperature of 300 K). The internal gate resistance is modeled by an external resistor $R_{\mathrm{g,int}}$, while the inductors L_{g}, L_{ks}, L_{s}, L_{d}, L_{diode}, and L_{ext} represent the layout and package parasitics. The resistors R_{Lg}, R_{Lks}, R_{Ls}, and R_{Ld} are used to model the frequency behavior of stray inductances L_{g}, L_{ks}, L_{s}, and L_{d}, respectively (cf., Fig. 4).

The small signal interterminal *C-V* characteristics were extracted from the S-Device mixed-mode simulations at a frequency of $f_1 = 10$ MHz by applying a quasi-stationary V_{ds} ramp at fixed V_{gs} directly at G-S, D-S and G-D ports of the MOSFET die, as shown in Fig. 4. The small signal TCAD extraction of *C-V*s is performed by applying an ac voltage source at one terminal, while the two other terminals are connected to the ac ground. The values of the differential capacitors C_{gs}, C_{gd}, C_{ds} are calculated from the small signal complex admittances Y_{gs}, Y_{gd}, and Y_{ds} determined at the G-S port, the G-D port, and the D-S port, respectively. The extracted values of interterminal MOSFET capacitors are shown in Fig. 5. In Fig. 5(a)–(d), it can be observed that C_{gs}, C_{gd}, and C_{ds} are functions of both V_{ds} and V_{gs}, which can be explained by a simplified circuit of distributed resistance and capacitance of a power MOSFET, as shown in Fig. 3(b) following the analysis presented in [21]. For very low V_{gs}, $V_{\mathrm{gs}} = [-10, -5]$ V, the channel region in the p-base and the n-type JFET region are enriched by holes. The

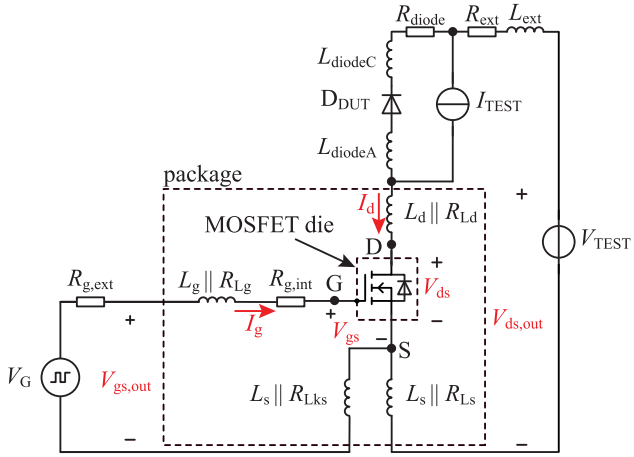

Fig. 4. Double-pulse test circuit used to analyze the dynamic MOSFET capacitance. MOSFET die represents a MOSFET model without the resistance of poly-silicon gate, which is in turn modeled by $R_{\mathrm{g,int}}$. Namely, the MOSFET models from MATLAB Simulink and S-Device TCAD simulator are connected in the circuit between the G, D, and S points.

gate-voltage dependence of C_{gs} and C_{gd} of SiC power MOSFETs was explained in [32]. With the increase of V_{gs}, the channel region first goes into depletion reducing C_{c} and leading to a very large value of R_{ch} (separating C_{c} from C_{dgd}), and then into inversion at around threshold voltage $V_{\mathrm{th}} = 3.2$ V. By further increasing V_{gs}, the channel inversion enhances, leading to an increase of C_{c} and decrease of R_{ch}. The C_{dgd} starts increasing due to a higher electron concentration at the SiC/SiO_2 interface at the top of the n-type JFET region attracted by a positive gate potential. The depletion of electrons in the n-type JFET region results in the reduction of C_{dgd} and is influenced by both V_{ds} and V_{gs}. This depletion leads to an increase of voltage-dependent resistance R_{JFET}. With increasing V_{ds}, the effective gate-source threshold voltage V_{th} reduces due to the drain-induced barrier lowering, i.e., the short-channel effect, which can be described by a reduction in R_{ch} and an increase in C_{c}. The ratio $R_{\mathrm{ch}}/(R_{\mathrm{jfet}}+R_{\mathrm{epi}})$ determines the portions of C_{dgd}, which can be attributed to C_{gs} and C_{gd}. Accordingly, the admittances Y_{gs}, Y_{gd}, Y_{ds} depend on the charge distribution in the JFET region and the channel, leading to the voltage-dependent behavior of the extracted (C_{gs}, C_{dg}, C_{ds}) values, as shown in Fig. 5(a)–(d). It should be noted that C_{ds} is extracted by applying the ac voltage source to the source terminal and connecting the gate and drain terminals to the ac ground. In the other configuration, i.e., the ac voltage source connected to the drain terminal, C_{ds} cannot be directly extracted from the small-signal TCAD simulations at $f_1 < 1$ GHz for a $V_{\mathrm{gs}} > V_{\mathrm{th}}$, due to the presence of the open channel, which leads to a negative and oscillating imaginary part of the simulated Y_{ds}.

Traps located at the SiC/SiO_2 interface can strongly affect both *I-V* and *C-V* characteristics of a SiC MOSFET. The traps are included in the proposed TCAD simulations based on the method presented in [33] and [34] for modeling the influence of interface traps on *I-V* device characteristics of 4H-SiC power MOSFETs. The model parameters describing the trap distribution are calibrated such that a very close match between the measured

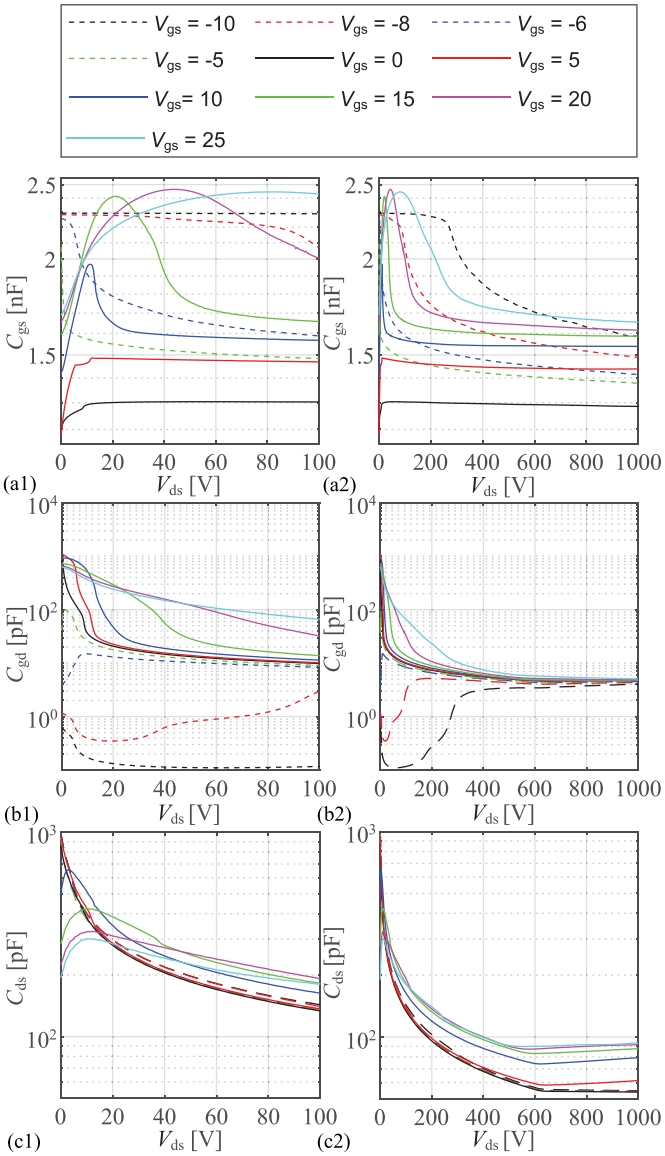

Fig. 5. *C-V* characteristics computed by quasi-static TCAD S-Device mixed-mode simulations of a 1.2 kV, 80 mΩ planar-gate SiC power MOSFET: (a) C_{gs}, (b) C_{gd}, (c) C_{ds} for 1) low V_{ds}, and 2) for high V_{ds} at V_{gs} equals −10 V, −8 V, −6 V, −5 V, 0 V, 5 V, 10 V, 15 V, 20 V, and 25 V.

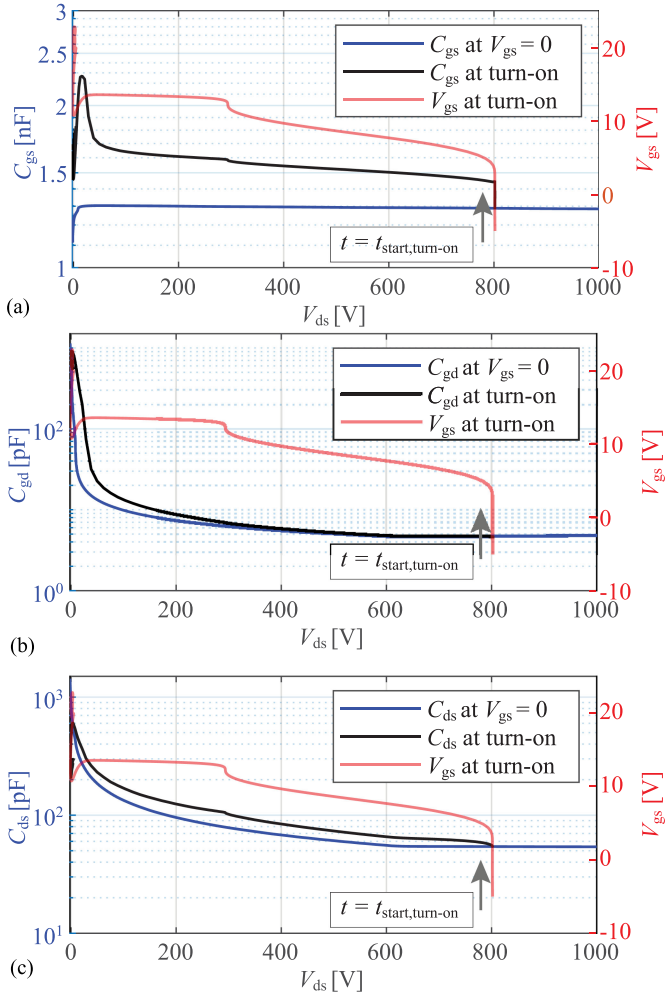

Fig. 6. *C-Vs* for $V_{gs} = 0$ and the trajectories of V_{gs} and *C-Vs* during the turn-ON switching transients computed by transient TCAD S-Device mixed-mode simulations of a 1.2 kV, 80 mΩ planar-gate SiC power MOSFET: (a) C_{gs}, (b) C_{gd}, and (c) C_{ds}. The arrows show the direction of V_{gs} change, while the turn-ON transient starts at the time point t equals $t_{start,turn\text{-}ON}$.

and simulated *I-V* curves was achieved. The model is based on an assumption of acceptor levels with a Gaussian type energy distribution $N_0 e^{-(E-E_0)^2/(2E_s^2)}$, where E is the energy of the level; the mean of the distribution E_0 is located at the minimum of 4H-SiC conduction band, i.e., $E_0 = E_c$; the standard deviation $E_s = 0.11$ eV; N_0=2e13 cm^{-2} eV^{-1}; and both electron and hole capture cross sections are equal to 1e-14 cm^{-2}. Employing these parameters, a significant frequency dependence of the interterminal MOSFET capacitances extracted by means of the developed TCAD MOSFET model in the frequency range up to 500 MHz has not been found, i.e., the frequency dependence was negligible within this study.

The impact of including a termination region in the TCAD simulation on the extracted switching loss for SiC MOSFETs with different die areas was investigated in [35]. There, it was shown that the termination area capacitance did only have a noticeable influence on the switching loss at low drain current. For commercial SiC power MOSFETs operated at nominal currents (this study), the impact of termination is not found to be significant.

An advantage of TCAD mixed-model simulations is the extraction of dynamic small-signal C_{gs}, C_{gd}, and C_{ds} during the turn-ON/OFF switching transients. The TCAD transient mixed-mode setup based on a DPT circuit as presented in Fig. 4 was used to simulate the dynamic switching behavior of a SiC power MOSFET. The current commutation between the SiC power MOSFET and a SiC Schottky diode [36] was simulated to extract the dynamic MOSFET capacitance at turn-ON and turn-OFF switching transients. The trajectories of C_{gs}, C_{gd}, and C_{ds} as functions of V_{ds} during turn-ON and turn-OFF for $V_{TEST} = 800$ V and $I_{TEST} = 20$ A are shown in Figs. 6 and 7, respectively, together with C_{gs}, C_{gd}, and C_{ds} for $V_{gs} = 0$, which can be typically obtained from datasheet values. It can be observed that during dV_{ds}/dt transient, i.e., the Miller phase, V_{gs} is changing from 5 to 12 V and, hence, cannot be assumed constant. In nominal

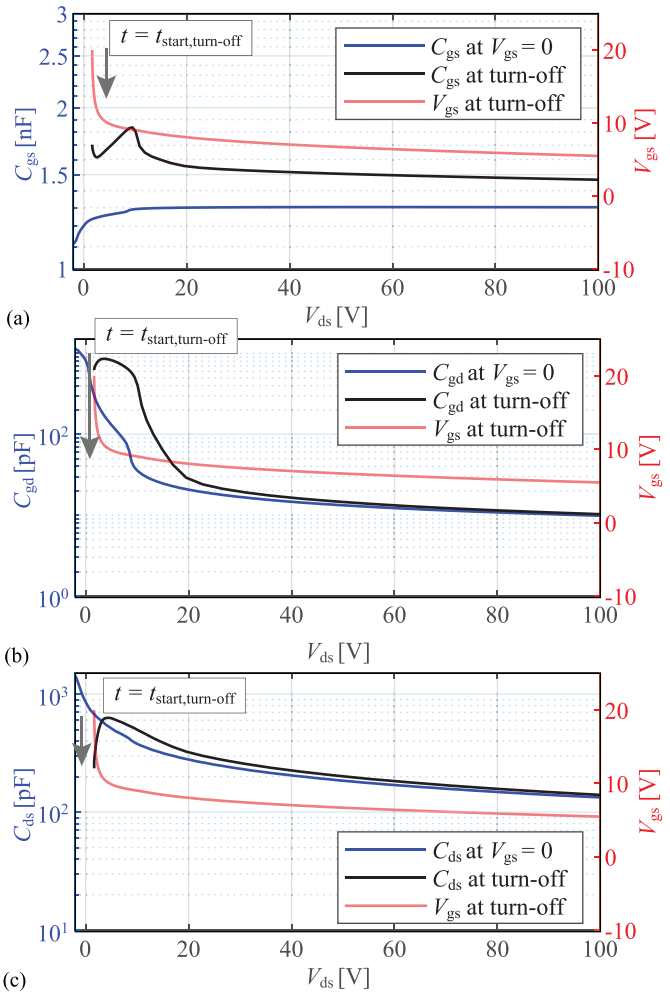

Fig. 7. *C-V*s for $V_{gs} = 0$ and the trajectories of V_{gs} and *C-V*s during the turn-OFF switching transients computed by transient TCAD S-Device mixed-mode simulations of a 1.2 kV, 80 mΩ planar-gate SiC power MOSFET: (a) C_{gs}, (b) C_{gd}, and (c) C_{ds}. The arrows show the direction of V_{gs} change, while the turn-OFF transient starts at the time point t equals $t_{\text{start,turn-OFF}}$. The *x*-axis, V_{ds}, is limited to 100 V to better visualize the nonlinear C-V behavior at lower voltages.

operation, operating points such as low V_{ds} and low $V_{gs} < V_{th}$, or high V_{ds} and high $V_{gs} \approx V_G$, never occur. The importance of the nonlinear behavior of C_{gs}, C_{gd}, and C_{ds} for correctly modeling the ohmic switching losses, the current and voltage delays, as well as the voltage and the current slopes, is shown in more detail in the following section.

IV. Three Interterminal Capacitance Compact Model of SiC Power MOSFETs

In this section, the 2-D TCAD simulation results are used to investigate the accuracy of well-established compact models of SiC power MOSFETs based on the three interterminal capacitance model with commonly adopted simplifications such as, e.g., constant C_{gs} [10], single-voltage dependent $C_{gd}(V_{gd})$ and $C_{ds}(V_{ds})$[3], [4]. A MATLAB Simulink MOSFET model, shown in Fig. 1 is developed by representing the *C-V* and *I-V* device characteristics as look-up tables extracted from the quasi-stationary TCAD MOSFET simulations described in Section III. The *C-V* look up tables were derived from TCAD data for $V_{gs} = [-20, +30]$ V with ΔV_{gs} step of 1 V, $V_{ds} = [-2, +100]$ V and ΔV_{ds} step of 0.5 V, $V_{ds} = [100, +1000]$ V and ΔV_{ds} step of 10 V, while the *I-V* look-up table was derived for $V_{gs} = [0, +30]$ V with ΔV_{gs} step of 0.2 V, and $V_{ds} = [-2, 1000]$ V with variable ΔV_{ds} steps from minimum 0.05 V at low V_{ds} to maximum 100 V at higher V_{ds}. A spline interpolation is used to extract C_{gs}, C_{gd}, and C_{ds} values at different operating points (V_{ds}, V_{gs}) in MATLAB Simulink. By adding additional (V_{ds}, V_{gs}) points in the *C-V* and *I-V* look-up tables, no improvements in the simulation results were observed.

The complexity of look-up tables is determined by interpolation algorithms and size of look-up tables [37]. In the presented simulations, the size of the *C-V*s is quite large in order to maintain high precision of the interpolated values. It was observed that the simulation time of switching transients when using the two-voltage dependent *C-V*s, $C(V_{gs}, V_{ds})$, is longer than when using the single-voltage dependent *C-V*s, $C(V_{gs}{=}0, V_{ds})$. Moreover, the Spice-based simulations shown in [25] shows better computational performance than the MATLAB Simulink simulations. In this article, the simulation time is not prioritized and the main focus is placed on the simulation accuracy, mainly on a quantitative determination of the errors made by employing specific modeling simplifications for predicting the dynamic behavior of fast switching power semiconductor devices such as SiC power MOSFETs, as shown below.

In experimental double-pulse switching measurements, only the total drain current I_d, the gate current I_g, the outer drain-source $V_{ds,out}$, and gate-source $V_{gs,out}$ voltages of a packaged device are measured, and the switching power losses are then determined as $P_{out} = I_d \cdot V_{ds,out}$. From a three interterminal capacitance model and the knowledge of package parasitics, the channel current, i.e., the current of $R_{ds,ON}$, and the internal voltage across the device can be accessed, so that it is possible to calculate the ohmic switching power losses as $P_{ch} = I_{ch} \cdot V_{ds}$.

The ohmic switching losses can be calculated in TCAD simulations as total power losses related to the current density and electric field across the MOSFET active cell. The ohmic switching losses calculated in this way comprise the heat generated in the distributed resistance within the MOSFET structure, which is not included in a three interterminal capacitance compact model, as shown in Fig. 1. On the other hand, total heat generated during a switching transient, which can be calculated in TCAD simulations, comprises not only ohmic (Joule) heat but as well as recombination-generation heat and Thomson–Peltier heat. The differences between the TCAD model and the three interterminal capacitance compact model with respect to the ohmic switching losses and the total heat losses will be addressed in a future publication in more detail.

A. SIMREF: TCAD versus MATLAB Simulink Simulations of Fast Switching Transients

The DPT circuit shown in Fig. 4 with the look-up table-based MOSFET model is implemented in MATLAB Simulink to compare the switching waveforms gained from the MATLAB-Simulink and the corresponding TCAD-mixed-mode

simulations. The fast switching transients are achieved by a small internal gate resistor $R_{\mathrm{g,int}}$ of 0.1 Ω, a $R_{\mathrm{g,ext}}$ of 2.5 Ω, and decoupled gate and power loops via a Kelvin source modeled by L_{ks} and R_{Lks}. In Figs. 8 and 9, a comparison between the TCAD mixed-mode simulations (using the MOSFET model shown in Fig. 2) and the MATLAB-Simulink simulations of the fast switching turn-ON and turn-OFF waveforms are shown for $I_{\mathrm{TEST}} = 20$ A and $V_{\mathrm{TEST}} = 800$ V. In the simulations, the turn-ON starts at the time $t_{\mathrm{start,turnON}} = 6\,\mu$s, while the turn-OFF starts at the time $t_{\mathrm{start,turnOFF}} = 1\,\mu$s. A very good matching between the simulation results is achieved, however, small differences between I_{Cds} and $I_{\mathrm{b,TCAD}}$ are visible that can be explained by the difference between the lumped and the distributed base resistance and capacitance: in MATLAB Simulink, the base current is modeled as I_{Cds}, while in the TCAD-mixed-mode simulation it is measured via the p-base contact at the half-cell level and later summed up using the active area scaling. No significant change of the simulated switching curves is observed by adding a resistor $R_{\mathrm{ds}} =$ 30-100 mΩ in series to C_{ds} in the MATLAB-Simulink MOSFET model. For slower switching transients, e.g., $R_{\mathrm{gg}} = 10\,\Omega$ and/or without a Kelvin source, the base current is lower and the influence of distributed base resistance and capacitance on the switching waveforms is less pronounced.

The simulations adopting certain assumptions are verified by comparing the prediction of total switching energy losses $E_{\mathrm{loss,out}}$, of ohmic switching energy losses $E_{\mathrm{loss,ch}}$, voltage $t_{\mathrm{delay,V}}$ and current $t_{\mathrm{delay,I}}$ delay, and the voltage $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ and current $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ rate of change. The signal (voltage or current) delay is calculated as a time interval from the beginning of switching event, i.e., $t = t_{\mathrm{start,turn\text{-}OFF}}$ or $t = t_{\mathrm{start,turn\text{-}ON}}$ to the time point when signal reaches 10% or 90% of V_{TEST} or I_{TEST}, depending on the switching transient. The signal rate of change is calculated as $\Delta X/t_{j\%-k\%}$, where $t_{j\%-k\%}$ is the time interval during which the signal changes from j % to k % of X_{TEST}, and $\Delta X = |X_1 - X_2|$, where $X_1 = j\%X_{\mathrm{TEST}}$ and $X_2 = k\%X_{\mathrm{TEST}}$, and $j, k =$ 10 or 90, while X represents either current or voltage. For example, for turn-OFF, during $t_{\mathrm{V,10\%-90\%}}$, V_{ds} changes from $V_1 = 10\%V_{\mathrm{TEST}}$ to $V_2 = 90\%V_{\mathrm{TEST}}$, while for turn-ON, during $t_{\mathrm{V,90\%-10\%}}$, V_{ds} changes from $V_1 = 90\%V_{\mathrm{TEST}}$ to $V_2 = 10\%V_{\mathrm{TEST}}$. The switching energy losses are calculated as $\int_{t_1}^{t_2} I \cdot V\mathrm{d}t$, where t_1 and t_2 are determined according to the convention typically specified in datasheets, e.g., in [38].

The energy losses at the turn-ON $E_{\mathrm{loss,out}}$ $(= \int_{t_1}^{t_2} I_{\mathrm{d}} \cdot V_{\mathrm{ds,out}}\mathrm{d}t)$ calculated in the TCAD and MATLAB Simulink simulations are 107 and 108 μJ, respectively, which is a difference of less than 1%. For the turn-OFF transient, $E_{\mathrm{loss,out}}$ calculated in the TCAD and MATLAB Simulink simulations are 26.3 and 26.4 μJ, respectively, which is a difference of less than 1%. It should be noted that the device channel current is switched off very fast via a small gate resistance, and it drops to zero before a fast rise of the voltage across the device, which in turn leads to very low ohmic turn-OFF switching losses $E_{\mathrm{loss,ch}} = \int_{t_1}^{t_2} I_{\mathrm{ch}} \cdot V_{\mathrm{ds}} = 0.79\,\mu$J. Accordingly, I_{d} and $V_{\mathrm{ds,out}}$ measured in the standard DPT experiments of fast switching transients and used to calculate $E_{\mathrm{loss,out}}$ cannot be used to correctly evaluate

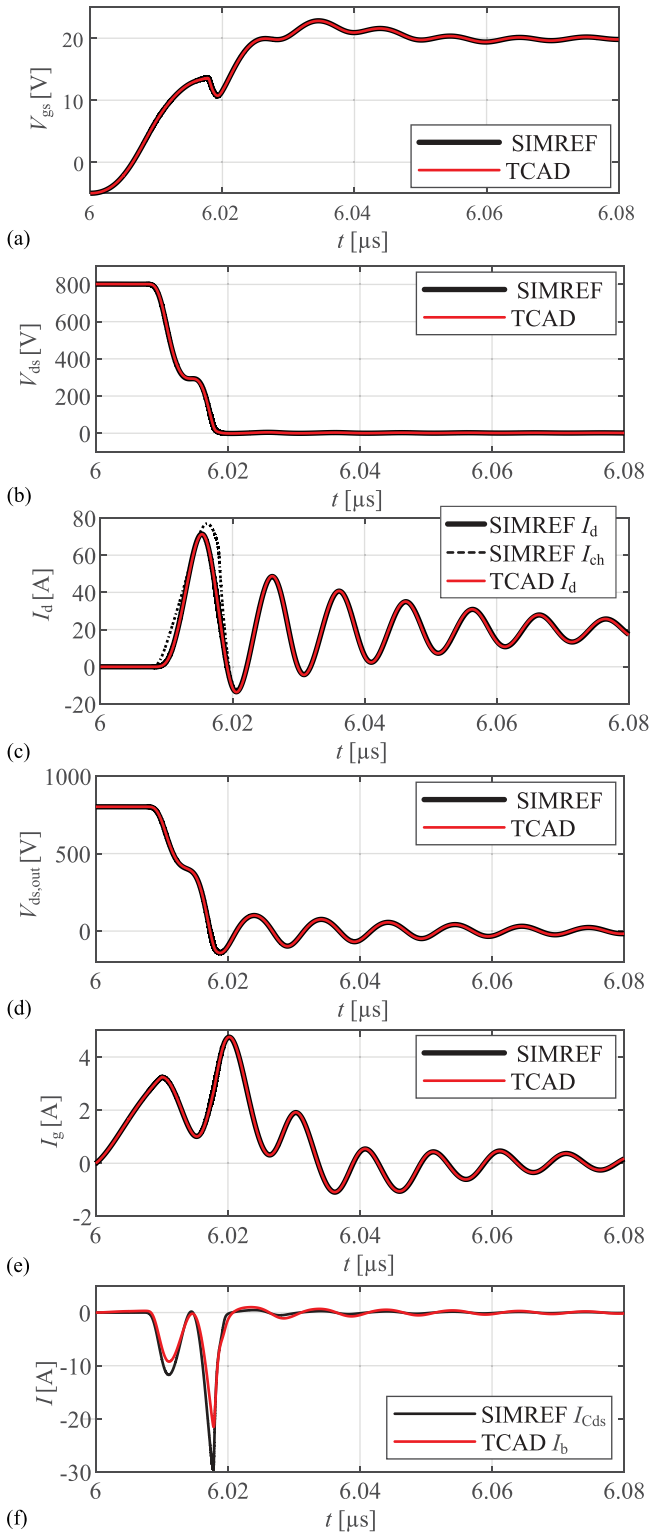

Fig. 8. Comparison between turn-ON fast switching waveforms gained from the TCAD mixed-mode simulations and the MATLAB Simulink simulation, SIMREF, with the look-up table-based MOSFET model using the DPT circuit shown in Fig. 4: (a) gate-source voltage V_{gs}, (b) the drain-source voltage V_{ds}, (c) the drain current I_{d}, (d) the outer drain-source voltage $V_{\mathrm{ds,out}}$, (e) the gate current I_{g}, (f) the base current $I_{\mathrm{b,TCAD}}$ from the TCAD simulation together with the drain-source capacitor current, I_{Cds} from MATLAB Simulink, cf., Figs. 1 and 2.

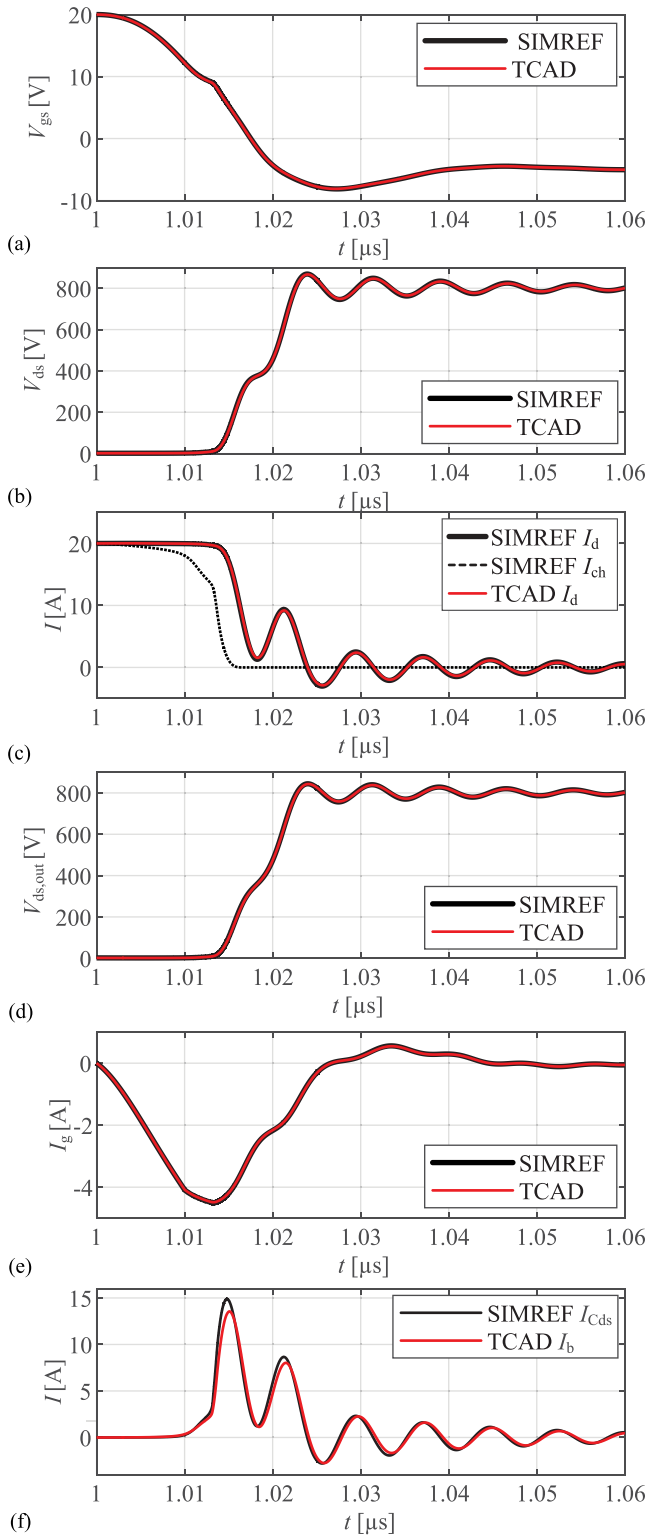

Fig. 9. Comparison between turn-OFF fast switching waveforms gained from the TCAD mixed-mode simulations and the MATLAB simulation, SIMREF, with the look-up table-based MOSFET model using the DPT circuit shown in Fig. 4: (a) the gate-source voltage V_{gs}, (b) the drain-source voltage V_{ds}, (c) the drain current I_d, (d) the outer drain-source voltage $V_{ds,out}$, (e) the gate current I_g, (f) the base current $I_{b,TCAD}$ from the TCAD simulation together with the drain-source capacitor current, I_{Cds} from MATLAB Simulink, cf., Figs. 1 and 2.

TABLE I
DESCRIPTION OF THE MATLAB SIMULINK SIMULATIONS PERFORMED USING DIFFERENT *C-V* MODELS

SIM	C_{gs}	C_{gd}	C_{ds}
SIMREF	(V_{gs}, V_{ds})	(V_{gs}, V_{ds})	(V_{gs}, V_{ds})
SIM2	off-state $(V_{gs} = 0, V_{ds})$	off-state $(V_{gs} = 0, V_{ds})$	off-state $(V_{gs}= 0, V_{ds})$
SIM3	(V_{gs}, V_{ds})	(V_{gs}, V_{ds})	off-state $(V_{gs} = 0, V_{ds})$
SIM4	off-state $(V_{gs}= 0, V_{ds})$	(V_{gs}, V_{ds})	off-state $(V_{gs} = 0, V_{ds})$
SIM5	constant $(V_{gs} = 0, V_{ds} = V_{test})$	off-state $(V_{gs} = 0, V_{ds})$	off-state $(V_{gs} = 0, V_{ds})$
SIM6	constant $(V_{gs} = 0, V_{ds} = V_{test})$	off-state $(V_{gs} = 0, V_{ds})$	constant $(V_{gs} = 0, V_{ds} = V_{test})$

the turn-OFF switching losses, i.e., $E_{loss,ch} \ll E_{loss,out}$. From the $E_{loss,out}$ calculation, and the waveforms shown in Figs. 8 and 9, it can be concluded that a compact model based on the three interterminal capacitance model can be used to represent the dynamic switching behavior of TCAD's planar-gate SiC power MOSFETs with high precision, if two-voltage (V_{gs}, V_{ds}) dependent *C-V* device characteristics are used. This MATLAB Simulink simulation, marked as SIMREF, is taken then as a reference simulation for the following analysis. Namely, five more simulations, SIM2-SIM6, described in Table I, were performed in MATLAB Simulink to analyze the impact of the assumptions typically used in literature. The results are shown in Section IV-B to IV-F.

B. SIM2: Effect of the OFF-State C-V Characteristics

Using the circuit shown in Fig. 4, the switching transient simulation SIM2 based on single-voltage dependent *C-V*s, i.e., the OFF-state $C_{gs}(V_{ds}, V_{gs} = 0)$, $C_{dg}(V_{ds}, V_{gs} = 0)$, $C_{ds}(V_{ds}, V_{gs} = 0)$, is verified starting from the reference simulation SIMREF, which employs the look-up table-based $C_{gs}(V_{ds}, V_{gs})$, $C_{gd}(V_{ds}, V_{gs})$, and $C_{ds}(V_{ds}, V_{gs})$. The corresponding MATLAB Simulink simulation results are shown in Figs. 10 and 11 for turn-ON and turn-OFF switching waveforms, respectively, and the comparison between two simulations is summarized in Table II. The results shown in Table II imply the following conclusions: The difference between SIMREF and SIM2 in terms of $\mathrm{d}V_{ds}/\mathrm{d}t$ is $\approx 6\,\%$ for the turn-ON. The assumptions used in SIM2 lead to an error of $13\,\%$ for the estimation of $E_{loss,ch}$, and an error of $7\,\%$ for the estimation of $E_{loss,out}$ for the turn-ON transient. From Fig. 11(e), a difference in the voltage time delay of 3 ns in the case SIMREF and SIM2 can be observed for the turn-OFF. In the DPT measurements, the accuracy of determining the voltage time delay highly depends on deskewing of measurement probes, which can be very challenging in terms of precision. Accordingly, when comparing the measurement results and the simulation results based on the OFF-state *C-V*s, this voltage time delay of 3 ns can be frequently overlooked. At turn-OFF, a significant difference of almost $100\,\%$ between the channel current slopes of SIMREF and SIM2 is observed.

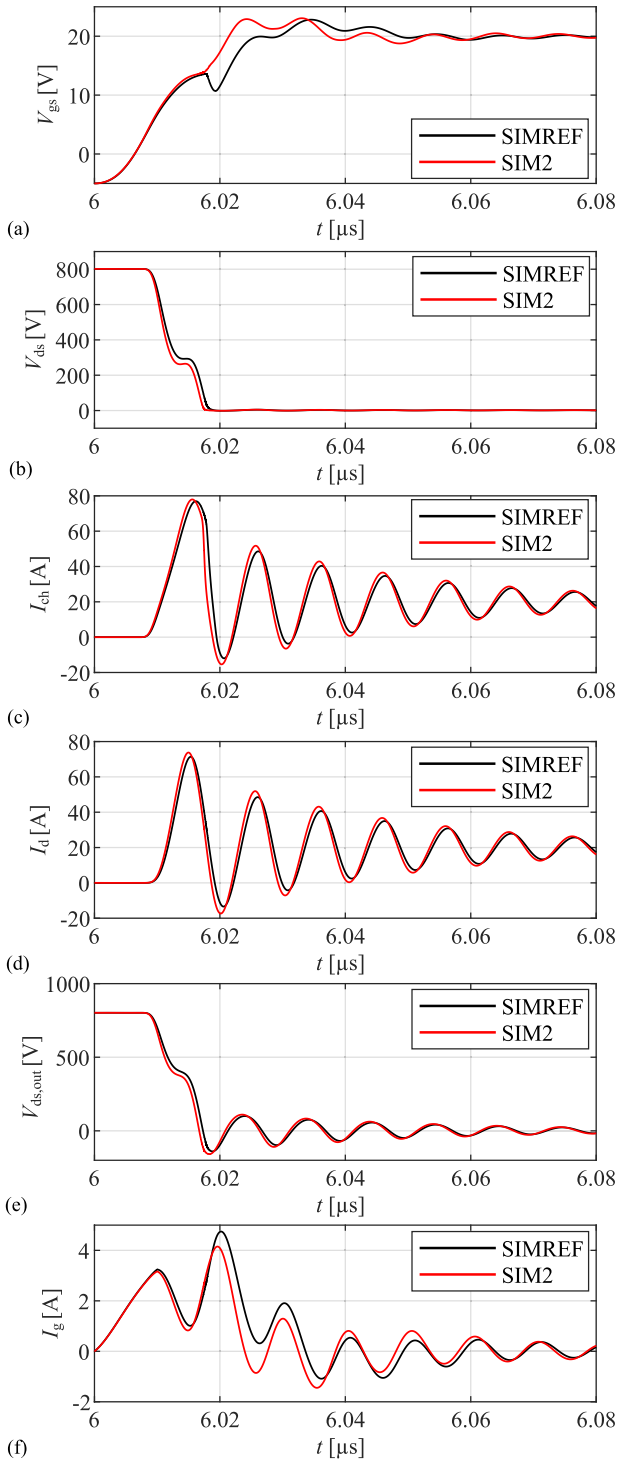

Fig. 10. Comparison of the MATLAB-Simulink simulation results SIMREF and SIM2 for the turn-ON switching transient: (a) V_{gs}, (b) the internal drain-source voltage V_{ds}, (c) the channel current I_{ch}, (d) total drain current I_d, (e) the external drain-source voltage $V_{ds,out}$, and (f) the gate current I_g.

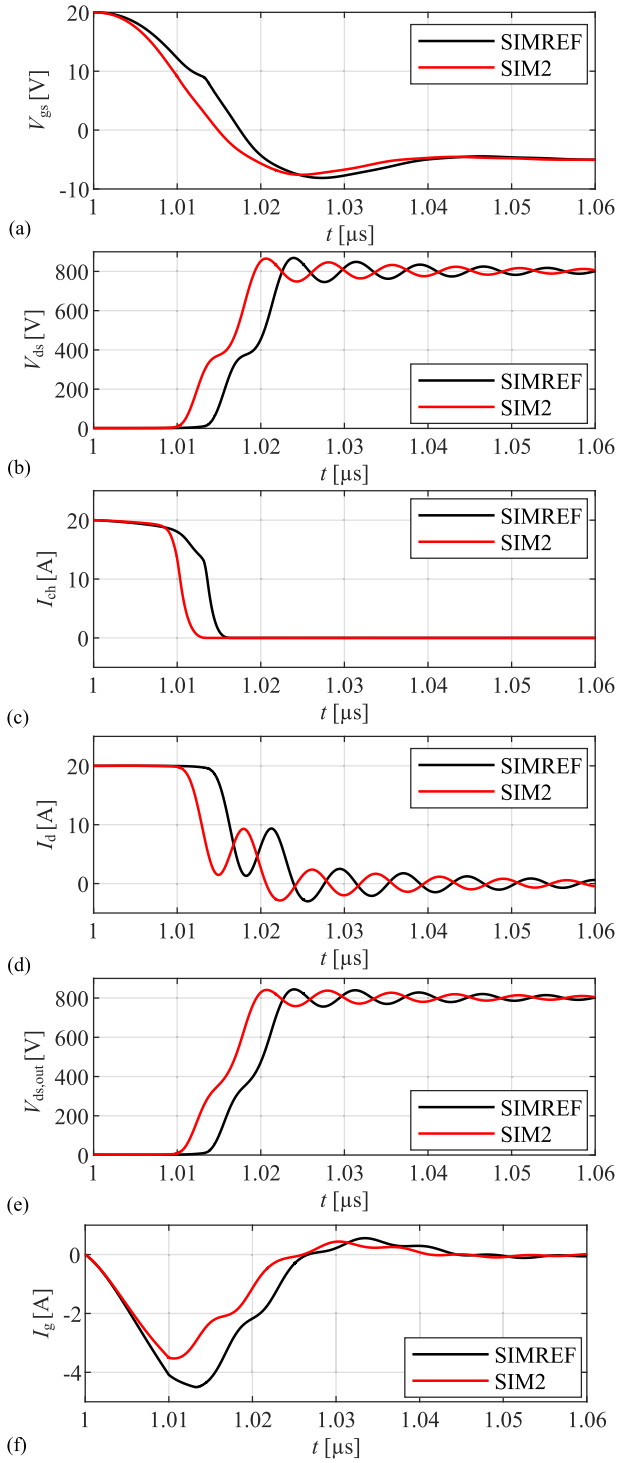

Fig. 11. Comparison of the MATLAB-Simulink simulation results SIMREF and SIM2 for the turn-OFF switching transient: (a) V_{gs}, (b) the internal drain-source voltage V_{ds}, (c) the channel current I_{ch}, (d) total drain current I_d, (e) the external drain-source voltage $V_{ds,out}$, and (f) the gate current I_g.

C. *SIM3: Effect of the OFF-State* $C_{ds}(V_{ds}, V_{gs} = 0)$

The importance of using the $C_{ds}(V_{ds}, V_{gs})$ was evaluated with the third simulation, SIM3, employing dynamic $C_{gs}(V_{ds}, V_{gs})$ and $C_{gd}(V_{ds}, V_{gs})$, and OFF-state $C_{ds}(V_{ds}, V_{gs} = 0)$, comparing the SIMREF and SIM3 simulation results. Differences of $\mathrm{d}V/\mathrm{d}t$, $\mathrm{d}I/\mathrm{d}t$ calculated from the simulation waveforms of SIMREF and SIM3 in the range of maximum 4 % lead to 4% and 0.2% relative error of $E_{loss,ch}$ and $E_{loss,out}$ at turn-ON, respectively. At the turn-OFF, $E_{loss,ch}$ and $E_{loss,out}$ are calculated in the simulation SIM3 with a relative error of 8.9% and 0.4%. Accordingly,

TABLE II
SWITCHING SIMULATION RESULTS COMPARISON: SIMREF VERSUS SIM2

	Turn-on			Turn-off		
Param.	SIMREF	SIM2	$\|\Delta\|$%	SIMREF	SIM2	$\|\Delta\|$%
$\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ [V/ns]	82.71	88.01	6.4	88.35	88.18	0.2
$t_{\mathrm{delay,Vds}}$ [ns]	9.74	9.55	1.9	14.68	11.37	22.5
$\mathrm{d}I_{\mathrm{ch}}/\mathrm{d}t$ [A/ns]	9.03	9.47	4.9	3.4	6.04	77.6
$t_{\mathrm{delay,Ich}}$ [ns]	8.74	8.64	1.1	10.04	9.01	10.2
$E_{\mathrm{loss,ch}}$ [μJ]	123	107	13.0	0.79	0.76	3.8
$E_{\mathrm{loss,out}}$ [μJ]	108	100	7.4	26.36	25.96	1.6
E_{driver} [μJ]	1.3	1	23.1	0.31	0.22	29.0

the dependence of C_{ds} on V_{gs} does not have a significant impact on the generation of switching losses.

D. SIM4: Effect of the OFF-State $C_{\mathrm{gs}}(V_{\mathrm{ds}}, V_{\mathrm{gs}} = 0)$

The effect of $C_{\mathrm{gs}}(V_{\mathrm{ds}}, V_{\mathrm{gs}})$ is assessed by comparing the results from SIMREF and the fourth simulation SIM4, based on $C_{\mathrm{gs}}(V_{\mathrm{ds}}, V_{\mathrm{gs}} = 0)$, $C_{\mathrm{dg}}(V_{\mathrm{ds}}, V_{\mathrm{gs}})$, $C_{\mathrm{ds}}(V_{\mathrm{ds}}, V_{\mathrm{gs}} = 0)$. Using SIMREF as a reference, $E_{\mathrm{loss,ch}}$ and $E_{\mathrm{loss,out}}$ at turn-ON are calculated in SIM4 with a relative error of 12 % and 7 %, respectively, while for the turn-OFF transient, with a relative error of 1.5 % and 0.6 %. At turn off, the difference in the voltage time delay is 0.87 ns, which is smaller than the difference of 3 ns in the case of SIM2. Additionally, the matching between SIMREF and SIM4 with respect to the slope of the channel current is improved to an error of less than 1 % in comparison to SIM2. The waveforms, which are the most affected by the assumption $C_{\mathrm{gs}}(V_{\mathrm{ds}}, V_{\mathrm{gs}} = 0)$ compared to Fig. 11, are shown in Fig. 12.

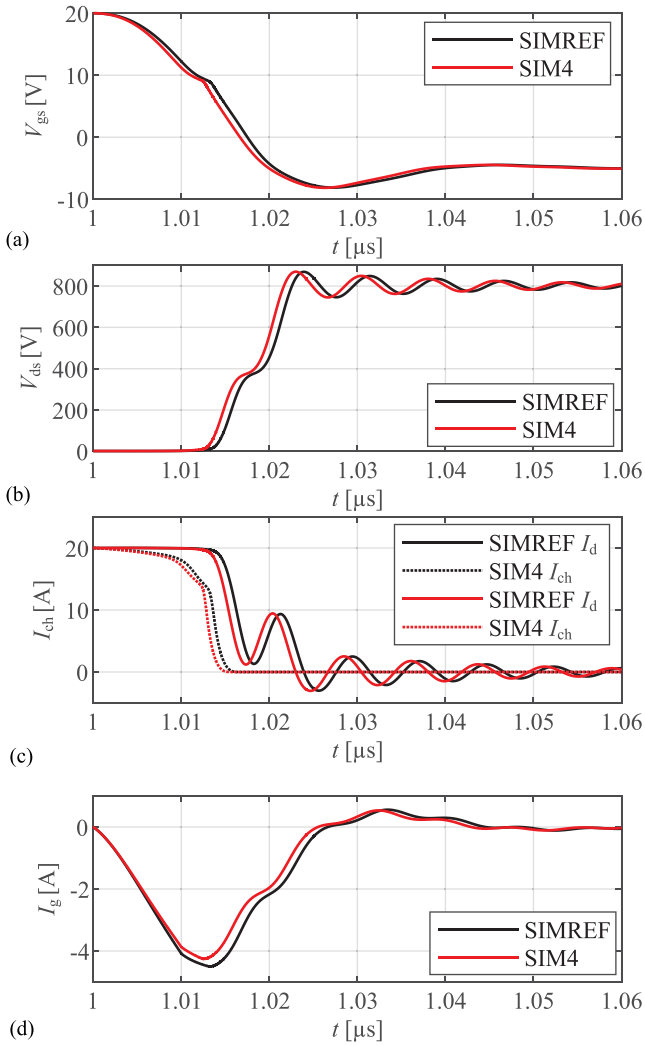

Fig. 12. Comparison of the MATLAB-Simulink simulation results SIMREF and SIM4 for the turn-OFF switching transient: (a) V_{gs}, (b) internal drain-source voltage V_{ds}, (c) channel I_{ch} and drain current I_{d}, and (d) gate current I_{g}.

E. SIM5: Effect of Constant C_{gs}

A SIM5 simulation was performed with a constant $C_{\mathrm{gs}} = C_{\mathrm{gs}}$ ($V_{\mathrm{ds,max}}$, $V_{\mathrm{gs}} = 0$), and the OFF-state C_{gd} and C_{ds}. The difference to SIM2 is almost negligible in terms of turn-OFF and turn-ON $E_{\mathrm{loss,ch}}$ and $E_{\mathrm{loss,out}}$ as well as the current and voltage switching waveforms.

F. SIM6: Effect of Constant C_{gs} and Constant C_{ds}

Further simplifications using a constant $C_{\mathrm{gs}} = C_{\mathrm{gs}}$ ($V_{\mathrm{ds,max}}$, $V_{\mathrm{gs}} = 0$) and a constant $C_{\mathrm{ds}} = C_{\mathrm{ds}}$ ($V_{\mathrm{ds,max}}$, $V_{\mathrm{gs}} = 0$), are verified by the sixth simulation SIM6. The voltage slope at turn-ON calculated from the SIM6 results, $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ is 91.5 V/ns, so that the difference between SIMREF and SIM6 in terms of $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ is ≈ 10 %, which is worse than in the case of SIM2. For the turn-OFF switching transients, $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ is increased by ≈ 3.6 % in SIM6 in comparison to SIMREF. Using SIMREF as a reference, $E_{\mathrm{loss,ch}}$ and $E_{\mathrm{loss,out}}$ at the turn-ON are calculated with relative errors of 18 % and 9 %, respectively, and with relative errors of 195 % and 77.5 %, at the turn-OFF, respectively. Therefore, when using constant C_{gs} and constant C_{ds}, a significantly decreased accuracy for the estimation of the energy switching losses can be expected than when using the OFF-state *C-V*s.

G. Summary of SIM2-SIM6 Results

According to the simulation results of SIM2-SIM6, the nonlinearity of C_{gd} is most important, which can be seen by comparing the results from SIMREF, SIM4, and SIM2. By adopting a single-voltage dependent C_{ds} (see SIM3), a relative error of only few % can be expected for the estimation of the energy switching losses. Using $C_{\mathrm{gs}} = $ const. and constant $C_{\mathrm{ds}} = $ const. is the worst combination of all analyzed modeling assumptions.

V. VERIFICATION BY SWITCHING MEASUREMENTS

This section presents the verification of the simulations results by means the DPT measurements. The approach to model the package and PCB layout parasitics of the measurements setup together with the measurement setup itself was described in more detail in [25]. The dynamic performance of the same type 1.2 kV,

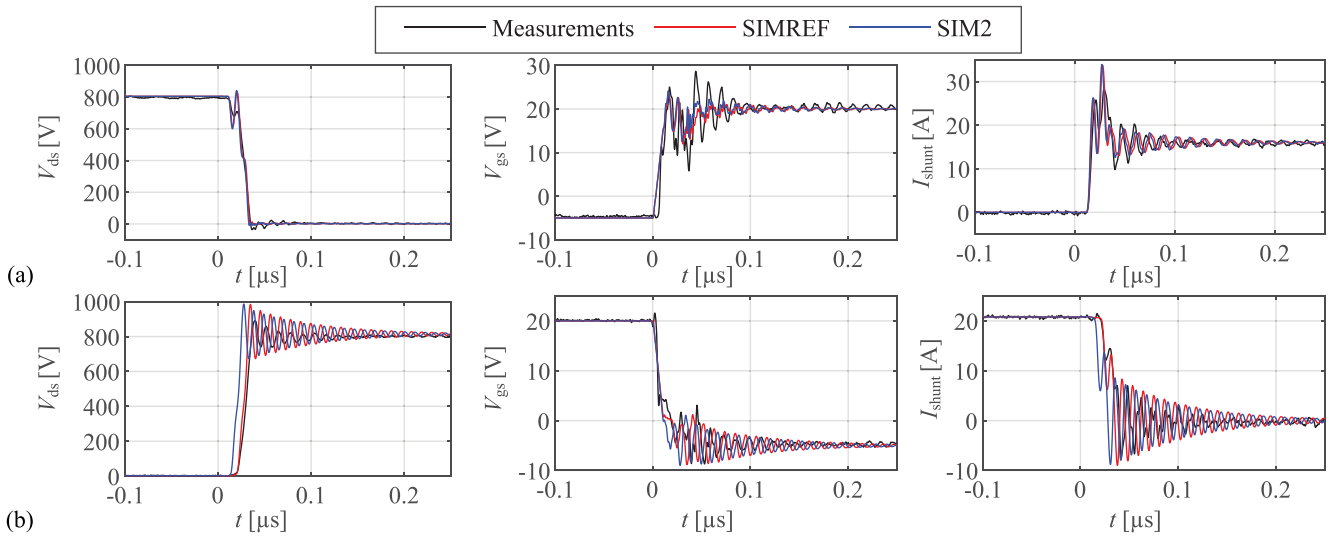

Fig. 13. Comparison between the measurements and the simulations of the switching waveforms ($V_{\mathrm{TEST}} = 800$ V) using the settings of SIM2 and SIMREF specified in Table I: (a) turn ON ($I_{\mathrm{TEST}} = 16$ A) and (b) turn OFF ($I_{\mathrm{TEST}} = 20.6$ A).

TABLE III
SIMULATED AND MEASURED ENERGY LOSSES OF THE TURN-ON AND TURN-OFF SWITCHING TRANSIENTS

	turn-on $E_{\mathrm{loss,out}}$ [μJ]	turn-on $E_{\mathrm{loss,ch}}$ [μJ]	turn-off $E_{\mathrm{loss,out}}$ [μJ]	turn-off $E_{\mathrm{loss,ch}}$[μJ]
SIMREF	215	241	65	28.7
SIM2	210	231	62	28.5
Measured	204	-	80	-

80 mΩ planar-gate SiC power MOSFET in TO-247-3 package is simulated using the settings of SIM2 and SIMREF specified in Table I. As only two- and three-mutually coupled inductors can be modeled in MATLAB Simulink, the mutual couplings as existing between PCB layout tracks had to be further simplified in comparison to the electromagnetic model of the PCB layout presented in [25]. The equivalent circuits of a high voltage probe (Keysight 10076 C 100:1, 500 MHz, 3.7 kVpk) used to measure the drain-source voltage; of a low voltage measurement probe (Keysight N2873 A, 500 MHz, 200 V) used to measure the gate-source voltage; as well as of a current shunt (T & M TTSDN current shunt SSDN-414-05) used to measure the source current were included in the simulations.

The comparison between the measured and the simulated switching current and voltage waveforms are presented for turn-ON and turn-OFF switching transients in Fig. 13. The measured and simulated switching energy losses $E_{\mathrm{sw,loss}}$ are summarized in Table III. In comparison to the simulations, the measured switching energy losses are determined from the measurable voltages across the device terminals, which include the effects of the package parasitics. The differences between the measured and simulated $E_{\mathrm{sw,loss}}$ results clearly show the difficulties of distinguishing the effects of package and layout parasitics, measurement probes and the voltage-dependent *C-V* and *I-V* device characteristics. Namely, if the frequency-dependent model of layout/package parasitics is not precise enough, the effects of two-voltage dependent *C-V* device characteristics with respect to $E_{\mathrm{sw,loss}}$ cannot be precisely determined as it was performed using a test circuit in Section IV. However, the differences between SIMREF and SIM2, and a good matching between SIMREF and measured waveforms for turn-OFF switching transients shown in Fig. 13(b) confirms the conclusions of Section IV-B. Accordingly, for reliable simulations of device dynamic performance, it is important to model both device characteristics and the effects of measurement probes and layout parasitics accurately.

VI. CONCLUSION

This article shows the voltage dependence of capacitance in vertical SiC power MOSFETs with lateral channel. It investigates the effect of two-voltage dependent ($V_{\mathrm{gs}}, V_{\mathrm{ds}}$) nonlinear *C-V* properties on the performance of the device in fast switching. TCAD device simulations allow the impact of layout parasitics and the device *I-V*s and *C-V*s characteristics on the device switching performance to be distinguished with a higher accuracy than it is possible by any kind of measurements. With the different approaches for the three interterminal capacitance model evaluated here, detailed insight is obtained on the origin of and impact on parameters such as measured switching energy losses $E_{\mathrm{loss,out}}$, ohmic switching energy losses $E_{\mathrm{loss,ch}}$, voltage $t_{\mathrm{delay,V}}$ and current $t_{\mathrm{delay,I}}$ delay, and voltage $\mathrm{d}V_{\mathrm{ds}}/\mathrm{d}t$ and current $\mathrm{d}I_{\mathrm{d}}/\mathrm{d}t$ rate of change. The modeling approach presented in this article is highly valuable for understanding the tradeoffs between accuracy and computational cost for predictive modeling of SiC power MOSFETs, and can also be applied to other fast switching power devices.

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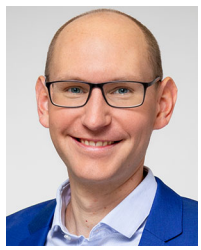

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